SDM450/SDA450
Device Specification
80-PC173-1 Rev. H

Qualcomm Technologies, Inc.

Device description

The SDM450/SDA450 device uses the advanced 14 nm FinFET process for lower active power dissipation and faster peak CPU performance. It includes a customized 64-bit ARM Cortex-A53 octa-core applications processor non-package-on-package (non-PoP) LPDDR3 SDRAM memory.

The latest air interface standards are supported, including:

- LTE up to Cat7 (FDD and TDD), including 2 × 20 CA
- WCDMA up to Rel-10 HSPA+, including 4C-HSDPA+ and HSDPA 2 + 1 CA
- TD-SCDMA up to DC-HSPA+ 64 QAM
- GSM, GPRS, and EDGE
- CDMA up to 1X Advanced and 1xEV-DOrB

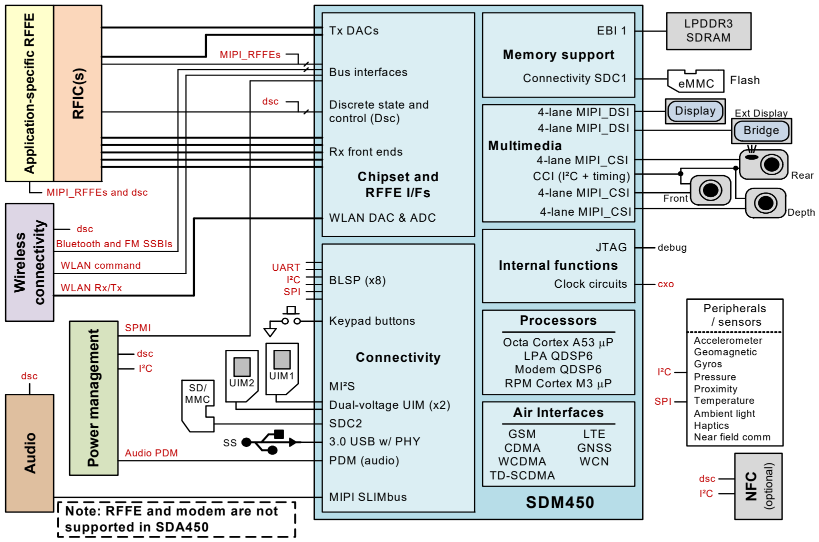
Key processor and memory characteristics include:

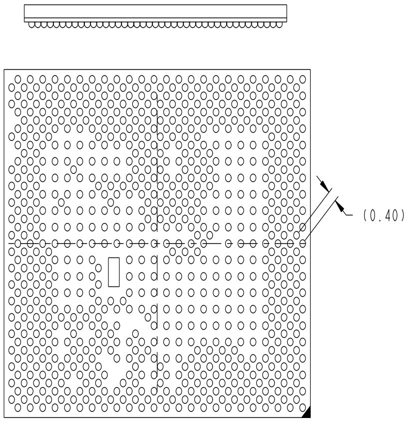
- Customized octa-core applications processor
  - Eight high performance cores at 1.8 GHz
- Qualcomm® Adreno™ GPU 506 graphics processing unit (GPU) with 64-bit addressing; designed for 600 MHz

Key features (see Section 1.2 for details)

- Advanced RF techniques with WTR3925 or with two WTR2965 devices
  - Downlink carrier aggregation (DLCA)
  - Uplink carrier aggregation (ULCA)
- Two 4-lane DSI D-PHY 1.1, FHD+
- Video 1080p at 60 fps, 2560 buffer width (10 layers blending), VESA DSC 1.1 Adreno GPU with Qualcomm® Universal Bandwidth Compression (UBWC)
- Three 4-lane CSI (4 + 4 + 4) D-PHY 1.2 at 2.1 Gbps per lane
- Dual 14-bit image signal processing (ISP): 13 MP and 13 MP, 21 MP at 30 fps ZSL with dual-ISP, or 13 MP 30 fps ZSL with single-ISP
- Support for USB 3.0, eMMC 5.1, and SD 3.0
- Low-power Qualcomm® sensor core with Qualcomm® Hexagon™ DSP to support always-on use cases
- WLAN 802.11 b/g/n/ac, DBS, Bluetooth 4.2, and FM with WCN3615, WCN3660B, and WCN3680B
- Non-PoP high-speed memory and LPDDR3 SDRAM designed for 933 MHz clock

SDM450/SDA450 high-level block diagram and 792 NSP package drawing





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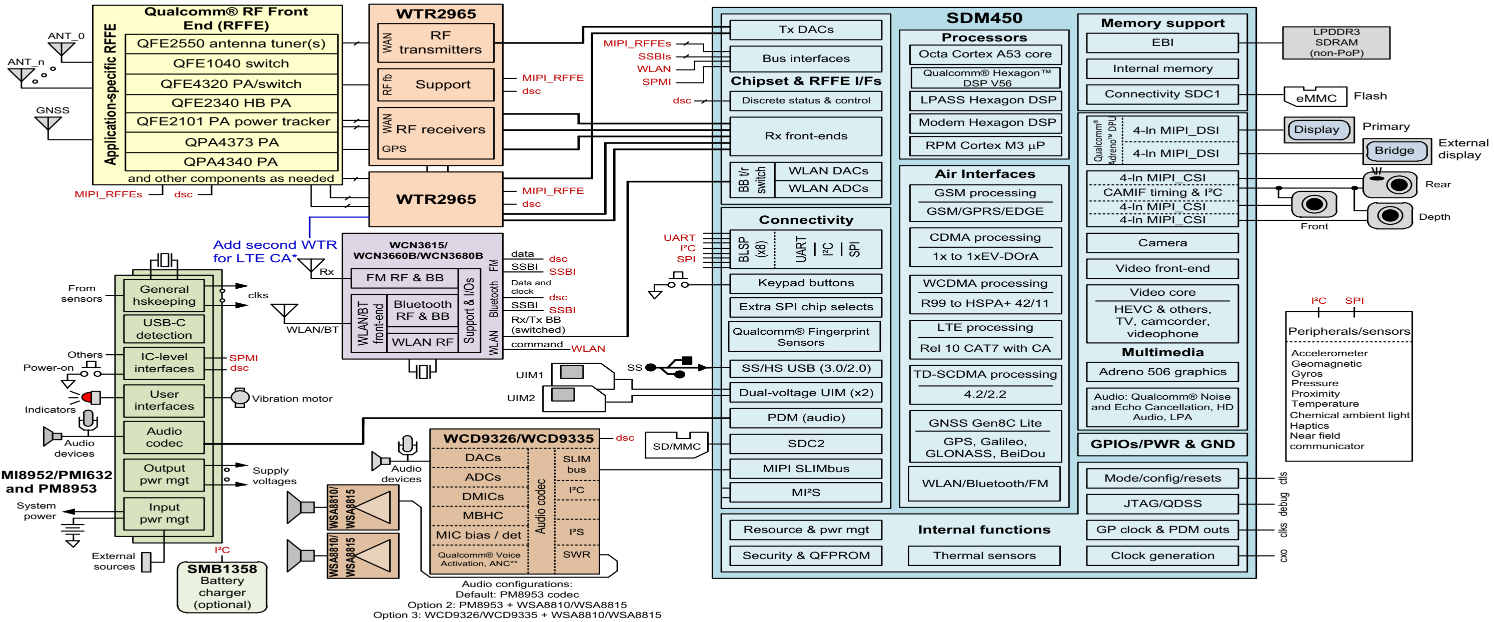
Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

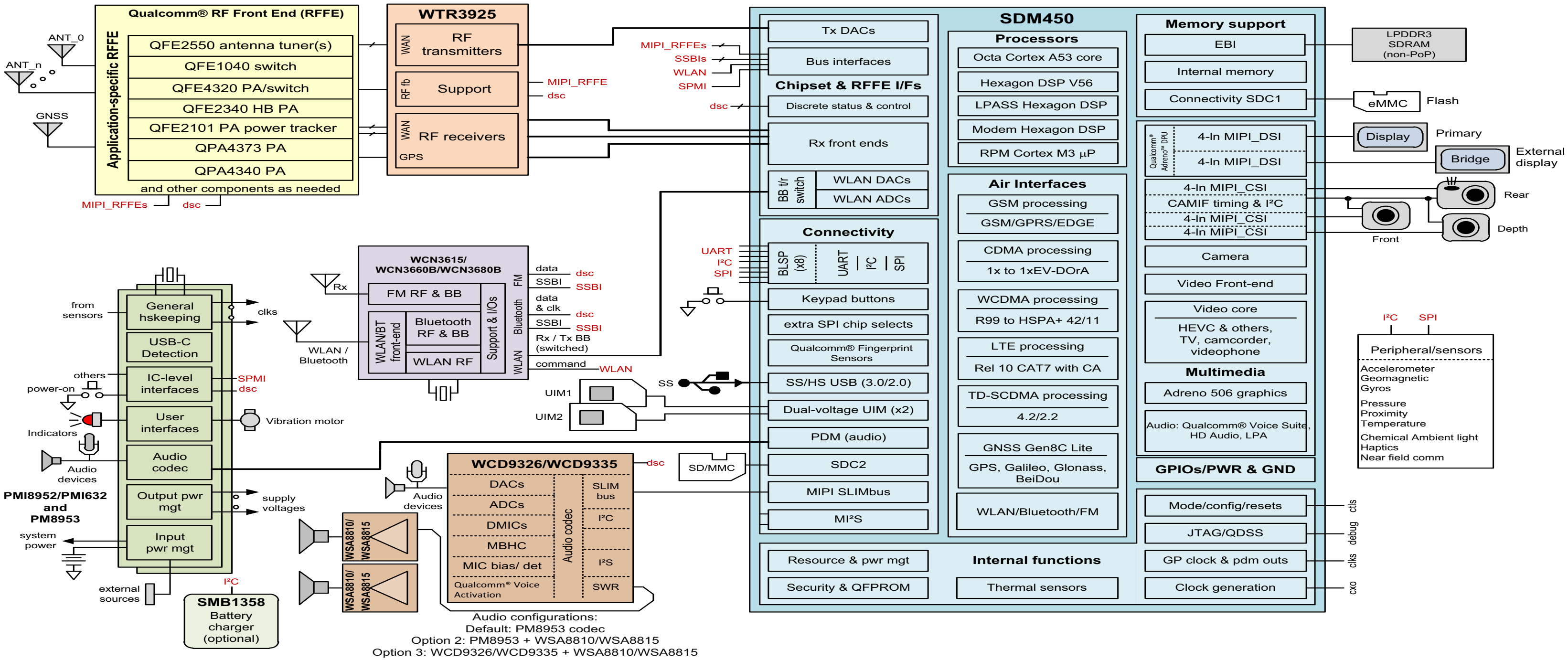
1.1 Functional block diagram



Audio configurations:
Default: PM8953 codec
Option 2: PM8953 + WSA8810/WSA8815
Option 3: WCD9326/WCD9335 + WSA8810/WSA8815
*Note: Single WTR2965 can support intra-band contiguous DL-CA.
**Note: ANC is supported only on WCD9335

***Notes**:
- Qualcomm continues the support on SDM450/SDA450 + PM8953 + PMI8952 platform with Android P (OTA Upgrades only)
- Qualcomm will support SDM450/SDA450 + PM8953 + PMI632 for new launches with O MR1 and P

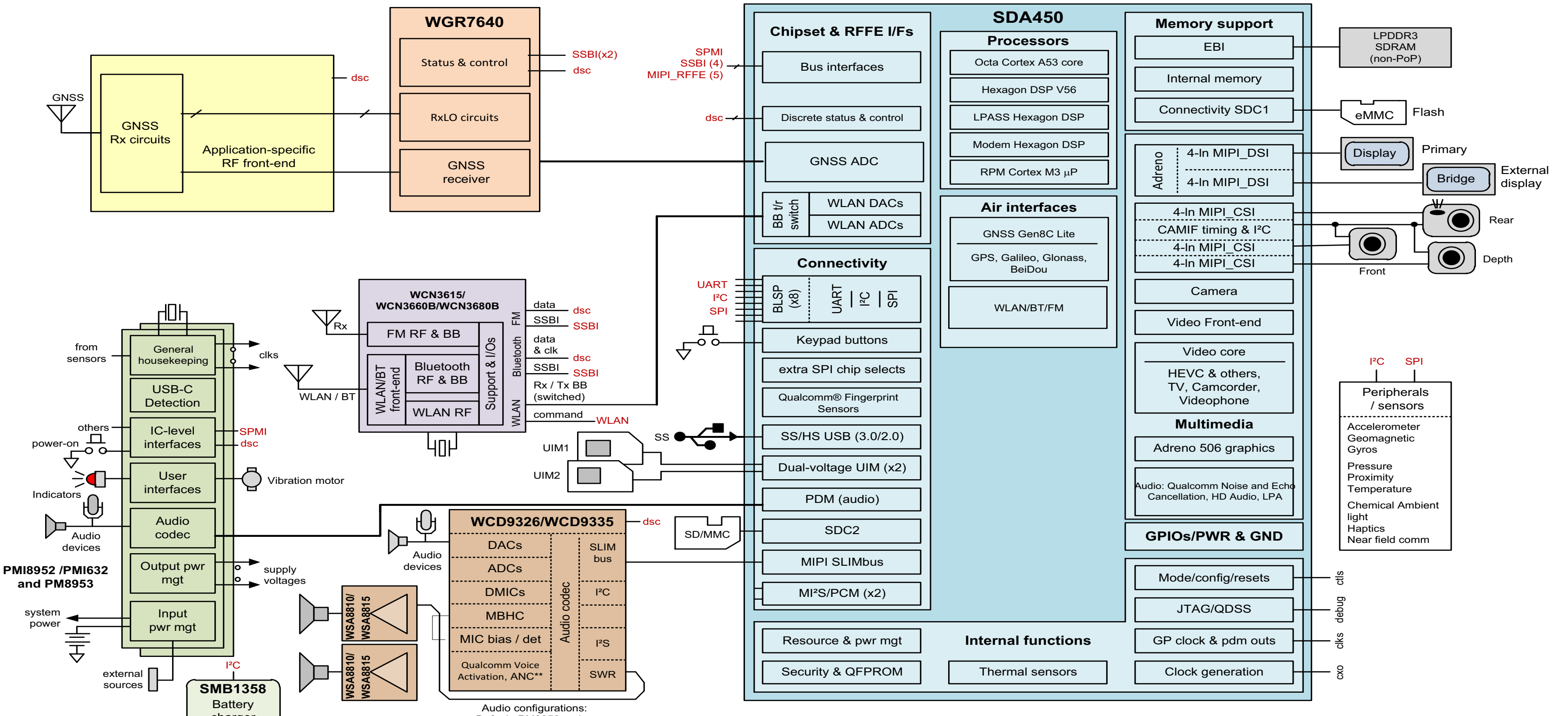
Figure 1-1 SDM450 functional block diagram and example application using WTR2965



Audio configurations:
Default: PM8953 codec
Option 2: PM8953 + WSA8810/WSA8815
Option 3: WCD9326/WCD9335 + WSA8810/WSA8815
**Note: ANC is supported only on WCD9335

***Notes**:
- Qualcomm continues the support on SDM450/SDA450 + PM8953 + PMI8952 platform with Android P (OTA Upgrades only)
- Qualcomm will support SDM450/SDA450 + PM8953 + PMI632 for new launches with O MR1 and P

Figure 1-2 SDM450 functional block diagram and example application using WTR3925



Audio configurations:
Default: PM8953 codec
Option 2: PM8953 + WSA8810/WSA8815
Option 3: WCD9326/WCD9335 + WSA8810/WSA8815
Note: ANC is supported only on WCD9335

***Notes**:
- Qualcomm continues the support on SDM450/SDA450 + PM8953 + PMI8952 platform with Android P (OTA Upgrades only)
- Qualcomm will support SDM450/SDA450 + PM8953 + PMI632 for new launches with O MR1 and P

Figure 1-3 SDA450 functional block diagram and example application

1.2 SDM450/SDA450 features

The software must enable some of the hardware features integrated within the SDM450/SDA450. To identify the enabled SDM450/SDA450 features, see the latest revision of the applicable software release notes.

Table 1-1 SDM450/SDA450 features

Feature	SDM450/SDA450 capability
Processors	
Applications	ARM Cortex-A53 microprocessor cores at 1.8 GHz ■ 64-bit processor ■ Octa-core: one quad with 512 KB L2 cache + one quad with 512 KB L2 cache ■ Primary boot processor
Modem system [1]	aDSP: Hexagon DSP V56 850 MHz 768 KB L2 caches ■ SDM450: DSDS
RPM system	Cortex M3: Modem power manager (MPM) MPM coordinates shutdown/wakeup, clock rates, and VDDs
Memory support	
System memory via EBI	Non-PoP LPDDR3 SDRAM; 32-bit wide; up to 933 MHz
Graphics internal memory	136 KB unified SRAM pool on-chip memory (GMEM)
External memory via SDC	eMMC v5.1/SD3.0 flash devices
RF support	
RF operating bands [1]	Defined by the WTR device
Air interfaces	
GSM [1]	Yes
CDMA [1]	Yes
WCDMA [1]	Yes
TD-SCDMA [1]	Yes
LTE [1]	Yes
WLAN/BT/FM	Yes: all (with WCN3680B/WCN3660B) (Applicable for both SDM450 and SDA450)
NFC	Yes
GNSS: Qualcomm® Location Suite engine	Gen 8C Lite; Support for three bands ***concurrently***: ■ GPS, BeiDou, and GLONASS or ■ GPS, BeiDou, and Galileo

Table 1-1 SDM450/SDA450 features (cont.)

Feature	SDM450/SDA450 capability
Multimedia	
Display interfaces MIPI_DSI General display features	FHD+; 16, 18, and 24 bpp RGB **NOTE:** Contact QTI for assistance on the display type and on the supported aspect ratio. Dual MIPI DSI four-lane Wi-Fi display: 1080p 30 fps (Snapdragon UBWC) FHD+; 1080p 30 fps external wireless display
Camera interfaces	Camera
Number of CSIs	Three; 2.1 Gbps per lane
Primary (CSI0)	Four-lane; supports CMOS and CCD sensors, up to 21 MP sensors
Secondary (CSI1)	Four-lane; supports CMOS and CCD sensors, up to 21 MP sensors
Tertiary (CSI2)	Four-lane; supports CMOS and CCD sensors, up to 21 MP sensors
Configurations supported	Pixel manipulations, camera modes, image effects, and postprocessing techniques, including defective pixel correction
General camera features	I^{2}C controls **NOTE:** The SDM450/SDA450 supports three CSI lanes (up to 21 MP); however, only two can operate concurrently.
Mobile display processor	Qualcomm® Snapdragon™ Display Engine 515 for display processing
Video applications performance	
Encode	1080p60, H.264, H.265, and VP8
Decode	1080p60, H.264, H.265, VP8, and VP9
Wireless display support (decode + encode)	1080p60D + 1080p30E
Graphics	Adreno 506; up to a 600 MHz 3D graphics accelerator
Audio	
Low-power audio	Low-power audio for MP3 and AAC 5.1 playback; surround sound
Voice codec support	Versatile: many audio playback and voice modes; encoders for audio and FM recording; many concurrency modes
Audio codec support	G711; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR
Enhanced audio	MP3; aacPlus, eAAC; AMR-NB, AMR-WB, G.711, Windows Media Audio (WMA) 9/10 Pro
Synthesizer	Dolby Digital Plus and DTS-HD surround sound Qualcomm® Noise and Echo Cancellation V6.1 and Qualcomm® Voice Suite Enhanced 3D audio solution /Stereo audio expansion feature/intelligent mixing algorithm 128-voice polyphony wavetable
Web technologies	V8 JavaScript Engine optimizations WebKit browser JPEG hardware decode acceleration Networking stack IP and HTTP tuning Flash 10.x and video processor decode optimization

Table 1-1 SDM450/SDA450 features (cont.)

Feature	SDM450/SDA450 capability
Messaging [1]	Text messages; text encoding for SMS Multimedia messaging services: combined video (MPEG-4), still image (JPEG), voice tag (AMR), and text sent as message
Connectivity	
BLSP ports	Eight, 4 bits each; multiplexed serial interface functions
UART	Yes: up to 4 Mbps (only four ports)
I^2C	Yes: cameras, sensors, near field communicator (NFC), SMB, and so on
Serial peripheral interface (SPI) (master only)	Yes: cameras, sensors, and so on
UIM	Two ports: dual voltage (1.8 V/2.85 V)
USB	One USB 3.0/USB 2.0
Secure digital interfaces	Up to two ports One 8-bit and one 4-bit SD 3.0; SD/MMC card; eMMC v5.1
Wireless connectivity	With WCN3680B/WCN3660B/WCN3615
WLAN	802.11 b/g/n/ac
Bluetooth	Bluetooth 4.2 LE and earlier
FM radio	Rx
Touchscreen support	Capacitive panels via external IC (I^2C, SPI, and interrupts)
Audio interfaces	
MI^2S	Two ports (primary and secondary ports)
SLIMbus	One port SLIMbus interface to WCD9326/WCD9335
CDC PDM port	Interface between SDM450/SDA450 and PM8953 for audio application
Configurable GPIOs	
Number of GPIO ports	142 GPIOs: GPIO_0 to GPIO_141
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	Secure boot, SFS, ARM TrustZone, Qualcomm® Trusted Execution Environment, secure debug, and Microsoft Windows Media DRM10
Crypto engine	Increased throughput via increased frequencies and a new internal AXI-based data master; support for multiple execution environments per Crypto; algorithm to accelerate file system encryption (AES-XTS), IPSec, and SSL (HMAC-SHA, CCM, CMAC)
QFPROM	Large fuse array, replaces previous-generation Qfuse chains; nonvolatile memory with faster and simpler programming
Security controller	Chip-wide configuration for security, feature enable, and debug; persistent storage of ID numbers and sensitive key data; secure HDCP key provisioning and secure debug facility; primary and secondary hardware key blocking for SFS

Table 1-1 SDM450/SDA450 features (cont.)

Feature	SDM450/SDA450 capability
PLLs and clocks	Multiple clock regimes; watchdog and sleep timers 19.2 MHz CXO master clock input General-purpose outputs: M/N: D counter and PDM
Resource and power manager	Fundamental to power management Key blocks: RPM core, Cortex M3, security controller, and MPM Improved efficiency via clock control, split-rail power collapse, and voltage scaling; several low-power sleep modes
Debug	JTAG and QDSS
Others	Thermal sensors, modes, and resets; and peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
WTR RFICs[1]	WTR3925 or two WTR2965
WLAN baseband data	One Rx and one Tx analog interface
GNSS baseband data	Rx analog interface
Status and control	SSBIs and discrete signals, as needed, via GPIOs
Power management	PM8953 + PMI8952/PMI632 Two 2-line SPMI; dedicated clock and reset lines; plus other GPIOs as needed
Package dimensions	792 NSP; 14 × 12 × 0.84 mm

1. Not applicable for SDA450

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The capital letters indicate the default pull direction, and is a prefix to other programmable options: ■ NP: pdpukp = default no-pull, with programmable options following the colon (:) ■ PD: nppukp = default pull-down, with programmable options following the colon (:) ■ PU: nppdkp = default pull-up, with programmable options following the colon (:) ■ KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad-voltage groupings for baseband circuits	
P1	Pad group 1 (EBI); tied to VDDPX_1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDDPX_2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDDPX_3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDDPX_5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDDPX_6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (eMMC I/O); tied to VDDPX_7 pins (1.8 V)
MIPI	Supply voltage for MIPI_CSI and MIPI_DSI circuits and I/Os

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
Output-current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated.
3.0 V (H) pads	Programmable drive strength, 2–8 mA, in 2 mA steps
Others [1]	Programmable drive strength, 2–16 mA, in 2 mA steps

[1] Digital pads other than EBI0 pads or high-voltage tolerant pads.

2.2 Pin assignments

2.2.1 Pin map

The SDM450/SDA450 is available in the 792 nanoscale package (NSP). Its bottom surface is equivalent to a 792 NSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details.

A high-level view of the pin assignments is shown in Figure 2-2. Each pin is colored to indicate the function type that it supports; these colors are defined in Figure 2-1.

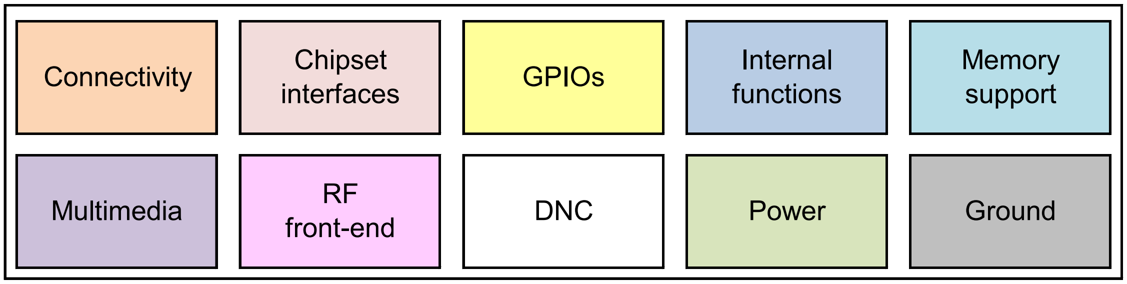


Figure 2-1 SDM450/SDA450 pin assignment legend

The text within Figure 2-2 is difficult to read when viewing an 8½"× 11" hard copy. Other viewing options are available:

- Print that one page on an 11" × 17" sheet.
- View the graphics PDF soft copy and zoom in — the resolution is sufficient for comfortable reading.
- Download the *SDM450/SDA450 Pin Assignment Spreadsheet* (80-PC173-1A). This Microsoft Excel spreadsheet lists all SDM450/SDA450 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: To download the pin assignment spreadsheet (80-PC173-1A), click the following link: https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PC173-1A

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

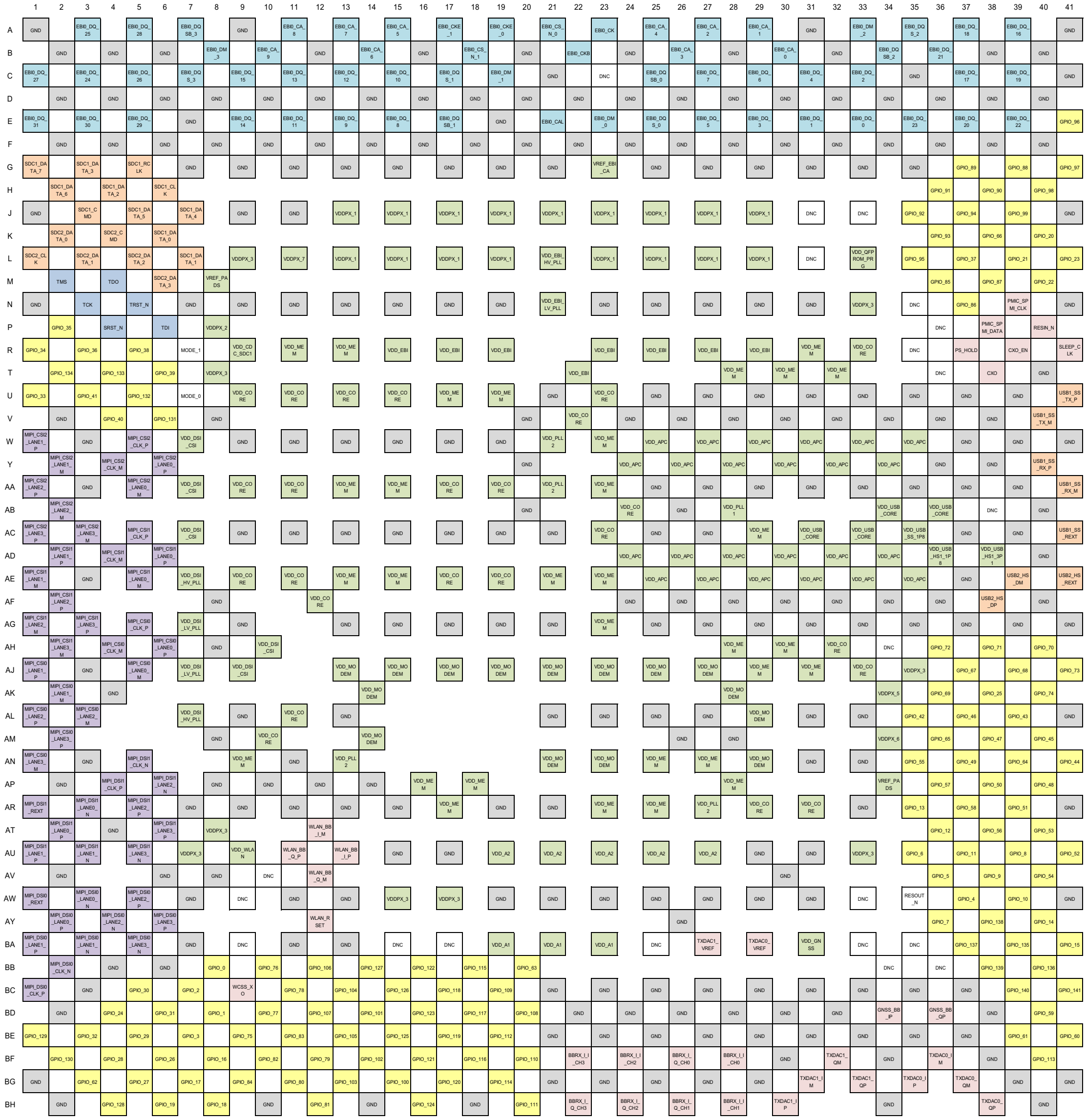
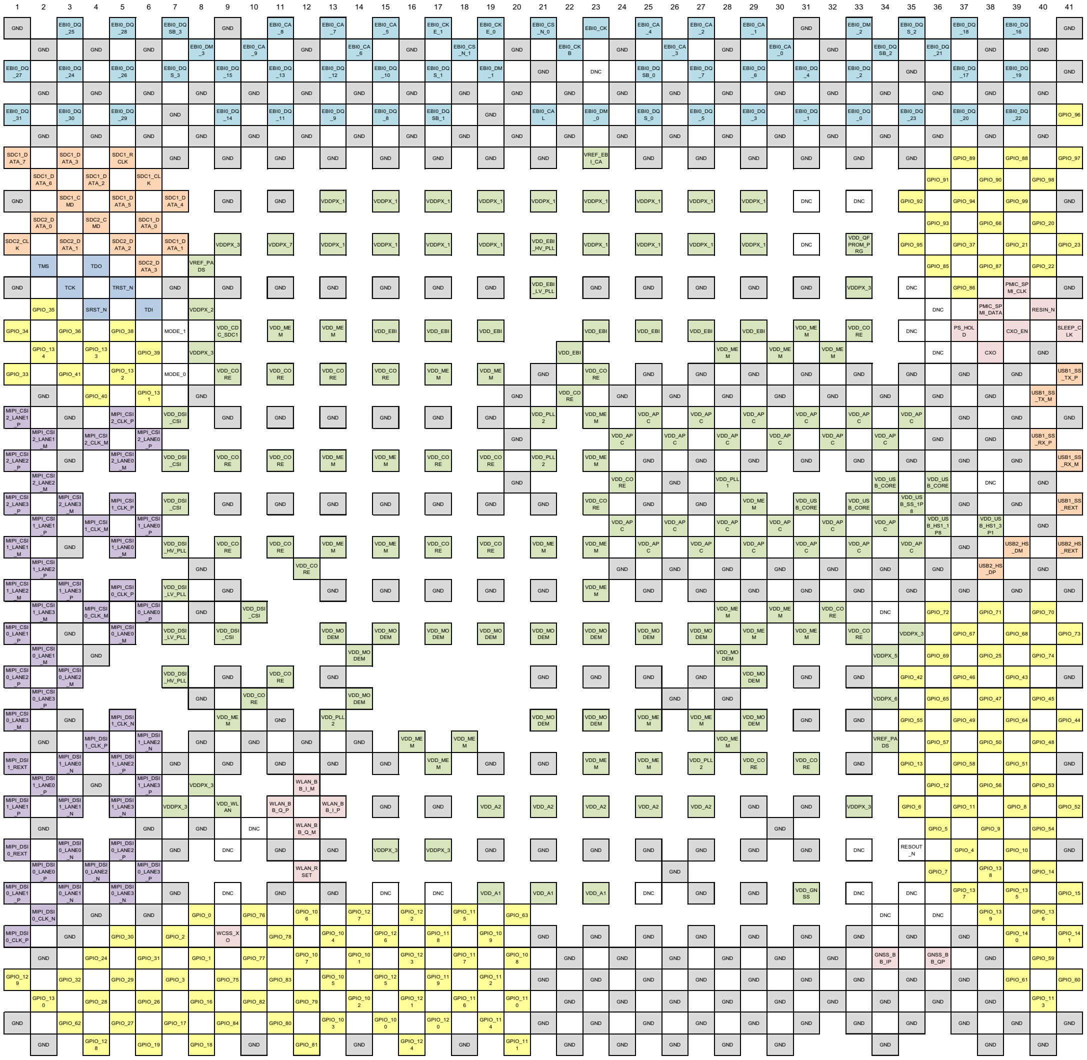


Figure 2-2 SDM450 pin assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41
A	GND		EBI0_DQ_25		EBI0_DQ_28		EBI0_DQSB_3		GND		EBI0_CA_8		EBI0_CA_7		EBI0_CA_5		EBI0_CKE_1		EBI0_CKE_0		EBI0_CS_N_0		EBI0_CK		EBI0_CA_4		EBI0_CA_2		EBI0_CA_1		GND		EBI0_DM_2		EBI0_DQS_2		EBI0_DQ_18		EBI0_DQ_16		GND
B		GND		GND		GND		EBI0_DM_3		EBI0_CA_9		GND		EBI0_CA_6		GND		EBI0_CS_N_1		GND		EBI0_CKB		GND		EBI0_CA_3		GND		EBI0_CA_0		GND		EBI0_DQSB_2		EBI0_DQ_21		GND		GND	
C	EBI0_DQ_27		EBI0_DQ_24		EBI0_DQ_26		EBI0_DQS_3		EBI0_DQ_15		EBI0_DQ_13		EBI0_DQ_12		EBI0_DQ_10		EBI0_DQS_1		EBI0_DM_1		GND		DNC		EBI0_DQSB_0		EBI0_DQ_7		EBI0_DQ_6		EBI0_DQ_4		EBI0_DQ_2		GND		EBI0_DQ_17		EBI0_DQ_19		GND
D		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND	
E	EBI0_DQ_31		EBI0_DQ_30		EBI0_DQ_29		GND		EBI0_DQ_14		EBI0_DQ_11		EBI0_DQ_9		EBI0_DQ_8		EBI0_DQSB_1		GND		EBI0_CAL		EBI0_DM_0		EBI0_DQS_0		EBI0_DQ_5		EBI0_DQ_3		EBI0_DQ_1		EBI0_DQ_0		EBI0_DQ_23		EBI0_DQ_20		EBI0_DQ_22		GPIO_96
F		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND	
G	SDC1_DATA_7		SDC1_DATA_3		SDC1_RCLK		GND		GND		GND		GND		GND		GND		GND		GND		VREF_EBI_CA		GND		GND		GND		GND		GND		GND		GPIO_89		GPIO_88		GPIO_97
H		SDC1_DATA_6		SDC1_DATA_2		SDC1_CLK																														GPIO_91		GPIO_90		GPIO_98	
J	GND		SDC1_CMD		SDC1_DATA_5		SDC1_DATA_4		GND		GND		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		DNC		DNC		GPIO_92		GPIO_94		GPIO_99		GND
K		SDC2_DATA_0		SDC2_CMD		SDC1_DATA_0																														GPIO_93		GPIO_66		GPIO_20	
L	SDC2_CLK		SDC2_DATA_1		SDC2_DATA_2		SDC1_DATA_1		VDDPX_3		VDDPX_7		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		VDD_EBI_HV_PLL		VDDPX_1		VDDPX_1		VDDPX_1		VDDPX_1		DNC		VDD_QFPROM_PRG		GPIO_95		GPIO_37		GPIO_21		GPIO_23
M		TMS		TDO		SDC2_DATA_3		VREF_PADS																												GPIO_85		GPIO_87		GPIO_22	
N	GND		TCK		TRST_N		GND		GND		GND		GND		GND		GND		GND		VDD_EBI_LV_PLL		GND		GND		GND		GND		GND		VDDPX_3		DNC		GPIO_86		PMIC_SPMI_CLK		GND
P		GPIO_35		SRST_N		TDI		VDDPX_2																												DNC		PMIC_SPMI_DATA		RESIN_N	
R	GPIO_34		GPIO_36		GPIO_38		MODE_1		VDD_CDC_SDC1		VDD_MEM		VDD_MEM		VDD_EBI		VDD_EBI		VDD_EBI				VDD_EBI		VDD_EBI		VDD_EBI		VDD_EBI		VDD_MEM		VDD_CORE		DNC		PS_HOLD		CXO_EN		SLEEP_CLK
T		GPIO_134		GPIO_133		GPIO_39		VDDPX_3														VDD_EBI						VDD_MEM		VDD_MEM		VDD_MEM				DNC		CXO		GND	
U	GPIO_33		GPIO_41		GPIO_132		MODE_0		VDD_CORE		VDD_CORE		VDD_CORE		VDD_CORE		VDD_MEM		VDD_MEM		GND		VDD_CORE		GND		GND		GND		GND		GND		GND		GND		GND		USB1_SS_TX_P
V		GND		GPIO_40		GPIO_131		GND										GND		VDD_CORE		GND		GND		GND		GND		GND		GND		GND		GND		USB1_SS_TX_M	
W	MIPI_CSI2_LANE1_P		GND		MIPI_CSI2_CLK_P		VDD_DSI_CSI		GND		GND		GND		GND		GND		GND		VDD_PLL2		VDD_MEM		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		GND		GND		GND
Y		MIPI_CSI2_LANE1_M		MIPI_CSI2_CLK_M		MIPI_CSI2_LANE0_P												GND				VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		GND		GND		USB1_SS_RX_P	
AA	MIPI_CSI2_LANE2_P		GND		MIPI_CSI2_LANE0_M		VDD_DSI_CSI		VDD_CORE		VDD_CORE		VDD_MEM		VDD_MEM		VDD_CORE		VDD_CORE		VDD_PLL2		VDD_MEM		GND		GND		GND		GND		GND		GND		GND		GND		USB1_SS_RX_M
AB		MIPI_CSI2_LANE2_M																		GND				VDD_CORE		GND		VDD_PLL1						VDD_USB_CORE		VDD_USB_CORE		DNC		GND	
AC	MIPI_CSI2_LANE3_P		MIPI_CSI2_LANE3_M		MIPI_CSI1_CLK_P		VDD_DSI_CSI		GND		GND		GND		GND		GND		GND		GND		VDD_CORE		GND		GND		VDD_MEM		VDD_USB_CORE		VDD_USB_CORE		VDD_USB_SS_1P8		GND		GND		USB1_SS_REXT
AD		MIPI_CSI1_LANE1_P		MIPI_CSI1_CLK_M		MIPI_CSI1_LANE0_P																		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_USB_HS1_1P8		VDD_USB_HS1_3P1		GND	
AE	MIPI_CSI1_LANE1_M		GND		MIPI_CSI1_LANE0_M		VDD_DSI_HV_PLL		VDD_CORE		VDD_CORE		VDD_MEM		VDD_MEM		VDD_CORE		VDD_CORE		VDD_MEM		VDD_MEM		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		VDD_APC		GND		USB2_HS_DM		USB2_HS_REXT
AF		MIPI_CSI1_LANE2_P						GND				VDD_CORE												GND		GND		GND		GND		GND		GND		GND		USB2_HS_DP		GND	
AG	MIPI_CSI1_LANE2_M		MIPI_CSI1_LANE3_P		MIPI_CSI0_CLK_P		VDD_DSI_LV_PLL		GND				GND		GND		GND		GND		GND		VDD_MEM		GND		GND		GND		GND		GND		GND		GND		GND		GND
AH		MIPI_CSI1_LANE3_M		MIPI_CSI0_CLK_M		MIPI_CSI0_LANE0_P		GND		VDD_DSI_CSI																		VDD_MEM		VDD_MEM		VDD_CORE		DNC		GPIO_72		GPIO_71		GPIO_70	
AJ	MIPI_CSI0_LANE1_P		GND		MIPI_CSI0_LANE0_M		VDD_DSI_LV_PLL		VDD_DSI_CSI				VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MODEM		VDD_MEM		VDD_MEM		VDD_CORE		VDDPX_3		GPIO_67		GPIO_68		GPIO_73
AK		MIPI_CSI0_LANE1_M		GND										VDD_MODEM														VDD_MODEM						VDDPX_5		GPIO_69		GPIO_25		GPIO_74	
AL	MIPI_CSI0_LANE2_P		MIPI_CSI0_LANE2_M				VDD_DSI_HV_PLL		GND		VDD_CORE		GND								GND		GND		GND		GND		VDD_MODEM		GND		GND		GPIO_42		GPIO_46		GPIO_43		GND
AM		MIPI_CSI0_LANE3_P						GND		VDD_CORE				VDD_MODEM												GND		GND						VDDPX_6		GPIO_65		GPIO_47		GPIO_45	
AN	MIPI_CSI0_LANE3_M		GND		MIPI_DSI1_CLK_N				VDD_MEM		GND		VDD_PLL2								VDD_MODEM		VDD_MODEM		VDD_MEM		VDD_MEM		VDD_MODEM		GND		GND		GPIO_55		GPIO_49		GPIO_64		GPIO_44
AP		GND		MIPI_DSI1_CLK_P		MIPI_DSI1_LANE2_N		GND		GND		GND		GND		VDD_MEM		VDD_MEM										VDD_MEM						VREF_PADS		GPIO_57		GPIO_50		GPIO_48	
AR	MIPI_DSI1_REXT		MIPI_DSI1_LANE0_N		MIPI_DSI1_LANE2_P		GND		GND		GND		GND		GND		VDD_MEM		GND		GND		VDD_MEM		VDD_MEM		VDD_PLL2		VDD_CORE		VDD_CORE		GND		GPIO_13		GPIO_58		GPIO_51		GND
AT		MIPI_DSI1_LANE0_P		GND		MIPI_DSI1_LANE3_P		VDDPX_3				WLAN_BB_I_M																								GPIO_12		GPIO_56		GPIO_53	
AU	MIPI_DSI1_LANE1_P		MIPI_DSI1_LANE1_N		MIPI_DSI1_LANE3_N		VDDPX_3		VDD_WLAN		WLAN_BB_Q_P		WLAN_BB_I_P		GND		GND		VDD_A2		VDD_A2		VDD_A2		VDD_A2		VDD_A2		GND		GND		VDDPX_3		GPIO_6		GPIO_11		GPIO_8		GPIO_52
AV		GND				GND		GND		DNC		WLAN_BB_Q_M																		GND						GPIO_5		GPIO_9		GPIO_54	
AW	MIPI_DSI0_REXT		MIPI_DSI0_LANE0_N		MIPI_DSI0_LANE2_P		GND		DNC		GND		GND		VDDPX_3		VDDPX_3		GND		GND		GND		GND		GND		GND		GND		DNC		RESOUT_N		GPIO_4		GPIO_10		GND
AY		MIPI_DSI0_LANE0_P		MIPI_DSI0_LANE2_N		MIPI_DSI0_LANE3_P						WLAN_RESET														GND										GPIO_7		GPIO_138		GPIO_14	
BA	MIPI_DSI0_LANE1_P		MIPI_DSI0_LANE1_N		MIPI_DSI0_LANE3_N		GND		DNC		GND		GND		DNC		DNC		VDD_A1		VDD_A1		VDD_A1		DNC		GND		GND		VDD_GNSS		DNC		DNC		GPIO_137		GPIO_135		GPIO_15
BB		MIPI_DSI0_CLK_N		GND		GND		GPIO_0		GPIO_76		GPIO_106		GPIO_127		GPIO_122		GPIO_115		GPIO_63														DNC		DNC		GPIO_139		GPIO_136	
BC	MIPI_DSI0_CLK_P		GND		GPIO_30		GPIO_2		WCSS_XO		GPIO_78		GPIO_104		GPIO_126		GPIO_118		GPIO_109		GND		GND		GND		GND		GND		GND		GND		GND		GND		GPIO_140		GPIO_141
BD		GND		GPIO_24		GPIO_31		GPIO_1		GPIO_77		GPIO_107		GPIO_101		GPIO_123		GPIO_117		GPIO_108		GND		GND		GND		GND		GND		GND		GNSS_BB_IP		GNSS_BB_QP		GND		GPIO_59	
BE	GPIO_129		GPIO_32		GPIO_29		GPIO_3		GPIO_75		GPIO_83		GPIO_105		GPIO_125		GPIO_119		GPIO_112		GND		GND		GND		GND		GND		GND		GND		GND		GND		GPIO_61		GPIO_60
BF		GPIO_130		GPIO_28		GPIO_26		GPIO_16		GPIO_82		GPIO_79		GPIO_102		GPIO_121		GPIO_116		GPIO_110		GND		GND		GND		GND		GND		GND		GND		GND		GND		GPIO_113	
BG	GND		GPIO_62		GPIO_27		GPIO_17		GPIO_84		GPIO_80		GPIO_103		GPIO_100		GPIO_120		GPIO_114		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND
BH		GND		GPIO_128		GPIO_19		GPIO_18		GND		GPIO_81		GND		GPIO_124		GND		GPIO_111		GND		GND		GND		GND		GND				GND				GND		GND	

Figure 2-3 SDA450 pin assignments

2.2.2 Pin descriptions

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 2-2: Boot configuration GPIOs

Table 2-3: Memory support functions

Table 2-4: Multimedia functions

Table 2-5: Connectivity functions

Table 2-8: Internal functions

Table 2-9: Chipset interface functions

Table 2-10: RF front-end interface functions

Table 2-11: GPIO ports

Table 2-12: No connection, do not connect, and reserved pins

Table 2-13: Power supply pins

Table 2-14: Ground pins

Table 2-2 Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Pad	Voltage	
BB12	BOOT_CONFIG[0]	GPIO_106	P3	DI B-PD:nppukp	fast_boot_select bit 0 Configurable I/O
BF40	BOOT_CONFIG[1]	GPIO_113	P3	DI B-PD:nppukp	fast_boot_select bit 1 Configurable I/O
BD12	BOOT_CONFIG[2]	GPIO_107	P3	DI B-PD:nppukp	fast_boot_select bit 2 Configurable I/O
BC19	BOOT_CONFIG[3]	GPIO_109	P3	DI B-PD:nppukp	fast_boot_select bit 3 Configurable I/O
BE13	BOOT_CONFIG[4]	GPIO_105	P3	DI B-PD:nppukp	fast_boot_select bit 4 Configurable I/O
BD20	BOOT_CONFIG[5]	GPIO_108	P3	DI B-PD:nppukp	fast_boot_select bit 5 Configurable I/O
BG19	BOOT_CONFIG[6]	GPIO_114	P3	DI B-PD:nppukp	fast_boot_select bit 6 Configurable I/O
BC13	BOOT_CONFIG[7]	GPIO_104	P3	DI B-PD:nppukp	fast_boot_select bit 7 Configurable I/O
BF20	BOOT_CONFIG[8]	GPIO_110	P3	DI B-PD:nppukp	fast_boot_select bit 8 Configurable I/O
U3	BOOT_CONFIG[9]	GPIO_41	P3	DI B-PD:nppukp	fast_boot_select bit 9 Configurable I/O
BE19	BOOT_CONFIG[10]	GPIO_112	P3	DI B-PD:nppukp	fast_boot_select bit 10 Configurable I/O

Table 2-2 Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Pad	Voltage	
BH20	BOOT_CONFIG[11]	GPIO_111	P3	DI B-PD:nppukp	fast_boot_select bit 11 Configurable I/O
P2	BOOT_CONFIG[12]	GPIO_35	P3	DI B-PD:nppukp	fast_boot_select bit 12 Configurable I/O
U5	BOOT_CONFIG[13]	GPIO_132	P3	DI B-PD:nppukp	fast_boot_select bit 13 Configurable I/O
BF2	BOOT_CONFIG[14]	GPIO_130	P3	DI B-PD:nppukp	fast_boot_select bit 14 Configurable I/O
L37	FORCED_USB_BOOT	GPIO_37	P3	DI B-PD:nppukp	Forced USB boot Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions: memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
LPDDR3 interface					
B30	EBI0_CA_0	–	P1	DO	LPDDR3 command/address bit 0
A29	EBI0_CA_1	–	P1	DO	LPDDR3 command/address bit 1
A27	EBI0_CA_2	–	P1	DO	LPDDR3 command/address bit 2
B26	EBI0_CA_3	–	P1	DO	LPDDR3 command/address bit 3
A25	EBI0_CA_4	–	P1	DO	LPDDR3 command/address bit 4
A15	EBI0_CA_5	–	P1	DO	LPDDR3 command/address bit 5
B14	EBI0_CA_6	–	P1	DO	LPDDR3 command/address bit 6
A13	EBI0_CA_7	–	P1	DO	LPDDR3 command/address bit 7
A11	EBI0_CA_8	–	P1	DO	LPDDR3 command/address bit 8
B10	EBI0_CA_9	–	P1	DO	LPDDR3 command/address bit 9
E21	EBI0_CAL	–	P1	AI	LPDDR3 calibration resistor
A23	EBI0_CK	–	P1	DO	LPDDR3 differential clock positive
B22	EBI0_CKB	–	P1	DO	LPDDR3 differential clock negative
A19	EBI0_CKE_0	–	P1	DO	LPDDR3 clock enable 0
A17	EBI0_CKE_1	–	P1	DO	LPDDR3 clock enable 1
A21	EBI0_CS_N_0	–	P1	DO	LPDDR3 chip select 0
B18	EBI0_CS_N_1	–	P1	DO	LPDDR3 chip select 1
E23	EBI0_DM_0	–	P1	DO	LPDDR3 data mask for byte 0
C19	EBI0_DM_1	–	P1	DO	LPDDR3 data mask for byte 1
A33	EBI0_DM_2	–	P1	DO	LPDDR3 data mask for byte 2
B8	EBI0_DM_3	–	P1	DO	LPDDR3 data mask for byte 3
E33	EBI0_DQ_0	–	P1	B	LPDDR3 data bit 0

Table 2-3 Pin descriptions: memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
E31	EBI0_DQ_1	–	P1	B	LPDDR3 data bit 1
C15	EBI0_DQ_10	–	P1	B	LPDDR3 data bit 10
E11	EBI0_DQ_11	–	P1	B	LPDDR3 data bit 11
C13	EBI0_DQ_12	–	P1	B	LPDDR3 data bit 12
C11	EBI0_DQ_13	–	P1	B	LPDDR3 data bit 13
E9	EBI0_DQ_14	–	P1	B	LPDDR3 data bit 14
C9	EBI0_DQ_15	–	P1	B	LPDDR3 data bit 15
A39	EBI0_DQ_16	–	P1	B	LPDDR3 data bit 16
C37	EBI0_DQ_17	–	P1	B	LPDDR3 data bit 17
A37	EBI0_DQ_18	–	P1	B	LPDDR3 data bit 18
C39	EBI0_DQ_19	–	P1	B	LPDDR3 data bit 19
C33	EBI0_DQ_2	–	P1	B	LPDDR3 data bit 2
E37	EBI0_DQ_20	–	P1	B	LPDDR3 data bit 20
B36	EBI0_DQ_21	–	P1	B	LPDDR3 data bit 21
E39	EBI0_DQ_22	–	P1	B	LPDDR3 data bit 22
E35	EBI0_DQ_23	–	P1	B	LPDDR3 data bit 23
C3	EBI0_DQ_24	–	P1	B	LPDDR3 data bit 24
A3	EBI0_DQ_25	–	P1	B	LPDDR3 data bit 25
C5	EBI0_DQ_26	–	P1	B	LPDDR3 data bit 26
C1	EBI0_DQ_27	–	P1	B	LPDDR3 data bit 27
A5	EBI0_DQ_28	–	P1	B	LPDDR3 data bit 28
E5	EBI0_DQ_29	–	P1	B	LPDDR3 data bit 29
E29	EBI0_DQ_3	–	P1	B	LPDDR3 data bit 3
E3	EBI0_DQ_30	–	P1	B	LPDDR3 data bit 30
E1	EBI0_DQ_31	–	P1	B	LPDDR3 data bit 31
C31	EBI0_DQ_4	–	P1	B	LPDDR3 data bit 4
E27	EBI0_DQ_5	–	P1	B	LPDDR3 data bit 5
C29	EBI0_DQ_6	–	P1	B	LPDDR3 data bit 6
C27	EBI0_DQ_7	–	P1	B	LPDDR3 data bit 7
E15	EBI0_DQ_8	–	P1	B	LPDDR3 data bit 8
E13	EBI0_DQ_9	–	P1	B	LPDDR3 data bit 9
E25	EBI0_DQS_0	–	P1	B	LPDDR3 differential data strobe for byte 0 positive
C17	EBI0_DQS_1	–	P1	B	LPDDR3 differential data strobe for byte 1 positive
A35	EBI0_DQS_2	–	P1	B	LPDDR3 differential data strobe for byte 2 positive
C7	EBI0_DQS_3	–	P1	B	LPDDR3 differential data strobe for byte 3 positive

Table 2-3 Pin descriptions: memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
C25	EBI0_DQSB_0	–	P1	B	LPDDR3 differential data strobe for byte 0 (-)
E17	EBI0_DQSB_1	–	P1	B	LPDDR3 differential data strobe for byte 1 (-)
B34	EBI0_DQSB_2	–	P1	B	LPDDR3 differential data strobe for byte 2 (-)
A7	EBI0_DQSB_3	–	P1	B	LPDDR3 differential data strobe for byte 3 (-)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions: multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Primary camera serial interface: four-lane MIPI-CSI (CSI0)					
AG5	MIPI_CSI0_CLK_P	–	CSI	AO	MIPI camera serial interface 0 clock – positive
AH4	MIPI_CSI0_CLK_M	–	CSI	AO	MIPI camera serial interface 0 clock – negative
AH6	MIPI_CSI0_LANE0_P	–	CSI	AI, AO	MIPI camera serial interface 0 lane 0 – positive
AJ5	MIPI_CSI0_LANE0_M	–	CSI	AI, AO	MIPI camera serial interface 0 lane 0 – negative
AJ1	MIPI_CSI0_LANE1_P	–	CSI	AI, AO	MIPI camera serial interface 0 lane 1 – positive
AK2	MIPI_CSI0_LANE1_M	–	CSI	AI, AO	MIPI camera serial interface 0 lane 1 – negative
AL1	MIPI_CSI0_LANE2_P	–	CSI	AI, AO	MIPI camera serial interface 0 lane 2 – positive
AL3	MIPI_CSI0_LANE2_M	–	CSI	AI, AO	MIPI camera serial interface 0 lane 2 – negative
AM2	MIPI_CSI0_LANE3_P	–	CSI	AI, AO	MIPI camera serial interface 0 lane 3 – positive
AN1	MIPI_CSI0_LANE3_M	–	CSI	AI, AO	MIPI camera serial interface 0 lane 3 – negative
Four-lane MIPI-CSI (CSI1)					
AC5	MIPI_CSI1_CLK_P	–	CSI	AO	MIPI camera serial interface 1 clock – positive
AD4	MIPI_CSI1_CLK_M	–	CSI	AO	MIPI camera serial interface 1 clock – negative
AD6	MIPI_CSI1_LANE0_P	–	CSI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AE5	MIPI_CSI1_LANE0_M	–	CSI	AI, AO	MIPI camera serial interface 1 lane 0 – negative
AD2	MIPI_CSI1_LANE1_P	–	CSI	AI, AO	MIPI camera serial interface 1 lane 1 – positive
AE1	MIPI_CSI1_LANE1_M	–	CSI	AI, AO	MIPI camera serial interface 1 lane 1 – negative
AF2	MIPI_CSI1_LANE2_P	–	CSI	AI, AO	MIPI camera serial interface 1 lane 2 – positive
AG1	MIPI_CSI1_LANE2_M	–	CSI	AI, AO	MIPI camera serial interface 1 lane 2 – negative
AG3	MIPI_CSI1_LANE3_P	–	CSI	AI, AO	MIPI camera serial interface 1 lane 3 – positive
AH2	MIPI_CSI1_LANE3_M	–	CSI	AI, AO	MIPI camera serial interface 1 lane 3 – negative
Four-lane MIPI CSI (CSI2)					
W5	MIPI_CSI2_CLK_P	–	CSI	AO	MIPI camera serial interface 2 clock – positive
Y4	MIPI_CSI2_CLK_M	–	CSI	AO	MIPI camera serial interface 2 clock – negative
Y6	MIPI_CSI2_LANE0_P	–	CSI	AI, AO	MIPI camera serial interface 2 lane 0 – positive

Table 2-4 Pin descriptions: multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AA5	MIPI_CSI2_LANE0_M	–	CSI	AI, AO	MIPI camera serial interface 2 lane 0 – negative
W1	MIPI_CSI2_LANE1_P	–	CSI	AI, AO	MIPI camera serial interface 2 lane 1 – positive
Y2	MIPI_CSI2_LANE1_M	–	CSI	AI, AO	MIPI camera serial interface 2 lane 1 – negative
AA1	MIPI_CSI2_LANE2_P	–	CSI	AI, AO	MIPI camera serial interface 2 lane 2 – positive
AB2	MIPI_CSI2_LANE2_M	–	CSI	AI, AO	MIPI camera serial interface 2 lane 2 – negative
AC1	MIPI_CSI2_LANE3_P	–	CSI	AI, AO	MIPI camera serial interface 2 lane 3 – positive
AC3	MIPI_CSI2_LANE3_M	–	CSI	AI, AO	MIPI camera serial interface 2 lane 3 – negative
Camera-timing and CCI signals					
BF6	CAM_MCLK0	GPIO_26	P3	DO B-PD:nppukp	Camera master clock 0 – rear camera Configurable I/Os
BG5	CAM_MCLK1	GPIO_27	P3	DO B-PD:nppukp	Camera master clock 1 – front camera Configurable I/Os
BF4	CAM_MCLK2	GPIO_28	P3	DO B-PD:nppukp	Camera master clock 2 – depth camera Configurable I/Os
BH4	CAM_MCLK3	GPIO_128	P3	DO B-PD:nppukp	Camera master clock 3 – depth camera Configurable I/Os
BE5	CCI_I2C_SDA0	GPIO_29	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 0 serial data Configurable I/Os
BC5	CCI_I2C_SCL0	GPIO_30	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 0 clock Configurable I/Os
BD6	CCI_I2C_SDA1	GPIO_31	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 1 serial data Configurable I/Os
BE3	CCI_I2C_SCL1	GPIO_32	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 1 clock Configurable I/Os
U1	CCI_TIMER0	GPIO_33	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/Os
R1	CCI_TIMER1	GPIO_34	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/Os
P2	CCI_TIMER2	GPIO_35	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/Os
R3	CCI_TIMER3	GPIO_36	P3	DO B-PD:nppukp	Camera control interface timer 3 Configurable I/Os
U3	CCI_TIMER4	GPIO_41	P3	DO B-PD:nppukp	Camera control interface timer 4 Configurable I/Os
R5	CCI_ASYNC_IN0	GPIO_38	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/Os
T6	CAM1_STANDBY_N	GPIO_39	P3	DO B-PD:nppukp	Rear camera standby Configurable I/Os
V4	CAM1_RST_N	GPIO_40	P3	DO B-PD:nppukp	Rear camera reset Configurable I/Os

Table 2-4 Pin descriptions: multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF2	CAM2_STANDBY_N 	 GPIO_130	P3	DO B-PD:nppukp	Depth camera standby Configurable I/Os
BE1	CAM2_RST_N 	 GPIO_129	P3	DO B-PD:nppukp	Depth camera reset Configurable I/Os
U5	CAM3_STANDBY_N 	 GPIO_132	P3	DO B-PD:nppukp	Front camera standby Configurable I/Os
V6	CAM3_RST_N 	 GPIO_131	P3	DO B-PD:nppukp	Front camera reset Configurable I/Os
Snapdragon Display Engine vertical sync					
BD4	GPIO_24	–	P3	DI	Snapdragon DE vertical sync – primary
AK38	GPIO_25	–	P3	DI	Snapdragon DE vertical sync – secondary
Display serial interface: Four-lane DSI0					
BB2	MIPI_DSI0_CLK_N	–	DSI	AO	MIPI display serial interface 0 clock – negative
BC1	MIPI_DSI0_CLK_P	–	DSI	AO	MIPI display serial interface 0 clock – positive
AW3	MIPI_DSI0_LANE0_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
AY2	MIPI_DSI0_LANE0_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
BA3	MIPI_DSI0_LANE1_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
BA1	MIPI_DSI0_LANE1_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
AY4	MIPI_DSI0_LANE2_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
AW5	MIPI_DSI0_LANE2_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
BA5	MIPI_DSI0_LANE3_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
AY6	MIPI_DSI0_LANE3_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
AW1	MIPI_DSI0_REXT	–	DSI	AI, AO	MIPI display serial interface 0 external calibration resistor
Display serial interface: Four-lane DSI1					
AN5	MIPI_DSI1_CLK_N	–	DSI	AO	MIPI display serial interface 1 clock – negative
AP4	MIPI_DSI1_CLK_P	–	DSI	AO	MIPI display serial interface 1 clock – positive
AR3	MIPI_DSI1_LANE0_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
AT2	MIPI_DSI1_LANE0_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
AU3	MIPI_DSI1_LANE1_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
AU1	MIPI_DSI1_LANE1_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
AP6	MIPI_DSI1_LANE2_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
AR5	MIPI_DSI1_LANE2_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
AU5	MIPI_DSI1_LANE3_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
AT6	MIPI_DSI1_LANE3_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
AR1	MIPI_DSI1_REXT	–	DSI	AI, AO	MIPI display serial interface 1 external calibration resistor

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-5 Pin descriptions: connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Super-speed USB 3.0					
AC41	USB1_SS_REXT	–	P3	AI, AO	USB1 super-speed – external resistor
AA41	USB1_SS_RX_M	–	P3	AI	USB1 super-speed receive – minus
Y40	USB1_SS_RX_P	–	P3	AI	USB1 super-speed receive – plus
V40	USB1_SS_TX_M	–	P3	AO	USB1 super-speed transmit – minus
U41	USB1_SS_TX_P	–	P3	AO	USB1 super-speed transmit – plus
AE39	USB2_HS_DM	–	P3	AI, AO	USB2 high-speed data – minus
AF38	USB2_HS_DP	–	P3	AI, AO	USB2 high-speed data – plus
AE41	USB2_HS_REXT	–	P3	AI	USB2 high-speed data – external resistor
BB38	USB_SS_SWITCH_SEL 	 GPIO_139	P3	DO B-PD:nppukp	USB Type-C switch control input Configurable I/O
Secure digital controller 1 (SDC 1) interface — supports dual voltage eMMC/NAND interface					
H6	SDC1_CLK	–	P7	B-NP:pdpukp	Secure digital controller 1 clock
G5	SDC1_RCLK	–	P7	DI-PD:nppukp	Secure digital controller 1 return clock
J3	SDC1_CMD	–	P7	B-PD:nppukp	Secure digital controller 1 command
K6	SDC1_DATA_0	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 0
L7	SDC1_DATA_1	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 1
H4	SDC1_DATA_2	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 2
G3	SDC1_DATA_3	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 3
J7	SDC1_DATA_4	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 4
J5	SDC1_DATA_5	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 5
H2	SDC1_DATA_6	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 6
G1	SDC1_DATA_7	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 7
Secure digital controller 2 (SDC 2) interface — supports dual voltage SD 3.0 card interface					
L1	SDC2_CLK	–	P2	BH-NP:pdpukp	Secure digital controller 2 clock
K4	SDC2_CMD	–	P2	BH-PD:nppukp	Secure digital controller 2 command
K2	SDC2_DATA_0	–	P2	BH-PD:nppukp	Secure digital controller 2 data bit 0
L3	SDC2_DATA_1	–	P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
L5	SDC2_DATA_2	–	P2	BH-PD:nppukp	Secure digital controller 2 data bit 2
M6	SDC2_DATA_3	–	P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
T4	SD_CARD_DET_N 	 GPIO_133	P3	DI B-PD:nppukp	Secure digital card detection Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AP38	SD_WRITE_PROTECT	GPIO_50	P3	DI B-PD:nppukp	Secure digital card write protection Configurable I/O
UIM interface – UIM 1					
AR39	UIM1_DATA	GPIO_51	P5	B B-PD:nppukp	Dual voltage UIM1 data Configurable I/O
AU41	UIM1_CLK	GPIO_52	P5	DO B-PD:nppukp	Dual voltage UIM1 clock Configurable I/O
AT40	UIM1_RESET	GPIO_53	P5	DO B-PD:nppukp	Dual voltage UIM1 reset Configurable I/O
AV40	UIM1_DETECT	GPIO_54	P3	DI B-PD:nppukp	UIM1 detect (nondual voltage) Configurable I/O
UIM interface – UIM 2					
AN35	UIM2_DATA	GPIO_55	P6	B B-PD:nppukp	Dual voltage UIM2 data Configurable I/O
AT38	UIM2_CLK	GPIO_56	P6	DO B-PD:nppukp	Dual voltage UIM2 clock Configurable I/O
AP36	UIM2_RESET	GPIO_57	P6	DO B-PD:nppukp	Dual voltage UIM2 reset Configurable I/O
AR37	UIM2_DETECT	GPIO_58	P3	DI B-PD:nppukp	UIM2 detect (nondual voltage) Configurable I/O
Additional UIM control					
AN37	UIM_BATT_ALARM	GPIO_49	P3	DI B-PD:nppukp	UIM battery alarm Configurable I/O
Sensor and keypad					
AL35	ACCEL_INT	GPIO_42	P3	DI B-PD:nppukp	Accelerometer sensor interrupt Configurable I/O
AL39	ALSP_INT_N	GPIO_43	P3	DI B-PD:nppukp	Ambient light sensor interrupt Configurable I/O
AN41	MAG_INT	GPIO_44	P3	DI B-PD:nppukp	Magnetic sensor interrupt Configurable I/O
AM40	GYRO_INT	GPIO_45	P3	DI B-PD:nppukp	Gyro sensor interrupt Configurable I/O
AL37	PRESSURE_INT	GPIO_46	P3	DI B-PD:nppukp	Pressure sensor interrupt Configurable I/O
M36	KEY_VOLP_N	GPIO_85	P3	DI B-PD:nppukp	Volume key interrupt Configurable I/O
N37	KEY_SNAPSHOT	GPIO_86	P3	DI B-PD:nppukp	Snapshot interrupt Configurable I/O
M38	KEY_FOCUS	GPIO_87	P3	DI B-PD:nppukp	Focus interrupt Configurable I/O
G39	KEY_HOME	GPIO_88	P3	DI B-PD:nppukp	Home key interrupt Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BD8	SMB_INT GPIO_1		P3	DO B-PD:nppukp	SMB charger interrupt Configurable I/O
Audio MI^{2}S master clocks					
AK38	PRI_MI2S_MCLK_A	GPIO_25	P3	DO B-PD:nppukp	Primary MI^{2}S master clock A Configurable I/O
AK38	SEC_MI2S_MCLK_A	GPIO_25	P3	DO B-PD:nppukp	Secondary MI^{2}S master clock A Configurable I/O
AK36	PRI_MI2S_MCLK_B	GPIO_69	P3	DO B-PD:nppukp	Primary MI^{2}S master clock B Configurable I/O
K38	PRI_MI2S_MCLK_C	GPIO_66	P3	DO B-PD:nppukp	Primary MI^{2}S master clock C Configurable I/O
K38	SEC_MI2S_MCLK_B	GPIO_66	P3	DO B-PD:nppukp	Secondary MI^{2}S master clock B Configurable I/O
Audio MI^{2}S interface 1 – primary					
H36	MI2S_1_SCK	GPIO_91	P3	B B-PD:nppukp	MI^{2}S 1-bit clock Configurable I/O
J35	MI2S_1_WS	GPIO_92	P3	B B-PD:nppukp	MI^{2}S 1 word select (L/R) Configurable I/O
K36	MI2S_1_D0	GPIO_93	P3	B B-PD:nppukp	MI^{2}S 1 serial data channel 0 Configurable I/O
G39	MI2S_1_D1	GPIO_88	P3	B B-PD:nppukp	MI^{2}S 1 serial data channel 1 Configurable I/O
J37	MI2S_1_D2	GPIO_94	P3	B B-PD:nppukp	MI^{2}S 1 serial data channel 2 Configurable I/O
L35	MI2S_1_D3	GPIO_95	P3	B B-PD:nppukp	MI^{2}S 1 serial data channel 3 Configurable I/O
Audio MI^{2}S interface 2 – secondary					
BA39	MI2S_2_SCK	GPIO_135	P3	B B-PD:nppukp	MI^{2}S 2-bit clock Configurable I/O
BB40	MI2S_2_WS	GPIO_136	P3	B B-PD:nppukp	MI^{2}S 2 word select (L/R) Configurable I/O
BA37	MI2S_2_D0	GPIO_137	P3	B B-PD:nppukp	MI^{2}S 2 serial data channel 0 Configurable I/O
AY38	MI2S_2_D1	GPIO_138	P3	B B-PD:nppukp	MI^{2}S 2 serial data channel 1 Configurable I/O
Audio codec interface					
AK40	CDC_PDM_RX2	GPIO_74	P3	DO B-PD:nppukp	PDM receive data channel 2 Configurable I/O
AJ41	CDC_PDM_RX1	GPIO_73	P3	DO B-PD:nppukp	PDM receive data channel 1 Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AH36	CDC_PDM_RX0	 GPIO_72	P3	DO B-PD:nppukp	PDM receive data channel 0 Configurable I/O
AH38	CDC_PDM_TX0	 GPIO_71	P3	DI B-PD:nppukp	PDM Transmit data channel 0 Configurable I/O
AH40	CDC_PDM_SYNC	 GPIO_70	P3	DO B-PD:nppukp	PDM synchronization signal Configurable I/O
AK36	CDC_PDM_CLK	 GPIO_69	P3	DO B-PD:nppukp	Audio codec PDM clock signal and codec master clock Configurable I/O
AJ37	CDC_PDM_RX0_DRE	GPIO_67	P3	DO B-PD:nppukp	PDN RX0 DRE data channel Configurable I/O
AJ39	CDC_PDM_RX1_DRE	GPIO_68	P3	DO PD:nppukp	PDN RX1 DRE data channel Configurable I/O
Audio SLIMbus – low-power audio subsystem					
AH40	SLIMBUS_CLK	 GPIO_70	P3	DO B-PD:nppukp	Low-power audio SLIMbus clock Configurable I/O
AH38	SLIMBUS_DATA0	 GPIO_71	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 0 Configurable I/O
AH36	SLIMBUS_DATA1	 GPIO_72	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 1 Configurable I/O
Digital microphone interface					
G37	DMIC0_CLK	 GPIO_89	P3	DO B-PD:nppukp	Digital MIC0 clock Configurable I/O
H38	DMIC0_DATA	 GPIO_90	P3	DI B-PD:nppukp	Digital MIC0 data Configurable I/O
J37	WSA_IO_DATA	 GPIO_94 MI2S_1_D2	P3	DI B-PD:nppukp B	WSA8810 current/voltage sense data for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) Configurable I/O MI^{2}S 1 serial data channel 2
L35	WSA_IO_CLK	 GPIO_95 MI2S_1_D3	P3	DO B-PD:nppukp B	WSA8810 current/voltage sense clock for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) Configurable I/O MI^{2}S 1 serial data channel 3
BAM-based low-speed peripheral interface 1 – BLSP 1					
BB8	BLSP1_3	 GPIO_0	P3	B B-PD:nppukp	BLSP 1 bit 3; SPI Configurable I/O
BD8	BLSP1_2	 GPIO_1	P3	B B-PD:nppukp	BLSP 1 bit 2; SPI Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BC7	BLSP1_1	GPIO_2	P3	B B-PD:nppukp	BLSP 1 bit 1; SPI/I^{2}C Configurable I/O
BE7	BLSP1_0	GPIO_3	P3	B B-PD:nppukp	BLSP 1 bit 0; SPI/I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 2 – BLSP 2					
AW37	BLSP2_3	GPIO_4	P3	B B-PD:nppukp	BLSP 2 bit 3; SPI/UART Configurable I/O
AV36	BLSP2_2	GPIO_5	P3	B B-PD:nppukp	BLSP 2 bit 2; SPI/UART Configurable I/O
AU35	BLSP2_1	GPIO_6	P3	B B-PD:nppukp	BLSP 2 bit 1; SPI/I^{2}C/UART Configurable I/O
AY36	BLSP2_0	GPIO_7	P3	B B-PD:nppukp	BLSP 2 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM based low speed peripheral interface 3 – BLSP 3					
AU39	BLSP3_3	GPIO_8	P3	B B-PD:nppukp	BLSP 3 bit 3; SPI Configurable I/O
AV38	BLSP3_2	GPIO_9	P3	B B-PD:nppukp	BLSP 3 bit 2; SPI Configurable I/O
AW39	BLSP3_1	GPIO_10	P3	B B-PD:nppukp	BLSP 3 bit 1; SPI/I^{2}C Configurable I/O
AU37	BLSP3_0	GPIO_11	P3	B B-PD:nppukp	BLSP 3 bit 0; SPI/I^{2}C Configurable I/O
BAM based low-speed peripheral interface 4 – BLSP 4					
AT36	BLSP4_3	GPIO_12	P3	B B-PD:nppukp	BLSP 4 bit 3; SPI/UART Configurable I/O
AR35	BLSP4_2	GPIO_13	P3	B B-PD:nppukp	BLSP 4 bit 2; SPI/UART Configurable I/O
AY40	BLSP4_1	GPIO_14	P3	B B-PD:nppukp	BLSP 4 bit 1; SPI/I^{2}C/UART Configurable I/O
BA41	BLSP4_0	GPIO_15	P3	B B-PD:nppukp	BLSP 4 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM-based low-speed peripheral interface 5 – BLSP 5					
BF8	BLSP5_3	GPIO_16	P3	B B-PD:nppukp	BLSP 5 bit 3; SPI/UART Configurable I/O
BG7	BLSP5_2	GPIO_17	P3	B B-PD:nppukp	BLSP 5 bit 2; SPI/UART Configurable I/O
BH8	BLSP5_1	GPIO_18	P3	B B-PD:nppukp	BLSP 5 bit 1; SPI/I^{2}C/UART Configurable I/O
BH6	BLSP5_0	GPIO_19	P3	B B-PD:nppukp	BLSP 5 bit 0; SPI/I^{2}C/UART Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 6 – BLSP 6					
K40	BLSP6_3	GPIO_20	P3	B B-PD:nppukp	BLSP 6 bit 3; SPI/UART Configurable I/O
L39	BLSP6_2	GPIO_21	P3	B B-PD:nppukp	BLSP 6 bit 2; SPI/UART Configurable I/O
M40	BLSP6_1	GPIO_22	P3	B B-PD:nppukp	BLSP 6 bit 1; SPI/I^{2}C/UART Configurable I/O
L41	BLSP6_0	GPIO_23	P3	B B-PD:nppukp	BLSP 6 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM-based low-speed peripheral interface 7 – BLSP 7					
BA37	BLSP7_3	GPIO_137	P3	B B-PD:nppukp	BLSP 7 bit 3; SPI Configurable I/O
AY38	BLSP7_2	GPIO_138	P3	B B-PD:nppukp	BLSP 7 bit 2; SPI Configurable I/O
BB40	BLSP7_1	GPIO_136	P3	B B-PD:nppukp	BLSP 7 bit 1; SPI/I^{2}C Configurable I/O
BA39	BLSP7_0	GPIO_135	P3	B B-PD:nppukp	BLSP 7 bit 0; SPI/I^{2}C Configurable I/O
BAM-based low-speed peripheral interface 8 – BLSP 8					
E41	BLSP8_3	GPIO_96	P3	B B-PD:nppukp	BLSP 8 bit 3; SPI Configurable I/O
G41	BLSP8_2	GPIO_97	P3	B B-PD:nppukp	BLSP 8 bit 2; SPI Configurable I/O
H40	BLSP8_1	GPIO_98	P3	B B-PD:nppukp	BLSP 8 bit 1; SPI/I^{2}C Configurable I/O
J39	BLSP8_0	GPIO_99	P3	B B-PD:nppukp	BLSP 8 bit 0; SPI/I^{2}C Configurable I/O
SPI extra chip selects (supplements BLSP ports configured for the SPI protocol)					
P2	SPI1_CS1	GPIO_35	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP1
R3	SPI1_CS2	GPIO_36	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP1
U3	SPI3_CS1	GPIO_41	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP3 Configurable I/O
AP38	SPI3_CS2	GPIO_50	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP3 Configurable I/O
AP40	SPI6_CS1	GPIO_48	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP6 Configurable I/O
AM38	SPI6_CS2	GPIO_47	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP6 Configurable I/O
G37	SPI7_CS1	GPIO_89	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP7 Configurable I/O
H38	SPI7_CS2	GPIO_90	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP7 Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

BLSP interfaces

The BAM integrates three serial bus cores: UARTDM, SPI, and I^{2}C. The SPI and I^{2}C cores are, in turn, integrated into a single core called the Qualcomm unified peripheral (QUP) where both the subcores share the same FIFO. The UARTDM is integrated separately with its own FIFO. All the cores share the same bus interface.

The external I/O ports of these cores are shared and only one of the cores can be used at any given time. However, in the mode where UARTDM is used as a two-pin UART interface, the I^{2}C, which is also a two-pin interface, can be used simultaneously with UART functionality. The BLSP supports the following serial protocols:

- UART_DM
- I^{2}C (master only), driven by QUP
- SPI, driven by QUP

Table 2-6 BLSP alternate function configurations

Pad name	Alternate functions		
GPIO[0]	SPI1_MOSI	–	–
GPIO[1]	SPI1_MISO	–	–
GPIO[2]	SPI1_CS	–	I2C1_SDA
GPIO[3]	SPI1_CLK	–	I2C1_SCL
GPIO[4]	SPI2_MOSI	UART2_Tx	–
GPIO[5]	SPI2_MISO	UART2_Rx	–
GPIO[6]	SPI2_CS	UART2_CTS	I2C2_SDA
GPIO[7]	SPI2_CLK	UART2_RTS	I2C2_SCL
GPIO[8]	SPI3_MOSI	–	–
GPIO[9]	SPI3_MISO	–	–
GPIO[10]	SPI3_CS	–	I2C3_SDA
GPIO[11]	SPI3_CLK	–	I2C3_SCL
GPIO[12]	SPI4_MOSI	UART4_Tx	–
GPIO[13]	SPI4_MISO	UART4_Rx	–
GPIO[14]	SPI4_CS	UART4_CTS	I2C4_SDA
GPIO[15]	SPI4_CLK	UART4_RTS	I2C4_SCL
GPIO[16]	SPI5_MOSI	UART5_Tx	–
GPIO[17]	SPI5_MISO	UART5_Rx	–
GPIO[18]	SPI5_CS	UART5_CTS	I2C5_SDA
GPIO[19]	SPI5_CLK	UART5_RTS	I2C5_SCL

Table 2-6 BLSP alternate function configurations

Pad name	Alternate functions		
GPIO[20]	SPI6_MOSI	UART6_Tx	–
GPIO[21]	SPI6_MISO	UART6_Rx	–
GPIO[22]	SPI6_CS	UART6_CTS	I2C6_SDA
GPIO[23]	SPI6_CLK	UART6_RTS	I2C6_SCL
GPIO[137]	SPI7_MOSI	–	–
GPIO[138]	SPI7_MISO	–	–
GPIO[136]	SPI7_CS	–	I2C7_SDA
GPIO[135]	SPI7_CLK	–	I2C7_SCL
GPIO[96]	SPI8_MOSI	–	–
GPIO[97]	SPI8_MISO	–	–
GPIO[98]	SPI8_CS	–	I2C8_SDA
GPIO[99]	SPI8_CLK	–	I2C8_SCL

Table 2-7 BLSP internal pin mapping

Options	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
GPIO pins BLSP 1		GPIO[0]	GPIO[1]	GPIO[2]	GPIO[3]
GPIO pins BLSP 2		GPIO[4]	GPIO[5]	GPIO[6]	GPIO[7]
GPIO pins BLSP 3		GPIO[8]	GPIO[9]	GPIO[10]	GPIO[11]
GPIO pins BLSP 4		GPIO[12]	GPIO[13]	GPIO[14]	GPIO[15]
GPIO pins BLSP 5		GPIO[16]	GPIO[17]	GPIO[18]	GPIO[19]
GPIO pins BLSP 6		GPIO[20]	GPIO[21]	GPIO[22]	GPIO[23]
GPIO pins BLSP 7		GPIO_137	GPIO_138	GPIO_136	GPIO_135
GPIO pins BLSP 8		GPIO_96	GPIO_97	GPIO_98	GPIO_99
1	4-pin UART	UART_Tx DO 4-pin UART Transmit data	UART_Rx DI 4-pin UART Receive data	UART_CTS DI 4-pin UART Clear-to-send	UART_RTS DO 4-pin UART Ready-for-receive
2	2-pin UART + I2C	UART_Tx DO 2-pin UART Transmit data	UART_Rx DI 2-pin UART Receive data	I2C_SDA B I^{2}C serial data	I2C_SCL B I^{2}C serial clock
3	4-pin SPI	SPI_MOSI B SPI master out Slave in	SPI_MISO B SPI master in Slave out	SPI_CS B SPI chip select	SPI_CLK B SPI clock
4	2-pin UART + GPIO	UART_Tx DO 2-pin UART Transmit data	UART_Rx DI 2-pin UART Receive data	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O

Table 2-7 BLSP internal pin mapping (cont.)

Options	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
5	I2C + GPIO	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	I2C_SDA B I^{2}C serial data	I2C_SCL B I^{2}C serial clock
6	GPIO	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O

As noted throughout the pin definition tables, GPIO assignments must be done carefully to avoid conflicts and to ensure that the intended functionality is achieved. For GPIOs that can be used as BLSPs, additional factors should be considered when making functional assignments:

- Extra chip selects are available when certain BLSPs are used for SPI:
  - BLSP 1, BLSP 3, BLSP 6, and BLSP 7 have an extra CS for SPI.
- SPI is only supported via BLSP, and each BLSP supports a different SPI.
- I^{2}C is supported by each BLSP. All BLSPs use bits [1:0] for I^{2}C.
- Additional I^{2}C ports (besides the BLSP versions) are available:
  - Camera
  - Audio codec (connected internally)

Table 2-8 Pin descriptions: internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
JTAG					
P4	SRST_N	–	P3	DI	JTAG reset for debug
N3	TCK	–	P3	DI	JTAG clock input
P6	TDI	–	P3	DI	JTAG data input
M4	TDO	–	P3	DO-Z	JTAG data output
M2	TMS	–	P3	B	JTAG mode-select input
N5	TRST_N	–	P3	DI	JTAG reset
General-purpose clocks, PDM, and related signals					
U1	GP_CLK0_A 	 GPIO_33	P3	DO B-PD:nppukp	General-purpose clock output 0A Configurable I/O
R3	GP_CLK0_B 	 GPIO_36	P3	DO B-PD:nppukp	General-purpose clock output 0B Configurable I/O
R1	GP_CLK1_A 	 GPIO_34	P3	DO B-PD:nppukp	General-purpose clock output 1A Configurable I/O
U3	GP_CLK1_B 	 GPIO_41	P3	DO B-PD:nppukp	General-purpose clock output 1B Configurable I/O
T6	GP_MN 	 GPIO_39	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O

Table 2-8 Pin descriptions: internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
K38	GP_PDM_0A 	 GPIO_66	P3	DO B-PD:nppukp	General-purpose PDM output 0A Configurable I/O
AP40	GP_PDM_0B 	 GPIO_48	P3	DO B-PD:nppukp	General-purpose PDM output 0B Configurable I/O
AM40	GP_PDM_1A 	 GPIO_45	P3	DO B-PD:nppukp	General-purpose PDM output 1A Configurable I/O
G37	GP_PDM_1B 	 GPIO_89	P3	DO B-PD:nppukp	General-purpose PDM output 1B Configurable I/O
BE41	GP_PDM_2A 	 GPIO_60	P3	DO B-PD:nppukp	General-purpose PDM output 2A Configurable I/O
R5	GP_PDM_2B 	 GPIO_38	P3	DO B-PD:nppukp	General-purpose PDM output 2B Configurable I/O
Reset and mode control					
U7	MODE_0	–	P3	DIS-PD	Mode control bit 0
R7	MODE_1	–	P3	DIS-PD	Mode control bit 1
AW35	RESOUT_N	–	P3	DO	Reset output
Wake-up pins for SDM power management					
BD8	GPIO_1	–	P3	B-PD:nppukp	General-purpose wake interrupt
AT36	GPIO_12	–	P3	B-PD:nppukp	General-purpose wake interrupt
BE1	GPIO_129	–	P3	B-PD:nppukp	General-purpose wake interrupt
AR35	GPIO_13	–	P3	B-PD:nppukp	General-purpose wake interrupt
BF2	GPIO_130	–	P3	B-PD:nppukp	General-purpose wake interrupt
V6	GPIO_131	–	P3	B-PD:nppukp	General-purpose wake interrupt
U5	GPIO_132	–	P3	B-PD:nppukp	General-purpose wake interrupt
T4	GPIO_133	–	P3	B-PD:nppukp	General-purpose wake interrupt
BA37	GPIO_137	–	P3	B-PD:nppukp	General-purpose wake interrupt
AY38	GPIO_138	–	P3	B-PD:nppukp	General-purpose wake interrupt
BB38	GPIO_139	–	P3	B-PD:nppukp	General-purpose wake interrupt
BC39	GPIO_140	–	P3	B-PD:nppukp	General-purpose wake interrupt
BC41	GPIO_141	–	P3	B-PD:nppukp	General-purpose wake interrupt
BG7	GPIO_17	–	P3	B-PD:nppukp	General-purpose wake interrupt
L39	GPIO_21	–	P3	B-PD:nppukp	General-purpose wake interrupt
AK38	GPIO_25	–	P3	B-PD:nppukp	General-purpose wake interrupt
BF4	GPIO_28	–	P3	B-PD:nppukp	General-purpose wake interrupt
BD6	GPIO_31	–	P3	B-PD:nppukp	General-purpose wake interrupt
R1	GPIO_34	–	P3	B-PD:nppukp	General-purpose wake interrupt
P2	GPIO_35	–	P3	B-PD:nppukp	General-purpose wake interrupt
R3	GPIO_36	–	P3	B-PD:nppukp	General-purpose wake interrupt
L37	GPIO_37	–	P3	B-PD:nppukp	General-purpose wake interrupt
R5	GPIO_38	–	P3	B-PD:nppukp	General-purpose wake interrupt

Table 2-8 Pin descriptions: internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AL35	GPIO_42	–	P3	B-PD:nppukp	General-purpose wake interrupt
AL39	GPIO_43	–	P3	B-PD:nppukp	General-purpose wake interrupt
AN41	GPIO_44	–	P3	B-PD:nppukp	General-purpose wake interrupt
AM40	GPIO_45	–	P3	B-PD:nppukp	General-purpose wake interrupt
AL37	GPIO_46	–	P3	B-PD:nppukp	General-purpose wake interrupt
AP40	GPIO_48	–	P3	B-PD:nppukp	General-purpose wake interrupt
AV36	GPIO_5	–	P3	B-PD:nppukp	General-purpose wake interrupt
AV40	GPIO_54	–	P3	B-PD:nppukp	UIM1 presence detection
AR37	GPIO_58	–	P3	B-PD:nppukp	UIM2 presence detection
BD40	GPIO_59	–	P3	B-PD:nppukp	General-purpose wake interrupt
BE41	GPIO_60	–	P3	B-PD:nppukp	General-purpose wake interrupt
BE39	GPIO_61	–	P3	B-PD:nppukp	General-purpose wake interrupt
BG3	GPIO_62	–	P3	B-PD:nppukp	General-purpose wake interrupt
BB20	GPIO_63	–	P3	B-PD:nppukp	General-purpose wake interrupt
AM36	GPIO_65	–	P3	B-PD:nppukp	General-purpose wake interrupt
AJ37	GPIO_67	–	P3	B-PD:nppukp	General-purpose wake interrupt
AH40	GPIO_70	–	P3	B-PD:nppukp	General-purpose wake interrupt
AH38	GPIO_71	–	P3	B-PD:nppukp	General-purpose wake interrupt
AH36	GPIO_72	–	P3	B-PD:nppukp	General-purpose wake interrupt
AJ41	GPIO_73	–	P3	B-PD:nppukp	General-purpose wake interrupt
AK40	GPIO_74	–	P3	B-PD:nppukp	General-purpose wake interrupt
BH12	GPIO_81	–	P3	B-PD:nppukp	General-purpose wake interrupt
M36	GPIO_85	–	P3	B-PD:nppukp	General-purpose wake interrupt
N37	GPIO_86	–	P3	B-PD:nppukp	General-purpose wake interrupt
M38	GPIO_87	–	P3	B-PD:nppukp	General-purpose wake interrupt
AV38	GPIO_9	–	P3	B-PD:nppukp	General-purpose wake interrupt
H38	GPIO_90	–	P3	B-PD:nppukp	General-purpose wake interrupt
H36	GPIO_91	–	P3	B-PD:nppukp	General-purpose wake interrupt
K36	GPIO_93	–	P3	B-PD:nppukp	General-purpose wake interrupt
G41	GPIO_97	–	P3	B-PD:nppukp	General-purpose wake interrupt
L7	SDC1_DATA_1	–	P7	BH-PD:nppukp	Secure digital controller 1 data bit 1
G3	SDC1_DATA_3	–	P7	BH-PD:nppukp	Secure digital controller 1 data bit 3
L3	SDC2_DATA_1	–	P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
M6	SDC2_DATA_3	–	P2	BH-PD:nppukp	SDC card detect wake up
P4	SRST_N	–	P3	DI	JTAG reset for debug

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-9 Pin descriptions: chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WTR-Rx baseband interface [2]					
BF28	BBRX_I_I_CH0	–	–	AI	Baseband receiver input, channel 0, in-phase
BH28	BBRX_I_I_CH1	–	–	AI	Baseband receiver input, channel 1, in-phase
BF24	BBRX_I_I_CH2	–	–	AI	Baseband receiver input, channel 2, in-phase
BF22	BBRX_I_I_CH3	–	–	AI	Baseband receiver input, channel 3, in-phase
BF26	BBRX_I_Q_CH0	–	–	AI	Baseband receiver input, channel 0, quadrature
BH26	BBRX_I_Q_CH1	–	–	AI	Baseband receiver input, channel 1, quadrature
BH24	BBRX_I_Q_CH2	–	–	AI	Baseband receiver input, channel 2, quadrature
BH22	BBRX_I_Q_CH3	–	–	AI	Baseband receiver input, channel 3, quadrature
WTR-Tx baseband interface [2]					
BF36	TXDAC0_IM	–	–	AO	Transmitter DAC 0 output, in-phase minus
BG35	TXDAC0_IP	–	–	AO	Transmitter DAC 0 output, in-phase plus
BG37	TXDAC0_QM	–	–	AO	Transmitter DAC 0 output, quadrature minus
BH38	TXDAC0_QP	–	–	AO	Transmitter DAC 0 output, quadrature plus
BA29	TXDAC0_VREF	–	–	AI	Transmitter DAC 0 voltage reference
BG31	TXDAC1_IM	–	–	AO	Transmitter DAC 1 output, in-phase minus
BH30	TXDAC1_IP	–	–	AO	Transmitter DAC 1 output, in-phase plus
BF32	TXDAC1_QM	–	–	AO	Transmitter DAC 1 output, quadrature minus
BG33	TXDAC1_QP	–	–	AO	Transmitter DAC 1 output, quadrature plus
BA27	TXDAC1_VREF	–	–	AI	Transmitter DAC 1 voltage reference
GNSS					
BD34	GNSS_BB_IP	–	–	AI	GNSS receiver baseband input, in-phase plus
BD36	GNSS_BB_QP	–	–	AI	GNSS receiver baseband input, quadrature plus
GSM [2]					
BB18	GSM_TX_PHASE_TXDAC1	GPIO_115	P3	DO B-PD:nppukp	GSM transmit phase adjusts data bit associated with TXDAC1 Configurable I/O
BD18	GSM_TX_PHASE_TXDAC0	GPIO_117	P3	DO B-PD:nppukp	GSM transmit phase adjusts data bit associated with TXDAC0 Configurable I/O
PMIC					
N39	PMIC_SPMI_CLK	–	P3	DO	Slave and PBUS interface for PMICs – clock
P38	PMIC_SPMI_DATA	–	P3	B	Slave and PBUS interface for PMICs – data
R37	PS_HOLD	–	P3	DO	Power supply hold signal to PMIC

Table 2-9 Pin descriptions: chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
P40	RESIN_N	–	P3	DI	Reset input
R41	SLEEP_CLK	–	P3	DI	Sleep clock
T38	CXO	–	P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
R39	CXO_EN	–	P3	DO	Core crystal oscillator enable
WLAN signals					
AT12	WLAN_BB_I_M	–	–	AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
AU13	WLAN_BB_I_P	–	–	AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
AV12	WLAN_BB_Q_M	–	–	AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
AU11	WLAN_BB_Q_P	–	–	AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
AY12	WLAN_RSET	–	–	AI	WLAN external resistor
BC9	WCSS_XO	–	–	DI	WLAN reference clock
BB10	WLAN_DATA[2]	GPIO_76	P3	B-PD:nppukp	WLAN data bit 2 Configurable I/Os
BD10	WLAN_DATA[1]	GPIO_77	P3	B-PD:nppukp	WLAN data bit 1 Configurable I/Os
BC11	WLAN_DATA[0]	GPIO_78	P3	B-PD:nppukp	WLAN data bit 0 Configurable I/Os
BF12	WLAN_SET	GPIO_79	P3	B-PD:nppukp	WLAN set Configurable I/Os
BG11	WLAN_CLK	GPIO_80	P3	B-PD:nppukp	WLAN clock Configurable I/Os
Bluetooth signals					
BE11	BT_CTRL	GPIO_83	P3	B-PD:nppukp	Bluetooth control Configurable I/Os
BG9	BT_DAT_STB	GPIO_84	P3	B-PD:nppukp	Bluetooth dual-function: data and strobe Configurable I/Os
BE9	BT_SSBI	GPIO_75	P3	B-PD:nppukp	Bluetooth single-wire serial bus interface Configurable I/Os
FM signals					
BH12	FM_SSBI	GPIO_81	P3	B-PD:nppukp	FM radio serial data interface Configurable I/O **Note**: If FM is not used, leave GPIO_81 as no connect (floating).
BF10	FM_SDI	GPIO_82	P3	B-PD:nppukp	FM radio single-wire serial bus interface Configurable I/O **Note**: If FM is not used, leave GPIO_82 as no connect (floating).

1. See Table 2-1 for parameter and acronym definitions.
2. Base band receiver input (BBRX), Transmitter DAC (TXDAC), and GSM TX configurations are not supported in SDA450. See *SDM450/SDA450 + PMI8952 + PM8953 Reference Schematic* (80-PC173-41), and *SDM450/SDA450 Digital Baseband Design Guidelines /Training Slides* (80-PC173-5B) for connection details.

Table 2-10 Pin descriptions: RF front-end functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
General RF control signal [2]					
BG15	GRFC(0)	GPIO_100	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/Os
BD14	GRFC(1)	GPIO_101	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O
BF14	GRFC(2)	GPIO_102	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
BG13	GRFC(3)	GPIO_103	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O
BC13	GRFC(4)	GPIO_104	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
BE13	GRFC(5)	GPIO_105	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
BB12	GRFC(6)	GPIO_106	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
BD12	GRFC(7)	GPIO_107	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
BD20	GRFC(8)	GPIO_108	P3	DO B-PD:nppukp	Generic RF controller bit 8 Configurable I/O
BC19	GRFC(9)	GPIO_109	P3	DO B-PD:nppukp	Generic RF controller bit 9 Configurable I/O
BF20	GRFC(10)	GPIO_110	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
BH20	GRFC(11)	GPIO_111	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
BE19	GRFC(12)	GPIO_112	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
BF40	GRFC(13)	GPIO_113	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
BG19	GRFC(14)	GPIO_114	P3	DO B-PD:nppukp	Generic RF controller bit 14 Configurable I/O
BB18	GRFC(15)/GSM1_tx_phase_d	GPIO_115	P3	DO B-PD:nppukp	Generic RF controller bit 15 Configurable I/O
BF18	GRFC(28)/ext_gps_lna_en0	GPIO_116	P3	DO B-PD:nppukp	Generic RF controller bit 28 Configurable I/O
BD18	GRFC(27)/GAM0_tx_phase_d	GPIO_117	P3	DO B-PD:nppukp	Generic RF controller bit 27 Configurable I/O
Qualcomm RF Front End [3]					
BC17	RFFE1_CLK	GPIO_118	P3	DO B-PD:nppukp	MIPI_RFFE 1 clock Configurable I/O
BE17	RFFE1_DATA	GPIO_119	P3	B B-PD:nppukp	MIPI_RFFE 1 data Configurable I/O

Table 2-10 Pin descriptions: RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BG17	RFFE2_CLK		P3	DO	MIPI_RFFE 2 clock
		GPIO_120		B-PD:nppukp	Configurable I/Os
BF16	RFFE2_DATA		P3	B	MIPI_RFFE 2 data
		GPIO_121		B-PD:nppukp	Configurable I/O
BC15	RFFE3_CLK		P3	DO	MIPI_RFFE 3 clock
		GPIO_126		B-PD:nppukp	Configurable I/O
BB14	RFFE3_DATA		P3	B	MIPI_RFFE 3 data
		GPIO_127		B-PD:nppukp	Configurable I/O
BB16	RFFE4_CLK		P3	DO	MIPI_RFFE 4 clock
		GPIO_122		B-PD:nppukp	Configurable I/O
BD16	RFFE4_DATA		P3	B	MIPI_RFFE 4 data
		GPIO_123		B-PD:nppukp	Configurable I/O
BH16	RFFE5_CLK		P3	DO	MIPI_RFFE 5 clock
		GPIO_124		B-PD:nppukp	Configurable I/O
BE15	RFFE5_DATA		P3	B	MIPI_RFFE 5 data
		GPIO_125		B-PD:nppukp	Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.
2. Only GPIO configurations are supported on GRFC pins in SDA450. See *SDM450/SDA450 + PMI8952 + PM8953 Reference Schematics* (80-PC173-41) and *SDM632 + PMI632 + PM8953 Reference Schematic* (80-PF078-41) for connection details.
3. RFFE_CLK and RFFE_DATA configuration is not supported in SDA450. However, the RFFE_CLK and RFFE_DATA can be used as the GPIO pins. See *SDM450/SDA450 + PMI8952 + PM8953 Reference Schematic* (80-PC173-41), *SDM632 + PMI632 + PM8953 Reference Schematic* (80-PF078-41), and *SDM450/SDA450 Digital Baseband Design Guidelines /Training Slides* (80-PC173-5B) for connection details.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, Qualcomm Technologies, Inc. (QTI) provides an Excel spreadsheet that lists all SDM450/SDA450 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.
Click the following link to download the *SDM450/SDA450 GPIO Configuration Spreadsheet* (80-PC173-1B) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PC173-1B

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.
For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-11 Pin descriptions: general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB8	GPIO_0		P3	B-PD:nppukp	Configurable I/O
		SPI1_MOSI		B	BLSP 1 bit 3; SPI
BD8	GPIO_1		P3	B-PD:nppukp	Configurable I/O
		SPI1_MISO		B	BLSP 1 bit 2; SPI
		SMB_INT		DO	SMB charger interrupt
BC7	GPIO_2		P3	B-PD:nppukp	Configurable I/O
		SPI1_CS		B	BLSP 1 bit 1; SPI
		I2C1_SDA		B	BLSP 1 bit 1; I^{2}C
BE7	GPIO_3		P3	B-PD:nppukp	Configurable I/O
		SPI1_CLK		B	BLSP 1 bit 0; SPI
		I2C1_SCL		B	BLSP 1 bit 0; I^{2}C
AW37	GPIO_4		P3	B-PD:nppukp	Configurable I/O
		SPI2_MOSI		B	BLSP 2 bit 3; SPI
		UART2_TX		B	BLSP 2 bit 3; UART
AV36	GPIO_5		P3	B-PD:nppukp	Configurable I/O
		SPI2_MISO		B	BLSP 2 bit 2; SPI
		UART2_RX		B	BLSP 2 bit 2; UART
		LDO_EN		DO	External LDO enable
AU35	GPIO_6		P3	B-PD:nppukp	Configurable I/O
		SPI2_CS		B	BLSP 2 bit 1; SPI
		UART2_CTS		B	BLSP 2 bit 1; UART
		I2C2_SDA		B	BLSP 2 bit 1; I^{2}C
AY36	GPIO_7		P3	B-PD:nppukp	Configurable I/O
		SPI2_CLK		B	BLSP 2 bit 0; SPI
		UART2_RTS		B	BLSP 2 bit 0; UART
		I2C2_SCL		B	BLSP 2 bit 0; I^{2}C

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AU39	GPIO_8		P3	B-PD:nppukp	Configurable I/O
		SPI3_MOSI		B	BLSP 3 bit 3; SPI
AV38	GPIO_9	SPI3_MISO	P3	B-PD:nppukp	Configurable I/O
				B	BLSP 3 bit 2; SPI
AW39	GPIO_10		P3	B-PD:nppukp	Configurable I/O
		SPI3_CS		B	BLSP 3 bit 1; SPI
		I2C3_SDA		B	BLSP 3 bit 1; I^{2}C
AU37	GPIO_11		P3	B-PD:nppukp	Configurable I/O
		SPI3_CLK		B	BLSP 3 bit 0; SPI
		I2C3_SCL		B	BLSP 3 bit 0; I2C
AT36	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		SPI4_MOSI		B	BLSP 4 bit 3; SPI
		UART4_TX		B	BLSP 4 bit 3; UART
AR35	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		SPI4_MISO		B	BLSP 4 bit 2; SPI
		UART4_RX		B	BLSP 4 bit 2; UART
AY40	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		UART4_CTS		B	BLSP 4 bit 1; UART
		I2C4_SDA		B	BLSP 4 bit 1; I2C
		SPI4_CS		B	BLSP 4 bit 1; SPI
BA41	GPIO_15		P3	B-PD:nppukp	Configurable I/O
		UART4_RTS		B	BLSP 4 bit 0; UART
		I2C4_SCL		B	BLSP 4 bit 0; I2C
		SPI4_CLK		B	BLSP 4 bit 0; SPI
BF8	GPIO_16		P3	B-PD:nppukp	Configurable I/O
		UART5_TX		B	BLSP 5 bit 3; UART
		SPI5_MOSI		B	BLSP 5 bit 3; SPI
BG7	GPIO_17		P3	B-PD:nppukp	Configurable I/O
		UART5_RX		B	BLSP 5 bit 2; UART
		SPI5_MISO		B	BLSP 5 bit 2; SPI
BH8	GPIO_18		P3	B-PD:nppukp	Configurable I/O
		UART5_CTS		B	BLSP 5 bit 1; UART
		I2C5_SDA		B	BLSP 5 bit 1; I2C
		SPI5_CS		B	BLSP 5 bit 1; SPI

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BH6	GPIO_19		P3	B-PD:nppukp	Configurable I/O
		UART5_RTS		B	BLSP 5 bit 0; UART
		I2C5_SCL		B	BLSP 5 bit 0; I^{2}C
		SPI5_CLK		B	BLSP 5 bit 0; SPI
K40	GPIO_20		P3	B-PD:nppukp	Configurable I/O
		UART6_TX		B	BLSP 6 bit 3; UART
		SPI6_MOSI		B	BLSP 6 bit 3; SPI
L39	GPIO_21		P3	B-PD:nppukp	Configurable I/O
		UART6_RX		B	BLSP 6 bit 2; UART
		SPI6_MISO		B	BLSP 6 bit 2; SPI
M40	GPIO_22		P3	B-PD:nppukp	Configurable I/O
		UART6_CTS		B	BLSP 6 bit 1; UART
		I2C6_SDA		B	BLSP 6 bit 1; I^{2}C
		SPI6_CS		B	BLSP 6 bit 1; SPI
L41	GPIO_23		P3	B-PD:nppukp	Configurable I/O
		UART6_RTS		B	BLSP 6 bit 0; UART
		I2C6_SCL		B	BLSP 6 bit 0; I^{2}C
		SPI6_CLK		B	BLSP 6 bit 0; SPI
BD4	GPIO_24		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_P		DI	SDE vertical sync – primary
AK38	GPIO_25		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_S		DI	SDE vertical sync – secondary
		PRI_MI2S_MCLK_A		DO	Primary MI^{2}S master clock A
		SEC_MI2S_MCLK_A		DO	Secondary MI^{2}S master clock A
BF6	GPIO_26		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK0		DO	Camera master clock 0 – rear camera
BG5	GPIO_27		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK1		DO	Camera master clock 1 – front camera
BF4	GPIO_28	CAM_MCLK2	P3	B-PD:nppukp	Configurable I/O Camera master clock 2 – depth camera
BE5	GPIO_29		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SDA0		B	Dedicated camera control interface I^{2}C 0 serial data
BC5	GPIO_30		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SCL0		B	Dedicated camera control interface I^{2}C 0 clock

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BD6	GPIO_31		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SDA1		B	Dedicated camera control interface I^{2}C 1 serial data
BE3	GPIO_32		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SCL1		B	Dedicated camera control interface I^{2}C 1 clock
U1	GPIO_33		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER0		DO	Camera control interface timer 0
		GP_CLK0_A		DO	General-purpose clock output 0A
R1	GPIO_34		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER1		DO	Camera control interface timer 1
		GP_CLK1_A		DO	General-purpose clock output 1A
P2	GPIO_35		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER2		DO	Camera control interface timer 2
		BOOT_CONFIG[12]		DI	fast_boot_select bit 12 (configure external boot device)
		SPI1_CS1		DO-Z	Chip select 1 for SPI on BLSP1
R3	GPIO_36		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER3		DO	Camera control interface timer 3
		SPI1_CS2		DO-Z	Chip select 2 for SPI on BLSP1
		GP_CLK0_B		DO	General-purpose clock output 0B
L37	GPIO_37		P3	B-PD:nppukp	Configurable I/O
		FORCED_USB_BOOT		DI	Forced USB boot
R5	GPIO_38		P3	B-PD:nppukp	Configurable I/O
		CCI_ASYNC_IN0		DI	Camera control interface async 0
		GP_PDM_2B		DO	General-purpose PDM output 2B

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
T6	GPIO_39	CAM1_STANDBY_N GP_MN	P3	B-PD:nppukp DO DO	Configurable I/O Rear camera standby General-purpose M/N:D counter output
V4	GPIO_40	 CAM1_RST_N	P3	B-PD:nppukp DO	Configurable I/O Rear camera reset
U3	GPIO_41	 CCI_TIMER4 SPI3_CS1 GP_CLK1_B BOOT_CONFIG[9]	P3	B-PD:nppukp DO DO-Z DO DI	Configurable I/O Camera control interface timer 4 Chip select 1 for SPI on BLSP3 General-purpose clock output 1B fast_boot_select bit 9 (configure external boot device)
AL35	GPIO_42	 ACCEL_INT	P3	B-PD:nppukp DI	Configurable I/O Accelerometer sensor interrupt
AL39	GPIO_43	 ALSP_INT_N	P3	B-PD:nppukp DI	Configurable I/O Ambient light sensor interrupt
AN41	GPIO_44	 MAG_INT	P3	B-PD:nppukp DI	Configurable I/O Magnetic sensor interrupt
AM40	GPIO_45	 GYRO_INT GP_PDM_1A	P3	B-PD:nppukp DI DO	Configurable I/O Gyro sensor interrupt General-purpose PDM output 1A
AL37	GPIO_46	 PRESSURE_INT	P3	B-PD:nppukp DI	Configurable I/O Pressure sensor interrupt
AM38	GPIO_47	 SPI6_CS2	P3	B-PD:nppukp DO-Z	Configurable I/O Chip select 2 for SPI on BLSP6
AP40	GPIO_48	 SPI6_CS1 GP_PDM_0B	P3	B-PD:nppukp DO-Z DO	Configurable I/O Chip select 1 for SPI on BLSP6 General-purpose PDM output 0B
AN37	GPIO_49	 UIM_BATT_ALARM	P3	B-PD:nppukp DI	Configurable I/O UIM battery alarm
AP38	GPIO_50	 SPI3_CS2 SD_WRITE_PROTECT	P3	B-PD:nppukp DO-Z DI	Configurable I/O Chip select 2 for SPI on BLSP3 Secure digital card write protection
AR39	GPIO_51	 UIM1_DATA	P5	B-PD:nppukp B	Configurable I/O Dual voltage UIM1 data
AU41	GPIO_52	 UIM1_CLK	P5	B-PD:nppukp DO	Configurable I/O Dual voltage UIM1 clock
AT40	GPIO_53	 UIM1_RESET	P5	B-PD:nppukp DO	Configurable I/O Dual voltage UIM1 reset

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AV40	GPIO_54		P3	B-PD:nppukp	Configurable I/O
		UIM1_PRESENT		DI	UIM1 detect (nondual voltage)
AN35	GPIO_55		P6	B-PD:nppukp	Configurable I/O
		UIM2_DATA		B	Dual voltage UIM2 data
AT38	GPIO_56		P6	B-PD:nppukp	Configurable I/O
		UIM2_CLK		DO	Dual voltage UIM2 clock
AP36	GPIO_57		P6	B-PD:nppukp	Configurable I/O
		UIM2_RESET		DO	Dual voltage UIM2 reset
AR37	GPIO_58		P3	B-PD:nppukp	Configurable I/O
		UIM2_PRESENT		DI	UIM2 detect (nondual voltage)
BD40	GPIO_59		P3	B-PD:nppukp	Configurable I/O
BE41	GPIO_60		P3	B-PD:nppukp	Configurable I/O
		GP_PDM_2A		DO	General-purpose PDM output 2A
BE39	GPIO_61		P3	B-PD:nppukp	Configurable I/O
BG3	GPIO_62		P3	B-PD:nppukp	Configurable I/O
BB20	GPIO_63		P3	B-PD:nppukp	Configurable I/O
AN39	GPIO_64		P3	B-PD:nppukp	Configurable I/O
AM36	GPIO_65		P3	B-PD:nppukp	Configurable I/O
K38	GPIO_66		P3	B-PD:nppukp	Configurable I/O
		PRI_MI2S_MCLK_C		DO	Primary MI^{2}S master clock C
		SEC_MI2S_MCLK_B		DO	Secondary MI^{2}S master clock B
		GP_PDM_0A		DO	General-purpose PDM output 0A
AJ37	GPIO_67		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX0_DRE		DO	RX0 DRE data channel
AJ39	GPIO_68		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX1_DRE		DO	RX1 DRE data channel
AK36	GPIO_69		P3	B-PD:nppukp	Configurable I/O
		PRI_MI2S_MCLK_B		DO	Primary MI^{2}S master clock B
		CDC_PDM_CLK		DO	Audio codec PDM 0 clock
AH40	GPIO_70		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_SYNC		DO	Audio codec PDM 0 sync
		SLIMBUS_CLK		DO	Low-power audio SLIMbus clock
AH38	GPIO_71		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_TX0		DI	Audio codec PDM 0 transmit 0
		SLIMBUS_DATA0		DO	Low-power audio SLIMbus data 0
AH36	GPIO_72		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX0		DO	Audio codec PDM 0 receive 0
		SLIMBUS_DATA1		DO	Low-power audio SLIMbus data 1

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AJ41	GPIO_73		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX1		DO	Audio codec PDM 0 receive 1
AK40	GPIO_74		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX2		DO	Audio codec PDM 0 receive 2
BE9	GPIO_75		P3	B-PD:nppukp	Configurable I/O
		BT_SSBI		B	Bluetooth single-wire serial bus interface
BB10	GPIO_76		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[2]		B	WLAN data bit 2
BD10	GPIO_77		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[1]		B	WLAN data bit 1
BC11	GPIO_78		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[0]		B	WLAN data bit 0
BF12	GPIO_79		P3	B-PD:nppukp	Configurable I/O
		WLAN_SET		B	WLAN set
BG11	GPIO_80		P3	B-PD:nppukp	Configurable I/O
		WLAN_CLK		B	WLAN clock
BH12	GPIO_81		P3	B-PD:nppukp	Configurable I/O
		FM_SSBI		B	FM radio serial data interface **Note**: If FM is not used, leave GPIO_81 as no connect (floating).
BF10	GPIO_82		P3	B-PD:nppukp	Configurable I/O
		FM_SDI		B	FM radio single-wire serial bus interface **Note**: If FM is not used, leave GPIO_82 as no connect (floating).
BE11	GPIO_83		P3	B-PD:nppukp	Configurable I/O
		BT_CTRL		B	Bluetooth control
BG9	GPIO_84		P3	B-PD:nppukp	Configurable I/O
		BT_DATA_STB		B	Bluetooth dual-function: data and strobe
M36	GPIO_85		P3	B-PD:nppukp	Configurable I/O
		KEY_VOLP_N		DI	Volume key interrupt
N37	GPIO_86		P3	B-PD:nppukp	Configurable I/O
		KEY_SNAPSHOT		DI	Snapshot interrupt
M38	GPIO_87		P3	B-PD:nppukp	Configurable I/O
		KEY_FOCUS		DI	Focus interrupt
G39	GPIO_88		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_D1		B	MI^{2}S 1 serial data channel 1
		KEY_HOME		DI	Home key interrupt

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
G37	GPIO_89	 DMIC0_CLK SPI7_CS1 GP_PDM_1B	P3	B-PD:nppukp DO DO-Z DO	Configurable I/O Digital MIC0 clock Chip select 1 for SPI on BLSP7 General-purpose PDM output 1B
H38	GPIO_90	 DMIC0_DATA SPI7_CS2	P3	B-PD:nppukp DI DO-Z	Configurable I/O Digital MIC0 data Chip select 2 for SPI on BLSP7
H36	GPIO_91	 MI2S_1_SCK	P3	B-PD:nppukp B	Configurable I/O MI^{2}S 1 bit clock
J35	GPIO_92	 MI2S_1_WS	P3	B-PD:nppukp B	Configurable I/O MI^{2}S 1 word select (L/R)
K36	GPIO_93	 MI2S_1_D0	P3	B-PD:nppukp B	Configurable I/O MI^{2}S 1 serial data channel 0
J37	GPIO_94	 WSA_IO_DATA MI2S_1_D2	P3	B-PD:nppukp DI B	Configurable I/O WSA8810 current/voltage sense data for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) MI^{2}S 1 serial data channel 2
L35	GPIO_95	 WSA_IO_CLK MI2S_1_D3	P3	B-PD:nppukp DO B	Configurable I/O WSA8810 current/voltage sense clock for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) MI^{2}S 1 serial data channel 3
E41	GPIO_96	 WSA_EN SPI8_MOSI	P3	B-PD:nppukp DO B	Configurable I/O WSA8810 enable BLSP 8 bit 0; SPI
G41	GPIO_97	 WSA_INTR SPI8_MISO	P3	B-PD:nppukp DO B	Configurable I/O WSA8810 interrupt BLSP 8 bit 1; SPI
H40	GPIO_98	 I2C8_SDA SPI8_CS	P3	B-PD:nppukp B B	Configurable I/O BLSP 8 bit 2; I^{2}C BLSP 8 bit 2; SPI
J39	GPIO_99	 I2C8_SCL SPI8_CLK	P3	B-PD:nppukp B B	Configurable I/O BLSP 8 bit 3; I^{2}C BLSP 8 bit 3; SPI
BG15 [2]	GPIO_100	 GRFC[0]	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 0
BD14	GPIO_101	GRFC[1]	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 1

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF14	GPIO_102	GRFC[2]	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 2
BG13	GPIO_103	GRFC[3]	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 3
BC13	GPIO_104	GRFC[4] BOOT_CONFIG[7]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 4 fast_boot_select bit 7 (configure external boot device)
BE13	GPIO_105	GRFC[5] BOOT_CONFIG[4]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 5 fast_boot_select bit 4 (configure external boot device)
BB12	GPIO_106	GRFC[6] BOOT_CONFIG[0]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 6 fast_boot_select bit 0 (configure external boot device)
BD12	GPIO_107	GRFC[7] BOOT_CONFIG[2]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 7 fast_boot_select bit 2 (configure external boot device)
BD20	GPIO_108	GRFC[8] BOOT_CONFIG[5]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 8 fast_boot_select bit 5 (configure external boot device)
BC19	GPIO_109	GRFC[9] BOOT_CONFIG[3]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 9 fast_boot_select bit 3 (configure external boot device)
BF20	GPIO_110	GRFC[10] BOOT_CONFIG[8]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 10 fast_boot_select bit 8 (configure external boot device)
BH20	GPIO_111	GRFC[11] BOOT_CONFIG[11]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 11 fast_boot_select bit 11 (configure external boot device)
BE19	GPIO_112	GRFC[12] BOOT_CONFIG[10]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 12 fast_boot_select bit 10 (configure external boot device)
BF40	GPIO_113	GRFC[13] BOOT_CONFIG[1]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 13 fast_boot_select bit 1 (configure external boot device)

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BG19	GPIO_114		P3	B-PD:nppukp	Configurable I/O
		GRFC[14]		DO	Generic RF controller bit 14
		BOOT_CONFIG[6]		DI	fast_boot_select bit 6 (configure external boot device)
BB18	GPIO_115		P3	B-PD:nppukp	Configurable I/O
		GRFC[15]		DO	Generic RF controller bit 15
		GSM_TX_PHASE_TXDAC1		DO	GSM transmit phase adjust data bit associated with TXDAC1
BF18	GPIO_116		P3	B-PD:nppukp	Configurable I/O
		EXT_GPS_LNA_EN0		DO	External LNA GPS enable
		GRFC[28]		DO	Generic RF controller bit 28
BD18	GPIO_117		P3	B-PD:nppukp	Configurable I/O
		GSM_TX_PHASE_TXDAC0	P3	DO	GSM transmit phase adjust data bit
				DO	associated with TXDAC0
		GRFC[27]			Generic RF controller bit 27
BC17 [2]	GPIO_118	RFFE1_CLK	P3	B-PD:nppukp	Configurable I/O
				DO	MIPI_RFFE 1 clock
BE17	GPIO_119	RFFE1_DATA	P3	B-PD:nppukp	Configurable I/O
				B	MIPI_RFFE 1 data
BG17	GPIO_120	RFFE2_CLK	P3	B-PD:nppukp	Configurable I/O
				DO	MIPI_RFFE 2 clock
BF16	GPIO_121	RFFE2_DATA	P3	B-PD:nppukp	Configurable I/O
				B	MIPI_RFFE 2 data
BB16	GPIO_122	RFFE4_CLK	P3	B-PD:nppukp	Configurable I/O
				DO	MIPI_RFFE 4 clock
BD16	GPIO_123	RFFE4_DATA	P3	B-PD:nppukp	Configurable I/O
				B	MIPI_RFFE 4 data
BH16	GPIO_124	RFFE5_CLK	P3	B-PD:nppukp	Configurable I/O
				DO	MIPI_RFFE 5 clock
BE15	GPIO_125	RFFE5_DATA	P3	B-PD:nppukp	Configurable I/O
				B	MIPI_RFFE 5 data
BC15	GPIO_126	RFFE3_CLK	P3	B-PD:nppukp	Configurable I/O
				DO	MIPI_RFFE 3 clock
BB14	GPIO_127	RFFE3_DATA	P3	B-PD:nppukp	Configurable I/O
				B	MIPI_RFFE 3 data
BH4	GPIO_128	CAM_MCLK3	P3	B-PD:nppukp	Configurable I/O
				DO	Camera master clock 3 – depth camera
BE1	GPIO_129	CAM2_RST_N	P3	B-PD:nppukp	Configurable I/O
				DO	Depth camera reset
BF2	GPIO_130	CAM2_STANDBY_N	P3	B-PD:nppukp	Configurable I/O
		BOOT_CONFIG[14]		DO	Depth camera standby
				DI	fast_boot_select bit 14 (configure external boot device)

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
V6	GPIO_131	CAM3_RST_N	P3	B-PD:nppukp	Configurable I/O
				DO	Front camera reset
U5	GPIO_132		P3	B-PD:nppukp	Configurable I/O
		CAM3_STANDBY_N		DO	Front camera standby
		BOOT_CONFIG[13]		DI	fast_boot_select bit 13 (configure external boot device)
T4	GPIO_133		P3	B-PD:nppukp	Configurable I/O
		SD_CARD_DET_N		DI	Secure digital card detection
T2	GPIO_134		P3	B-PD:nppukp	Configurable I/O
BA39	GPIO_135		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_SCK		B	MI^{2}S 2 bit clock
		I2C7_SCL		B	BLSP 7 bit 2; I^{2}C
		SPI7_CLK		B	BLSP 7 bit 2; SPI
BB40	GPIO_136		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_WS		B	MI^{2}S 2 word select (L/R)
		I2C7_SDA		B	BLSP 7 bit 3; I^{2}C
		SPI7_CS		B	BLSP 7 bit 3; SPI
BA37	GPIO_137		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D0		B	MI^{2}S 2 serial data
		SPI7_MOSI		B	BLSP 7 bit 0; SPI
AY38	GPIO_138		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D1		B	MI^{2}S 2 serial data channel 1
		SPI7_MISO		B	BLSP 7 bit 1; SPI
BB38	GPIO_139		P3	B-PD:nppukp	Configurable I/O
		USB_SS_SWITCH_SEL		DO	USB Type-C switch control
BC39	GPIO_140		P3	B-PD:nppukp	Configurable I/O
BC41	GPIO_141		P3	B-PD:nppukp	Configurable I/O

1. See Table 2-1 for the parameter and acronym definitions.
2. In SDA450:
   GPIO 100 to GPIO 117 does not support a GRFC configuration.
   GPIO 115 and GPIO 117 does not support a GSM specific configuration.
   GPIO 118 to GPIO 127 does not support a RFFE_CLK and RFFE_DATA configuration.
   See *SDM450/SDA450 + PMI8952 + PM8953 Reference Schematics* (80-PC173-41) and *SDM632 + PMI632 + PM8953 Reference Schematic* (80-PF078-41) for connection details.

Table 2-12 Pin descriptions: no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
AB38, AH34, AV10, AW9, AW33, BA9, BA15, BA17, BA25, BA33, BB34, BA35, BB36, C23, J31, J33, L31, N35, P36, R35, T36	DNC	Do not connect; connected internally; do not connect externally.

Table 2-13 Pin descriptions: power-supply pins

Pad #	Pad name	Functional description
AD24, AD26, AD28, AD30, AD32, AD34, AE25, AE27, AE29, AE31, AE33, AE35, W25, W27, W29, W31, W33, W35, Y24, Y26, Y28, Y30, Y32, Y34	VDD_APC	Power for applications microprocessors
AA9, AA11, AA17, AA19, AB24, AC23, AE9, AE11, AE17, AE19, AF12, AH32, AJ33, AL11, AM10, AR29, AR31, R33, U9, U11, U13, U15, U23, V22	VDDCX_1	Power for digital core circuits
AA13, AA15, AA23, AC29, AE13, AE15, AE21, AE23, AG23, AH28, AH30, AJ29, AJ31, AN9, AN25, AN27, AP16, AP18, AP28, AR17, R11, R13, R31, T28, T30, T32, U17, U19, W23, AR23, AR25	VDD_MEM (MX)	Power for on-chip memory
AA7, AC7, AH10, AJ9, W7	VDD_DSI_CSI	Power for MIPI CSI DSI circuits
AE7, AL7	VDD_DSI_HV_PLL	Power pad for MIPI_DSI 1.2 V circuits
AG7, AJ7	VDD_DSI_LV_PLL	Power pad for MIPI_DSI 0.9 V circuits
R15, R17, R19, R23, R25, R27, R29, T22	VDD_EBI	Power for EBI
L21	VDD_EBI_HV_PLL	Power pad for EBI 1.2 V circuits
N21	VDD_EBI_LV_PLL	Power pad for EBI 0.9 V circuits
AU19, AU21, AU23, AU25, AU27	VDD_A2 [1]	Power for analog circuits – high voltage (**Note:** Do not connect to power (GND pad) for SDA450)
BA19, BA21, BA23	VDD_A1 [1]	Power for analog circuits – low voltage (**Note:** Do not connect to power (GND pad) for SDA450)
AP34	VREF_PADS	Power for Vbias pads – UIM Vbias pad
M8	VREF_PADS	Power for Vbias pads – SDC1 Vbias pads
G23	VREF_EBI_CA	LPDDR3 CA reference voltage
AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AK14, AK28, AL29, AM14, AN21, AN23, AN29	VDD_MODEM	Power for modem circuits
BA31	VDD_GNSS	Power for GNSS circuits
J13, J15, J17, J19, J23, J25, J27, J29, L13, L15, L17, L19, L23, L25, L27,L29, J21	VDDPX_1	Power for pad group 1 – EBI pads
P8	VDDPX_2	Power for pad group 2 – SDC2 pads
AJ35, AT8, AU7, AU33, AW15, AW17, L9, N33, T8	VDDPX_3	Power for pad group 2 – most I/O pads
AK34	VDDPX_5	Power for pad group 5 – UIM1 pads
AM34	VDDPX_6	Power for pad group 6 – UIM2 pads
L11	VDDPX_7	Power for pad group 7 – eMMC I/O pads
AB28	VDD_PLL1	Power for PLL circuits – low voltage
AA21, AN13, AR27, W21	VDD_PLL2	Power for PLL circuits – high voltage
L33	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise GND

Table 2-13 Pin descriptions: power-supply pins (cont.)

Pad #	Pad name	Functional description
R9	VDD_CDC_SDC1	Power for secure digital calibration delay circuits
AC35	VDD_USB_SS_1P8	Power for USB PHY interface – low voltage
AD36	VDD_USB_HS1_1P8	Power for USB PHY interface – low voltage
AD38	VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage
AB34, AB36, AC31, AC33	VDD_USB_CORE	Power for USB core 0.925 V
AU9	VDD_WLAN	Power for WLAN ADC circuits

1. See *SDM450/SDA450 + PMI8952 + PM8953 Reference Schematic* (80-PC173-41), *SDM632 + PMI632 + PM8953 Reference Schematic* (80-PF078-41), and *SDM450 Digital Baseband Design Guidelines /Training Slides* (80-PC173-5B) for connection details.

Table 2-14 Pin descriptions: ground pins

Pad #	Pad name	Functional description
A1, A31, A41, A9, AA25, AA27, AA29, AA3, AA31, AA33, AA35, AA37, AA39, AB20, AB26, AB40, AC11, AC13, AC15, AC17, AC19, AC21, AC25, AC27, AC37, AC39, AC9, AD40, AE3, AE37, AF24, AF26, AF28, AF30, AF32, AF34, AF36, AF40, AF8, AG13, AG15, AG17, AG19, AG21, AG25, AG27, AG29, AG31, AG33, AG35, AG37, AG39, AG41, AG9, AH8, AJ3, AK4, AL13, AL21, AL23, AL25, AL27, AL31, AL33, AL41, AL9, AM26, AM28, AM8, AN11, AN3, AN31, AN33, AP10, AP12, AP14, AP2, AP8, AR11, AR13, AR15, AR19, AR21, AR33, AR41, AR7, AR9, AT4, AU15, AU17, AU29, AU31, AV2, AV30, AV6, AV8, AW11, AW13, AW19, AW21, AW23, AW25, AW27, AW29, AW31, AW41, AW7, AY26, B12, B16, B2, B20, B24, B28, B32, B38, B4, B40, B6, BA11, BA13, BA7, BB4, BB6, BC21, BC23, BC25, BC27, BC29, BC3, BC31, BC33, BC35, BC37, BD2, BD22, BD24, BD26, BD28, BD30, BD32, BD38, BE21, BE23, BE25, BE27, BE29, BE31, BE33, BE35, BE37,BF30, BF34, BF38, BG1, BG21, BG23, BG25, BG27, BG29, BG39, BG41, BH10, BH14, BH18, BH2,BH34, BH40, C21, C35, C41, D10, D12, D14, D16, D18, D2, D20, D22, D24, D26, D28, D30, D32, D34, D36, D38, D4, D40, D6, D8, E19, E7, F10, F12, F14, F16, F18, F2, F20, F22, F24, F26, F28, F30, F32, F34, F36, F38, F4, F40, F6, F8, G11, G13, G15, G17, G19, G21, G25, G27, G29, G31, G33, G35, G7, G9, J1, J11, J41, J9, N1, N11, N13, N15, N17, N19, N23, N25, N27, N29, N31, N41, N7, N9, T40, U21, U25, U27, U29, U31, U33, U35, U37, U39, V2, V20, V24, V26, V28, V30, V32, V34, V36, V38, V8, W11, W13, W15, W17, W19, W3, W37, W39, W41, W9, Y20, Y36, Y38	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-2) reflect conditions that the SDM450/SDA450 device is exposed to beyond the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individual when all other parameters are within their specified operating ranges. Functionality and long-term reliability are expected within the operating conditions, as described in Section 3.2 and Section 3.3.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_A1 VDD_DSI_CSI VDD_DSI_HV_PLL VDD_EBI_HV_PLL VDD_GNSS VDDPX_1	Power for analog circuits – low voltage for PA DAC and TxDAC circuits Power for MIPI DSI pads Power for DSI high-voltage PLL pads Power for EBI high-voltage PLL pads Power for GNSS circuits Power for pad group 1 – EBI pads	-0.3	1.441	V
VDD_A2	Power for analog circuits – high voltage for analog baseband receiver circuits	-0.3	2.09	V
VDDPX_2	Power for pad group 2			
	SDC2 pads low voltage	-0.3	2.09	V
	SDC2 pads high voltage	-0.3	3.344	V
VDD_PLL2	Power for PLL circuits – high voltage	-0.3	2.09	V
VDD_USB_HS1_1P8/ VDD_USB_SS_1P8	Power for USB PHY interface – low voltage	-0.3	2.057	V
VDD_USB_CORE VDD_EBI_LV_PLL	Power for USB core circuits Power for EBI low voltage PLL pads	-0.3	1.0505	V
VDDPX_3	Power for pad group 3 – most I/O pads	-0.3	2.09	V
VDDPX_5	Power for pad group 5			
	UIM1 pads low voltage	-0.3	2.09	V
	UIM1 pads high voltage	-0.3	3.344	V
VDDPX_6	Power for pad group 6			
	UIM2 pads low voltage	-0.3	2.09	V
	UIM2 pads high voltage	-0.3	3.344	V
VDDPX_7	Power for pad group 7 – SDC1 pads	-0.3	2.09	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_WLAN	Power for WLAN ADC circuits	-0.3	1.463	V
VDD_DSI_LV_PLL	Power for DSI low voltage PLL pads	-0.3	1.0505	V
VDD_QFPROM_PRG	Power for programming the QFPROM	-0.3	2.079	V
VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage	-0.3	3.52	V
VDD_APC	Power for VDD_APC pads	-0.3	1.267	V
VDD_CORE	Power for VDD_CORE pads	-0.3	1.1781	V
VDD_MODEM	Power for VDD_MODEM pads	-0.3	1.1781	V
VDD_MEM	Power for VDD_MEM pads	-0.3	1.1781	V
Signal pins				
V_IN	Voltage on any nonpower input pin	-0.3	V_{xx} + 20% [1]	V
VIN_P7	Voltage on any eMMC input pin	-0.30	2.45	V
I_IN	Latch-up current	-100	100	mA
ESD protection – see Section 7.1.				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2). SDM450/SDA450 meets all performance specifications listed in Section 3.3 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings never exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ [1]	Max	Unit
Power-supply voltages					
VDD_A1 VDD_DSI_CSI VDD_DSI_HV_PLL VDD_EBI_HV_PLL VDD_GNSS VDDPX_1	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits Power for MIPI DSI pads Power for DSI high-voltage PLL pads Power for EBI high-voltage PLL pads Power for GNSS circuits Power for pad group 1 – EBI pads	1.18	1.225	1.31	V
VDD_A2	Power for analog circuits–high voltage for analog baseband receiver circuits	1.70	1.8	1.90	V
VDDPX_2	Power for pad group 2				
	SDC2 pads low voltage	1.70	1.8	1.90	V
	SDC2 pads high voltage	2.70	2.95	3.04	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDD_PLL2	Power for PLL circuits – high voltage	1.70	1.8	1.90	V
VDD_USB_HS1_1P8/ VDD_USB_SS_1P8	Power for USB PHY interface – low voltage	1.72	1.8	1.87	V
VDD_USB_CORE VDD_EBI_LV_PLL	Power for USB core circuits Power for EBI low voltage PLL pads	0.910	0.925	0.955	V
VDDPX_3	Power for pad group 3 – most I/O pads	1.70	1.8	1.90	V
VDDPX_5	Power for pad group 5				
	UIM1 pads low voltage	1.70	1.8	1.90	V
	UIM1 pads high voltage	2.70	2.95	3.04	V
VDDPX_6	Power for pad group 6				
	UIM2 pads low voltage	1.70	1.8	1.90	V
	UIM2 pads high voltage	2.70	2.95	3.04	V
VDDPX_7	Power for pad group 7 – SDC1 pads	1.70	1.8	1.90	V
VDD_WLAN	Power for WLAN ADC circuits	1.19	1.3	1.377	V
VDD_DSI_LV_PLL	Power for DSI low voltage PLL pads	0.910	0.925	0.955	V
VDD_QFPROM_PRG	Power for programming the QFPROM	1.71	1.8	1.89	V
VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage	2.94	3.075	3.20	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
	Fuse programming temperature (case)	+10	+25	+85	°C
T_A [2]	3GPP2 mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP mode operating temperature (ambient)	-20	+25	+60	°C

1. Typical voltages represent the recommended output settings of the companion PMIC device
2. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.

Table 3-3 Operating conditions for voltage rails with AVS

Parameter [1]		Min	Typ	Max	Unit
VDD_APC	Quad Cortex A53 (operating at maximum frequency of 1.8 GHz)				
	Turbo_L1	0.810	–	1.152	V
	Nominal mode	0.680	–	0.932	V
	SVS [2] mode	0.575	–	0.805	V
	Low SVS	0.510	–	0.693	V

Table 3-3 Operating conditions for voltage rails with AVS (cont.)

Parameter [1]		Min	Typ	Max	Unit
VDD_CORE	Turbo mode	0.760	–	1.071	V
	Nominal mode	0.660	–	0.930	V
	SVS mode	0.560	–	0.772	V
	Low SVS	0.510	–	0.693	V
VDD_MODEM	Turbo mode	0.760	–	1.071	V
	Nominal mode	0.660	–	0.930	V
	SVS mode	0.560	–	0.772	V
	Low SVS	0.510	–	0.693	V
VDD_MEM	Turbo mode	0.790	–	1.071	V
	Nominal mode	0.790	–	0.983	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. AVS Type I is not enabled on the APC rail in SVS mode.

3.2.1 Core voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE retention mode. This technique decreases the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. These fuses are used by the software.

The fuse locations in Table 3-4 see the Bits[5:3] of address 0xA4124 for VDD_CORE. The fuse locations in Table 3-5 see the Bits [2:0] of address 0xA4124 for VDD_MEM. For more information, see the *SDM450 Hardware Register Description* (80-PC173-2X).

Table 3-4 Core voltage in retention mode

VDD_CORE [1]	Bit 5 (MSB)	Bit 4	Bit 3 (LSB)
0.4	1	0	0
0.448	0	1	1
0.504	0	1	0
0.552	0	0	1
0.6	0	0	0

1. The specified VDD_CORE voltages are PMIC settings.

Table 3-5 Core voltage in retention mode

VDD_MEM [1]	Bit 2 (MSB)	Bit 1	Bit 0 (LSB)
0.488	1	0	0
0.552	0	1	1
0.584	0	1	0
0.648	0	0	1
0.696	0	0	0

1. The specified VDD_MEM voltages are PMIC settings.

3.3 Power delivery network specification

The following subsections contain the maximum impedance specifications for the power delivery network (PDN).

NOTE: Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, they should contact QTI for assistance. The *SDM450 Digital Baseband Design Guidelines/Training Slides* (80-PC173-5B) also provides guidance.

Table 3-6 Power distribution network impedance vs. frequency

Power domain	Maximum impedance (mΩ) [1]			Port number	Pin numbers of positive ports	Pin numbers of negative ports
	DCR	1 MHz to 25 MHz	100 MHz			
VDD_APC	5	30	120	1	Y34, Y32, Y30, Y28, Y26, Y24, W35, W33, W31, W29, W27, W25, AE35, AE33, AE31, AE29, AE27, AE25, AD34, AD32, AD30, AD28, AD26, AD24	Y36, V36, V34, V32, V30, V28, V26, V24, U37, U35, U33, U31, U29, U27, U25, AG37, AG35, AG33, AG31, AG29, AG27, AG25, AF36, AF34, AF32, AF30, AF28, AF26, AF24, AC25, AA35, AA33, AA31, AA29, AA27, AA25
VDD_MODEM						
SDM450 VDD_MODEM	5	25	100	1	AN29, AN23, AN21, AM14, AL29, AK28, AK14, AJ27, AJ25, AJ23, AJ21, AJ19, AJ17, AJ15, AJ13	AR15, AP14, AR19, AN31, AL31, AL27, AL25, AL23, AL21, AL13, AG21, AG19, AG17, AG15, AG13
SDA450 VDD_MODEM	15	46	184	1	AN29, AN23, AN21, AM14, AL29, AK28, AK14, AJ27, AJ25, AJ23, AJ21, AJ19, AJ17, AJ15, AJ13	AR15, AP14, AR19, AN31, AL31, AL27, AL25, AL23, AL21, AL13, AG21, AG19, AG17, AG15, AG13
VDD_CORE	15	46	184	1	AA11, AA9, U15, U13, U11, U9	V8, N15, N13, N11, N9, W15, W13, W11, W9
	30	236	942	2	AJ33, AH32	AG33, AG31
	30	236	942	3	AR31, AR29	AR19, AN31, AR33, AL25, AL23, AL21, AU31, AU29
	30	236	942	4	R33	N31
	15	40	160	5	U23, V22, AB24, AC23, AE11, AE9, AM10, AL11, AE19, AE17, AA19, AA17, AF12	AM8, AL9, AG9, AG15, AG13, AA25, AC25, U25, V24, Y20, AC19, AC17, AC11, AC9, AG19, AG17, W19, W17

Table 3-6 Power distribution network impedance vs. frequency (cont.)

Power domain	Maximum impedance (mΩ) [1]			Port number	Pin numbers of positive ports	Pin numbers of negative ports
	DCR	1 MHz to 25 MHz	100 MHz			
VDD_MEM	20	94	376	1	AN9	AL9, AL13, AN11
	20	55	220	2	AP16, AP18, AR17	AP14, AR15, AU15, AU17, AR19
	15	42	168	3	AC29, AA23, W23, T32, R31, T30, T28	AC25, AA33, AA31, AA29, AA27, AA25, N27, N29, U25, U27, U29, U31, V32, V30, V28, V26, V24
	15	42	168	4	AJ31, AJ29, AG23, AE23, AH30, AH28, AE21	AG31, AG33, AF32, AF30, AG29, AF28, AG27, AF26, AG25, AF24
	20	94	376	5	U19, U17, R13, R11, AA15, AA13, AE15, AE13	AG19, AG17, AC19, AC17, AC11, W11, N19, N17, N15, W19, W17, N13, N11, W15, W13, AC15, AC13, AG15, AG13, Y20
	20	94	376	6	AP28, AN27, AN25	AN31, AL27, AL25

1. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz and proceeding to each higher frequency point defined.

Table 3-7 VDDPX_1 and VDD_EBI PDN specification

Power domain	Maximum impedance (mΩ)	Maximum effective impedance (mΩ) [1, 2, 3]				Port number	Pin numbers of positive ports	Pin numbers of negative ports
	DCR	1 MHz	3 MHz	10 MHz	200 MHz			
VDDPX_1	45	75	200	200	1500	1	J21	G21
		75	200	200	1250	2	J15, L15, J13, L13	N15, N13, G15, G13
		75	200	200	1250	3	J29, L29, J27, L27	N29, N27, G29, G27
		75	200	200	1250	4	J17, L17	N17, G17
		75	200	200	1250	5	J25, L25	N25, G25
		75	200	200	1250	6	J23, L23, J19, L19	N23, N19, G19
VDD_EBI	45	100	230	330	3250	1	R17, R15	N17, N15
		100	230	330	3250	2	R27, R29	N29, N27
		100	230	330	3250	3	R19	N19
		100	230	330	3400	4	R25, R23	N23, N25
		100	230	330	3400	5	T22	N23

1. The maximum effective impedance is the sum of the self-impedance and coupling impedance with other ports of the same power domain.
2. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz and proceeding to each higher frequency point defined.
3. PDN specification at 1 MHz is defined when the PMIC output pin shorted to GND in the simulation.

3.4 DC power characteristics

3.4.1 Average operating current

The measured power dB is part of the software release notes DCN.

3.4.2 Dhrystone and rock bottom maximum power

Table 3-8 Dhrystone and rock bottom maximum power for SDM450/SDA450 devices

SDM version	Octa core Dhrystone (Watt) [1], [2], [3] at 85°C (Tj)	Rock bottom (mW) [4] at 30°C (Tj)
SDM450/SDA450 1.8 GHz	4.4	7.5

1. This octa core Dhrystone specification applies to SDM450 CS devices.
2. Dhrystone power should be measured on the VDD_APC rail, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).
4. Rock bottom (VDD_CORE and VDD_MEM) should be measured at the VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at the retention voltage.

3.5 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire SDM450/SDA450 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of certain PMIC pins. Dedicated circuits continuously monitor several events that might trigger a power-on sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset. The PM8953 device complements the PMI8952/PMI632 device to meet the system’s power management needs. For details, see the *PM8953 Power Management IC Device Specification* (80-P2536-1).

The power-on sequence is shown in Figure 3-1.

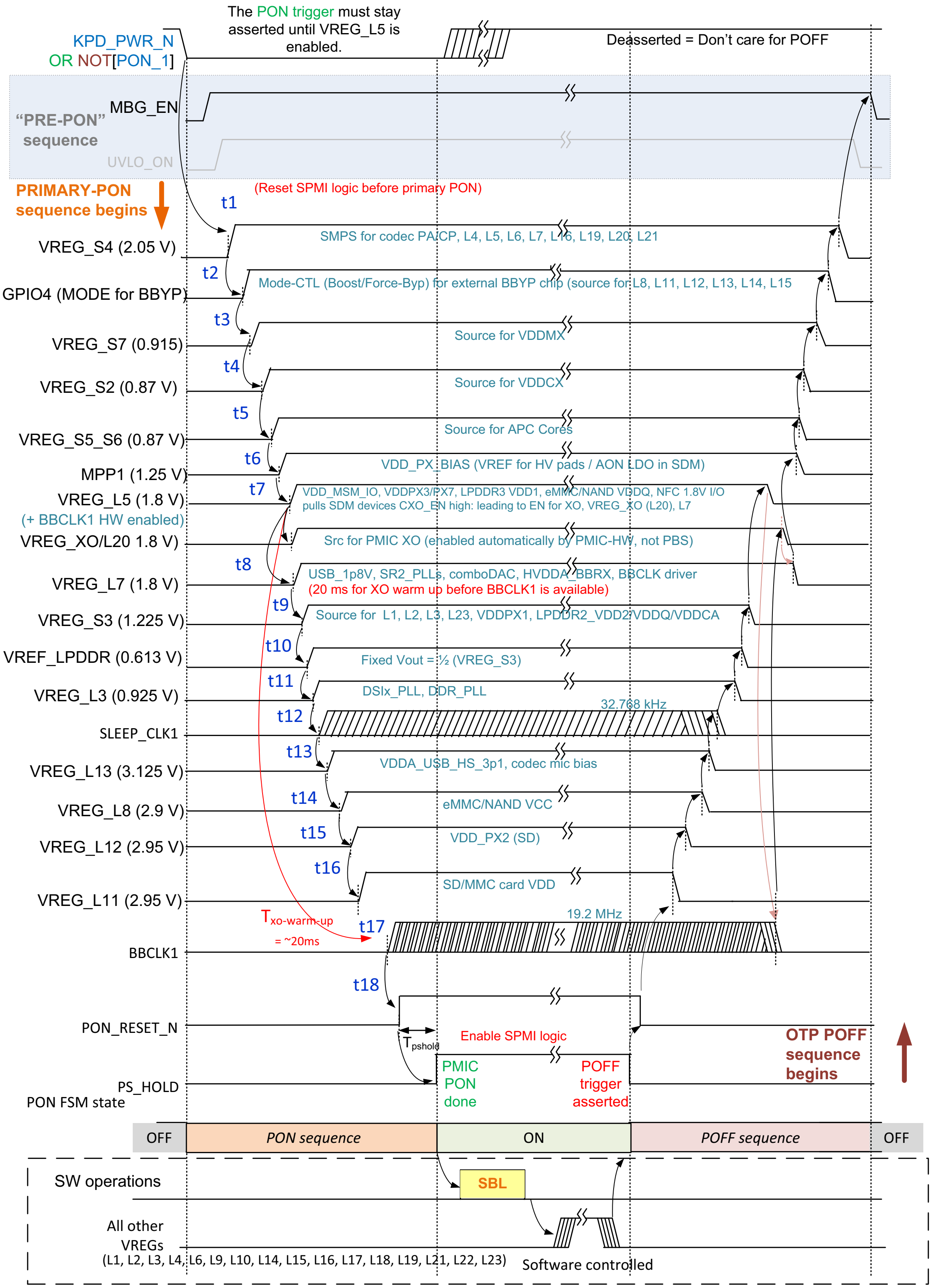


Figure 3-1 Power-on sequence

3.6 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some digital I/Os are dedicated for interconnections between the SDM450/SDA450 and other ICs within the QTI chipset; therefore, specifications are not required.
- Some digital I/Os are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-9 Digital I/O characteristics for VDDPX_1 (1.2 V)

Parameter	Comments	Min	Max	Unit
V_{REF}	Reference voltage	0.49 × VDDPX_1	0.51 × VDDPX_1	V
V_{IH}	High-level input voltage, CMOS/Schmitt-LPRx	0.65 × VDDPX_1	–	V
V_{IL}	Low-level input voltage CMOS/ Schmitt-LPRx	–	0.35 × VDDPX_1	V
V_{IH}	High-level input voltage, CMOS/Schmitt-MPRx	VDDPX_1/2+0.1	–	V
V_{IL}	Low-level input voltage CMOS/ Schmitt-MPRx	–	VDDPX_1/2-0.1	V
I_{IH}	Input high leakage current, no pull-down	–	5	µA
I_{IL}	Input low leakage current, no pull-up	-5	–	µA
I_{IHPD}	Input high leakage current, with pull-down	40	3000	µA
I_{ILPU}	Input low leakage current, with pull-up	-3000	-40	µA
V_{OH}	High-level output voltage, CMOS, at rated drive strength-configuration G [1]	0.355	–	V
V_{OL}	Low-level output voltage, CMOS, at rated drive strength- configuration G [2]	–	0.35	V
I_{OZHKP}	High-level, tri-state leakage, with keeper	-1200	-10	µA
I_{OZLKP}	Low-level, tri-state leakage, with keeper	10	1200	µA
$C_{I/O}$	I/O capacitance	1.25	2.5	pF

1. See Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
2. Input capacitance and I/O capacitance values are guaranteed by design but are not 100% tested.

Table 3-10 DC specification of VDDPX_3 = 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	0.65 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	-0.3 V	0.35 × VDDPX_3	V
V_{IH}	High-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	0.7 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	-0.3 V	0.3 × VDDPX_3	V
V_{SHYS}	Schmitt hysteresis voltage, (hihys_en = LOW)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage, (hihys_en = HIGH)	300	–	mV
I_{IH}	Input high leakage current with no pull-down (see note1)	–	1	µA
I_{IL}	Input low leakage current with no pull-down (see note1)	-1	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20 K)	-27.5 (60 K)	µA Ω
I_{OZH}	High-level, tri-state leakage current with no pull-down [1]	–	1	µA
I_{OZL}	Low-level, tri-state leakage current with no pull-up [1]	-1	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	97.5 (20 K)	27.5 (60 K)	µA Ω
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20 K)	-7.5 (60 K)	µA Ω
I_{OZLKP}	Low-level, tri-state leakage current with keeper [2]	7.5 (60 K)	22.5 (20 K)	µA Ω
V_{OH}	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V
$R_{PULL-UP}$	Pull-up resistance	20 K	60 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	20 K	60 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	20 K	60 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	20 K	60 K	Ω

Table 3-10 DC specification of VDDPX_3 = 1.8 V GPIOs (cont.)

Parameter	Description	Min	Max	Units
RFFE pins				
$R_{PULL-UP}$	Pull-up resistance	–	41.25 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	–	41.25 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	–	41.25 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	–	41.25 K	Ω

1. Pin voltage = VDDPX_3 maximum. For keeper pins, pin voltage = VDDPX_3 maximum - 0.45 V.
2. Pin voltage = GND and supply = VDDPX_3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX_3 maximum.

Table 3-11 Digital I/O characteristics for VDDPX_7 = 1.8 V nominal (SDC1)

Parameter	Description	Min	Typ	Max	Units
V_{OH}	High-level output voltage	VDDPX_7 - 0.45 V	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45 V	V
V_{IH}	High-level input voltage	0.65 × VDDPX_7	–	VDDPX_7 + 0.3 V	V
V_{IL}	Low-level input voltage	-0.3 V	–	0.35 × VDDPX_7	V
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω

Table 3-12 Digital I/O characteristics for VDDPX_2 = 2.95 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX_2	–	VDDPX_2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDPX_2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current with pull-down	–	–	10	μA
I_{IL}	Input low leakage current with pull-up	-10	–	–	μA
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	10	μA
I_{OZL}	Low-level, tri-state leakage current with no pull-up	-10	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω

Table 3-12 Digital I/O characteristics for VDDPX_2 = 2.95 V nominal (SDC2) (cont.)

Parameter	Description	Min	Typ	Max	Units
V_{OH}	High-level output voltage	0.75 × VDDPX_2	–	VDDPX_2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDPX_2	V

1. Pin voltage = VDDPX_3 maximum. For keeper pins, pin voltage = VDDPX_3 maximum - 0.45 V.

Table 3-13 Digital I/O characteristics for VDDPX_2 = 1.8 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current with pull-down	–	–	5	μA
I_{IL}	Input low leakage current with pull-up	-5	–	–	μA
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	5	μA
I_{OZL}	Low-level, tri-state leakage current with no pull-up	-5	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 Digital I/O characteristics for VDDPX_X = 2.95 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_X	–	VDDPX_X + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_X	V
V_{HYS}	Schmitt hysteresis voltage [1]	100	–	–	mV
I_{IH}	Input high leakage current with pull-down	-20	–	20	μA
I_{IL}	Input low leakage current with pull-down	–	–	1000	μA
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	10	μA
I_{OZL}	Low-level, tri-state leakage current with no pull up	-10	–	–	μA

Table 3-14 Digital I/O characteristics for VDDPX_X = 2.95 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
$R_{PULL\text{-}UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL\text{-}DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER\text{-}UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER\text{-}DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage [2]	0.8 × VDDPX_X	–	VDDPX_X	V
V_{OL}	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH and VIL are only applicable for the I/O signal.
2. UIM specifies VOL = 0.2 × VDDPX_X (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDDPX_X (RST) and 0.7 × VDDPX_X (CLK, I/O). The worst-case VOL and VOH values are used in Table 3-14.

Table 3-15 Digital I/O characteristics for VDDPX_X = 1.8 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_X	–	VDDPX_X + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_X	V
V_{HYS}	Schmitt hysteresis voltage [1]	100	–	–	mV
I_{IH}	Input high leakage current with pull-down	-20	–	20	µA
I_{IL}	Input low leakage current with pull-down	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current with no pull-up	-5	–	–	µA
$R_{PULL\text{-}UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL\text{-}DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER\text{-}UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER\text{-}DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage [2]	0.8 × VDDPX_X	–	VDDPX_X	V
V_{OL}	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH and VIL are only applicable for the I/O signal.
2. UIM specifies VOL = 0.2 × VDDPX_X (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDDPX_X (RST) and 0.7 × VDDPX_X (CLK, I/O). The worst-case VOL and VOH are used in Table 3-15.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-2) with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using the following relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = V_{DDPX\_X} - \left(\frac{\%drive \times 450}{100}\right) mV$$

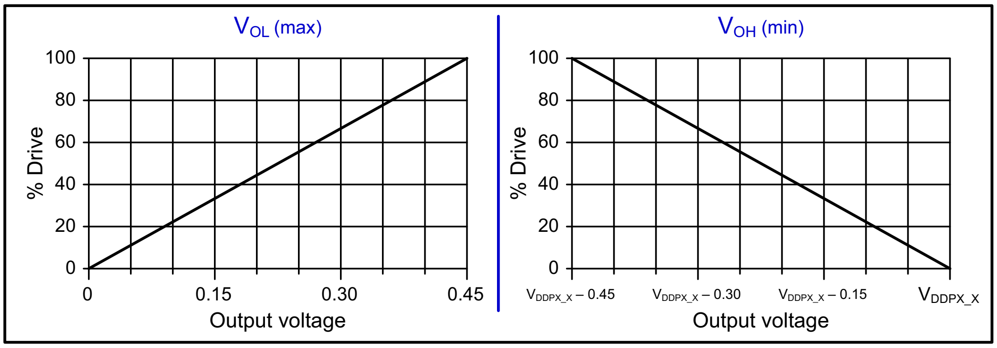


Figure 3-2 IV curve for V_{OL} and V_{OH} (valid for all V_{DDPX_X})

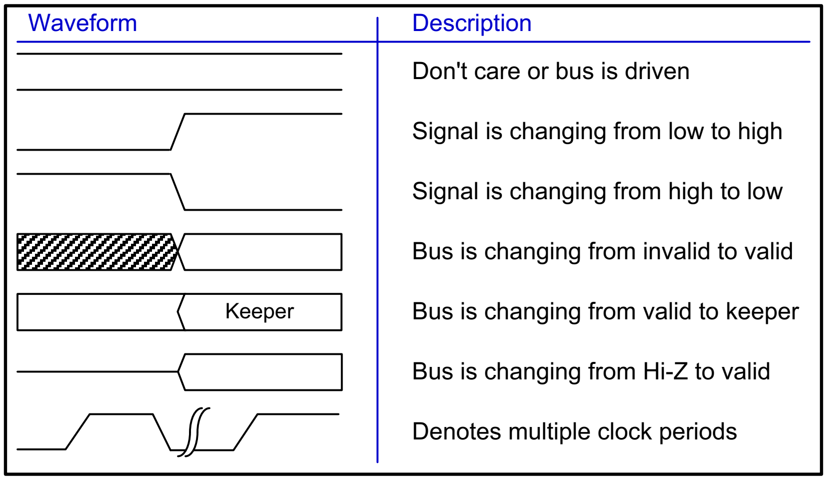
3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included in this section.

NOTE: All SDM450/SDA450 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described in more detail in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-3.



Waveform	Description
	Don't care or bus is driven
	Signal is changing from low to high
	Signal is changing from high to low
	Bus is changing from invalid to valid
Keeper	Bus is changing from valid to keeper
	Bus is changing from Hi-Z to valid
	Denotes multiple clock periods

Figure 3-3 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize SDM450/SDA450 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-4.

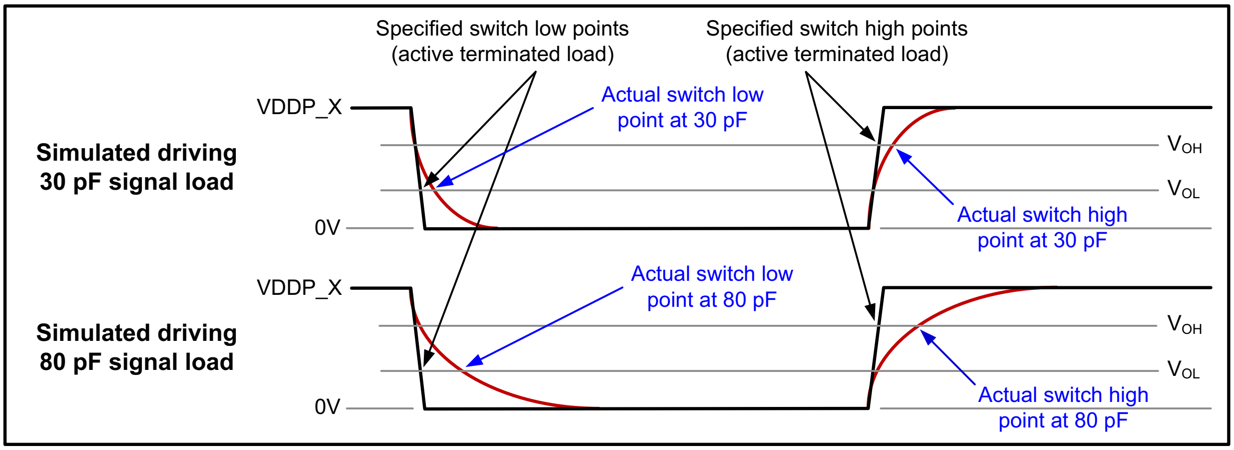


Figure 3-4 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SDM450/SDA450 and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The SDM450/SDA450 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_X} supply (Figure 3-5). The input switch point for pure input-only pads is designed to be $V_{DDPX\_X}/2$ (or 50% of V_{DDPX_X}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_X} for V_{IL} and 65% of V_{DDPX_X} for V_{IH}.

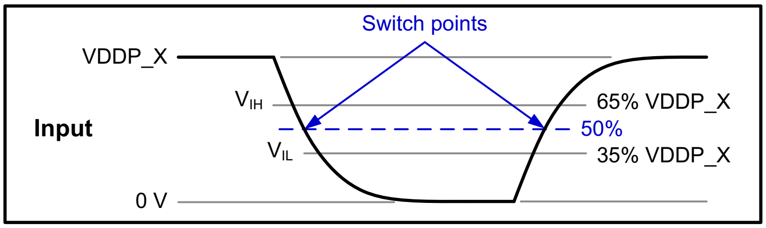


Figure 3-5 Digital input-signal switch points

Outputs (address, chip selects, clocks, and so on) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over the worst-case process/voltage/temperature. Since the pad output structures (Figure 3-6) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- $V_{OH} \sim V_{DDPX\_X}$ - 50 mV or more
- $V_{OL} \sim$ 50 mV or less

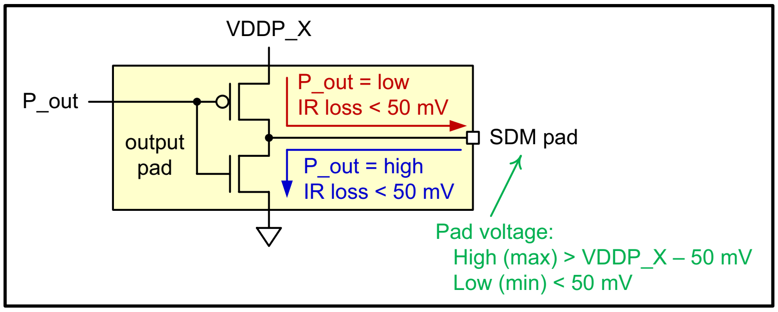


Figure 3-6 Output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DDPX_X} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) provides approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) provides approximately 1.25 mA or more at ½ × [V_{DDPX_X} - 50 mV + V_{OH} (min)].

The output pads are CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slow rates limit high-frequency spectral components that desensitize the companion radio.

The output drivers' rise time [**t**(r)] and fall time [**t**(f)] values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described previously.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers may get worse, and hold time numbers may get better.

3.8.1 EBI0 memory support

The EBI0 port is dedicated to the non-PoP LPDDR3 SDRAM memory that is attached to the SDM450/SDA450 chipset.

3.8.1.1 LPDDR3 SDRAM strobe

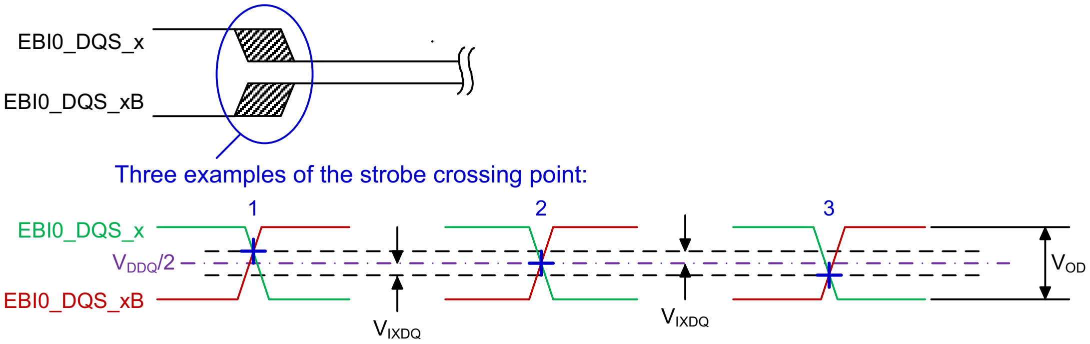


Figure 3-7 DDR SDRAM EBI0_DQS_x and EBI0_DQS_xB

Table 3-16 DDR SDRAM DQS timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock crossover point	± offset from VDDQ/2	-120	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

3.8.1.2 LPDDR3 SDRAM read and write timing

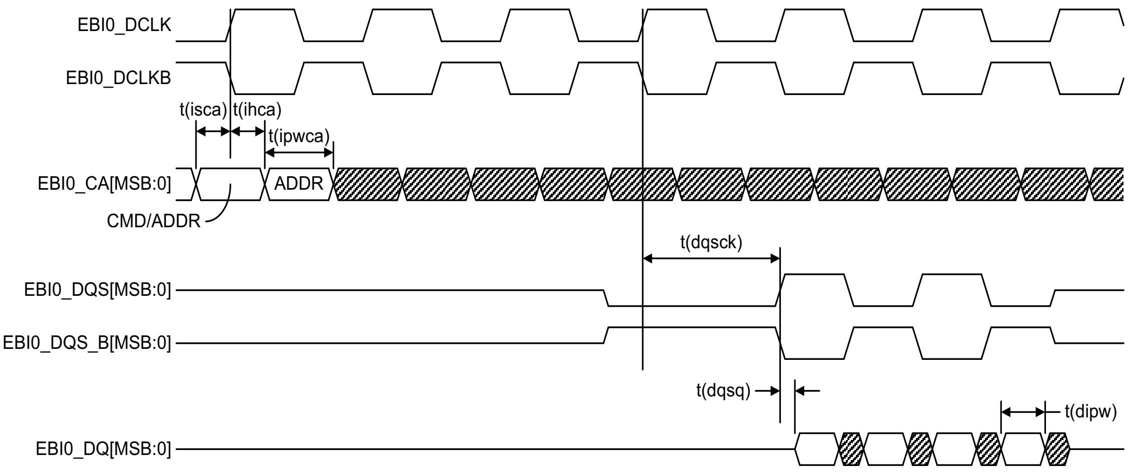


Figure 3-8 DDR SDRAM read timing

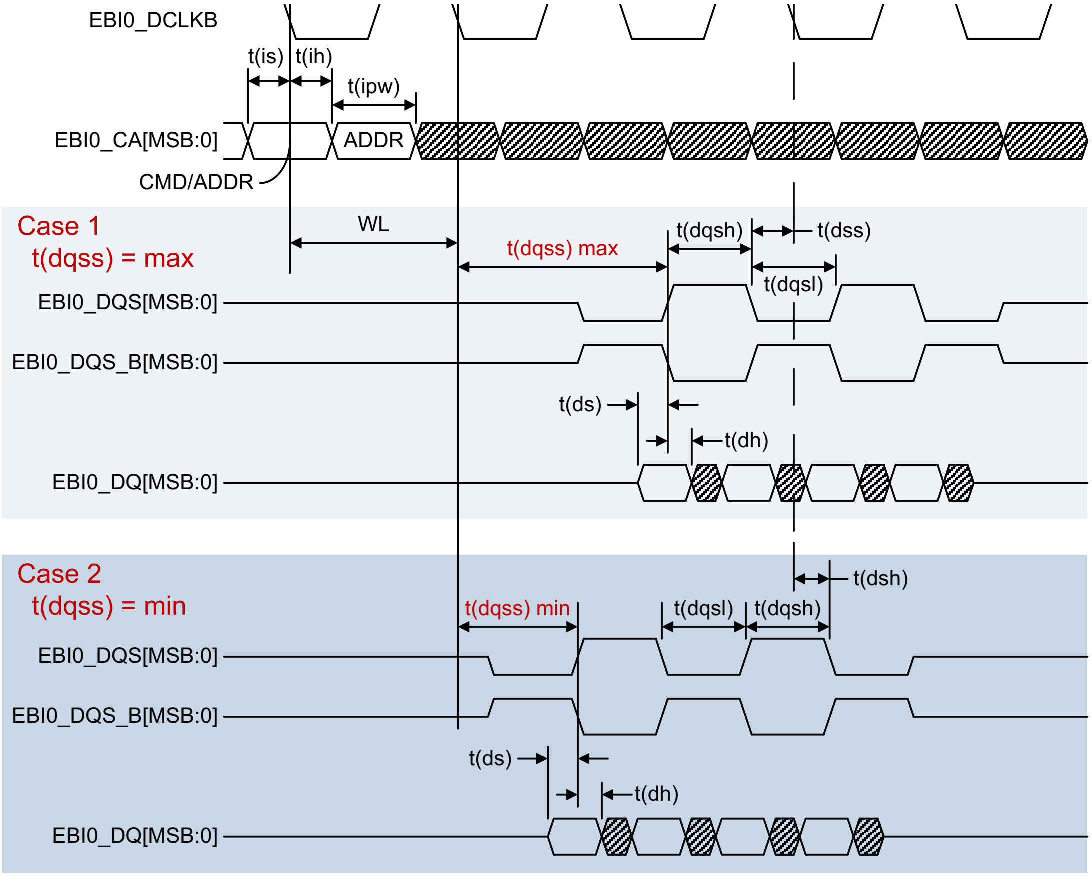


Figure 3-9 DDR SDRAM write timing

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.10.1 for secure digital interface details.

3.8.3 NOR memory on SPI

SPI can be used to support NOR memory devices with appropriate user-modified software. See Section 3.10.8 for the serial peripheral interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SDM450/SDA450 device supports up to three four-lane camera interfaces or up to four (two four-lane and two one-lane) camera interfaces.

Table 3-17 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	SDM variations
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported	None
MIPI Alliance Specification for DPHY v1.2	None	None
MIPI Alliance Specification for CPHY v1.0	None	None

3.9.2 Audio support

The SDM450/SDA450 supports the WCD9326 and WCD9335 audio codec ICs to provide the system’s audio functions. SDM audio-related interface options with the WCD include:

- SLIMbus: Section 3.10.4
- I^{2}S: Section 3.10.5
- I^{2}C: Section 3.10.6

See the *WCD9326 Audio Codec Device Specification* (80-NT793-1) and the *WCD9335 Audio Codec Device Specification* (80-NT781-1) for the performance characteristics.

3.9.3 Display support

SDM450/SDA450 supports two 4-lane MIPI_DSI.

Table 3-18 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	SDM variations
MIPI Alliance Specification for Display Serial Interface	None	None
MIPI Alliance Specification for D-PHY V1.2	None	None

3.10 Connectivity

The connectivity functions supported by the SDM450/SDA450 that require electrical specifications include:

- SD, including SD cards and MMC
- USB host/slave support with built-in physical layer (PHY)
- UIM ports, including dual-voltage options
- SLIMbus interface
- I^{2}S interfaces
- Touchscreen connections
- Through proper configuration of the eight BLSP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - I^{2}C interfaces
  - SPI ports

Pertinent specifications for these functions are detailed in the following subsections.

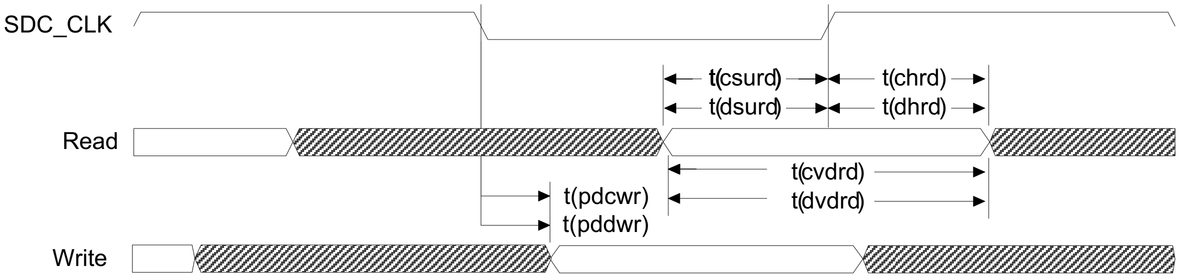
NOTE: In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

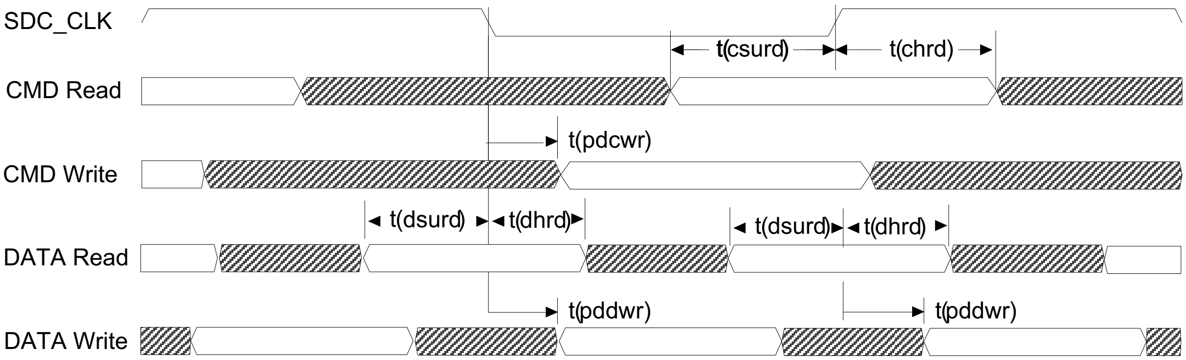
Table 3-19 Supported SD standards and exceptions

Applicable standard	Feature exceptions	SDM variations
Embedded Multimedia Card (e.MMC) Specification version 5.1	None	Timing specifications: see Figure 3-10.
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

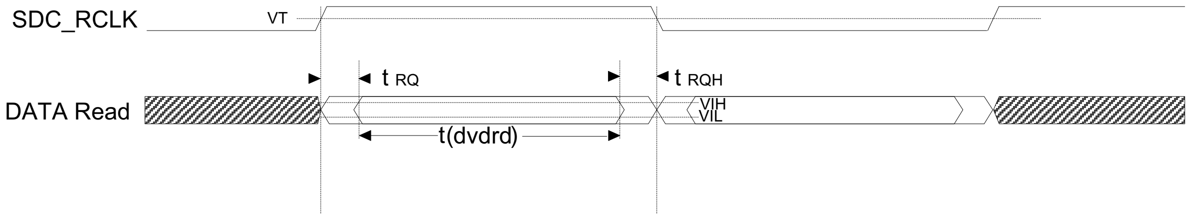
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

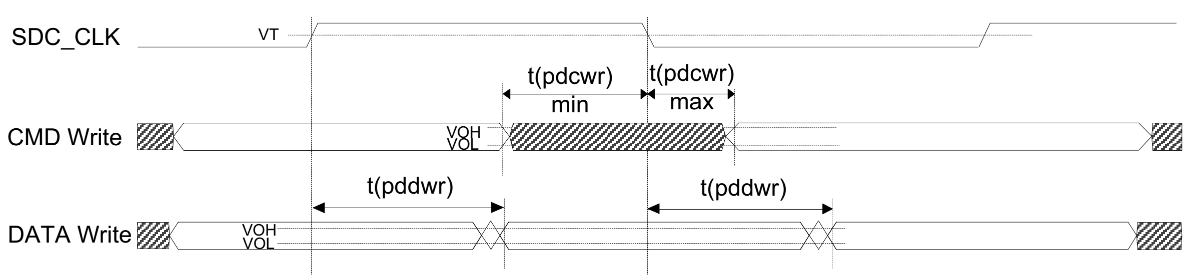


Figure 3-10 SD interface timing

3.10.2 USB interfaces

Table 3-20 Supported USB standards and exceptions

Applicable standard	Feature exceptions	SDM variations
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None	None

3.10.3 UIM interface

Table 3-21 Supported UIM standards and exceptions

Applicable standard	Feature exceptions	SDM variations
ISO/IEC 7816-3	None	None

3.10.4 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions	SDM variations
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

3.10.5 I^{2}S interfaces

Legacy I^{2}S interfaces for primary and secondary microphones and speakers.

Table 3-23 Supported I^{2}S standards and exceptions

Applicable standards	Feature exceptions	SDM variations
Philips I2S Bus Specifications revised June 5, 1996 (Available for free download.)	None	Timing - see Figure 3-11 When an external SCK clock is used, a duty cycle between 45% to 55% is required.

Figure 3-11 I²S timing diagram

Table 3-24 I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit	Note x% of T
Using internal SCK							
Frequency		–	–	–	12.288	MHz	–
T	Clock period	–	81.380	–	–	ns	–
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns	–
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns	–
t(sr)	SD and WS input setup time	–	16.276	–	–	ns	20
t(hr)	SD and WS input hold time	–	0	–	–	ns	–
t(dtr)	SD and WS output delay	–	–	–	24.414	ns	30
t(htr)	SD and WS output hold time	–	0	–	–	ns	–
Using external SCK							
Frequency		–	–	–	12.288	MHz	–
T	Clock period	–	81.380	–	–	ns	–

Table 3-24 I^{2}S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit	Note x% of T
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns	–
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns	–
t(sr)	SD and WS input setup time	–	16.276	–	–	ns	20
t(hr)	SD and WS input hold time	–	0	–	–	ns	–
t(dtr)	SD and WS output delay	–	–	–	24.414	ns	15
t(htr)	SD and WS output hold time	–	0	–	–	ns	–

1. Load capacitance between 10 pF to 40 pF.

3.10.6 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.10.7) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.7 I^{2}C interface

Table 3-25 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions	SDM variations
I^{2}C Specification, version 3.0	None	Multi-master, slave mode, and 10-bit addressing are not supported.

3.10.8 Serial peripheral interface

The SDM450/SDA450 supports SPI as a master only. Any one of the eight BLSP ports can be configured as an SPI master.

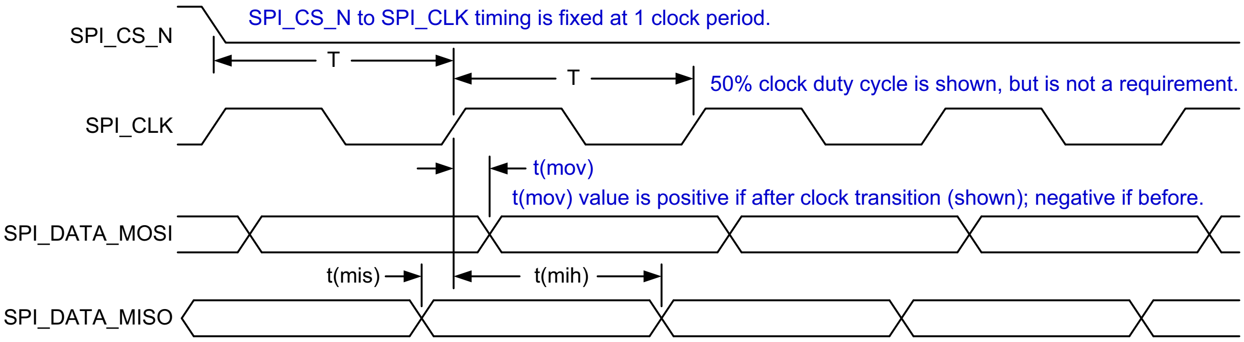


Figure 3-12 SPI master timing diagram

Table 3-26 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz XO input

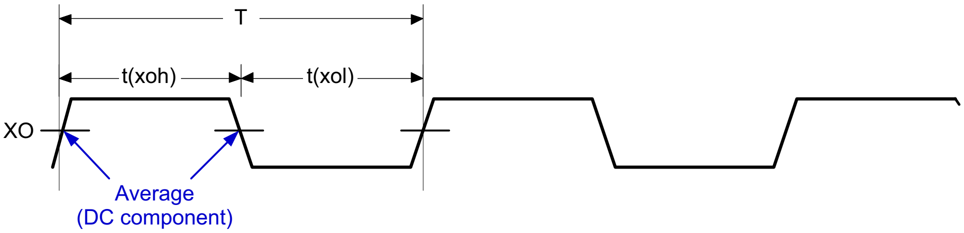


Figure 3-13 XO timing parameters

Table 3-27 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal, and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.11.1.2 Sleep clock

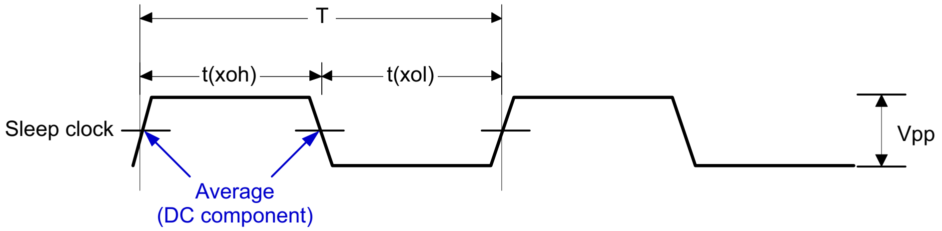


Figure 3-14 Sleep-clock timing parameters

Table 3-28 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T	Sleep-clock period		–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

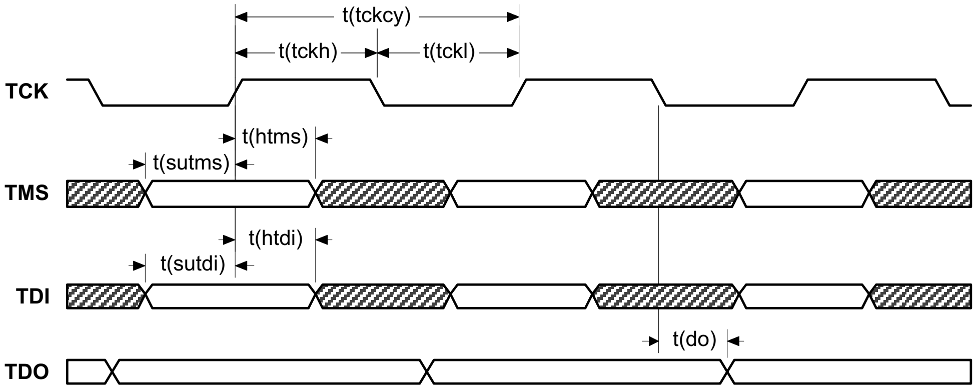


Figure 3-15 JTAG interface timing diagram

Table 3-29 JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data output delay		–	–	15	ns

3.11.4 SWD

Figure 3-16 SWD write and read AC timing diagram

Table 3-30 AC timing parameters

Parameter		Min	Max	Unit
$\mathbf{T}_{os}$	SWDIO output skew to the falling edge of SWDCLK	0	17.5	ns
$\mathbf{T}_{su}$	Input setup time between SWDIO and the rising edge of SWDCLK	4	–	ns
$\mathbf{T}_{hd}$	Input hold time between SWDIO and the rising edge of SWDCLK	1	–	ns

3.12 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-9 and Table 2-11. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary and therefore are not specified.

3.12.1 RFFE

Table 3-31 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	SDM variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

3.12.2 SPMI

Table 3-32 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	SDM variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

4 Mechanical information

4.1 Device physical dimensions

The SDM450/SDA450 is available in the 792 NSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 792 NSP has a 14 mm by 12 mm body, with a maximum height of 0.84 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 792 NSP outline drawing is shown in Figure 4-1.

NOTE: Click the following links to download the *Package Outline Drawing, 792 NSP, 14.0 × 12.0 × 0.84 mm, S145, M450* (NT90-P5074-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-P5074-1

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NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

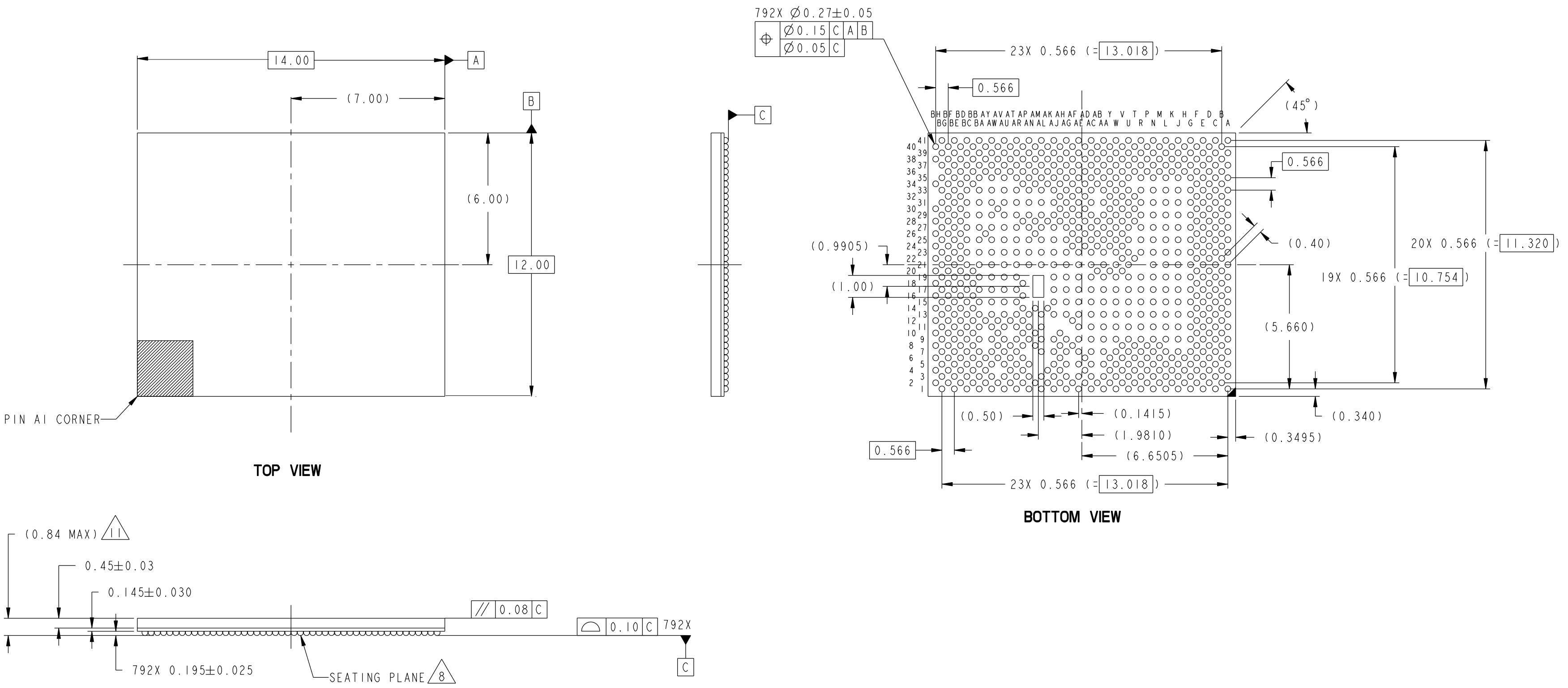


Figure 4-1 792 NSP (14 × 12 × 0.84 mm) outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing. https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-P5074-1

4.2 SDM450 Part marking

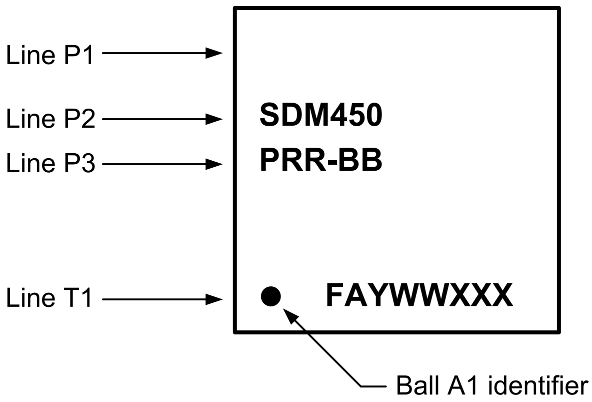


Figure 4-2 SDM450 device marking (top view, not to scale)

Table 4-1 SDM450 marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm name or logo
P2	SDM450	Qualcomm Technologies, Inc. (QTI) product name
P3	PRR-BB	P = product configuration code ■ See Table 4-4 for assigned values. RR = product revision ■ See Table 4-4 for assigned values. BB = feature code ■ See Table 4-4 for assigned values.
	Blank or variable	Space below line P3 and above T1
T1	FAYWWXXX	F = supply source code ■ F = J (Samsung) ■ F = H (GLOBALFOUNDRIES) A = assembly site code ■ A = E (ASE, Taiwan) ■ A = U (Amkor, China) ■ A = K (SPIL, Taiwan) ■ A = H (JCET STATS ChipPAC, Korea) Y = single-digit year WW = work week (based on calendar year) XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE: For complete marking definitions of all SDA450 variants and revisions, see the *SDM450/SDA450 Device Revision Guide* (80-PC173-4).

4.3 SDA450 Part marking

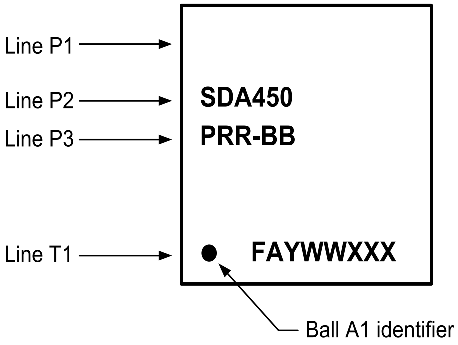


Figure 4-3 SDA450 device marking (top view, not to scale)

Table 4-2 SDA450 marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm name or logo
P2	SDA450	Qualcomm Technologies, Inc. (QTI) product name
P3	PRR-BB	P = product configuration code ■ See Table 4-4 for assigned values. RR = product revision ■ See Table 4-4 for assigned values. BB = feature code ■ See Table 4-4 for assigned values.
	Blank or variable	Space below line P3 and above T1
T1	FAYWWXXX	F = supply source code ■ F = J (Samsung) ■ F = H (GLOBALFOUNDRIES) A = assembly site code ■ A = E (ASE, Taiwan) ■ A = U (Amkor, China) ■ A = K (SPIL, Taiwan) ■ A = H (JCET STATS ChipPAC, Korea) Y = single-digit year WW = work week (based on calendar year) XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE: For complete marking definitions of all SDA450 variants and revisions, see the *SDM450/SDA450 Device Revision Guide* (80-PC173-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-3.

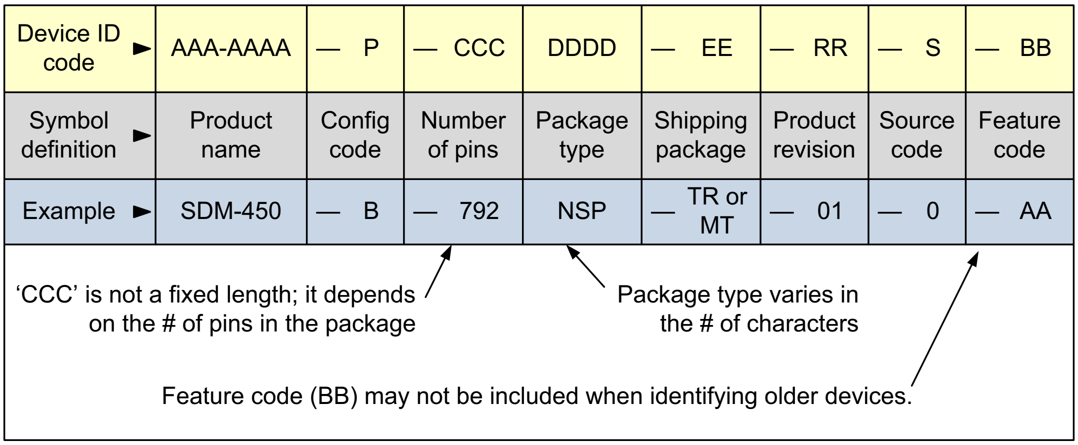
Table 4-3 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.4 Device ordering information

4.4.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-4.



Device ID code ►	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	SDM-450	— B	— 792	NSP	— TR or MT	— 01	— 0	— AA

'CCC' is not a fixed length; it depends on the # of pins in the package

Package type varies in the # of characters

Feature code (BB) may not be included when identifying older devices.

Figure 4-4 Device identification code

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type [1]	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [2]	Hardware revision number	FEATURE_ID [3]	S value [4]	Comments
SDM450	ES	B01-AA	0x0 009A 0E1	0x48	0	1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD display, Cat6, CDMA
		D01-AA		0x43		1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD display, Cat6, non-CDMA
		F01-AA		0x49	0	1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD display, Cat7, CDMA
		H01-AA		0x46		1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD display, Cat7, non-CDMA
	CS	B01-AA		0x48	0	1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD+ display, Cat6, CDMA
		D01-AA		0x43		1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD+ display,Cat6, non-CDMA
		F01-AA		0x49	0	1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD+ display, Cat7, CDMA
		H01-AA		0x46		1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD+ display, Cat7, non-CDMA
SDA450	CS	A01-AA	0x0 00B9 0E1	0x0	0	1.8 GHz octa core CPU, 933 MHz DDR, 600 MHz GPU, 21 MP camera, 1080p video, FHD+ display

1. All devices with the date code (YWW) are CS devices.
    - ASE ≥ 728
    - JCET STATS ChipPAC ≥ 728
    - Amkor ≥ 726
    - SPIL ≥ 727
2. BB is the feature code that identifies an IC’s specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
3. See Table 4-3. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.

4. S is the source configuration code that identifies all of the qualified die fabrication source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-5.

Table 4-5 Source configuration code

S value	Die	F value = J	F value = H
0	Digital	Samsung	GLOBALFOUNDRIES
Other columns and rows will be added in a future revision of this document, if needed.			

4.4.2 Daisy chain devices

The SDM450 daisy chain ordering part number is TP-792NSP-1.

4.5 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	One year	≤ 30°C/60% RH
2a	Four weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SDM450 rating** **SDA450 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SDM450/SDA450 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.6 Thermal characteristics

Rather than provide thermal resistance values q_{JC} and q_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE: Click the following link to download the SDA450/SDA450 thermal package model, *SDM450 792NSP Package Thermal Model Icepak* (HS11-PC173-5HW) from the CreatePoint website.
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PC173-5HW

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

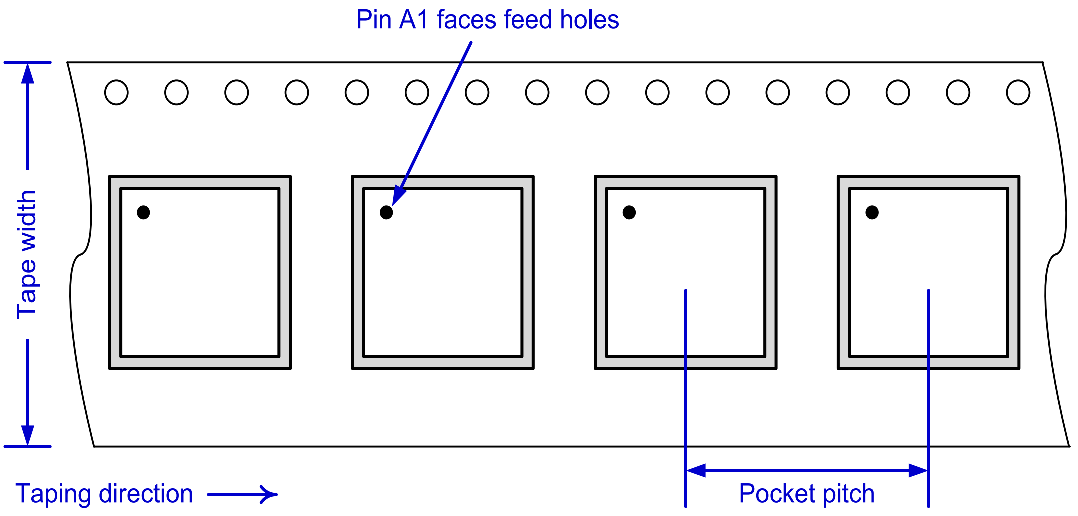
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SDM450/SDA450 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

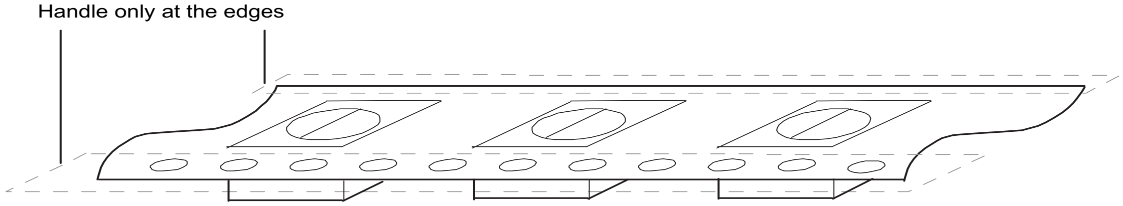


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

Store the SDM450/SDA450 devices delivered in tape and reel carriers in a sealed, moisture barrier, and antistatic bags. See the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before installing onto a PCB.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SDM450/SDA450 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SDM450/SDA450 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its Sn/Ag/Cu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. All SMT process recommendations described in Section 6.2 can be performed using daisy chain components.

Ordering information is given in Section 4.4.

Daisy chain PCB routing recommendations are available for download.

NOTE: Click the following link to download *Daisy Chain Interconnect, 792 NSP, 14.0 × 12.0 mm* (DS90-P5074-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-P5074-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 lists the SDM450/SDA450 reliability evaluation report for 792 NSP from Samsung.

Table 7-1 Silicon reliability results – Samsung

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	240	Passed DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	240	Passed FIT < 50 [1]
Mean time to failure (MTTF) t = $1/\lambda$ in million hours (Total samples from three different wafer lots)	240	Passed MTTF > 20 [1]
ESD – human body model (HBM) rating JESD22-A114-F Target 1000 V (Total samples from one wafer lot)	3	Passed 1000 V
ESD – charged device model (CDM) rating JESD22-C101-D Target 250 V (Total samples from one wafer lot)	3	Passed 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C (Total samples from one wafer lot)	6	Passed
Latch-up (Vsupply over voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C (Total samples from one wafer lot)	6	Passed

1. The cumulative DPPM, FIT, and MTTF are based on multiple products under the Samsung 14 nm LPP process.

Table 7-2 Package reliability results – Samsung

Tests, standards, and conditions	AST sample size	ATC sample size	SCK sample size	SPIL sample size	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	693	Passed [1]
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cph **Preconditioning:** JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration or 110°C/85% RH and 264-hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration or 110°C/85% RH and 264-hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	96	Passed [1]
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	231	Passed [1]
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	–	–	N/A See note.
Physical dimensions: JESD22-B100-A (Total samples from three different assembly lots at each SAT)	30	30	30	30	Passed [1]
Die shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	15	Passed [1]

1. Data is leveraged from other previously qualified NSP packages that are similar to this configuration.

7.2 Reliability qualifications summary

Table 7-1 lists the SDM450/SDA450 reliability evaluation report for 792 NSP from GLOBALFOUNDRIES.

Table 7-3 Silicon reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	357	Passed DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	357	Passed FIT < 50 [1]
Mean time to failure (MTTF) t = $1/\lambda$ in million hours (Total samples from three different wafer lots)	357	Passed MTTF > 20 [1]
ESD – HBM rating JESD22-A114-F Target 1000 V (Total samples from one wafer lot)	3	Passed 1000 V
ESD – CDM rating JESD22-C101-D Target 250 V (Total samples from one wafer lot)	3	Passed 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C (Total samples from one wafer lot)	6	Passed
Latch-up (Vsupply over voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C (Total samples from one wafer lot)	6	Passed

1. The cumulative DPPM, FIT, and MTTF are based on multiple products under the GLOBALFOUNDRIES 14 nm LPP process.

Table 7-4 Package reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	AST sample size	ATC sample size	SCK sample size	SPIL sample size	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	693	Passed [1]
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cph **Preconditioning:** JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	96	Passed [1]
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	231	Passed [1]
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	–	–	N/A See note.
Physical dimensions: JESD22-B100-A (Total samples from three different assembly lots at each SAT)	30	30	30	30	Passed [1]
Die shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	15	Passed [1]
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	Passed [1]
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	Passed [1]

1. Data is leveraged from other previously qualified NSP packages that are similar to this configuration.

7.3 Qualification sample description

Device characteristics

Device name:	SDM450/SDA450
Package type:	792 NSP
Package body size:	14 mm × 12 mm × 0.84 mm
Lead count:	792
Lead composition:	SAC125/Ni
Fab process:	14 nm FinFET
Fab sites:	Samsung, GLOBALFOUNDRIES
Assembly sites:	JCET STATS ChipPAC, Korea Amkor, China ASE, Taiwan SPIL, Taiwan
Solder ball pitch:	0.4 mm

Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	May 2017	Initial release
B	August 2017	■ Global: Updated the information for the FHD+ display ■ Table 4-4 Device identification details: Added the CS information to support the FHD+ display
C	December 2017	■ Global: □ Added a new variant, SDA450 □ Updated the title ■ Added notes to reflect the SDA450 deviation from SDM450 ■ Section 1.1 Functional block diagram: Added the SDA450 functional block diagram ■ Figure 2-3 SDA450 pin assignments: Added a new pin assignments sheet for SDA450 ■ Table 3-6 Power distribution network impedance vs. frequency: Added the PDN specification for VDD_MODEM voltage in SDA450 ■ Section 4.3 SDA450 Part marking: Added a new section for SDA450 ■ Table 4-4 Device identification details: Added the CS information of SDA450
D	March 2018	Global: Removed all the FHD+ values across the document
E	April 2018	Table 4-4 Device identification details: Updated the Hardware ID for a few variants
F	April 2018	Global: Updated the block diagram to support PMI632
G	September 2018	■ *Figure 3-11 I2S timing diagram:* Updated the I^{2}S timing diagram ■ *Table 3-24 I2S interface timing:* □ Added a new column to show the X% of T □ Updated the max value of t(dtr) SD and WS output delay
H	October 2018	■ Section 1.1 *Functional block diagram*: Added note

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

Document release date: October 24, 2018

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