Device description

The SDM710 includes the next generation of the Qualcomm® Snapdragon™ 700 series processor and LTE modem.
Key processor and memory characteristics include:

- 10 nm LPP FinFET process for lower active power dissipation and faster CPU performance
- 11.1 × 10.5 mm non package-on-package (non-PoP)
- A customized 64-bit ARM v-8 compliant applications processor (Qualcomm® Kryo™ 360 CPU)
  - Kryo Gold: dual high-performance cores 2.208 GHz
  - Kryo Silver: hexa low-power cores 1.708 GHz
- Qualcomm® Adreno™ GPU 616 graphics processing unit (GPU) with 64-bit addressing; designed for 500 MHz
- Dedicated Compute DSP for Computer Vision and Video Post Processing. Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (dual HVX 512)
- Low-power island (LPI) – contains DSP shared between Snapdragon sensor core and low-power audio subsystem. The Snapdragon sensor supports always-on use cases.
- Dual-channel non-PoP high-speed memory, LPDDR4X SDRAM designed for 1866 MHz clock (2 × 16 bit)

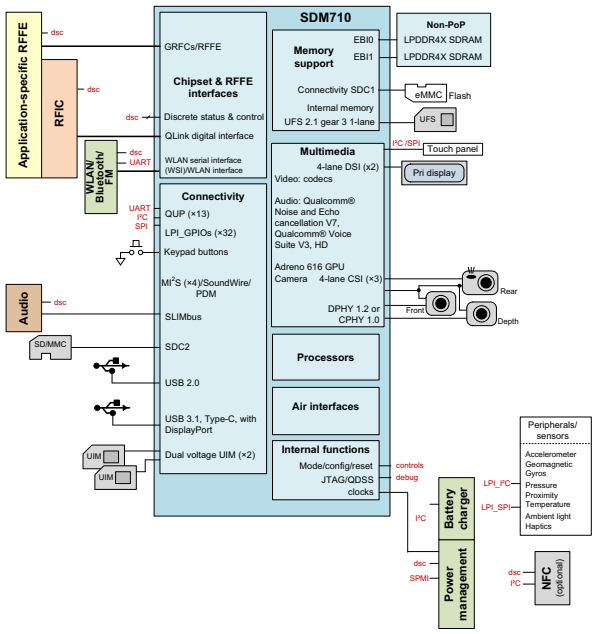
The latest air interface standards are supported, including:

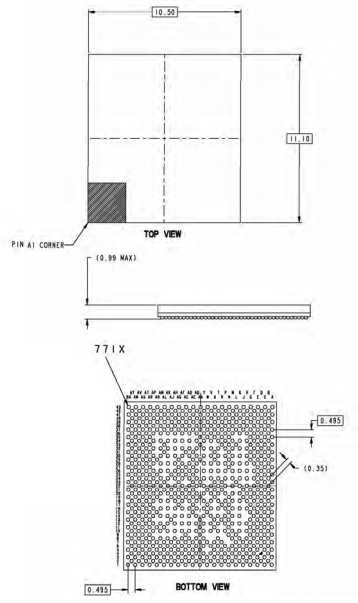
- LTE Cat12/13 (FDD and TDD)
- DC-HSPA+
- TD-SCDMA
- WCDMA
- CDMA up to 1X advanced and 1xEV-DOrA

Key features (see Section 1.2 for details)

- Always-on subsystem with RPMh for hardware-based resource and power management
- Qualcomm® Universal Bandwidth Compression (UBWC) 2.0, 2x compression with camera, display, and DSP
- More RF operating bands and advanced techniques with SDR660:
  - Sixth-generation LTE multimode modem Rel. 13
  - Up to 800 Mbps LTE peak throughput for downlink and 150 Mbps for uplink
  - 3DL/1UL and 2DL/2UL LTE (60 MHz CA across RF bands)
  - 256 QAM DL
- Display support: 2880 × 1440 at 60fps, up to 10 hardware layers, Qualcomm® Low-Power Picture Enhancement display feature, and Qualcomm® TruPalette™ display feature, VESA DSC 1.1
- Two 4-lane DSIs D-PHY 1.2 at 2.5 Gbps per lane or C-PHY 1.0 at 17 Gbps (2.5 G symbols per trio per second)
- Dual 14-bit image signal processing (ISP) + 1 Lite ISP: 20 + 20 + 2 MP at 26 fps to support 32 MP/30 fps.
- Three 4-lane CSIs (4/4/4 or 4/4/2/1) D-PHY 1.2 at 2.5 Gbps per lane or three 3-lane C-PHY 1.0 at 17 Gbps (2.5 G symbols per trio per second)
- Support for UFS 2.1 gear 3 (one-lane), eMMC 5.1, and SD 3.0
- Support for USB 3.1 Type-C with DisplayPort and USB 2.0
- WCN3990: WLAN 2 × 2 802.11a/b/g/n/ac with DBS and 160 MHz, Bluetooth 5.0 and FM
- WCN3980: WLAN 1 × 1 802.11a/b/g/n/ac and Bluetooth 5.0 and FM

SDM710 high-level block diagram and 771 PSP drawing





Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

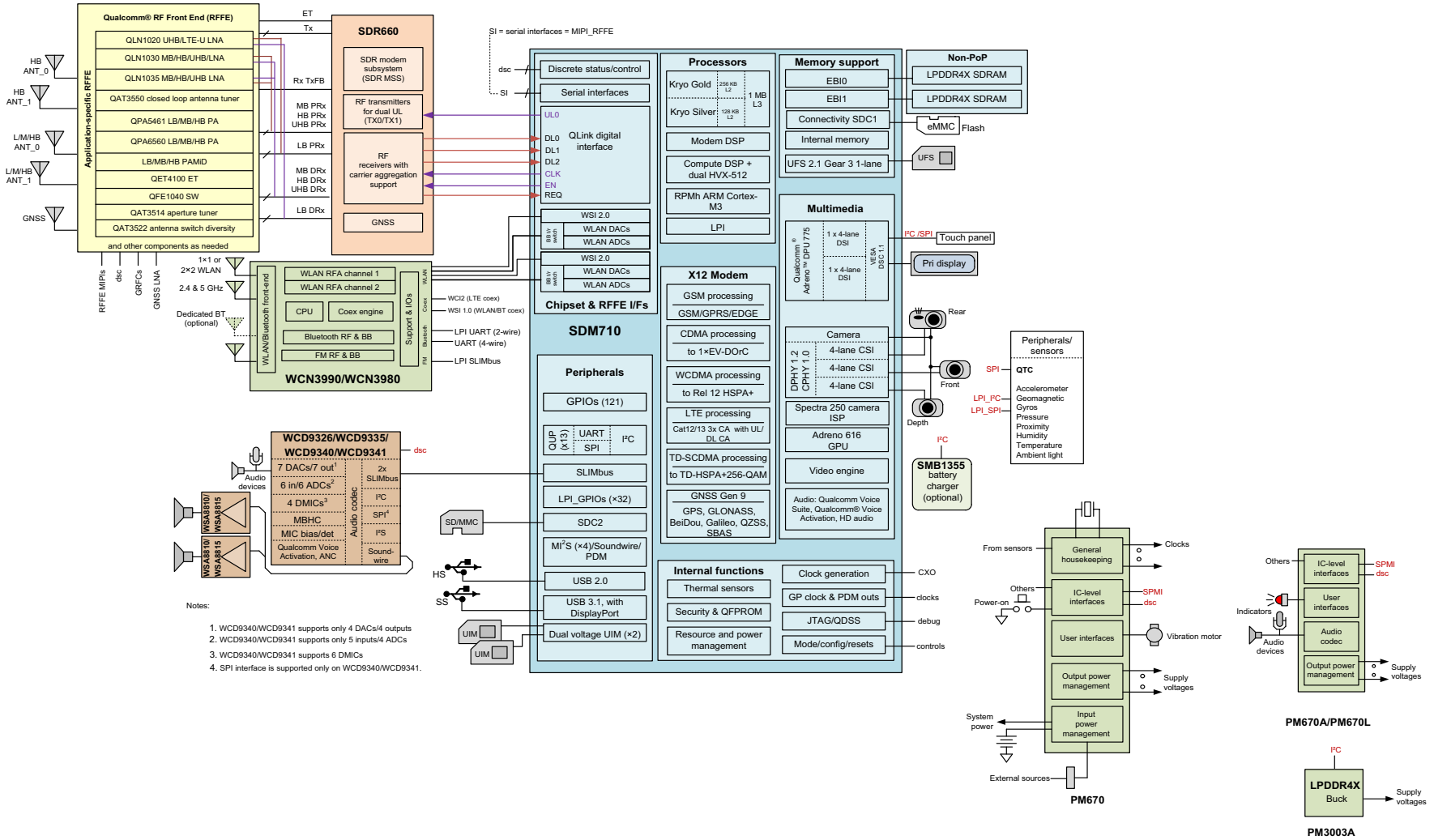


Figure 1-1 SDM710 functional block diagram and example application

1.2 SDM710 features

NOTE: Some of the hardware features integrated within the SDM710 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SDM710 features.

Table 1-1 SDM710 features

Feature	SDM710 capability
Processors	
Applications	64-bit applications processor (Kryo 360) with 1 MB L3 cache ■ Dual high-performance Kryo cores 2.208 GHz – Gold cluster with 256 KB L2 cache per core ■ Hexa low-power Kryo cores 1.708 GHz – Silver cluster with 128 KB L2 cache per core Note: Exact maximum frequency values will be updated during CS timeframe.
Digital signal processing	Compute DSP with Hexagon Vector eXtensions (dual-HVX512)
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Low-power island	Low-power island with Hexagon DSP consists of Snapdragon sensor core and low-power audio subsystem
Memory support	
System memory via EBI	Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM designed for a 1866 MHz clock (2 × 16 bit) 512 KB system cache
Other internal memory	256 KB IMEM 512 KB GMEM for graphics
External memory Via	 UFS 2.1 gear 3 (one-lane), eMMC 5.1, and SD 3.0
RF support	
RF operating bands	Defined by the RF transceiver SDR device
Air interfaces	See Table 1-2 for variant support.
GSM	Yes
CDMA	Yes
WCDMA	Yes
TD-SCDMA	Yes
LTE	Yes (CAT12/CAT13 3 × 20 CA at 800 Mbps DL and 150 Mbps UL capability)
WLAN/Bluetooth	Yes (with WCN3990/WCN3980)
Advanced techniques	Up to 3 DL CA, up to 2 UL CA, 4 × 4 MIMO using single TRx, LTE-U, and LAA
GNSS – Integrated Qualcomm® Location Suite engine	Gen 9; GPS, GLONASS, BeiDou, Galileo, QZSS, and SBAS

Table 1-1 SDM710 features (cont.)

Feature	SDM710 capability
Multimedia	
Display support	
MIPI-DSI	Two 4-lane; DSI D-PHY 1.2 or C-PHY 1.0; VESA DSC 1.1
DisplayPort	DisplayPort 1.4+ data concurrency over USB
Miracast	Yes; v2.0 (4k at 30 fps)
Example combinations	■ 2880 × 1440 at 60fps + 4K30 DisplayPort 10-bit or 4K30 Miracast ■ ADv4, 10-layer, HDR10 ■ VESA DSC 1.1
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, and OLED panels
Camera interfaces	2x ISP 14 bit + 1x Lite ISP: 20 + 20 + 2 MP at 26 fps and 32 MP at 30 fps
MIPI-CSI	MIPI combination DPHY 1.2/CPHY 1.0 configurable in either 4/4/4 or 4/4/2/1 ■ D-PHY: 2.5 Gbps/lane ■ C-PHY: ~17 Gbps (2.5 G symbols per trio per second)
Performance	■ Real-time sensor input resolution: 20 + 20 + 2 MP ■ 32 MP 30 ZSL with a dual ISP ■ 20 MP 26 ZSL with a single ISP
Mobile display processor	Snapdragon display engine 775
Video applications performance	
Encode	4K30 8-bit: H.264/VP8/HEVC
Decode	4K30 8-bit: H.264/HEVC/VP9 4K30 10-bit: HEVC/VP9
Concurrency	4K30 decode + 1080p30 encode
Graphics	■ Adreno 616, 3D graphics accelerator with 64-bit addressing, 500 MHz (maximum frequency) ■ OpenGL ES 3.2, Vulkan, DX12.2 ■ OpenCL 2.0, DirectCompute, RenderScript
Audio Option 1: PM670A/PM670L codec with integrated speaker amplifier Option 2: PM670A/PM670L codec + WSA8810/WSA8815 speaker amplifier Option 3: WCD9326 + WCD9335 codec + WSA8810/WSA8815 speaker amplifier Option 4: WCD9340 codec + WSA8810/WSA8815 speaker amplifier Option 5: WCD9341 codec + WSA8810/WSA8815 speaker amplifier	
Low-power audio	Low power; 7.1 surround sound
Voice codec support	EVRC, EVRC-B, and EVRC-WB G.711 and G.729A/AB GSM-FR, GSM-EFR, and GSM-HR AMR-NB, AMR-WB, AMR-eAMR, and AMR-BeAMR
Audio codec support	MP3; AAC; HE AAC v1, v2; WMA 9/Pro; Dolby AC-3, eAC-3, DTS-HD, FLAC, APE, ALAC, and AIFF

Table 1-1 SDM710 features (cont.)

Feature	SDM710 capability
Enhanced audio	■ Surround sound: Dolby Digital, Dolby Atmos, and DTS-HD ■ Qualcomm® Audio Post-processing ■ Qualcomm Noise and Echo Cancellation v7 and Qualcomm Voice Suite v3 ■ WSA8810/WSA8815 speaker protection
Connectivity	
Qualcomm universal peripheral (QUP) ports	13, 4 bits each; multiplexed serial interface functions
UART	UART interface available on all QUPs. HS-UART available on GPIO QUP6, QUP7 and LPI core QUP3, QUP4, QUP5
I^2C	I^2C interface available on all QUPs up to 1 Mbps for touch, sensors, near field communicator (NFC), and so on; dedicated controller for each port
SPI	SPI interfaces available on all QUPs for cameras, sensors, and so on; dedicated controller for each port
CCI I^2C	Two dedicated I^2C interfaces for camera
UIM	Two – dual voltages (1.8 V and 2.95 V)
USB	USB 3.1, which can support Type-C with DisplayPort
Secure digital interfaces	■ 8-bit port SDC1 and 4-bit port SDC2; eMMC5.1 and SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card; eSD boot
Audio interfaces	
SLIMbus	One port SLIMbus interface to WCD9326/WCD9335/WCD9340/WCD9341
MI^2S	Four ports
CDC PDM port	Interface between SDM710 and PM670A/PM670L for audio application
SWR	SoundWire interface to WSA8810/WSA8815
Wireless connectivity	WCN3990 2 × 2 802.11ac RF WCN3980 1 × 1 802.11ac RF
Touchscreen support	Capacitive panels via ext IC (I^2C, SPI, and interrupts) QTC800H, QTC801S, and QTC401 Qualcomm® improveTouch™ Processing controller
Configurable GPIOs	
Number of GPIO ports	121
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs

Table 1-1 SDM710 features (cont.)

Feature	SDM710 capability
Internal functions	
Security General hardware security features Crypto engines TrustZone services DRM support in hardware	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment, hardware supported KeyStore Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), inline crypto engine (FIPS-compliant) Secure file system, fast trusted storage PlayReady SL2000/SL3000, Widevine level 1, ISDB-T, and CPZ for GPU and DSP
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, QDSS, and ETM
Others	Thermal sensors, modes and resets, and peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
SDR RF transceivers QLink digital interface	■ Three downlink lanes and one uplink lane ■ Improved layout, routing, package, and signal integrity
Power management	PM670 ■ Integrated switching charger with Qualcomm® Quick Charge™ technology 4.0 support ■ Six switching regulators and 18 LDOs ■ 38.4 MHz system clock generation PM670A/PM670L ■ AMOLED variant PM670A and LCD variant PM670L support ■ Integrated audio codec ■ Five switching regulators and 10 LDOs PM3003A ■ Buck regulator for LPDDR4X
Wireless connectivity WLAN baseband data Bluetooth	 I/Q differential pair interface UART interface
Fabrication technology and package	
Digital die	10 nm FinFET process for lower active power dissipation
Non-PoP – small, thermally efficient package	771 PSP: 11.1 × 10.5 × 0.99 mm; 0.35 mm pitch

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
LTE	
Category	12/13
Carrier aggregation	FDD and TDD; up to 60 MHz CA is not symmetric uplink and downlink; it is 60 MHz down and 40 MHz up.
CA direction	Uplink and downlink
Other LTE support	■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ Four-way Rx diversity ■ 4 × 4 MIMO using single TRx, LTE-U, and LAA
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1xSLTE and 1xSRLTE ■ hVoLTE and hSRLTE
Multi-SIM	
3G	3G + GSM DSDS
4G	4G + GSM DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite with global navigation satellite system (GNSS) support	
Gen 9	GPS, GLONASS, BeiDou, Galileo, QZSS, and SBAS

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN3990	802.11ac, 2 × 2 MIMO with DBS support
With WCN3980	802.11ac, 1 × 1 MIMO

Table 1-4 Wireless connectivity summary by standard (cont.)

Standard	Feature descriptions
Bluetooth	
With WCN3990/WCN3980	Bluetooth 5.0 and earlier
FM	
With WCN3990/WCN3980	Rx

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
P2	Pad group 2 (SDC2); 1.8 V or 2.95 V
P3	Pad group 3 (most peripherals); 1.8 V
P5	Pad group 5 (UIM1); 1.8 V or 2.95 V
P6	Pad group 6 (UIM2); 1.8 V or 2.95 V
P7	Pad group 7 (eMMC); tied to VDD_P7 pins (1.8 V only)
P10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
P11	Pad group 11 (CXO); 1.8 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SDM710 is available in the 771 PSP. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

The text within Figure 2-1 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.
- Download the *SDM670/SDM710 Pin Assignment and GPIO Configuration Spreadsheet* (80-PB873-1A) – this Microsoft Excel spreadsheet lists all SDM670/SDM710 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PB873-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PB873-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

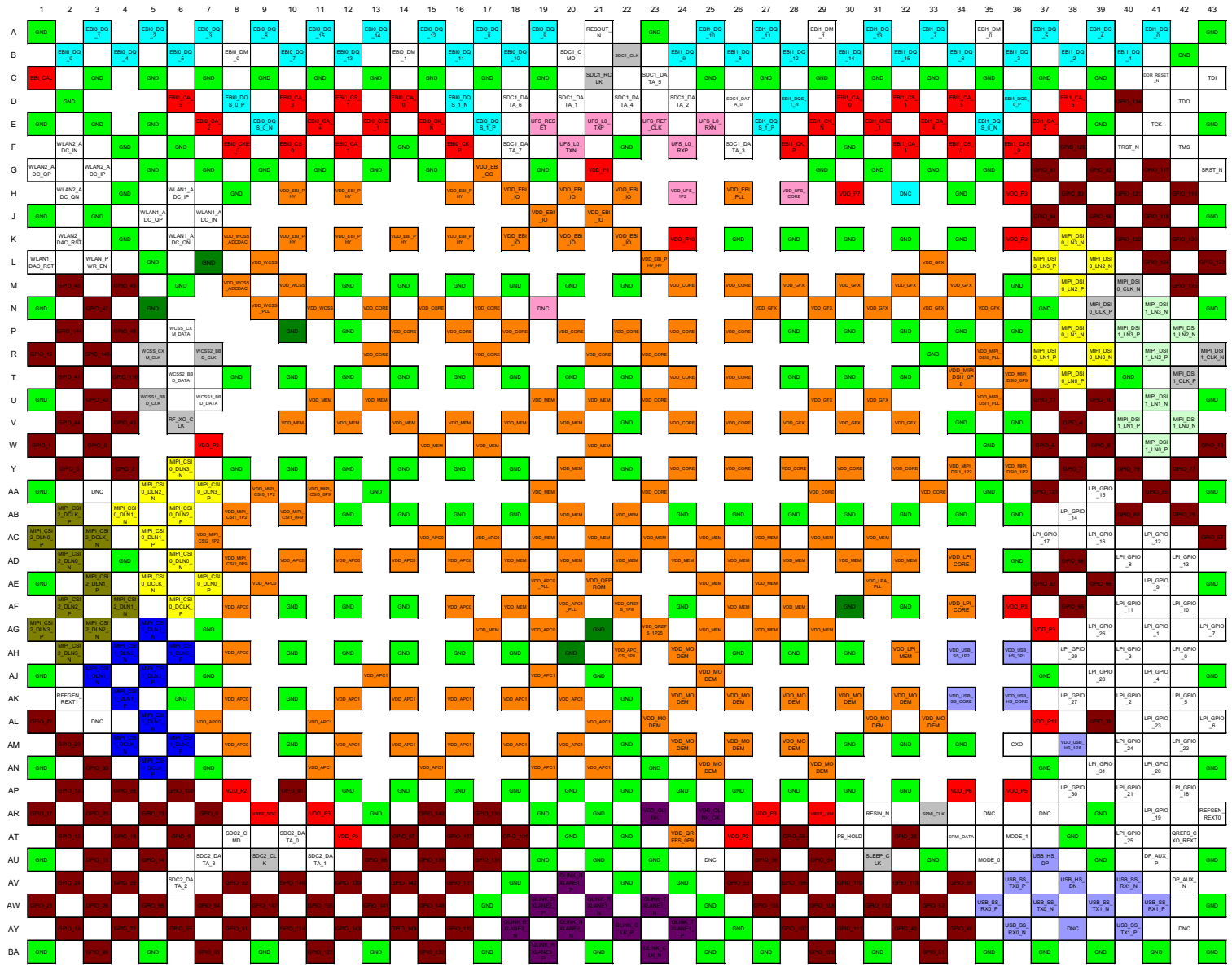


Figure 2-1 SDM710 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AM36	CXO		P11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
C1	EBI_CAL		–	AI	EBI0 LPDDR4X calibration resistor
D14	EBI0_CA_0		EBI	DO	EBI0 LPDDR4X command/address bit 0
F12	EBI0_CA_1		EBI	DO	EBI0 LPDDR4X command/address bit 1
E7	EBI0_CA_2		EBI	DO	EBI0 LPDDR4X command/address bit 2
D10	EBI0_CA_3		EBI	DO	EBI0 LPDDR4X command/address bit 3
E11	EBI0_CA_4		EBI	DO	EBI0 LPDDR4X command/address bit 4
D6	EBI0_CA_5		EBI	DO	EBI0 LPDDR4X command/address bit 5
E15	EBI0_CK_N		EBI	DO	EBI0 LPDDR4X differential clock - negative
F16	EBI0_CK_P		EBI	DO	EBI0 LPDDR4X differential clock - positive
F8	EBI0_CKE_0		EBI	DO	EBI0 LPDDR4X clock enable 0
E13	EBI0_CKE_1		EBI	DO	EBI0 LPDDR4X clock enable 1
F10	EBI0_CS_0		EBI	DO	EBI0 LPDDR4X chip select 0
D12	EBI0_CS_1		EBI	DO	EBI0 LPDDR4X chip select 1
B8	EBI0_DM_0		EBI	DO	EBI0 LPDDR4X data mask for byte 0
B14	EBI0_DM_1		EBI	DO	EBI0 LPDDR4X data mask for byte 1
B2	EBI0_DQ_0		EBI	B	EBI0 LPDDR4X data bit 0
A3	EBI0_DQ_1		EBI	B	EBI0 LPDDR4X data bit 1
A5	EBI0_DQ_2		EBI	B	EBI0 LPDDR4X data bit 2
A7	EBI0_DQ_3		EBI	B	EBI0 LPDDR4X data bit 3
B4	EBI0_DQ_4		EBI	B	EBI0 LPDDR4X data bit 4
B6	EBI0_DQ_5		EBI	B	EBI0 LPDDR4X data bit 5
A9	EBI0_DQ_6		EBI	B	EBI0 LPDDR4X data bit 6
B10	EBI0_DQ_7		EBI	B	EBI0 LPDDR4X data bit 7
A17	EBI0_DQ_8		EBI	B	EBI0 LPDDR4X data bit 8
A19	EBI0_DQ_9		EBI	B	EBI0 LPDDR4X data bit 9
B18	EBI0_DQ_10		EBI	B	EBI0 LPDDR4X data bit 10
B16	EBI0_DQ_11		EBI	B	EBI0 LPDDR4X data bit 11
A15	EBI0_DQ_12		EBI	B	EBI0 LPDDR4X data bit 12
B12	EBI0_DQ_13		EBI	B	EBI0 LPDDR4X data bit 13
A13	EBI0_DQ_14		EBI	B	EBI0 LPDDR4X data bit 14
A11	EBI0_DQ_15		EBI	B	EBI0 LPDDR4X data bit 15
E9	EBI0_DQS_0_N		EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 – negative
D16	EBI0_DQS_1_N		EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 – negative
D8	EBI0_DQS_0_P		EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 – positive
E17	EBI0_DQS_1_P		EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
D30	EBI1_CA_0		EBI	DO	EBI1 LPDDR4X command/address bit 0
F32	EBI1_CA_1		EBI	DO	EBI1 LPDDR4X command/address bit 1
E37	EBI1_CA_2		EBI	DO	EBI1 LPDDR4X command/address bit 2
D34	EBI1_CA_3		EBI	DO	EBI1 LPDDR4X command/address bit 3
E33	EBI1_CA_4		EBI	DO	EBI1 LPDDR4X command/address bit 4
D38	EBI1_CA_5		EBI	DO	EBI1 LPDDR4X command/address bit 5
E29	EBI1_CK_N		EBI	DO	EBI1 LPDDR4X differential clock – negative
F28	EBI1_CK_P		EBI	DO	EBI1 LPDDR4X differential clock – positive
F36	EBI1_CKE_0		EBI	DO	EBI1 LPDDR4X clock enable 0
E31	EBI1_CKE_1		EBI	DO	EBI1 LPDDR4X clock enable 1
F34	EBI1_CS_0		EBI	DO	EBI1 LPDDR4X chip select 0
D32	EBI1_CS_1		EBI	DO	EBI1 LPDDR4X chip select 1
A35	EBI1_DM_0		EBI	DO	EBI1 LPDDR4X data mask for byte 0
A29	EBI1_DM_1		EBI	DO	EBI1 LPDDR4X data mask for byte 1
A41	EBI1_DQ_0		EBI	B	EBI1 LPDDR4X data bit 0
B40	EBI1_DQ_1		EBI	B	EBI1 LPDDR4X data bit 1
A25	EBI1_DQ_10		EBI	B	EBI1 LPDDR4X data bit 10
A27	EBI1_DQ_11		EBI	B	EBI1 LPDDR4X data bit 11
B28	EBI1_DQ_12		EBI	B	EBI1 LPDDR4X data bit 12
A31	EBI1_DQ_13		EBI	B	EBI1 LPDDR4X data bit 13
B30	EBI1_DQ_14		EBI	B	EBI1 LPDDR4X data bit 14
B32	EBI1_DQ_15		EBI	B	EBI1 LPDDR4X data bit 15
B38	EBI1_DQ_2		EBI	B	EBI1 LPDDR4X data bit 2
B36	EBI1_DQ_3		EBI	B	EBI1 LPDDR4X data bit 3
A39	EBI1_DQ_4		EBI	B	EBI1 LPDDR4X data bit 4
A37	EBI1_DQ_5		EBI	B	EBI1 LPDDR4X data bit 5
B34	EBI1_DQ_6		EBI	B	EBI1 LPDDR4X data bit 6
A33	EBI1_DQ_7		EBI	B	EBI1 LPDDR4X data bit 7
B26	EBI1_DQ_8		EBI	B	EBI1 LPDDR4X data bit 8
B24	EBI1_DQ_9		EBI	B	EBI1 LPDDR4X data bit 9
E35	EBI1_DQS_0_N		EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 – negative
D28	EBI1_DQS_1_N		EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 – negative
D36	EBI1_DQS_0_P		EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 – positive
E27	EBI1_DQS_1_P		EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 – positive
C41	DDR_RESET_N		EBI	DO	LPDDR4X reset (shared by EBIs)
AV42	DP_AUX_N		–	AI, AO	DisplayPort auxiliary channel – negative
AU41	DP_AUX_P		–	AI, AO	DisplayPort auxiliary channel – positive
AF6	MIPI_CSI0_DCLK_P	DNC	CSI	AI	MIPI CSI 0, differential clock – positive
AE5	MIPI_CSI0_DCLK_N	MIPI_CSI0_TLN0_A	CSI	AI	MIPI CSI 0, differential clock – negative
AE7	MIPI_CSI0_DLN0_P	MIPI_CSI0_TLN0_B	CSI	AI	MIPI CSI 0, differential lane 0 – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AD6	MIPI_CSI0_DLN0_N	MIPI_CSI0_TLN0_C	CSI	AI	MIPI CSI 0, differential lane 0 – negative
AC5	MIPI_CSI0_DLN1_P	MIPI_CSI0_TLN1_A	CSI	AI	MIPI CSI 0, differential lane 1 – positive
AB4	MIPI_CSI0_DLN1_N	MIPI_CSI0_TLN1_B	CSI	AI	MIPI CSI 0, differential lane 1 – negative
AB6	MIPI_CSI0_DLN2_P	MIPI_CSI0_TLN1_C	CSI	AI	MIPI CSI 0, differential lane 2 – positive
AA5	MIPI_CSI0_DLN2_N	MIPI_CSI0_TLN2_A	CSI	AI	MIPI CSI 0, differential lane 2 – negative
AA7	MIPI_CSI0_DLN3_P	MIPI_CSI0_TLN2_B	CSI	AI	MIPI CSI 0, differential lane 3 – positive
Y6	MIPI_CSI0_DLN3_N	MIPI_CSI0_TLN2_C	CSI	AI	MIPI CSI 0, differential lane 3 – negative
AN5	MIPI_CSI1_DCLK_P	DNC	CSI	AI	MIPI CSI 1, differential clock – positive
AM4	MIPI_CSI1_DCLK_N	MIPI_CSI1_TLN0_A	CSI	AI	MIPI CSI 1, differential clock – negative
AM6	MIPI_CSI1_DLN0_P	MIPI_CSI1_TLN0_B	CSI	AI	MIPI CSI 1, differential lane 0 – positive
AL5	MIPI_CSI1_DLN0_N	MIPI_CSI1_TLN0_C	CSI	AI	MIPI CSI 1, differential lane 0 – negative
AK4	MIPI_CSI1_DLN1_P	MIPI_CSI1_TLN1_A	CSI	AI	MIPI CSI 1, differential lane 1– positive
AJ3	MIPI_CSI1_DLN1_N	MIPI_CSI1_TLN1_B	CSI	AI	MIPI CSI 1, differential lane 1 – negative
AJ5	MIPI_CSI1_DLN2_P	MIPI_CSI1_TLN1_C	CSI	AI	MIPI CSI 1, differential lane 2 – positive
AH4	MIPI_CSI1_DLN2_N	MIPI_CSI1_TLN2_A	CSI	AI	MIPI CSI 1, differential lane 2 – negative
AH6	MIPI_CSI1_DLN3_P	MIPI_CSI1_TLN2_B	CSI	AI	MIPI CSI 1, differential lane 3 – positive
AG5	MIPI_CSI1_DLN3_N	MIPI_CSI1_TLN2_C	CSI	AI	MIPI CSI 1, differential lane 3 – negative
AB2	MIPI_CSI2_DCLK_P	DNC	CSI	AI	MIPI CSI 2, differential clock – positive
AC3	MIPI_CSI2_DCLK_N	MIPI_CSI2_TLN0_A	CSI	AI	MIPI CSI 2, differential clock – negative
AC1	MIPI_CSI2_DLN0_P	MIPI_CSI2_TLN0_B	CSI	AI	MIPI CSI 2, differential lane 0 – positive
AD2	MIPI_CSI2_DLN0_N	MIPI_CSI2_TLN0_C	CSI	AI	MIPI CSI 2, differential lane 0 – negative
AE3	MIPI_CSI2_DLN1_P	MIPI_CSI2_TLN1_A	CSI	AI	MIPI CSI 2, differential lane 1 – positive
AF4	MIPI_CSI2_DLN1_N	MIPI_CSI2_TLN1_B	CSI	AI	MIPI CSI 2, differential lane 1 – negative
AF2	MIPI_CSI2_DLN2_P	MIPI_CSI2_TLN1_C	CSI	AI	MIPI CSI 2, differential lane 2 – positive
AG3	MIPI_CSI2_DLN2_N	MIPI_CSI2_TLN2_A	CSI	AI	MIPI CSI 2, differential lane 2 – negative
AG1	MIPI_CSI2_DLN3_P	MIPI_CSI2_TLN2_B	CSI	AI	MIPI CSI 2, differential lane 3 – positive
AH2	MIPI_CSI2_DLN3_N	MIPI_CSI2_TLN2_C	CSI	AI	MIPI CSI 2, differential lane 3 – negative
M40	MIPI_DSI0_CLK_N	MIPI_DSI0_TLN1_C	DSI	AO	MIPI display serial interface 0 clock – negative
N39	MIPI_DSI0_CLK_P	MIPI_DSI0_TLN1_B	DSI	AO	MIPI display serial interface 0 clock – positive
R39	MIPI_DSI0_LN0_N	MIPI_DSI0_TLN0_B	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
T38	MIPI_DSI0_LN0_P	MIPI_DSI0_TLN0_A	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
P38	MIPI_DSI0_LN1_N	MIPI_DSI0_TLN1_A	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
R37	MIPI_DSI0_LN1_P	MIPI_DSI0_TLN0_C	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
L39	MIPI_DSI0_LN2_N	MIPI_DSI0_TLN2_B	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
M38	MIPI_DSI0_LN2_P	MIPI_DSI0_TLN2_A	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
K38	MIPI_DSI0_LN3_N	DNC	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
L37	MIPI_DSI0_LN3_P	MIPI_DSI0_TLN2_C	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
R43	MIPI_DSI1_CLK_N	MIPI_DSI1_TLN1_C	DSI	AO	MIPI display serial interface 1 clock – negative
T42	MIPI_DSI1_CLK_P	MIPI_DSI1_TLN1_B	DSI	AO	MIPI display serial interface 1 clock – positive
V42	MIPI_DSI1_LN0_N	MIPI_DSI1_TLN0_B	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
W41	MIPI_DSI1_LN0_P	MIPI_DSI1_TLN0_A	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
U41	MIPI_DSI1_LN1_N	MIPI_DSI1_TLN1_A	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
V40	MIPI_DSI1_LN1_P	MIPI_DSI1_TLN0_C	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
P42	MIPI_DSI1_LN2_N	MIPI_DSI1_TLN2_B	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
R41	MIPI_DSI1_LN2_P	MIPI_DSI1_TLN2_A	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
N41	MIPI_DSI1_LN3_N	DNC	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
P40	MIPI_DSI1_LN3_P	MIPI_DSI1_TLN2_C	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
AU35	MODE_0		P3	DIS-PD:nppukp	Mode control bit 0 – unconnected for native mode
AT36	MODE_1		P3	DIS-PD:nppukp	Mode control bit 1 – unconnected for native mode
AR33	SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – clock
AT34	SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – data
AT30	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
BA23	QLINK_CLK_N		–	AO	QLink clock – negative
AY22	QLINK_CLK_P		–	AO	QLink clock – positive
AW21	QLINK_RXLANE1_N		–	AI	QLink downlink lane 1 – negative
AV20	QLINK_RXLANE1_P		–	AI	QLink downlink lane 1 – positive
AY20	QLINK_RXLANE2_N		–	AI	QLink downlink lane 2 – negative
AW19	QLINK_RXLANE2_P		–	AI	QLink downlink lane 2– positive
AY18	QLINK_RXLANE3_N		–	AI	QLink downlink lane 3 – negative
BA19	QLINK_RXLANE3_P		–	AI	QLink downlink lane 3 – positive
AW23	QLINK_TXLANE1_N		–	AO	QLink uplink lane 1 – negative
AY24	QLINK_TXLANE1_P		–	AO	QLink uplink lane 1 – positive
AT42	QREFS_CXO_REXT		–	AI, AO	External resistor for on-die clocking
AR43	REFGEN_REXT0		–	AI	East-side high-speed interface – external resistor
AK2	REFGEN_REXT1		–	AI	West-side high-speed interface – external resistor
AR31	RESIN_N		P3	DI	Reset input
A21	RESOUT_N		P3	DO	Reset output
V6	RF_XO_CLK		P3	DI	WLAN reference clock
B22	SDC1_CLK		P7	B-NP: pdpukp	Secure digital controller 1 clock
B20	SDC1_CMD		P7	B-PD: nppukp	Secure digital controller 1 command
D26	SDC1_DATA_0		P7	B-PD: nppukp	Secure digital controller 1 data bit 0
D20	SDC1_DATA_1		P7	B-PD: nppukp	Secure digital controller 1 data bit 1
D24	SDC1_DATA_2		P7	B-PD: nppukp	Secure digital controller 1 data bit 2
F26	SDC1_DATA_3		P7	B-PD: nppukp	Secure digital controller 1 data bit 3
D22	SDC1_DATA_4		P7	B-PD: nppukp	Secure digital controller 1 data bit 4
C23	SDC1_DATA_5		P7	B-PD: nppukp	Secure digital controller 1 data bit 5
D18	SDC1_DATA_6		P7	B-PD: nppukp	Secure digital controller 1 data bit 6
F18	SDC1_DATA_7		P7	B-PD: nppukp	Secure digital controller 1 data bit 7
C21	SDC1_RCLK		P7	DI-PD: pdpukp	Secure digital controller 1 return clock
AU9	SDC2_CLK		P2	BH-NP: dpukp	Secure digital controller 2 clock

Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AT8	SDC2_CMD		P2	BH-PD: nppukp	Secure digital controller 2 command
AT10	SDC2_DATA_0		P2	BH-NP: nppukp	Secure digital controller 2 data bit 0
AU11	SDC2_DATA_1		P2	BH-PD: nppukp	Secure digital controller 2 data bit 1
AV6	SDC2_DATA_2		P2	BH-NP: nppukp	Secure digital controller 2 data bit 2
AU7	SDC2_DATA_3		P2	BH-PD: nppukp	Secure digital controller 2 data bit 3
AU31	SLEEP_CLK		P3	DI	Sleep clock
G43	SRST_N		P3	DI-PU	JTAG reset for debug
E41	TCK		P3	DI-PU	JTAG clock input
C43	TDI		P3	DI-PU:nppdkp	JTAG data input
D42	TDO		P3	DO-Z	JTAG data output
F42	TMS		P3	DI-PU:nppdkp	JTAG mode select input
F40	TRST_N		P3	DI-PD:nppukp	JTAG reset
E25	UFS_L0_RXN		P10	AI	UFS receive lane 0 – negative
F24	UFS_L0_RXP		P10	AI	UFS receive lane 0 – positive
F20	UFS_L0_TXN		P10	AO	UFS transmit lane 0 – negative
E21	UFS_L0_TXP		P10	AO	UFS transmit lane 0 – positive
E23	UFS_REF_CLK		P10	DO-Z-PD: nppukp	UFS reference clock
E19	UFS_RESET		P10	DO-Z-PD: nppukp	UFS reset
AV38	USB_HS_DN		–	AI, AO	USB high-speed data – negative
AU37	USB_HS_DP		–	AI, AO	USB high-speed data – positive
AY36	USB_SS_RX0_N		–	AI	USB super-speed receive 0 – negative
AW35	USB_SS_RX0_P		–	AI	USB super-speed receive 0 – positive
AV40	USB_SS_RX1_N		–	AI	USB super-speed receive 1 – negative
AW41	USB_SS_RX1_P		–	AI	USB super-speed receive 1 – positive
AW37	USB_SS_TX0_N		–	AO	USB super-speed transmit 0 – negative
AV36	USB_SS_TX0_P		–	AO	USB super-speed transmit 0 – positive
AW39	USB_SS_TX1_N		–	AO	USB super-speed transmit 1 – negative
AY40	USB_SS_TX1_P		–	AO	USB super-speed transmit 1 – positive
R5	WCSS_CXM_CLK		P3	DO	WLAN coexistence module command clock (WSI 1.0)
P6	WCSS_CXM_DATA		P3	B	WLAN coexistence module command data (WSI 1.0)
U5	WCSS1_BBD_CLK		P3	DO	WLAN chain 1 baseband command clock (WSI 2.0)
U7	WCSS1_BBD_DATA		P3	B	WLAN chain 1 baseband command data (WSI 2.0)
R7	WCSS2_BBD_CLK		P3	DO	WLAN chain 2 baseband command clock (WSI 2.0)
T6	WCSS2_BBD_DATA		P3	B	WLAN chain 2 baseband command data (WSI 2.0)
L3	WLAN_PWR_EN		P3	DO	WLAN power enable
J7	WLAN1_ADC_IN		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase negative
H6	WLAN1_ADC_IP		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase positive
K6	WLAN1_ADC_QN		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
J5	WLAN1_ADC_QP		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature positive
L1	WLAN1_DAC_RST		–	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
F2	WLAN2_ADC_IN		–	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase negative
G3	WLAN2_ADC_IP		–	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase positive
H2	WLAN2_ADC_QN		–	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature negative
G1	WLAN2_ADC_QP		–	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature positive
K2	WLAN2_DAC_RST		–	AI, AO	WLAN chain 2 digital-to-analog converter external resistor

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SDM710 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PB873-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PB873-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AY14	GPIO_149	–	RFFE1_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 1 interface clock
AW15	GPIO_148	–	RFFE1_DATA BOOT_CONFIG(10)	P3	B-PD:nppukp B DI	Configurable I/O RF front-end 1 interface data Boot configuration control bit 10
AW9	GPIO_147	–	RFFE2_CLK GRFC33	P3	B-PD:nppukp DO DO	Configurable I/O RF front-end 2 interface clock Generic RF controller bit 33
AV10	GPIO_146	–	RFFE2_DATA GRFC34 BOOT_CONFIG(11)	P3	B-PD:nppukp B DO DI	Configurable I/O RF front-end 2 interface data Generic RF controller bit 34 Boot configuration control bit 11
R3	GPIO_145	Y	GPS_TX_AGGRESSOR LTE_COEX_RX	P3	B-PD:nppukp DI DI	Configurable I/O Tx level may degrade GNSS receiver (A) UART Rx for LTE coexistence
P2	GPIO_144	Y	LTE_COEX_TX	P3	B-PD:nppukp DO	Configurable I/O UART Tx for LTE coexistence
AY12	GPIO_143	–	GRFC5 GPS_TX_AGGRESSOR	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 5 Tx level may degrade GNSS receiver (D)
AV14	GPIO_142	–	RFFE5_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 5 interface clock
AW13	GPIO_141	–	RFFE5_DATA BOOT_CONFIG(12)	P3	B-PD:nppukp B DI	Configurable I/O RF front-end 5 interface data Boot configuration control bit 12
AR15	GPIO_140	–	RFFE4_CLK GRFC36	P3	B-PD:nppukp DO DO	Configurable I/O RF front-end 4 interface clock Generic RF controller bit 36
AU15	GPIO_139	–	RFFE4_DATA BOOT_CONFIG(9)	P3	B-PD:nppukp B DI	Configurable I/O RF front-end 4 interface data Boot configuration control bit 9
AU17	GPIO_138	–	RFFE3_CLK GRFC32	P3	B-PD:nppukp DO DO	Configurable I/O RF front-end 3 interface clock Generic RF controller bit 32
AT16	GPIO_137	–	RFFE3_DATA GRFC35 BOOT_CONFIG(8)	P3	B-PD:nppukp B DO DI	Configurable I/O RF front-end 3 interface data Generic RF controller bit 35 Boot configuration control bit 8
AR17	GPIO_136	–	GRFC1 BOOT_CONFIG(13)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 1 Boot configuration control bit 13

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AW11	GPIO_135	–	GRFC0 PA_INDICATOR	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 0 PA transmit indicator
D40	GPIO_134	–		P3	B-PD:nppukp	Configurable I/O
AA37	GPIO_133	Y	BOOT_CONFIG(3)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 3
BA15	GPIO_132	Y	GRFC2 BOOT_CONFIG(14)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 2 Boot configuration control bit 14
AV16	GPIO_131	Y	QLINK_ENABLE	P3	B-PD:nppukp DO	Configurable I/O QLink enable
AV12	GPIO_130	Y	QLINK_REQUEST	P3	B-PD:nppukp DI	Configurable I/O QLink request
BA11	GPIO_127	Y	GRFC3 BOOT_CONFIG(6)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 3 Boot configuration control bit 6
F38	GPIO_126	Y		P3	B-PD:nppukp	Configurable I/O
M42	GPIO_125	Y	QUP_L6_9_CS	P3	B-PD:nppukp DO	Configurable I/O QUP 9, lane 6: SPI_CS3
L41	GPIO_124	Y	QUP_L5_9_CS QDSS_TRACECLK_A	P3	B-PD:nppukp DO DO	Configurable I/O QUP 9, lane 5: SPI_CS2 QDSS trace clock A
L43	GPIO_123	Y	QUP_L4_9_CS QDSS_TRACECTL_A	P3	B-PD:nppukp DO DO	Configurable I/O QUP 9, lane 4: SPI_CS1 QDSS trace control A
K40	GPIO_122	Y	QDSS_TRACEDATA_5A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 5 A
H40	GPIO_121	Y	QDSS_TRACEDATA_4A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 4 A
K42	GPIO_120	Y	QDSS_TRACEDATA_3A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 3 A
J41	GPIO_119	Y	QDSS_TRACEDATA_2A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 2 A
H42	GPIO_118	Y	QDSS_TRACEDATA_1A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 1 A
G41	GPIO_117	Y	QDSS_TRACEDATA_0A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 0 A
T4	GPIO_116	Y	BOOT_CONFIG(15)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 15
AY16	GPIO_115	Y	GRFC9 GPS_TX_AGGRESSOR	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 9 Tx level may degrade GNSS receiver F
AY10	GPIO_114	Y	GRFC8 GPS_TX_AGGRESSOR	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 8 Tx level may degrade GNSS receiver E
AV32	GPIO_113	Y	UIM_BATT_ALARM EDP_HOT_PLUG_DETECT	P3	B-PD:nppukp DI DI	Configurable I/O UIM battery alarm Display port hot plug detection
AW31	GPIO_112	Y	UIM1_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM1 presence detection
AY30	GPIO_111	–	UIM1_RESET	P5	B-PD:nppukp DO	Configurable I/O UIM1 reset (dual voltage)
AV30	GPIO_110	–	UIM1_CLK	P5	B-PD:nppukp DO	Configurable I/O UIM1 clock (dual voltage)

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BA29	GPIO_109	–	UIM1_DATA	P5	B-PD:nppukp B	Configurable I/O UIM1 data (dual voltage)
AW29	GPIO_108	Y	UIM2_PRESENT QUP_L3(13)	P3	B-PD:nppukp DI DI DO	Configurable I/O UIM2 presence detection QUP 13, lane 3: UART_RX QUP 13, lane 3: SPI_CS0
AY28	GPIO_107	–	UIM2_RESET QUP_L2(13) QUP_L6_8_CS	P6	B-PD:nppukp DO DO DO DO	Configurable I/O UIM2 reset (dual voltage) QUP 13, lane 2: UART_TX QUP 13, lane 2: SPI_SCLK QUP 8, lane 6: SPI_CS3
AV28	GPIO_106	–	UIM2_CLK QUP_L1(13) QUP_L5_8_CS	P6	B-PD:nppukp DO DO B DO DO	Configurable I/O UIM2 clock (dual voltage) QUP 13, lane 1: UART_RFR QUP 13, lane 1: I2C_SCL QUP 13, lane 1: SPI_MOSI QUP 8, lane 5: SPI_CS2
AW27	GPIO_105	–	UIM2_DATA QUP_L0(13) QUP_L4_8_CS	P6	B-PD:nppukp B DI B DI DO	Configurable I/O UIM2 data (dual voltage) QUP 13, lane 0: UART_CTS QUP 13, lane 0: I2C_SDA QUP 13, lane 0: SPI_MISO QUP 8, lane 4: SPI_CS1
AT18	GPIO_101	Y	GRFC4 BOOT_CONFIG(0)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 4 Boot configuration control bit 0
AP6	GPIO_100	–	BOOT_CONFIG(2)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 2
J39	GPIO_99	–	BOOT_CONFIG(1)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 1
AU13	GPIO_98	–	RFFE6_DATA MDP_VSYNC_S BOOT_CONFIG(7)	P3	B-PD:nppukp B DI DI	Configurable I/O RF front-end 6 interface data MDP vertical sync – secondary B Boot configuration control bit 7
AT14	GPIO_97	Y	RFFE6_CLK GRFC37 MDP_VSYNC_P	P3	B-PD:nppukp DO DO DI	Configurable I/O RF front-end 6 interface clock Generic RF controller bit 37 MDP vertical sync – primary B
AW5	GPIO_96	Y	QUP_L3(7) SD_CARD_DET_N	P3	B-PD:nppukp DI DO DI	Configurable I/O QUP 7, lane 3: UART_RX QUP 7, lane 3: SPI_CS0 Secure digital card detection
AY6	GPIO_95	Y	QUP_L2(7) GP_PDM_0A	P3	B-PD:nppukp DO DO DO	Configurable I/O QUP 7, lane 2: UART_TX QUP 7, lane 2: SPI_SCLK General-purpose PDM output 0 A
AW7	GPIO_94	–	QUP_L1(7)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 7, lane 1: UART_RFR QUP 7, lane 1: I2C_SCL QUP 7, lane 1: SPI_MOSI
BA7	GPIO_93	–	QUP_L0(7) QDSS_TRACEDATA_13A	P3	B-PD:nppukp DI B DI DO	Configurable I/O QUP 7, lane 0: UART_CTS QUP 7, lane 0: I2C_SDA QUP 7, lane 0: SPI_MISO QDSS trace data bit 13 A
AV8	GPIO_92	Y	QUP_L3(4)	P3	B-PD:nppukp DI DO	Configurable I/O QUP 4, lane 3: UART_RX QUP 4, lane 3: SPI_CS0

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AY8	GPIO_91	Y	QUP_L2(4) QDSS_CTI_TRIG1_IN_B	P3	B-PD:nppukp DO DO DI	Configurable I/O QUP 4, lane 2: UART_TX QUP 4, lane 2: SPI_SCLK QDSS trigger input 1 B
AP10	GPIO_90	–	MDP_VSYNC0_OUT QUP_L1(4) MDP_VSYNC1_OUT MDP_VSYNC2_OUT MDP_VSYNC3_OUT QDSS_CTI_TRIG1_OUT_B	P3	B-PD:nppukp DI DO B DO DI DI DI DO	Configurable I/O MDP vertical sync QUP 4, lane 1: UART_RFR QUP 4, lane 1: I2C_SCL QUP 4, lane 1: SPI_MOSI MDP vertical sync MDP vertical sync MDP vertical sync QDSS trigger output 1 B
BA3	GPIO_89	Y	QUP_L0(4)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 4, lane 0: UART_CTS QUP 4, lane 0: I2C_SDA QUP 4, lane 0: SPI_MISO
J37	GPIO_84	Y	QUP_L3(15)	P3	B-PD:nppukp DI DO	Configurable I/O QUP 15, lane 3: UART_RX QUP 15, lane 3: SPI_CS0
H38	GPIO_83	–	QUP_L2(15)	P3	B-PD:nppukp DO DO	Configurable I/O QUP 15, lane 2: UART_TX QUP 15, lane 2: SPI_SCLK
G39	GPIO_82	–	QUP_L1(15)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 15, lane 1: UART_RFR QUP 15, lane 1: I2C_SCL QUP 15, lane 1: SPI_MOSI
G37	GPIO_81	–	QUP_L0(15)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 15, lane 0: UART_CTS QUP 15, lane 0: I2C_SDA QUP 15, lane 0: SPI_MISO
AB40	GPIO_80	Y	QDSS_TRACEDATA_12A	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 12 A
AB42	GPIO_79	Y	MI2S_2_MCLK GP_PDM_2A QDSS_TRACEDATA_11A	P3	B-PD:nppukp DO DO DO	Configurable I/O MI2S 2 master clock General-purpose PDM 2 A output QDSS trace data bit 11 A
W43	GPIO_78	Y	MI2S_3_DATA1 GCC_GP_CLK_1B	P3	B-PD:nppukp B DO	Configurable I/O MI2S 3 serial data channel 1 Global general-purpose clock 1 B
Y42	GPIO_77	Y	MI2S_3_DATA0 QUP_L6_1 QDSS_TRACEDATA_10A	P3	B-PD:nppukp B DO DO	Configurable I/O MI2S 3 serial data channel 0 QUP 1, lane 6: SPI_CS3 QDSS trace data bit 10 A
Y40	GPIO_76	–	MI2S_3_WS QUP_L5_1 QDSS_TRACEDATA_9A	P3	B-PD:nppukp B DO DO	Configurable I/O MI2S 3 word select QUP 1, lane 5: SPI_CS2 QDSS trace data bit 9 A
AA41	GPIO_75	–	MI2S_3_SCK QUP_L4_1 QDSS_TRACEDATA_8A	P3	B-PD:nppukp B DO DO	Configurable I/O MI2S 3 bit clock QUP 1, lane 4: SPI_CS1 QDSS trace data bit 8 A
AD38	GPIO_68	Y	MI2S_1_DATA1 QUP_L3(8)	P3	B-PD:nppukp B DI DO	Configurable I/O MI2S 1 data channel 1 QUP 8, lane 3: UART_RX QUP 8, lane 3: SPI_CS0
AE37	GPIO_67	–	MI2S_1_DATA0 QUP_L2(8)	P3	B-PD:nppukp B DO DO	Configurable I/O MI2S 1 data channel 0 QUP 8, lane 2: UART_TX QUP 8, lane 2: SPI_SCLK

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AE39	GPIO_66	Y	MI2S_1_WS QUP_L1(8) GP_PDM_1A SWR_DATA	P3	B-PD:nppukp B DO B DO DO B	Configurable I/O MI2S 1 word select QUP 8, lane 1: UART_RFR QUP 8, lane 1: I2C_SCL QUP 8, lane 1: SPI_MOSI General-purpose PDM output 1 A SoundWire data
AF38	GPIO_65	–	MI2S_1_SCK QUP_L0(8) SWR_CLK	P3	B-PD:nppukp B DI B DI DO	Configurable I/O MI2S 1 bit clock QUP 8, lane 0: UART_CTS QUP 8, lane 0: I2C_SDA QUP 8, lane 0: SPI_MISO SoundWire clock
AC43	GPIO_57	Y	MI2S_4_MCLK FORCED_USB_BOOT GCC_GP_CLK_1A	P3	B-PD:nppukp DO DI DO	Configurable I/O MI2S 4 master clock Forced USB boot Global general-purpose clock 1 A
AU27	GPIO_56	Y	QUP_L1(10)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 10, lane 1: UART_RFR QUP 10, lane 1: I2C_SCL QUP 10, lane 1: SPI_MOSI
AT28	GPIO_55	Y	QUP_L0(10)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 10, lane 0: UART_CTS QUP 10, lane 0: I2C_SDA QUP 10, lane 0: SPI_MISO
AU29	GPIO_54	Y	QUP_L3(10) GP_PDM_0B	P3	B-PD:nppukp DI DO DO	Configurable I/O QUP 10, lane 3: UART_RX QUP 10, lane 3: SPI_CS0 General-purpose PDM 0 B output
AV26	GPIO_53	Y	QUP_L2(10)	P3	B-PD:nppukp DO DO	Configurable I/O QUP 10, lane 2: UART_TX QUP 10, lane 2: SPI_SCLK
AW33	GPIO_52	Y	QUP_L3(12) QDSS_CTI_TRIG0_IN_A	P3	B-PD:nppukp DI DO DI	Configurable I/O QUP 12, lane 3: UART_RX QUP 12, lane 3: SPI_CS0 QDSS trigger input 0 A
BA33	GPIO_51	–	QUP_L2(12) QDSS_CTI_TRIG0_OUT_A	P3	B-PD:nppukp DO DO DO	Configurable I/O QUP 12, lane 2: UART_TX QUP 12, lane 2: SPI_SCLK QDSS trigger output 0 A
AV34	GPIO_50	–	QUP_L1(12)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 12, lane 1: UART_RFR QUP 12, lane 1: I2C_SCL QUP 12, lane 1: SPI_MOSI
AY34	GPIO_49	Y	QUP_L0(12)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 12, lane 0: UART_CTS QUP 12, lane 0: I2C_SDA QUP 12, lane 0: SPI_MISO
P4	GPIO_48	Y	QUP_L3(6)	P3	B-PD:nppukp DI DO	Configurable I/O QUP 6, lane 3: UART_RX QUP 6, lane 3: SPI_CS0
N3	GPIO_47	–	QUP_L2(6)	P3	B-PD:nppukp DO DO	Configurable I/O QUP 6, lane 2: UART_TX QUP 6, lane 2: SPI_SCLK
M2	GPIO_46	Y	QUP_L1(6)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 6, lane 1: UART_RFR QUP 6, lane 1: I2C_SCL QUP 6, lane 1: SPI_MOSI
M4	GPIO_45	–	QUP_L0(6)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 6, lane 0: UART_CTS QUP 6, lane 0: I2C_SDA QUP 6, lane 0: SPI_MISO

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
V2	GPIO_44	Y	QUP_L3(3) QDSS_TRACEDATA_15A	P3	B-PD:nppukp DI DO DO	Configurable I/O QUP 3, lane 3: UART_RX QUP 3, lane 3: SPI_CS0 QDSS trace data bit 15 A
V4	GPIO_43	Y	QUP_L2(3) QDSS_TRACEDATA_14A	P3	B-PD:nppukp DO DO DO	Configurable I/O QUP 3, lane 2: UART_TX QUP 3, lane 2: SPI_SCLK QDSS trace data bit 14 A
U3	GPIO_42	–	QUP_L1(3) QDSS_TRACEDATA_7A	P3	B-PD:nppukp DO B DO DO	Configurable I/O QUP 3, lane 1: UART_RFR QUP 3, lane 1: I2C_SCL QUP 3, lane 1: SPI_MOSI QDSS trace data bit 7 A
T2	GPIO_41	Y	QUP_L0(3) QDSS_TRACEDATA_6A	P3	B-PD:nppukp DI B DI DO	Configurable I/O QUP 3, lane 0: UART_CTS QUP 3, lane 0: I2C_SDA QUP 3, lane 0: SPI_MISO QDSS trace data bit 6 A
AY32	GPIO_40	Y		P3	B-PD:nppukp	Configurable I/O
AL39	GPIO_39	Y	BOOT_CONFIG(4)	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 4
AT32	GPIO_38	Y	USB_PHY_PS	P3	B-PD:nppukp DI	Configurable I/O USB PHY port select
AN3	GPIO_30	Y	QUP_L3(2) QDSS_TRACECTL_B	P3	B-PD:nppukp DI DO DO	Configurable I/O QUP 2, lane 3: UART_RX QUP 2, lane 3: SPI_CS0 QDSS trace control B
AM2	GPIO_29	–	QUP_L2(2) QDSS_TRACEDATA_15B	P3	B-PD:nppukp DO DO DO	Configurable I/O QUP 2, lane 2: UART_TX QUP 2, lane 2: SPI_SCLK QDSS trace data bit 15 B
AP4	GPIO_28	–	QUP_L1(2) QDSS_TRACEDATA_14B	P3	B-PD:nppukp DO B DO DO	Configurable I/O QUP 2, lane 1: UART_RFR QUP 2, lane 1: I2C_SCL QUP 2, lane 1: SPI_MOSI QDSS trace data bit 14 B
AL1	GPIO_27	–	QUP_L0(2) QDSS_TRACEDATA_13B	P3	B-PD:nppukp DI B DI DO	Configurable I/O QUP 2, lane 0: UART_CTS QUP 2, lane 0: I2C_SDA QUP 2, lane 0: SPI_MISO QDSS trace data bit 13 B
AW3	GPIO_26	Y	CCI_ASYNC0 QDSS_TRACEDATA_12B	P3	B-PD:nppukp DI DO	Configurable I/O Camera control interface async 0 QDSS trace data bit 12 B
AV4	GPIO_25	–	CCI_TIMER4 CCI_ASYNC2 QDSS_TRACEDATA_11B	P3	B-PD:nppukp DO DI DO	Configurable I/O Camera control interface timer 4 Camera control interface async 2 QDSS trace data bit 11 B
AV2	GPIO_24	Y	CCI_TIMER3 CCI_ASYNC1 QDSS_TRACEDATA_10B	P3	B-PD:nppukp DO DI DO	Configurable I/O Camera control interface timer 3 Camera control interface async 1 QDSS trace data bit 10 B
AR5	GPIO_23	–	CCI_TIMER2 QDSS_TRACEDATA_9B	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 2 QDSS trace data bit 9 B
AY4	GPIO_22	Y	CCI_TIMER1 GCC_GP_CLK_3B QDSS_TRACECLK_B	P3	B-PD:nppukp DO DO DO	Configurable I/O Camera control interface timer 1 Global general-purpose clock 3 B QDSS trace clock B

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AW1	GPIO_21	–	CCI_TIMER0 GCC_GP_CLK_2B QDSS_TRACEDATA_8B	P3	B-PD:nppukp DO DO DO	Configurable I/O Camera control interface timer 0 Global general-purpose clock 2 B QDSS trace data bit 8 B
AR3	GPIO_20	Y	CCI_I2C1_SCL QUP_L3(1) QDSS_TRACEDATA_7B	P3	B-PD:nppukp B DI DO DO	Configurable I/O Dedicated camera control interface I2C 1 clock QUP 1, lane 3: UART_RX QUP 1, lane 3: SPI_CS0 QDSS trace data bit 7 B
AP2	GPIO_19	–	CCI_I2C1_SDA QUP_L2(1) QDSS_TRACEDATA_6B	P3	B-PD:nppukp B DO DO DO	Configurable I/O Dedicated camera control interface I2C 1 serial data QUP 1, lane 2: UART_TX QUP 1, lane 2: SPI_SCLK QDSS trace data bit 6 B
AT4	GPIO_18	–	CCI_I2C0_SCL QUP_L1(1) QDSS_TRACEDATA_5B	P3	B-PD:nppukp B DO B DO DO	Configurable I/O Dedicated camera control interface I2C 0 clock QUP 1, lane 1: UART_RFR QUP 1, lane 1: I2C_SCL QUP 1, lane 1: SPI_MOSI QDSS trace data bit 5 B
AR1	GPIO_17	–	CCI_I2C0_SDA QUP_L0(1) QDSS_TRACEDATA_4B	P3	B-PD:nppukp B DI B DI DO	Configurable I/O Dedicated camera control interface I2C 0 serial data QUP 1, lane 0: UART_CTS QUP 1, lane 0: I2C_SDA QUP 1, lane 0: SPI_MISO QDSS trace data bit 4 B
AY2	GPIO_16	–	CAM_MCLK3 QDSS_TRACEDATA_3B	P3	B-PD:nppukp DO DI	Configurable I/O Camera master clock 3 QDSS trace data bit 3 B
AT2	GPIO_15	–	CAM_MCLK2 QDSS_TRACEDATA_2B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 2 QDSS trace data bit 2 B
AU5	GPIO_14	–	CAM_MCLK1 QDSS_TRACEDATA_1B	P3	B-PD:nppukp DO DI	Configurable I/O Camera master clock 1 QDSS trace data bit 1 B
AU3	GPIO_13	–	CAM_MCLK0 QDSS_TRACEDATA_0B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 0 QDSS trace data bit 0 B
R1	GPIO_12	–	MDP_VSYNC_E	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – external
U37	GPIO_11	Y	MDP_VSYNC_S	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – secondary A
U39	GPIO_10	Y	MDP_VSYNC_P QUP_L6_0_CS	P3	B-PD:nppukp DI DO	Configurable I/O MDP vertical sync – primary A QUP 0, lane 6: SPI_CS3
AT6	GPIO_9	–	QUP_L5_0_CS	P3	B-PD:nppukp DO	Configurable I/O QUP 0, lane 5: SPI_CS2
AR7	GPIO_8	–	QUP_L4_0_CS GP_PDM_1B	P3	B-PD:nppukp DO DO	Configurable I/O QUP 0, lane 4: SPI_CS1 General-purpose PDM output 1 B
Y38	GPIO_7	–	QUP_L1(9)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 9, lane 1: UART_RFR QUP 9, lane 1: I2C_SCL QUP 9, lane 1: SPI_MOSI

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
W39	GPIO_6	–	QUP_L0(9)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 9, lane 0: UART_CTS QUP 9, lane 0: I2C_SDA QUP 9, lane 0: SPI_MISO
W37	GPIO_5	Y	QUP_L3(9) QDSS_CTI_TRIG0_IN_B	P3	B-PD:nppukp DI DO DI	Configurable I/O QUP 9, lane 3: UART_RX QUP 9, lane 3: SPI_CS0 QDSS trigger input 0 B
V38	GPIO_4	–	QUP_L2(9) QDSS_CTI_TRIG0_OUT_A	P3	B-PD:nppukp DO DO DO	Configurable I/O QUP 9, lane 2: UART_TX QUP 9, lane 2: SPI_SCLK QDSS trigger output 0 A
Y2	GPIO_3	Y	QUP_L3(0)	P3	B-PD:nppukp DI DO	Configurable I/O QUP 0, lane 3: UART_RX QUP 0, lane 3: SPI_CS0
Y4	GPIO_2	–	QUP_L2(0)	P3	B-PD:nppukp DO DO	Configurable I/O QUP 0, lane 2: UART_TX QUP 0, lane 2: SPI_SCLK
W1	GPIO_1	Y	QUP_L1(0)	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 0, lane 1: UART_RFR QUP 0, lane 1: I2C_SCL QUP 0, lane 1: SPI_MOSI
W3	GPIO_0	–	QUP_L0(0)	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 0, lane 0: UART_CTS QUP 0, lane 0: I2C_SDA QUP 0, lane 0: SPI_MISO
LPI pins						
AN39	LPI_GPIO_31	Y	LPI_QCA_SB_CLK	P3	B-PD:nppukp DO	Bluetooth/FM SLIMbus clock
AP38	LPI_GPIO_30	Y	LPI_QCA_SB_DATA	P3	B-PD:nppukp B	Bluetooth/FM SLIMbus data
AH38	LPI_GPIO_29	Y	LPI_MI2S_1_MCLK_B LPI_DMIC2_DATA	P3	B-PD:nppukp DO DI	LPI MI2S master clock B LPI DMIC 2 data
AJ39	LPI_GPIO_28	Y	LPI_MI2S_4_DATA3 LPI_DMIC2_CLK GP_PDM_2B QDSS_CTI_TRIG1_IN_A	P3	B-PD:nppukp B DO DO DI	LPI quaternary MI2S data channel 3 LPI DMIC 2 clock General-purpose PDM 2 B output QDSS trigger input 1 A
AK38	LPI_GPIO_27	Y	LPI_MI2S_4_DATA2 LPI_DMIC1_DATA QDSS_CTI_TRIG1_OUT_A BOOT_CONFIG(5)	P3	B-PD:nppukp B DI DO DI	LPI quaternary MI2S data channel 2 LPI DMIC 1 data QDSS trigger output 1 A Boot configuration control bit 5
AG39	LPI_GPIO_26	Y	LPI_MI2S_4_DATA1 LPI_DMIC1_CLK	P3	B-PD:nppukp B DO	LPI quaternary MI2S data channel 0 LPI DMIC 1 clock
AT40	LPI_GPIO_25	Y	LPI_MI2S_4_DATA0 LPI_CDC_PDM_RX2	P3	B-PD:nppukp B DO	LPI quaternary MI2S data channel 0 Audio codec PDM receive 2
AM40	LPI_GPIO_24	Y	LPI_MI2S_4_WS LPI_CDC_PDM_RX1_DRE GCC_GP_CLK_3A	P3	B-PD:nppukp B DO DO	LPI quaternary MI2S word select Audio codec PDM receive 1 (DRE) Global general-purpose clock 3 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AL41	LPI_GPIO_23	Y		P3	B-PD:nppukp	
			LPI_MI2S_4_SCK		B	LPI quaternary MI2S bit clock
			LPI_CDC_PDM_RX1		DO	Audio codec PDM receive 1
			GCC_GP_CLK_2A		DO	Global general-purpose clock 2 A
AM42	LPI_GPIO_22	–		P3	B-PD:nppukp	
			LPI_CDC_PDM_RX0_DRE		DO	Audio codec PDM receive 0 (DRE)
			LPI_MI2S_1_MCLK_A		DO	LPI MI2S 1 master clock A
AP40	LPI_GPIO_21	–		P3	B-PD:nppukp	
			LPI_AUD_SLIMBUS_DATA1		B	LPI audio SLIMbus data channel 1
			LPI_CDC_PDM_RX0		DO	Audio codec PDM receive data channel 0
AN41	LPI_GPIO_20	Y		P3	B-PD:nppukp	
			LPI_AUD_SLIMBUS_DATA0		B	LPI audio SLIMbus data channel 0
			LPI_CDC_PDM_TX0		DI	Audio codec PDM transmit data channel
AR41	LPI_GPIO_19	–		P3	B-PD:nppukp	
			LPI_CDC_PDM_SYNC		DO	Audio codec PDM synchronization signal
			LPI_AUDIO_REF_CLK		DO	Audio reference clock
AP42	LPI_GPIO_18	Y		P3	B-PD:nppukp	
			LPI_AUD_SLIMBUS_CLK		DO	LPI audio SLIMbus clock
			LPI_CDC_PDM_CLK		DO	Audio codec PDM clock signal and codec master clock
AC37	LPI_GPIO_17	–		P3	B-PD:nppukp	
			LPI_QUP_L1(3)		DO	LPI QUP 3, lane 1: UART_RFR
					B	LPI QUP 3, lane 1: I2C_SCL
					DO	LPI QUP 3, lane 1: SPI_MOSI
			LPI_QUP_L1(4)		DO	LPI QUP 4, lane 1: UART_RFR
					B	LPI QUP 4, lane 1: I2C_SCL
					DO	LPI QUP 4, lane 1: SPI_MOSI
			LPI_QUP_L3(5)		DI	LPI QUP 5, lane 3: UART_RX
					DO	LPI QUP 5, lane 3: SPI_CS0
AC39	LPI_GPIO_16	–		P3	B-PD:nppukp	
			LPI_QUP_L0(3)		DI	LPI QUP 3, lane 0: UART_CTS
					B	LPI QUP 3, lane 0: I2C_SDA
					DI	LPI QUP 3, lane 0: SPI_MISO
			LPI_QUP_L0(4)		DI	LPI QUP 4, lane 0: UART_CTS
					B	LPI QUP 4, lane 0: I2C_SDA
					DI	LPI QUP 4, lane 0: SPI_MISO
			LPI_QUP_L2(5)		DO	LPI QUP 5, lane 2: UART_TX
					DO	LPI QUP 5, lane 2: SPI_SCLK
AA39	LPI_GPIO_15	–		P3	B-PD:nppukp	
			LPI_QUP_L3(4)		DI	LPI QUP 4, lane 3: UART_RX
			LPI_QUP_L1(5)		DO	LPI QUP 4, lane 3: SPI_CS0
					DO	LPI QUP 5, lane 1: UART_RFR
					B	LPI QUP 5, lane 1: I2C_SCL
					DO	LPI QUP 5, lane 1: SPI_MOSI
AB38	LPI_GPIO_14	–		P3	B-PD:nppukp	
			LPI_QUP_L2(4)		DO	LPI QUP 4, lane 2: UART_TX
			LPI_QUP_L0(5)		DO	LPI QUP 4, lane 2: SPI_SCLK
					DI	LPI QUP 5, lane 0: UART_CTS
					B	LPI QUP 5, lane 0: I2C_SDA
					DI	LPI QUP 5, lane 0: SPI_MISO

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AD42	LPI_GPIO_13	–		P3	B-PD:nppukp	
			LPI_QUP_L3(3)		DI	LPI QUP 3, lane 3: UART_RX
			LPI_QUP_L4(5)		DO	LPI QUP 3, lane 3: SPI_CS0
					DO	LPI QUP 5, lane 4: SPI_CS1
AC41	LPI_GPIO_12	–		P3	B-PD:nppukp	
			LPI_QUP_L2(3)		DO	LPI QUP 3, lane 2: UART_TX
					DO	LPI QUP 3, lane 2: SPI_SCLK
AF40	LPI_GPIO_11	–		P3	B-PD:nppukp	
			LPI_MI2S_2_DATA1		B	LPI MI2S 2 serial data channel 1
			LPI_QUP_L3(2)		DI	LPI QUP 2, lane 3: UART_RX
					DO	LPI QUP 2, lane 3: SPI_CS0
AF42	LPI_GPIO_10	–		P3	B-PD:nppukp	
			LPI_MI2S_2_DATA0		B	LPI MI2S 2 serial data channel 0
			LPI_QUP_L2(2)		DO	LPI QUP 2, lane 2: UART_TX
					DO	LPI QUP 2, lane 2: SPI_SCLK
			LPI_QUP_L6(4)		DO	LPI QUP 4, lane 6: SPI_CS3
			LPI_QUP_L6(5)		DO	LPI QUP 5, lane 6: SPI_CS3
AE41	LPI_GPIO_9	–		P3	B-PD:nppukp	
			LPI_MI2S_2_WS		B	LPI MI2S 2 word select
			LPI_QUP_L6(1)		DO	LPI QUP 1, lane 6: SPI_CS3
			LPI_QUP_L1(2)		DO	LPI QUP 2, lane 1: UART_RFR
					B	LPI QUP 2, lane 1: I2C_SCL
					DO	LPI QUP 2, lane 1: SPI_MOSI
AD40	LPI_GPIO_8	–		P3	B-PD:nppukp	
			LPI_MI2S_2_SCK		B	LPI MI2S 2 bit clock
			LPI_QUP_L4(0)		DO	LPI QUP 0, lane 4: SPI_CS1
			LPI_QUP_L0(2)		DI	LPI QUP 2, lane 0: UART_CTS
					B	LPI QUP 2, lane 0: I2C_SDA
					DI	LPI QUP 2, lane 0: SPI_MISO
AG43	LPI_GPIO_7	–		P3	B-PD:nppukp	
			LPI_QUP_L5(1)		DO	LPI QUP 1, lane 5: SPI_CS2
			LPI_QUP_L5(2)		DO	LPI QUP 2, lane 5: SPI_CS2
			LPI_QUP_L5(3)		DO	LPI QUP 3, lane 5: SPI_CS2
AL43	LPI_GPIO_6	–		P3	B-PD:nppukp	
			LPI_QUP_L2(0)		DO	LPI QUP 0, lane 2: UART_TX
			LPI_QUP_L4(1)		DO	LPI QUP 0, lane 2: SPI_SCLK
					DO	LPI QUP 1, lane 4: SPI_CS1
			LPI_QUP_L4(2)		DO	LPI QUP 2, lane 4: SPI_CS1
AK42	LPI_GPIO_5	–		P3	B-PD:nppukp	
			LPI_QUP_L3(0)		DI	LPI QUP 0, lane 3: UART_RX
					DO	LPI QUP 0, lane 3: SPI_CS0
			LPI_QUP_L3(1)		DI	LPI QUP 1, lane 3: UART_RX
					DO	LPI QUP 1, lane 3: SPI_CS0
			LPI_QUP_L6(2)		DO	LPI QUP 2, lane 6: SPI_CS3
AJ41	LPI_GPIO_4	–		P3	B-PD:nppukp	
			LPI_QUP_L2(1)		DO	LPI QUP 1 lane 2: UART_TX
					DO	LPI QUP 1 lane 2: SPI_SCLK
			LPI_QUP_L6(3)		DO	LPI QUP 3, lane 6: SPI_CS3
			LPI_QUP_L4(3)		DO	LPI QUP 3, lane 4: SPI_CS1
AH40	LPI_GPIO_3	–		P3	B-PD:nppukp	
			LPI_QUP_L1(1)		DO	LPI QUP 1, lane 1: UART_RFR
					B	LPI QUP 1, lane 1: I2C_SCL
					DO	LPI QUP 1, lane 1: SPI_MOSI

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AK40	LPI_GPIO_2	–	LPI_QUP_L0(1)	P3	B-PD:nppukp DI B DI	LPI QUP 1, lane 0: UART_CTS LPI QUP 1, lane 0: I2C_SDA LPI QUP 1, lane 0: SPI_MISO
AG41	LPI_GPIO_1	–	LPI_QUP_L1(0)	P3	B-PD:nppukp DO B DO	LPI QUP 0, lane 1: UART_RFR LPI QUP 0, lane 1: I2C_SCL LPI QUP 0, lane 1: SPI_MOSI
AH42	LPI_GPIO_0	–	SYNC_OUT LPI_QUP_L0(0)	P3	B-PD:nppukp DI B DI	32 kHz clock output for synchronization LPI QUP 0, lane 0: UART_CTS LPI QUP 0, lane 0: I2C_SDA LPI QUP 0, lane 0: SPI_MISO

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad #	Pad name	Functional description
AC15, AC17, AD10, AD12, AD14, AD16, AE9, AF8, AF16, AG19, AH8, AK8, AL7, AM8	VDD_APC0	Power for the Kryo Silver application processor
AJ13, AJ19, AK12, AK14, AK16, AK18, AK20, AL11, AL21, AM12, AM14, AM16, AM18, AM20, AN11, AN15, AN19, AN21	VDD_APC1	Power for the Kryo Gold application processor
AA23, AA29, AA33, M24, M26, N13, N15, N17, P14, P16, P18, P20, P22, P24, P26, R13, R17, R21, R23, T24, T26, U23, V24, V26, Y24, Y26, Y28, Y30, Y32	VDD_CORE	Power for the digital core circuits
AA19, AB20, AB22, AC19, AC21, AC23, AC25, AC27, AC29, AC31, AD18, AD20, AD22, AD24, AD26, AD28, AD30, AD32, AE25, AE27, AF18, AF26, AF28, AG17, AG25, AG27, AG29, U11, U13, U19, U21, V10, V12, V14, V16, V18, V20, W15, W17, W21, Y20	VDD_MEM	Power for an on-chip memory
L33, M28, M30, M32, M34, N27, N29, N31, N33, N35, U29, U31, V28, V30, V32	VDD_GFX	Power for the graphics
AH24, AJ25, AK24, AK26, AK28, AK30, AK32, AL23, AL31, AL33, AM24, AM26, AM28, AN25, AN29	VDD_MODEM	Power for the modem circuits
AH22	VDD_APC_CS_1P8	Power for the APC current sense circuits
AE19	VDD_APC0_PLL	Power for the application processor PLL circuits
AF20	VDD_APC1_PLL	Power for the application processor PLL circuits
AD34, AF34	VDD_LPI_CORE	Power for the LPI core
AH32	VDD_LPI_MEM	Power for the LPI core memory
AE21	VDD_QFPROM	Power for programming the QFPROM
AK36	VDD_USB_HS_CORE	Power for the USB HS core circuits
AM38	VDD_USB_HS_1P8	Power for the USB HS 1.8 V circuits
AH36	VDD_USB_HS_3P1	Power for the USB HS 3.1 V circuits
AH34	VDD_USB_SS_1P2	Power for the USB SS 1.2 V circuits
AK34	VDD_USB_SS_CORE	Power for the USB SS core circuits
G17	VDD_EBI_CC	Power for the EBI clock circuits
H18, H22	VDD_EBI_IO_CC	Power for the EBI I/O clock circuits
H10, H12, H16, K10, K12, K14, K16	VDD_EBI_PHY	Power for the EBI PHY circuits
L23	VDD_EBI_PHY_HV	Power for the EBI PHY high-voltage circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
H20, J19, J21, K18, K20, K22	VDD_EBI_IO	Power for the EBI I/O circuits
H26	VDD_EBI_PLL	Power for the EBI PLL circuits
AE31	VDD_LPA_PLL	Power for the audio circuits
AA11	VDD_MIPI_CSI0_0P9	Power for the MIPI CSI0 0.9 V circuits
AA9	VDD_MIPI_CSI0_1P2	Power for the MIPI CSI0 1.2 V circuits
AB10	VDD_MIPI_CSI1_0P9	Power for the MIPI CSI1 0.9 V circuits
AB8	VDD_MIPI_CSI1_1P2	Power for the MIPI CSI1 1.2 V circuits
AD8	VDD_MIPI_CSI2_0P9	Power for the MIPI CSI2 0.9 V circuits
AC7	VDD_MIPI_CSI2_1P2	Power for the MIPI CSI2 1.2 V circuits
R35	VDD_MIPI_DSI0_PLL	Power for the MIPI DSI0 PLL circuits
U35	VDD_MIPI_DSI1_PLL	Power for the MIPI DSI1 PLL circuits
T36	VDD_MIPI_DSI0_0P9	Power for the MIPI DSI0 0.9 V circuits
Y36	VDD_MIPI_DSI0_1P2	Power for the MIPI DSI0 1.2 V circuits
T34	VDD_MIPI_DSI1_0P9	Power for the MIPI DSI1 0.9 V circuits
Y34	VDD_MIPI_DSI1_1P2	Power for the MIPI DSI1 1.2 V circuits
AR25	VDD_QLINK_CK	Power for the QLink clock circuits
AR23	VDD_QLINK	Power for the QLink circuits
AT24	VDD_QREFS_0P9	Reference voltage for the QREFS 0.9 V circuits
AG23	VDD_QREFS_1P25	Reference voltage for the QREFS 1.25 V circuits
AF22	VDD_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits
H24	VDD_UFS_1P2	Power for the UFS 1.2 V circuits
H28	VDD_UFS_CORE	Power for the UFS core circuits
K8, M8	VDD_WCSS_ADCDAC	Power for the WCSS ADC and DAC
N9	VDD_WCSS_PLL	Power for the WCSS PLL circuits
L9, M10, N11	VDD_WCSS	Power for the WCSS circuits
G21	VDD_P1	Power for the pad group 1 – EBI pads
AP8	VDD_P2	Power for the pad group 2 – SDC2 pads
AF36, AG37, AR11, AR27, AT12, AT26, H36, K36, W7	VDD_P3	Power for the pad group 3 – most I/O pads
AP36	VDD_P5	Power for the pad group 5 – UIM1 pads
AP34	VDD_P6	Power for the pad group 6 – UIM2 pads
H30	VDD_P7	Power for the pad group 7 – eMMC pads
K24	VDD_P10	Power for the pad group 10 – UFS pad
AL37	VDD_P11	Power for the pad group 11 – CXO pad
AR9	VREF_SDC	Reference voltage for an SDC
AR29	VREF_UIM	Reference voltage for an UIM

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AA3, AL3, AR37, AR35, AU25, AY38, AY42, H32, N19	DNC	Do not connect; connected internally, do not connect externally
A1, A23, A43, AA1, AA13, AA35, AA43, AB12, AB14, AB16, AB18, AB24, AB26, AB28, AB30, AB32, AB34, AB36, AD4, AD36, AE1, AE43, AF10, AF12, AF14, AF24, AF30, AF32, AG7, AG21, AH10, AH12, AH14, AH16, AH18, AH20, AH26, AH28, AH30, AJ1, AJ7, AJ21, AJ37, AJ43, AK6, AK10, AK22, AM10, AM22, AM30, AM32, AM34, AN1, AN7, AN23, AN37, AN43, AP12, AP14, AP16, AP18, AP20, AP22, AP24, AP26, AP28, AP30, AP32, AR13, AR19, AR21, AR39, AT20, AT22, AT38, AU1, AU19, AU21, AU23, AU33, AU39, AU43, AV18, AV22, AV24, AW17, AW25, AW43, AY26, B42, BA1, BA5, BA9, BA13, BA17, BA21, BA25, BA27, BA31, BA35, BA37, BA39, BA41, BA43, C3, C5, C7, C9, C11, C13, C15, C17, C19, C25, C27, C29, C31, C33, C35, C37, C39, D2, E1, E3, E5, E39, E43, F4, F6, F14, F22, F30, G5, G7, G9, G11, G13, G15, G19, G29, G31, G33, G35, H4, H8, H34, J1, J3, J43, K4, K26, K28, K30, K32, K34, L5, L7, M6, M12, M14, M16, M18, M20, M22, M36, N1, N5, N37, N43, P10, P12, P28, P30, P32, P34, P36, R33, T8, T10, T12, T14, T16, T18, T20, T22, T28, T30, T32, T40, U1, U43, V22, V34, V36, W35, Y8, Y10, Y12, Y14, Y16, Y18, Y22	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	-0.3	1.19	V
VDD_APC1	Kryo Gold application processor	-0.3	1.330	V
VDD_EBI_PLL VDD_MIPI_DSI_0P9 VDD_MIPI_CSI_0P9 VDD_QLINK_CK VDD_QLINK VDD_UFS_CORE VDD_USB_HS_CORE VDD_USB_SS_CORE VDD_QREFS_0P9	EBI PHY PLL circuits MIPI DSI 0.9 V circuits MIPI CSI 0.9 V circuits QLink clock circuits QLink circuits UFS core circuits USB digital core circuits USB SS core circuits Reference voltage for QREFS	-0.3	1.01	V
VDD_LPI_CORE	LPI core	-0.3	1.19	V
VDD_LPI_MEM	LPI core memory	-0.3	1.19	V
VDD_CORE	Digital core circuits	-0.3	1.19	V
VDD_MEM VDD_LPA_PLL VDD_APC0_PLL VDD_APC1_PLL	On-chip memory Audio circuits Application processor PLL circuits	-0.3	1.19	V
VDD_EBI_PHY VDD_EBI_CC	EBI PHY circuits EBI clock circuits	-0.3	1.19	V
VDD_MODEM	Modem circuits	-0.3	1.19	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_QFPROM	Programming the QFPROM; otherwise, ground	-0.3	2.07	V
VDD_P11	Digital pad circuits – CXO			
VDD_USB_HS_1P8	USB HS1 1.8 V circuits			
VDDA_APC_CS_1P8	APC current sense circuits			
VDD_QREFS_1P8	Reference voltage for QREFS			
VDD_P1	Digital pad circuits – EBI	-0.3	1.29	V
VDD_P2	Digital pad circuits – SDC2 Low voltage High voltage	-0.3	3.33	V
VDD_P3	Digital pad circuits – most I/Os	-0.3	2.09	V
VDD_P7	Digital pad circuits – eMMC	-0.3	2.09	V
VDD_P5	Digital pad circuits – UIM1 dual-voltage Low voltage High voltage	-0.3	3.33	V
VDD_P6	Digital pad circuits – UIM2 dual-voltage Low voltage High voltage	-0.3	3.33	V
VDD_P10	Digital pad circuits – UFS clock	-0.3	1.38	V
VDD_EBI_PHY_HV	EBI PHY high-voltage circuits			
VDD_MIPI_CSI_1P2	MIPI CSI 1.2 V circuits			
VDD_MIPI_DSI_1P2	MIPI DSI 1.2 V circuits			
VDD_USB_SS_1P2	USB SS 1.2 V circuits			
VDD_UFS_1P2	UFS 1.2 V circuits			
VDD_WCSS_ADCDAC	WCSS ADC and DAC	-0.3	1.5	V
VDD_WCSS	WCSS circuits	-0.3	0.95	V
VDD_WCSS_PLL	WCSS PLL circuits			
VDD_EBI_IO VDD_EBI_IO_CC	EBI I/O circuits	-0.3	0.72	V
VDD_USB_HS_3P1	USB HS1 3.1 V circuits	-0.3	3.52	V

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-3). The SDM710 meets all performance specifications listed in Section 3.3 through Section 3.11, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor			
	Turbo	0.64	1.080	V
	Nominal	0.574	0.939	V
	SVS-L1	0.52	0.939	V
	SVS	0.52	0.939	V
	Low-SVS	0.52	0.939	V
VDD_APC1	Kryo Gold application processor			
	Boost	0.74	1.216	V
	Turbo-L2	0.74	1.216	V
	Turbo-L1	0.68	1.216	V
	Nominal-L1	0.612	1.005	V
	Nominal	0.56	1.005	V
	SVS-L1	0.52	1.005	V
	SVS	0.52	1.005	V
	Low-SVS	0.52	1.005	V
VDD_LPI_CORE	LPI core			
	Turbo	0.66	1.071	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.790	V
	Low-SVS	0.485	0.728	V
	Min-SVS	0.485	0.728	V
VDD_LPI_MEM	LPI memory			
	Turbo	0.74	1.076	V
	Nominal	0.74	1.001	V
	SVS-L1 [2]	0.74	0.860	V
VDD_MODEM	Modem circuits			
	Turbo	0.66	1.076	V
	Nominal_L1	0.63	1.001	V
	Nominal	0.595	0.939	V
	SVS_L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low_SVS	0.485	0.724	V
	Min_SVS	0.485	0.724	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_GFX	Graphics			
	Turbo_L1	0.7	1.148	V
	Turbo	0.66	1.076	V
	Nominal_L1	0.63	1.001	V
	Nominal	0.595	0.939	V
	SVS_L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low_SVS	0.485	0.724	V
	Min_SVS	0.485	0.724	V
VDD_CORE	Digital core circuits			
	Turbo	0.66	1.076	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low-SVS	0.485	0.724	V
	Min-SVS	0.485	0.724	V
VDD_MEM	Memory circuits and analog PLL circuits			
VDD_LPA_PLL	Turbo	0.74	1.076	V
VDD_APC0_PLL	Nominal	0.74	1.001	V
VDD_APC1_PLL	SVS-L1 [2]	0.74	0.860	V
VDD_EBI_PHY	EBI PHY circuits			
VDD_EBI_CC	EBI clock circuits			
	Turbo	0.74	1.076	V
	Nominal	0.74	1.001	V
	SVS-L1	0.74	0.860	V
VDD_WCSS	WCSS circuits			
VDD_WCSS_PLL	Nominal [2]	0.74	0.860	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for this power domain is a static setting. There is no scaling.

Table 3-3 Operating conditions

Parameter [1]		Min	Type [2]	Max	Unit
Power supply voltages					
VDD_EBI_PLL	EBI PHY PLL circuits	0.83	0.88	0.92	V
VDD_MIPI_DSI_0P9	MIPI DSI 0.9 V circuits				
VDD_MIPI_CSI_0P9	MIPI CSI 0.9 V circuits				
VDD_QLINK_CK	QLink clock circuits				
VDD_QLINK	QLink circuits				
VDD_UFS_CORE	UFS core circuits				
VDD_USB_HS_CORE	USB digital core circuits				
VDD_USB_SS_CORE	USB SS core circuits				
VDD_QREFS_0P9	Reference voltage for QREFS				

Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Type [2]	Max	Unit
VDD_QFPROM	Programming the QFPROM; otherwise, ground				
VDD_P11	Digital pad circuits – CXO				
VDD_USB_HS_1P8	USB HS1 1.8 V circuits	1.72	1.8	1.88	V
VDDA_APC_CS_1P8	APC current sense circuits				
VDD_QREFS_1P8	Reference voltage for QREFS				
VDD_P1	Digital pad circuits – EBI	1.07	1.12	1.17	V
VDD_P2	Digital pad circuits – SDC2				
	Low voltage	1.7	1.808	1.9	V
	High voltage	2.72	2.928	3.03	V
VDD_P3	Digital pad circuits – most I/Os	1.7	1.8	1.9	V
VDD_P7	Digital pad circuits – eMMC	1.7	1.8	1.9	V
VDD_P5	Digital pad circuits – UIM1 dual-voltage				
	Low voltage	1.7	1.808	1.9	V
	High voltage	2.72	2.96	3.03	V
VDD_P6	Digital pad circuits – UIM2 dual-voltage				
	Low voltage	1.7	1.808	1.9	V
	High voltage	2.72	2.96	3.03	V
VDD_P10	Digital pad circuits – UFS clock	1.15	1.2	1.25	V
VDD_EBI_PHY_HV	EBI PHY high-voltage circuits				
VDD_MIPI_CSI_1P2	MIPI CSI 1.2 V circuits				
VDD_MIPI_DSI_1P2	MIPI DSI 1.2 V circuits				
VDD_USB_SS_1P2	USB SS 1.2 V circuits				
VDD_UFS_1P2	UFS 1.2 V circuits				
VDD_WCSS_ADCDAC	WCSS ADC and DAC	1.17	1.304	1.36	V
VDD_EBI_IO VDD_EBI_IO_CC	EBI I/O circuits	0.57	0.6	0.64	V
VDD_USB_HS_3P1	USB HS1 3.1 V circuits	2.96	3.088	3.2	V
Thermal conditions					
T_j	Device operating temperature (junction)	–	–	+95	°C
T_A [3]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.

3.2.1 Core and memory voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE and VDD_MEM retention mode. This technique reduces the leakage of the digital logic and memory by reducing VDD to the

minimum required to maintain the register and memory state. The V (MIN) for state retention is found through characterization.

Table 3-4 Core voltage in retention mode [1, 2]

VDD_CORE	Bit 63 (MSB)	Bit 62	Bit 61 (LSB)
0.4 V	1	0	0
0.44V	0	1	1
0.48V	0	1	0
0.52 V	0	0	1
0.56 V	1	1	1

1. The VDD_CORE voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x00780134.

Table 3-5 Memory voltage in retention mode [1, 2]

VDD_MEM	Bit 19 (MSB)	Bit 18	Bit 17 (LSB)
0.488 V	1	0	0
0.54 V	0	1	1
0.592 V	0	1	0
0.644 V	0	0	1

1. The VDD_MEM voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x00780148.

3.3 Power distribution network (PDN)

The impedances of the distribution networks that deliver power to the SDM/SDA device are critical to its supply voltages, not just at DC, but over a wide range of frequencies. An inadequate PDN could cause the minimum/maximum values to be violated. Table 3-6 through Table 3-9 list the PDN maximum impedance specifications.

Table 3-6 PDN specifications – lumped

Power domain	Specification [1]			Pin numbers of positive ports	Pin numbers of negative ports
	Maximum DC resistance	Parameters for max impedance (z_{spec}) calculation [2]			
		R_{mid_freq} (mΩ)	Inductance L (pH)		
VDD_APC0	5	22	130	AG19, AM8, AL7, AK8, AH8, AF8, AF16, AE9, AD16, AD14, AC15, AD12, AD10, AC17	AH18, AB14, AN7, AM10, AK6, AK10, AJ7, AH16, AH10, AG7, AF14, AF12, AF10, AB18, AB16
VDD_APC1	2	17	100	AN21, AN19, AN15, AN11, AM20, AM18, AM16, AM14, AM12, AL21, AL11, AK20, AK18, AK16, AK14, AK12, AJ19, AJ13	AP20, AP18, AP16, AP14, AP12, AM22, AM10, AK22, AK10, AJ21, AH18, AH16, AH14, AH12, AH10
VDD_MODEM	7	29	170	AH24, AN29, AN25, AM28, AM26, AM24, AL33, AL31, AL23, AK32, AK30, AK28, AK26, AK24, AJ25	AF24, AP32, AP30, AP28, AP26, AP24, AN23, AM34, AM32, AM30, AM22, AK22, AH30, AH28, AH26
VDD_CORE	5	24	130	Y32, Y30, Y28, Y26, Y24, V26, V24, U23, T26, T24, R23, R21, R17, R13, P26, P24, P22, P20, P18, P16, P14, N17, N15, N13, M26, M24, AA33, AA29, AA23	Y22, V22, T28, T22, T20, T18, T16, T14, T12, P28, P12, M22, M20, M18, M16, M14, M12, K26, AB34, AB32, AB30, AB28, AB26, AB24, AA35
VDD_MEM	5	24	130	AF26, AE25, Y20, W21, W17, W15, V20, V18, V16, V14, V12, V10, U21, U19, U13, U11, AG29, AG27, AG25, AG17, AF28, AF26, AF18, AE27, AD32, AD30, AD28, AD26, AD24, AD22, AD20, AD18, AC31, AC29, AC27, AC25, AC23, AC21, AC19, AB22, AB20, AA19	AF32, Y22, Y18, Y16, Y14, Y12, Y10, V22, T22, T20, T18, T16, T14, T12, T10, AH30, AH28, AH26, AH18, AH16, AF24, AB32, AB30, AB28, AB26, AB24, AB18
VDD_WCSS	55	101	600	N11, M10, L9	P12, M12
VDD_LPI_CORE	70	83	499	AD34, AF34	AB36, AB34, AD36
VDD_LPI_MEM	100	172	1050	AH32	AF32
VDD_GFX	3	20	119	V32, V30, V28, U31, U29, N35, N33, N31, N29, N27, M34, M32, M30, M28, L33	V34, T32, T30, T28, R33, P36, P34, P32, P30, P28, N37, M36, K34, K32, K30, K28

1. Both lumped and distributed DC specifications must be met. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz and proceeding to each higher frequency point defined.
2. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and AC inductance (L) values from this table.

   Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) ranges from 1 MHz to 200 MHz.

Table 3-7 PDN specifications – distributed

Power domain	Specification [1]			Port number	Pin numbers of positive ports	Pin numbers of negative ports
	Maximum DC resistance	Parameters for max impedance (z_{spec}) calculation [2]				
		R_{mid_freq} (mΩ)	Inductance L (pH)			
VDD_CORE	6	27	149	1	P20, P18, R17, N17, P16, N15, P14, R13, N13	T20, T18, T16, T14, T12, P12, M12, M14, M16, M18, M20
	6	36	200	2	AA33, Y32, Y30, AA29, Y28, AA23, Y26, Y24, V26, V24, U23, T26, T24, P26, P24, M26, M24, R23, P22, R21	K26, AA35, AB34, AB32, AB30, AB28, AB26, AB24, Y22, V22, T28, P28, T22, T20, M22
VDD_MEM	6	27	149	1	AA19, AB20, AB22, AC23, AC21, AC19, AD22, AD20, AD18, AF18, AG17	AB24, Y22, Y18, AB18, AH16, AH18
	7	31	175	2	AD32, AC31, AD30, AC29, AD28, AC27, AC25, AD24, AD26, AE27, AE25, AF28, AF26, AG29, AG27, AG25	AF24, AB24, AB26, AB28, AB30, AB32, AF32, AH30, AH28, AH26
	6	36	200	3	V10, U11, V12, U13, V14, W15, V16, W17, V18, U19, U21, V20, W21, Y20	Y10, Y12, Y14, Y16, Y18, Y22, V22, T22, T20, T18, T16, T14, T12, T10

1. Both lumped and distributed DC specifications must be met. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz and proceeding to each higher frequency point defined.
2. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and AC inductance (L) values from this table

Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) ranges from 1 MHz to 200 MHz.

Table 3-8 PDN specifications – LPDDR4X

Power domain	Specification [1]			Pin numbers of positive ports	Pin numbers of negative ports
	Maximum DC resistance	Parameters for max impedance (z_{spec}) calculation [2]			
		R_{mid_freq} (mΩ)	Inductance L (pH)		
VDD_EBI_PHY	30	75	1000	K16, K14, K12, K10, H16, H12, H10	M16, M14, M12, H8, G9, G11, F14, G13, G15
VDD_EBI_IO	10	307	600	K22, K18, K20, J21, J19, H20	M22, M20, M18, F22, G19

1. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz and proceeding to each higher frequency point defined.
2. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and AC inductance (L) values from this table

Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) ranges from 1 MHz to 200 MHz.

Table 3-9 PDN specifications – SERDES

PMIC regulator	Power domain	Voltage (V)	Maximum DC resistance (mΩ)	Parameters for max impedance (z_{spec}) calculation [1]		Pin number of positive ports	Pin number of negative ports
				R_{mid_freq} (mΩ)	Inductance L (pH)		
VREG_L1A	VDD_MIPI_CSI_1P2	1.232	2400	235	1500	AA9	Y10, Y8
			2400	235	1500	AB8	Y10, Y8
			2400	235	1500	AC7	Y10, Y8
	VDD_MIPI_DSI_1P2		1200	157	1000	Y36	AA35, W35
			1200	157	1000	Y34	AA35, W35
	VDD_UFS_1P2		857	235	1500	H24	K26
	VDD_USB_SS_1P2		500	196	1250	AH34	AF32
VREG_L1B	VDD_UFS_CORE	0.928	438	176	1125	H28	K28, G29
	VDD_USB_SS_CORE		159	138	880	AK34	AM34
	VDD_USB_HS_CORE		1250	235	1500	AK36	AM34
	VDD_MIPI_DSI_0P9		350	169	1080	T36	V36, P36
			350	169	1080	T34	V34, P34
	VDD_MIPI_CSI_0P9		521	235	1500	AA11	AB12, Y12, Y10
			521	235	1500	AB10	AB12, Y12, Y10
			521	235	1500	AD8	AB12, Y12, Y10
	VDD_QLINK		729	235	1500	AR23	AU23, AT22
	VDD_QLINK_CK		625	235	1500	AR25	AP26, AP24
VREG_L7B	VDD_USB_HS_3P1	3.136	4393	235	1500	AH36	AJ37
VREG_L10A	VDD_USB_HS_1P8	1.8	600	157	1000	AM38	AN37

1. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and AC inductance (L) values from this table

Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) ranges from 1 MHz to 200 MHz.

3.4 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire SDM710 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. See the appropriate PMIC device specification, such as the *PM670A/PM670L Power Management IC Device Specification* (80-PD120-1) or the *PM670 Power Management IC Device Specification* (80-PD119-1) for details.

A high-level summary of the required default power-on sequence is:

1. VDD_MEM (on-chip memory), VDD_APC0_PLL, VDD_APC1_PLL, VDD_EBI_PHY (EBI PHY circuits), VDD_EBI_CC, and VDD_LPA_PLL (PLL circuits – low voltage)
2. VDD_LPI_MEM (LPI core memory)
3. VDD_CORE (digital core circuits)

4. VDD_LPI_CORE (LPI core)
5. VDD_WCSS and VDD_WCSS_PLL (WCSS PLL circuits)
6. GEN 1.8 V IO
7. VREF_SDC, VREF_UIM, and VDD_QREFS_1P25
8. VDD_WCSS_ADCDAC (WCSS ADC and DAC circuits)
9. VDD_P10 (UFS clock), VDD_EBI_PHY_HV (EBI PHY high-voltage circuit), VDD_MIPI_CSI0_1P2, VDD_MIPI_CSI1_1P2, VDD_MIPI_CSI2_1P2, VDD_MIPI_DSI0_1P2, VDD_MIPI_DSI1_1P2, VDD_UFS_1P2, and VDD_USB_SS_1P2
10. VDD_EBI_IO and VDD_EBI_IO_CC (LPDDR4X)
11. VDD_EBI_PLL, VDD_MIPI_DSI0_PLL, VDD_MIPI_DSI1_PLL, VDD_MIPI_CSI0_0P9, VDD_MIPI_CSI1_0P9, VDD_MIPI_CSI2_0P9, VDD_MIPI_DSI0_0P9, VDD_MIPI_DSI1_0P9, VDD_QREFS_0P9, VDD_QLINK_CK, VDD_USB_SS_CORE, VDD_USB_HS_CORE, VDD_UFS_CORE, and VDD_QLINK
12. VDD_QFPROM, CXO (VDD_P11), VDD_QREFS_1P8, VDD_USB_HS_1P8, and VDD_APC_CS_1P8
13. VDD_USB_HS_3P1
14. VDD_P2 (digital pad circuits: SDC2 [low voltage and high voltage])
15. VDD_MODEM
16. VDD_APC0

Comments regarding this sequence include:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_PX), so that the internal circuits can take control of the I/Os and pads. If pad voltages power up first, the output drivers might be stuck in unknown states and might cause large leakage currents until VDD_CORE powers on.
- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_CORE reaches 90% of its value, the VDD_P3 supply can start ramping up.

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the document *SDM670/SDM710 Linux Android Current Consumption Data* (80-PB873-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-10 Dhrystone and rock bottom maximum power

SDM version	Cortex-A53 quad core Dhrystone (W) at 85°C (Tj) [1, 2, 3]	Rock bottom (mW) at 30°C (Tj) [4]
SDM710	3.5	9.5

1. This Kryo Gold dual core Dhrystone specification applies to SDM710 CS devices that run at 2.208 GHz.
2. Dhrystone power should be measured on the VDD_APC1 rail, right before PDN capacitors (with a small serial sampling resistor inserted, if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and the average window should be > 1 ms (or > 1250 samples).
4. Rock bottom power should be measured when VDD_MEM is at retention voltage and VDD_CORE is power collapsed in sleep mode. See AIR1 in Table 3-1 Test definitions in the *SDM670/SDM710 Linux Android Current Consumption Data* (80-PB873-7) document for the test setup.

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SDM device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-11 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_P3	VDD_P3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDD_P3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_P3	VDD_P3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDD_P3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	1.0	µA
I_{IL}	Input low leakage current [1]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [1]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	µA (kΩ)

Table 3-11 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{OH}	High-level output voltage, CMOS	VDD_P3 - 0.45	VDD_P3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
2. Pin voltage = VDD_P3 maximum. For keeper pins, pin voltage = VDD_P3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDD_P3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_P3 maximum.

Table 3-12 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDD_P2	–	VDD_P2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_P2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_P2	–	VDD_P2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDD_P2	V

Table 3-13 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ

Table 3-13 SDC 1.8 V mode DC specifications (cont.)

Parameter	Description	Min	Typ	Max	Units
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 UICC 3 V mode DC specifications (VDD_P5 and VDD_P6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDD_Px	–	VDD_Px	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. VHYS is not a required specification for UICC.
3. UICC specifies VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case VOH is used in this table.
4. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O). The worse-case VOL is used in this table.

NOTE: UICC supply range for class B is 2.7 V to 3.3 V.

Table 3-15 UICC 1.8 V mode DC specifications (VDD_P5 and VDD_P6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDD_Px	–	VDD_Px	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. VHYS is not a required specification for UICC.
3. UICC specifies VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case VOH is used in this table.
4. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.3 V (I/O). The worse-case VOL is used in this table.

NOTE: UICC supply range for class C is 1.62 V to 1.98 V.

Table 3-16 Digital I/O characteristics for VDD_P10 nominal (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDD_P10	V
V_{OH}	Output high-level voltage	0.75 × VDD_P10	VDD_P10	V
$R_{PULL-UP}$	Pull-up resistance	100	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	100	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	µA

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1), with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

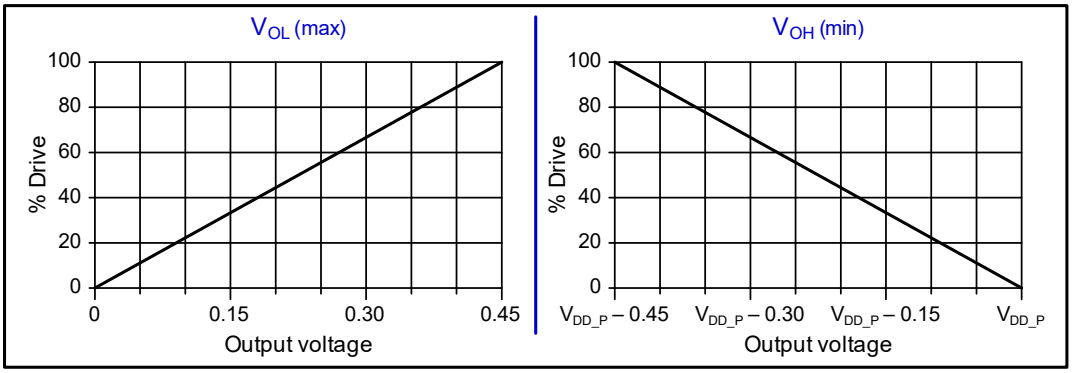


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_Px})

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE: All SDM710 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

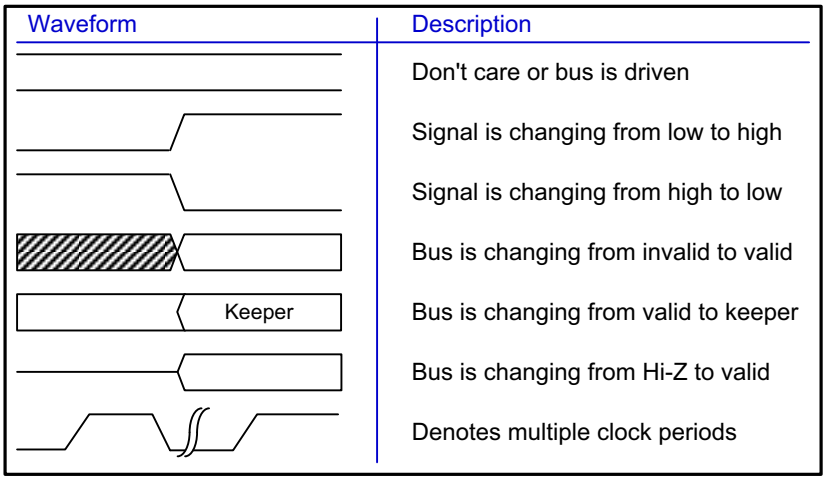


Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SDM710 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

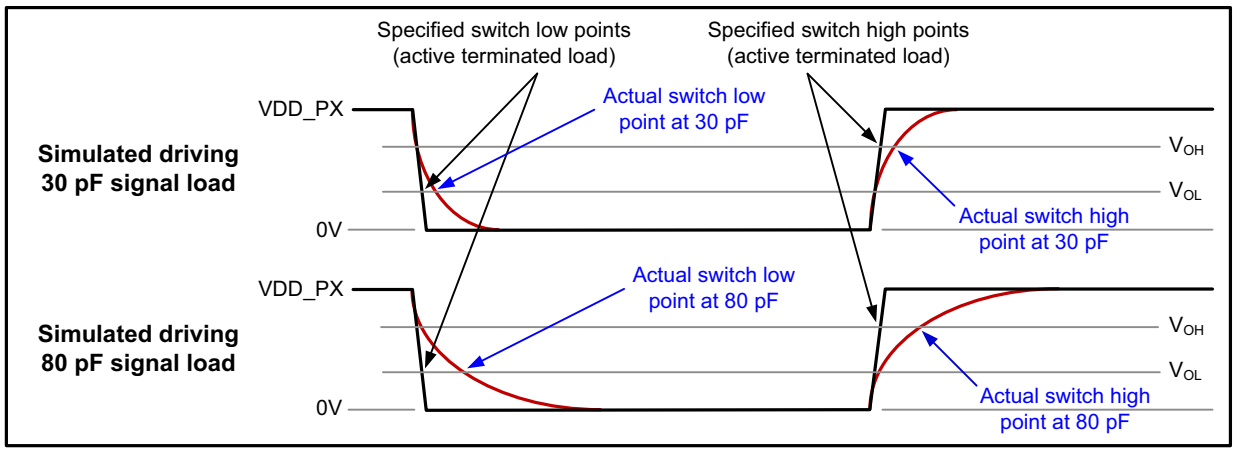


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SDM device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SDM710 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated V_{DD_PX} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

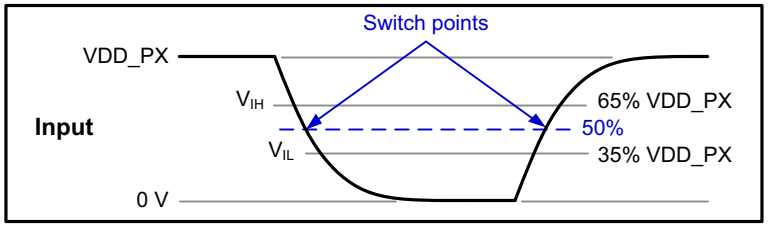


Figure 3-4 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DD_PX} - 50 mV or more
- V_{OL} ~ 50 mV or less

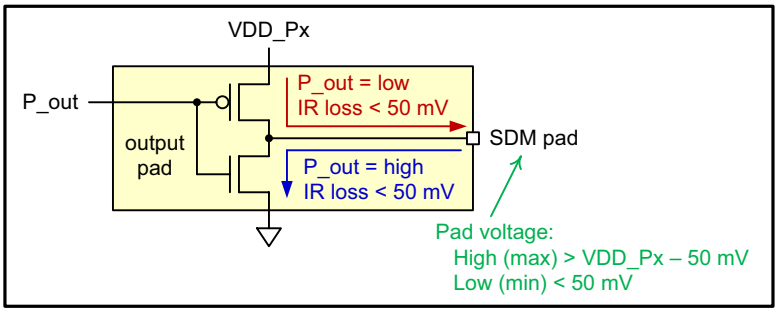


Figure 3-5 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both the input and output behaviors were described above.

3.7 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.7.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4x SDRAM memory that is attached to the SDM710 chipset.

3.7.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.9.1 for secure digital interface details.

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SDM710 device supports up to three DPHY or CPHY camera interfaces.

Table 3-17 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	The maximum supported data rate is 1.5 Gsps.

3.8.2 Audio support

The SDM710 provides the system's digital audio functions that supplement one of the two analog audio codec implementations:

- Integrated into the PM670A/PM670L device, a proprietary PDM interface (Section 3.9.8) using LPI_GPIO[18:25] communicates audio data with the PMIC's audio codec.
- A dedicated audio codec, such as the WCD9340/WCD9341/WCD9326/WCD9335, uses the industry standard SLIMbus interface (Section 3.9.6) via LPI_GPIO[19:20].

Other SDM audio-related interface options include:

- SLIMbus – Section 3.9.6
- I^2S – Section 3.9.7
- Audio PDM – Section 3.9.8
- Digital microphone – Section 3.9.9
- SoundWire – Section 3.9.10
- I^2C – Section 3.9.12

See the *WCD9340/WCD9341 Audio Codec Device Specification* (80-P4986-1) for performance characteristics.

See the *WCD9326 Audio Codec Device Specification* (80-NT793-1) for performance characteristics.

See the *WCD9335 Audio Codec Device Specification* (80-NT781-1) for performance characteristics.

3.8.3 Display support

The SDM710 device supports up to two DPHY displays.

Table 3-18 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

3.9 Connectivity

The connectivity functions supported by the SDM710 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Universal integrated circuit card (UICC) interface
- DisplayPort support over USB Type-C
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power interchip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Dedicated I^2C interfaces for camera (CCI I^2C)
- Through proper configuration of the 13 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

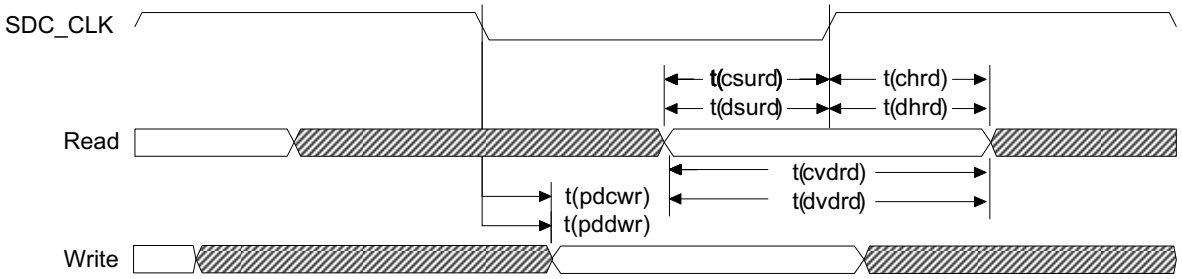
NOTE: In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

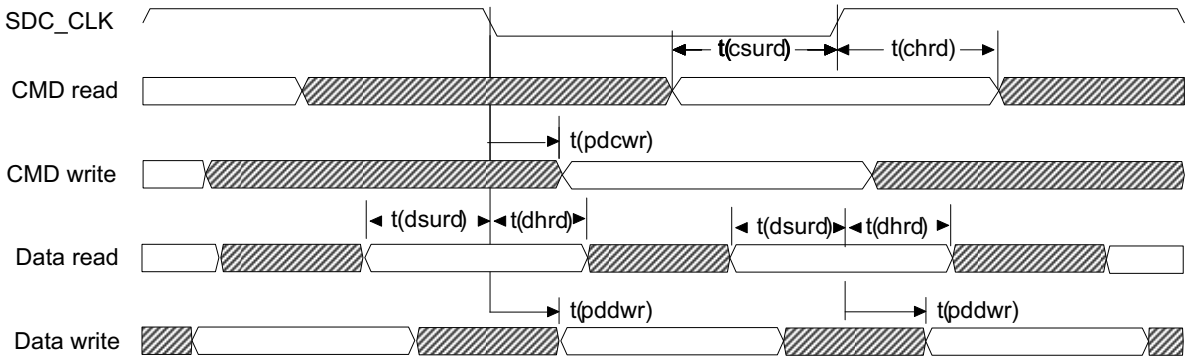
Table 3-19 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

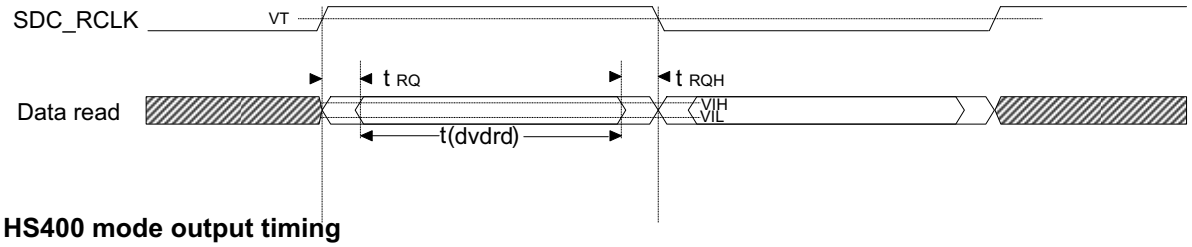
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

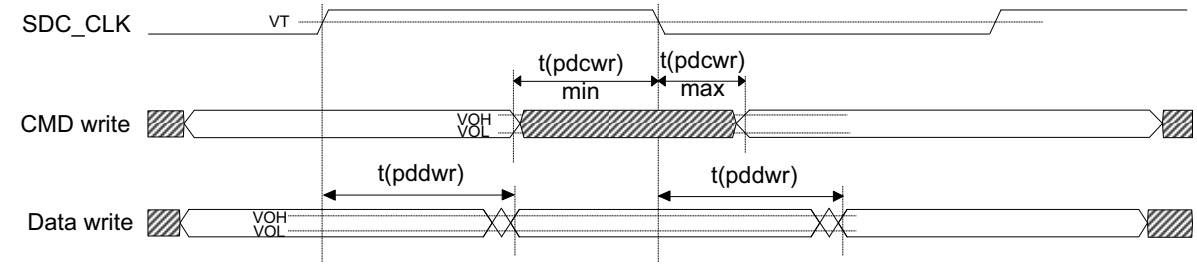


Figure 3-6 SD interface timing

3.9.2 USB interfaces

Table 3-20 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.9.3 DisplayPort

Table 3-21 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.9.4 UFS interface

Table 3-22 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 2.1	None

3.9.5 UICC interface

Table 3-23 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.6 SLIMbus interface

Table 3-24 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.9.7 I²S interfaces

There are two I²S interface types supported by the SDM710:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI2S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-25 applies to MI2S.

Table 3-25 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996 (Available for free download.)	None

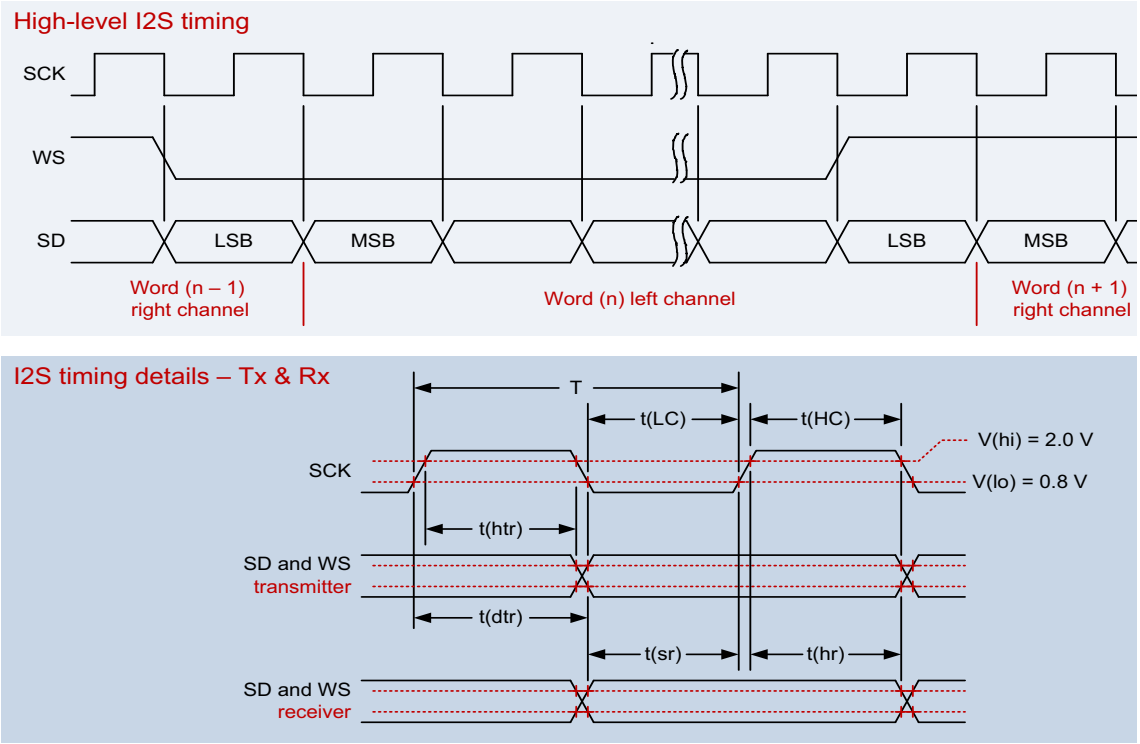


Figure 3-7 I2S timing diagram

Table 3-26 I²S interface timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency[1]		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 · T	–	0.55 · T	ns
t(LC)	Clock low	–	0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 · T	–	0.55 · T	ns
t(LC)	Clock low	–	0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
t(htr)	SD and WS output hold time	–	–	–	–	ns

1. Load capacitance is between 10 and 40 pF.

3.9.8 Audio PDM

This is a proprietary PDM interface, so details are not provided. For general audio performance, see the *PM670A/PM670L Power Management IC Device Specification* (80-PD120-1) or the *PM670 Power Management IC Device Specification* (80-PD119-1).

3.9.9 Digital microphone PDM interface

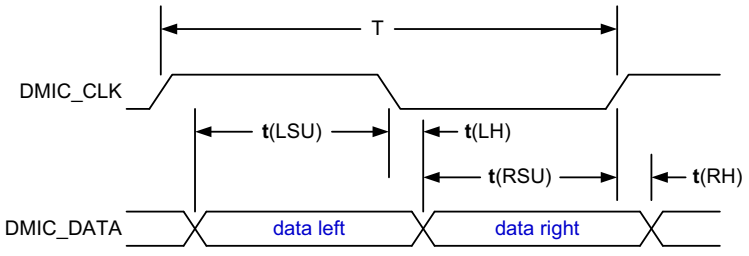


Figure 3-8 Digital microphone PDM interface timing

Table 3-27 Digital microphone timing

Parameter		Min	Typ	Max	Units
T	DMIC clock period	163	–	1666	ns
t(LSU)	Data left setup time to clock falling edge	5	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	5	–	–	ns
t(RH)	Data right hold time to clock falling edge	0	–	–	ns

3.9.10 SoundWire

SDM710 SoundWire PHY timing parameters, as specified in Table 3-28, are compliant to clock and data specifications, as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04. See Figure 3-9 and Figure 3-10.

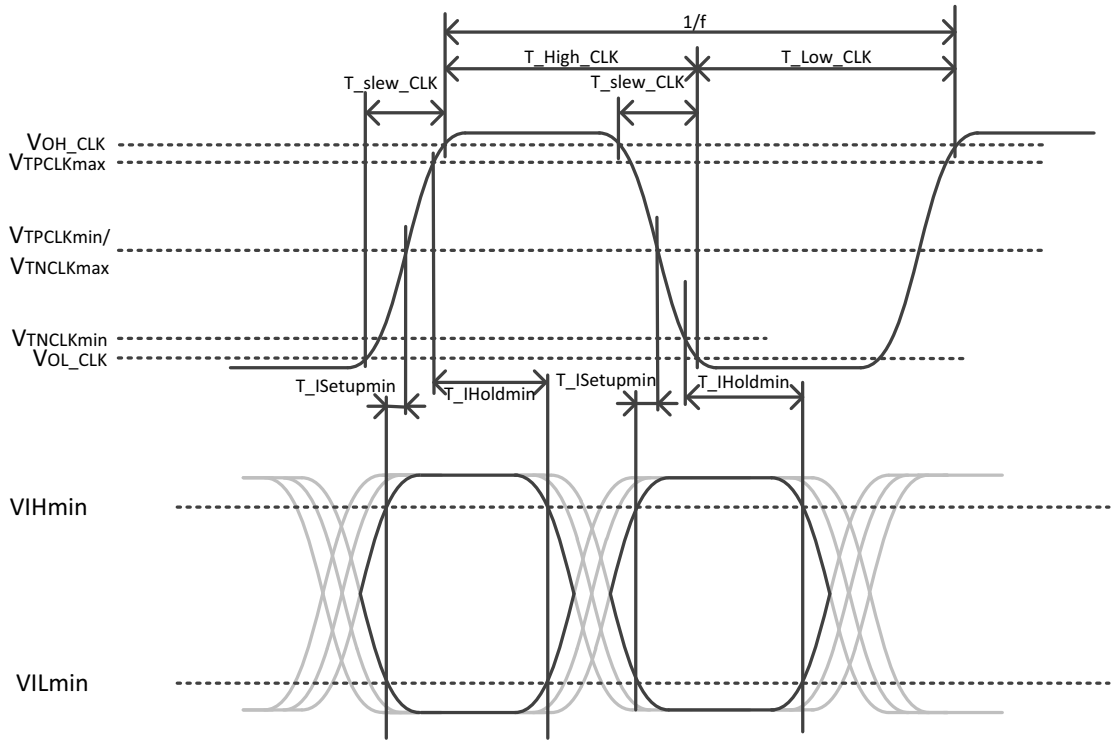


Figure 3-9 PHY timing – clock output/input and data input

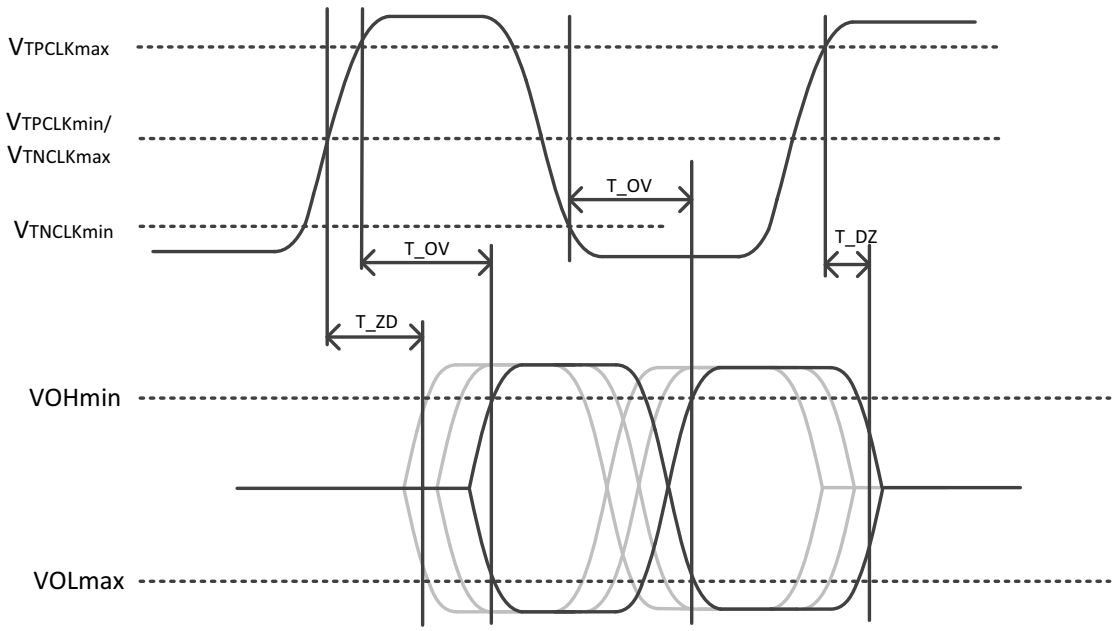


Figure 3-10 PHY timing – clock output and data output

Table 3-28 PHY timing parameters (1.8 V systems)

Name	Description	Min	Typ	Max	Units
VOH_CLK	Voltage level for clock high output	1.36D	–	–	V
VOL_CLK	Voltage level for clock low output	–	–	0.36	V
T_slew_CLK	Slew time for positive or negative clock edge on clock output	4.68	5.32	6.01	ns
T_High_CLK	Duration of high half-period on clock output	35.3	–	–	ns
T_Low_CLK	Duration of low half-period on clock output	35.3	–	–	ns
DC_Out_Clock	Duty cycle generated at clock output	46	–	54	%
DC_In_Clock	Duty cycle received at clock input	–	–	–	%
T_DZ	Time to disable data output after positive or negative edge on clock input	–	–	4	ns
T_ZD	Time to enable data output after positive or negative edge on clock input	7.9	–	–	ns
T_OV	Time for data output to remain stable or valid after positive or negative edge on clock input	–	–	27.6	ns
T_OH	Time for data output to remain stable after positive or negative edge on clock input	6.7	–	–	ns
t_ISetup_min	Minimum setup time demanded by a data input prior to a positive or negative edge on clock input	–	–	0	ns
t_IHold_min	Minimum hold time demanded by a data input after to a positive or negative edge on clock input	–	–	4	ns
Frequency	Clock output frequency	–	–	12.288	MHz

3.9.11 Touchscreen connections

Touchscreen panels are supported using I2C buses (Section 3.9.12) and GPIOs configured as discrete digital inputs (Section 3.5) or through SPI bus (Section 3.9.13) through LPI GPIO.

3.9.12 I2C interface

Table 3-29 Supported I2C standards and exceptions

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, and 10-bit addressing are not supported.

3.9.13 Serial peripheral interface

The SDM710 supports SPI as a master only. Any one of the 13 QUP ports can be configured as an SPI master.

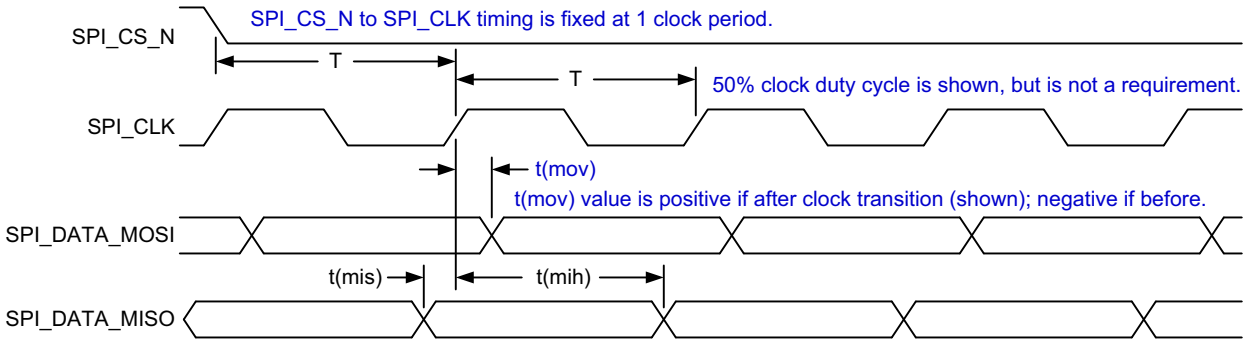


Figure 3-11 SPI master timing diagram

Table 3-30 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	9	–	–	ns
t(cl)	Clock low	9	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

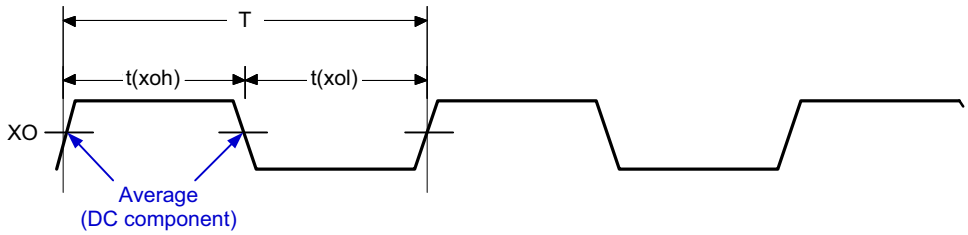


Figure 3-12 XO timing parameters

Table 3-31 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.10.1.2 Sleep clock

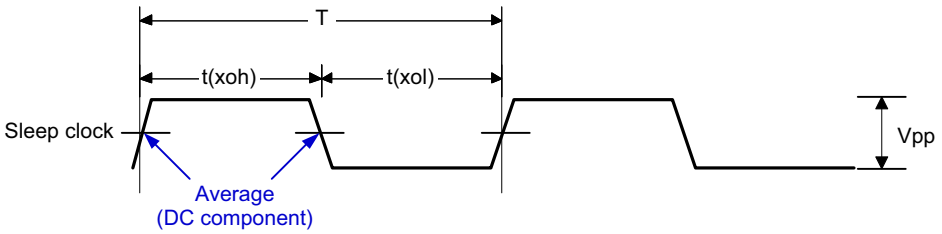


Figure 3-13 Sleep-clock timing parameters

Table 3-32 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.5.

3.10.3 JTAG

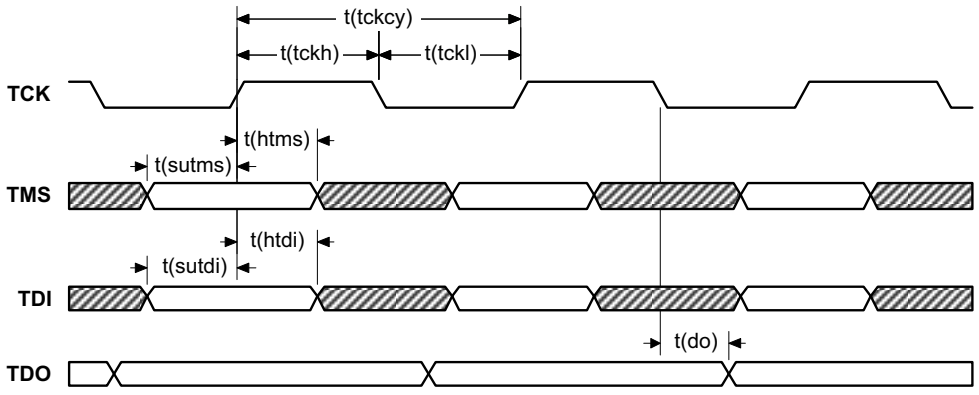


Figure 3-14 JTAG interface timing diagram

Table 3-33 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

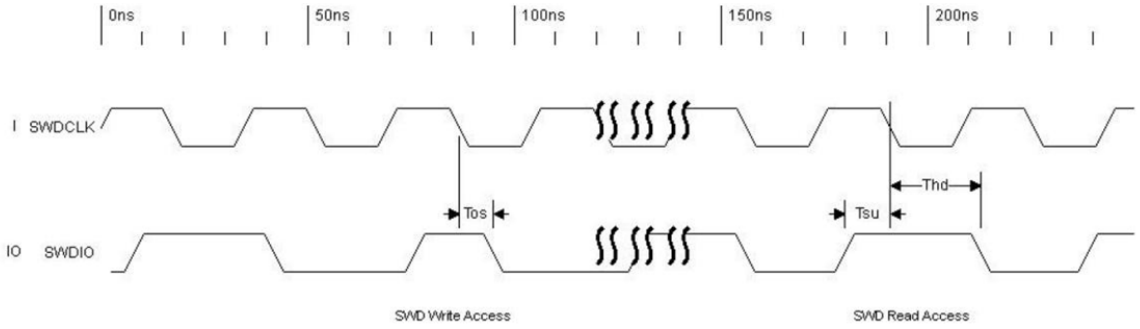


Figure 3-15 SWD write and read AC timing diagram

Table 3-34 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	17.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

3.11 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-3. The digital I/Os must meet the logic-level requirements specified in Section 3.5. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.11.1 RF front end (RFFE)

Table 3-35 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None

3.11.2 System power management interface (SPMI)

Table 3-36 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SDM710 device is available in the 771 PSP, a 10.5 × 11.1 × 0.99 mm non-PoP package. The package includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE: Click the following links to download *Package Outline Drawing, 771 PSP, 10.5 × 11.1 × 0.99 mm, S248, M530* (NT90-PB845-1) from the Qualcomm CreatePoint website.
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PB845-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

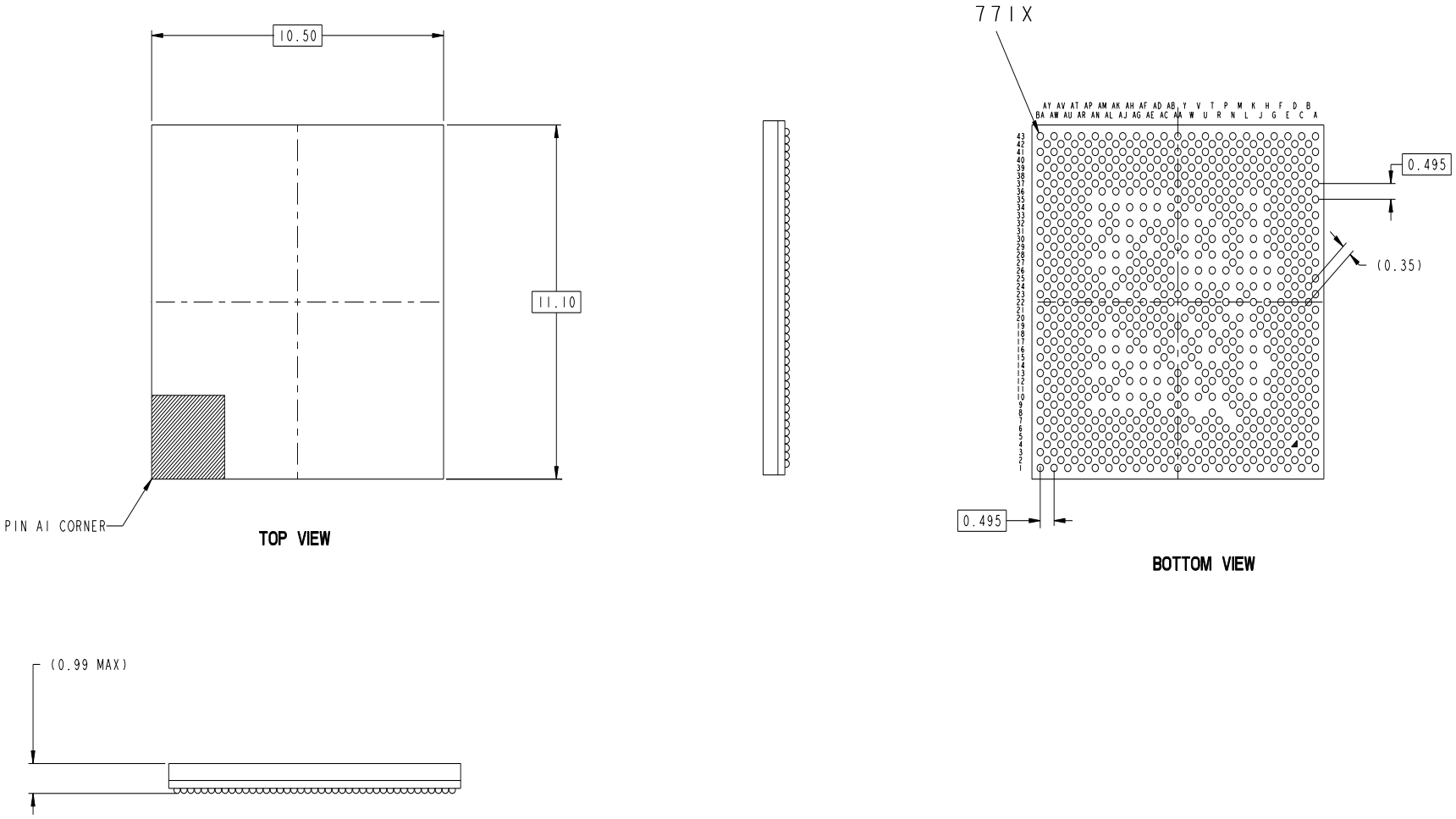


Figure 4-1 Simplified 771 PSP (10.5 × 11.1 × 0.99 mm) outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PB845-1

4.2 SDM710 part marking

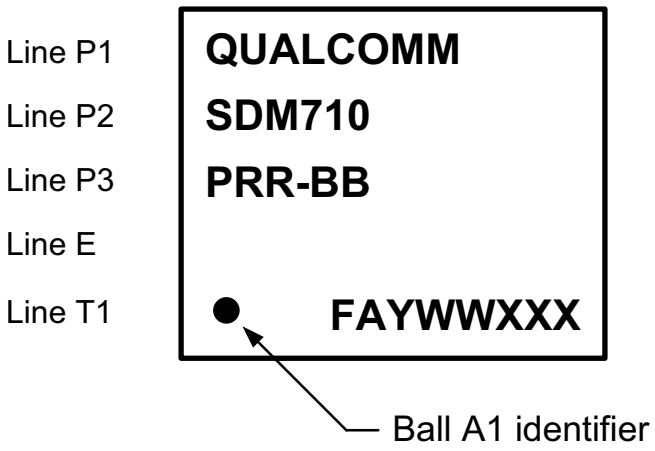


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm name or logo
P2	SDM710	Qualcomm Technologies, Inc. (QTI) product name
P3	PRR-BB	P = product configuration code ■ See Table 4-3 for assigned values. RR = product revision code ■ See Table 4-3 for assigned values. BB = feature code ■ See Table 4-3 for assigned values.
E	Blank or variable	Additional content as necessary
T1	FAYWWXXX	F = supply source code ■ F = J (Samsung) A = assembly site code ■ A = E (ASE, Taiwan) ■ A = K (SPIL, Taiwan) ■ A = H (JCET STATS ChipPAC, Korea) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE: For complete marking definitions of all SDM710 variants and revisions, see the *SDM710 Device Revision Guide* (80-PG301-4).

The 28-bit QFPROM PTE register is summarized in Table 4-2.

Table 4-2 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the JTAG ID.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	SDM-710	— 0	— 771	PSP	— MT	— 00	— 0	— AA

'CCC' is not a fixed length; it depends on the # of pins in the package

Package type varies in the # of characters

Feature code (BB) may not be included when identifying older devices.

Figure 4-3 SDM710 example device identification code

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [1]	Hardware revision number	FEATURE_ID [2]	Hardware version	S value [3]	Comments
SDM710	CS	001-AA	0x1 00DB 0E1	0x0	v1.1	0	2.208 GHz (Kryo Gold)/1.708 GHz (Kryo Silver) CPU 2 + 6, 32 MP 20 + 20 camera, QHD+, 2880 × 1440, A616, HVX, 8SL DL 800 Mbps, 2SL UL 150 Mbps, 4 × 4 MIMO, CDMA

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. FEATURE_ID combined with hardware revision number defines unique product variants.
3. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-4.

Table 4-4 Source configuration code

S value	Die	F value = J	F value = TBD	F value = TBD	F value = TBD
0	Digital	Samsung			
Other columns and rows will be added in future revisions of this document, if needed.					

4.3.2 Daisy chain devices

The SDM710 daisy chain ordering part number is TP-771PSP-MT-1.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-5.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SDM710 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SDM710 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE For more information, see *SDM670 771PSP Package Thermal Model Icepak* (HS11-PB873-5HW) and *SDM670 771PSP Package Thermal Model FloTHERM* (HS11-PB873-6HW).

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

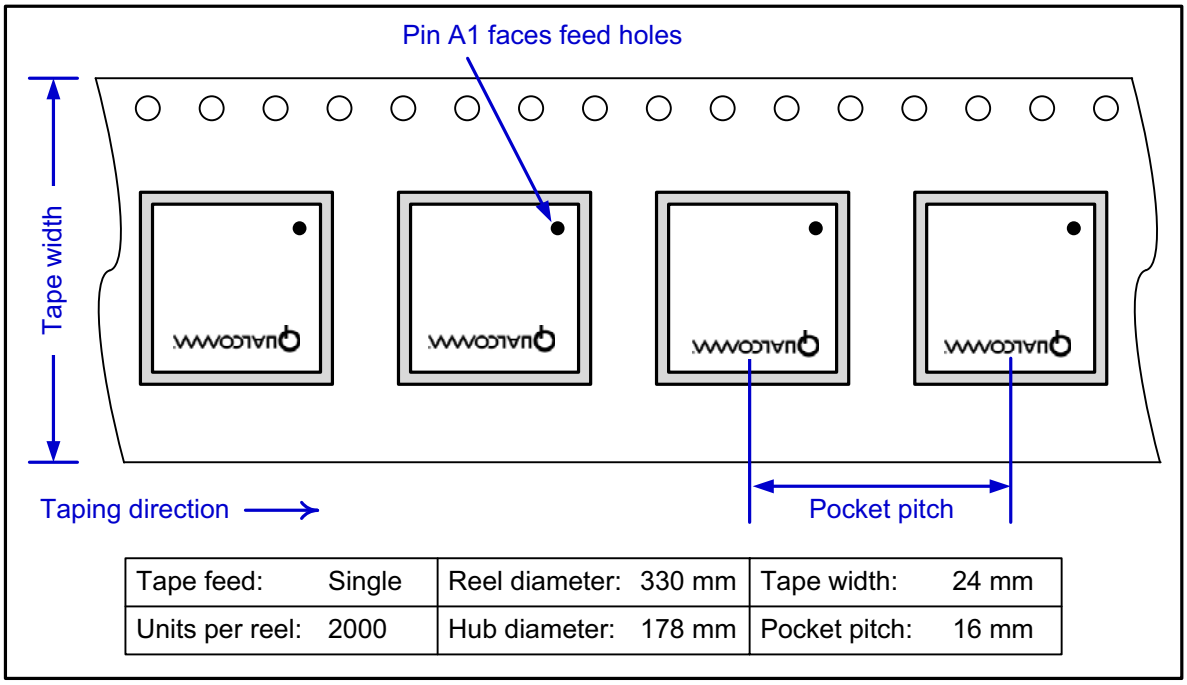
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SDM710 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

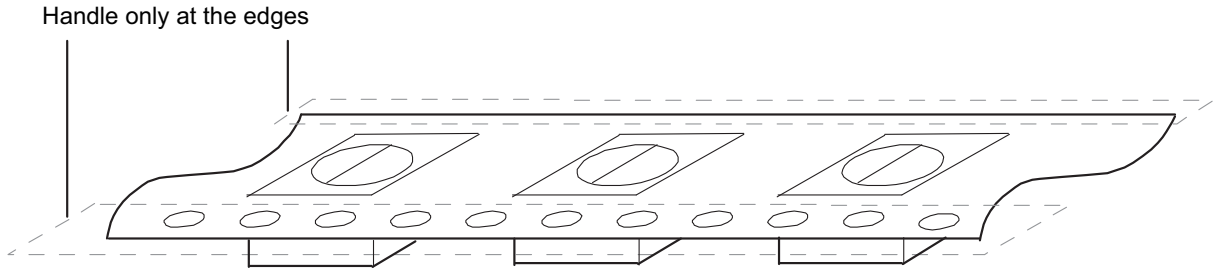


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

SDM710 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SDM710 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SDM710 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy chain components.

Ordering information is given in Section 4.3.2.

Daisy chain PCB routing recommendations are available for download.

NOTE: Click the following link to download *Daisy Chain Interconnect, 771 PSP, 10.5 × 11.1 mm* (DS90-PB845-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-PB845-1

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7 Part reliability

7.1 Reliability qualifications summary

SDM710 reliability evaluation report for 771 FCPSP device from Samsung S1.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	383	DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	383	Pass FIT < 100
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	383	> 20
ESD – Human body model (HBM) rating JESD22-A114-F (Total samples from one wafer lot)	48 (2 lots)	1000 V
ESD – Charged device model (CDM) rating JESD22-C101-D (Total samples from one wafer lot)	12 (2 lots)	250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	12 (2 lots)	Passed
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C (Total samples from one wafer lot)	12 (2 lots)	Passed

1. One unit failed ELFR for MBIST, and the failing die was at the extreme edge of the die. FA showed contact to gate shorted because of Mask misalignment

Table 7-2 Package reliability results

Tests, standards, and conditions	SCK sample size	SPIL sample size	ASE sample size	Result
Moisture resistance test (MRT): J-STD-020D Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	Passed
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	231	Passed
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hrs duration *or* 110°C/85% RH and 264 hrs duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	231	Passed
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hrs duration *or* 110°C/85% RH and 264 hrs duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	231	Passed
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1 hours Total samples from three different assembly lots	231	231	231	Passed
Flammability UL-STD-94 **Note:** Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–		See note under test column.
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	78	78	78	Passed
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	15	Passed

Table 7-2 Package reliability results

Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	15	15	15	Passed
Internal/external visual (Total samples from three different assembly lots at each SAT)	78	78	15	Passed

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	SDM710
Package type	771 PSP
Package body size	11.1 × 10.5 × 0.99 mm
Ball count	771
Ball composition	SAC125/Ni
Fab process	10 nm FinFET
Fab sites	Samsung
Assembly sites	ASE, Taiwan SPIL, Taiwan JCET STATS ChipPAC, Korea
Solder ball pitch	0.35 mm

8 Revision history

Revision	Date	Description
A	March 2018	Initial release
B	May 2018	■ Global: □ Updated the exact maximum frequency of Kryo Gold and Kryo Silver □ Changed Bluetooth 5.x to Bluetooth 5.0 □ Updated the camera input resolution from 16 + 16 MP to 16 + 16 + 2 MP ■ Table 1-1 SDM710 features: □ Updated DX specification 12.x to 12.2 □ Updated OpenCL 2.x to 2.0 ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Added a new row for the operating conditions for voltage rails with AVS Type-1 ■ Table 3-3 Operating conditions: Removed case temperature (Tc) details and added junction temperature (Tj) ■ Section 3.3 Power distribution network (PDN): Updated the PDN specifications with $\mathbf{R_{mid\_freq}}$ and inductance values ■ *Section 3.4.1 Average operating current: Updated the SDM670/SDM710 Linux Android Current Consumption Data* (80-PB873-7) document title ■ Table 3-10 Dhrystone and rock bottom maximum power: Updated the footnote ■ Table 4-3 Device identification details: □ Sample type corrected from ES to CS □ Updated the signaling link from 4 SL UL to 2SL UL ■ Section 5.1.1 Tape and reel information: Corrected the wrong direction description in tape and reel ■ *Section 7.1 Reliability qualifications summary:* Added part reliability information

Revision	Date	Description
C	May 2018	Changed process node from 10 nm LPE to 10 nm LPP
D	October 2018	■ Global: Updated the camera specification from 16 + 16 + 2 MP at 30 fps to 20 + 20 + 2MP at 26 fps. ■ Table 3-3 *Operating conditions*: Corrected the minimum value of ■ VDD_USB_HS_3P1 from 2.96D to 2.96. ■ Table 3-9 *PDN specifications – SERDES*: Corrected the pin number of positive ports for VDD_UFS_1P2 to H24. ■ Table 3-10 *Dhrystone and rock bottom maximum power*: Corrected the footnote for rock bottom power. ■ Section 4.5 *Thermal characteristics*: Updated the document references in the Note.

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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