Device description

The SM6225 device is the next generation of the Snapdragon® 600 series processor and LTE modem. It is designed with 6 nm process for superior performance and power efficiency.

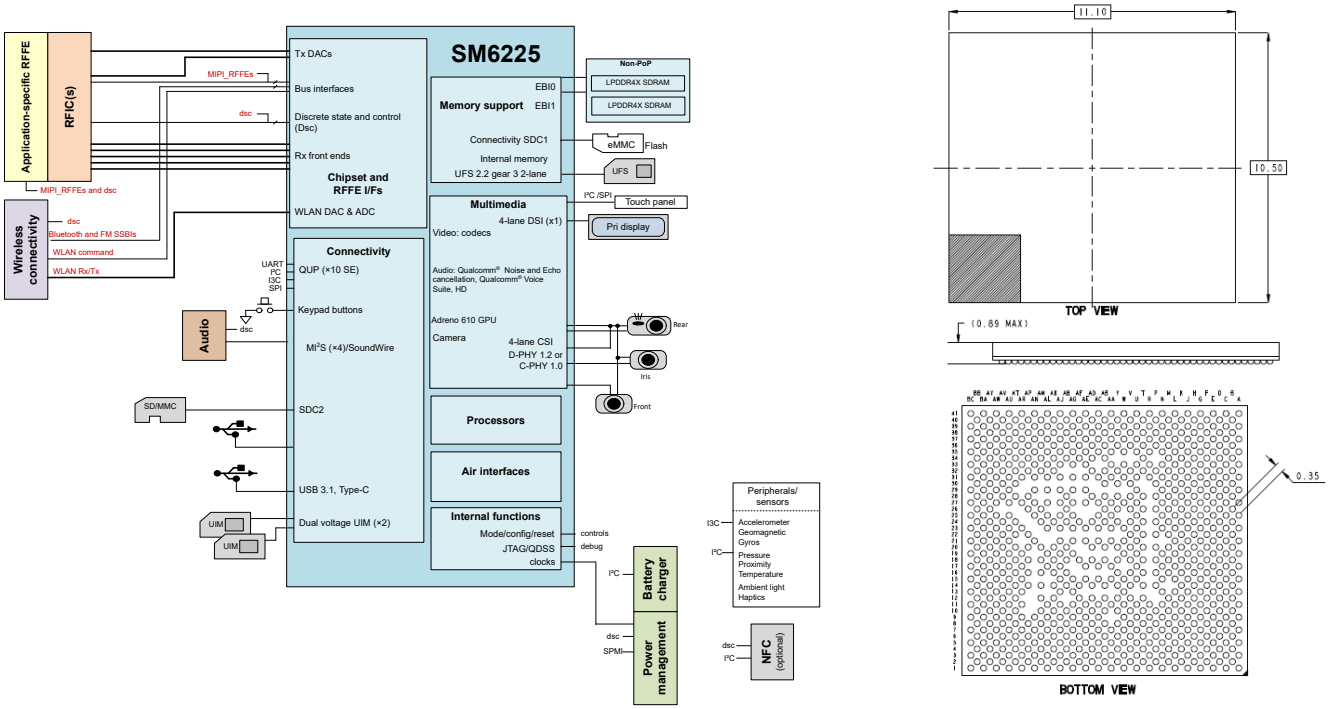
SM6225 includes the following key components:

- Qualcomm® Kryo™ CPU architecture with Quad Cortex-A73 and Quad Cortex-A53, delivering increased speed and sustained performance
- Qualcomm® Adreno™ GPU with 64-bit addressing for vivid games and videos
- Qualcomm® AI Engine powers smarter, more intuitive on-device interactions. Qualcomm® Hexagon™ DSP with dual Vector eXtensions
- Integrated low- power island (LPI) DSP for sensors and audio
- Qualcomm Spectra™ ISP supports up to 64 MP for SM6225-AB and 108 MP for SM6225-AD capture and zero shutter lag, capturing stunning, detailed images with multi-camera support
- Dual-frequency GNSS and India NavIC satellite system provide precise location with up to 6x more accuracy in dense urban areas

Key features

- Low-power audio subsystem combined with the Qualcomm® Aqstic Audio Technologies for reliable voice activation and robust voice call
- Wi-Fi 6-ready to support faster connections and increased battery life, enhanced Bluetooth 5.1 capability, and WPA-3 security
- Display support: FHD+ at 90 Hz for SM6225-AB and 120 Hz for SM6225-AD, four hardware layers, 10-bit end-to-end, Rounded Corner, and Notch Optimization for improve UI performance
- Triple Image Signal Processing (ISP): 13 MP + 13 MP + 5 MP, 16 MP + 16 MP at 30 fps captures all new angles with multi-camera support
- Always-on subsystem with RPM for power management
- Qualcomm Universal Bandwidth Compression (UBWC) with display and GPU
- Support for UFS 2.2 gear3 (two-lane), eMMC 5.1, and SD 3.0

SM6225 high-level block diagram and PSP807 package outline drawing



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1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

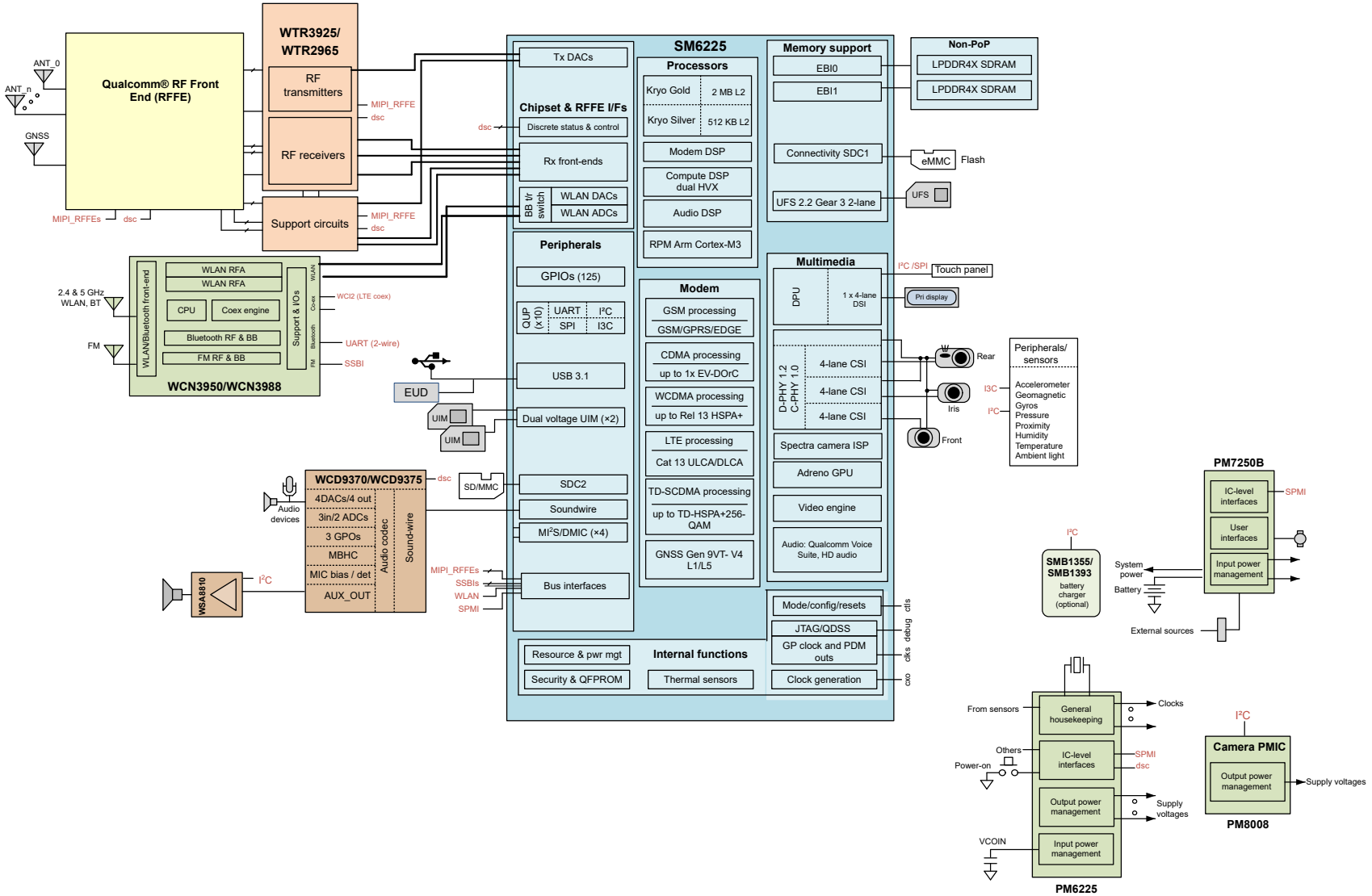


Figure 1-1 SM6225 functional block diagram and example application

1.2 SM6225 features

NOTE Some of the hardware features integrated within the SM6225 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM6225 features.

Table 1-1 SM6225 features

Feature	SM6225 capability
Processors	
Applications	64-bit applications processor (Kryo) ■ Quad high-performance Kryo cores – Gold cluster with 2 MB L2 cache ■ Quad low-power Kryo cores – Silver cluster with 512 KB L2 cache
Digital signal processing	Qualcomm Hexagon DSP with dual HVX
Always-on system	Always-on subsystem with always-on processor power management (RPM) for voltage control and regulation, clock management, and resource communication.
Memory support	
Memory	Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM (2 × 16 bit) at 2133 MHz
Storage	
External Memory	UFS 2.2 gear 3 (two-lane), eMMC 5.1, and SD 3.0
RF support	
RF operating bands	Defined by the RF transceiver device
Air interfaces	See Table 1-2 for variant support.
GSM	Yes
CDMA	Yes
WCDMA	Yes
TD-SCDMA	Yes
LTE	Yes (Cat13 DL, Cat13 UL, up to 256-QAM, 2x CA)
WLAN/Bluetooth	Yes (with WCN3950/WCN3988)
Antenna sharing	No
GNSS: Qualcomm® Location engine	Gen 9 GPS, GLONASS, BeiDou, Galileo, NavIC, and QZSS. QZSS is supported with WTR3925.
Multimedia	
Display support	
MIPI-DSI	1x MIPI DSI-2 v1.0, 4-Lanes D-PHY, Up to 1.5 Gbps/Lane
General display features	■ Up to FHD+ (1080 × 2520), 60 Hz/90 Hz for SM6225-AB and 120 Hz for SM6225-AD, up to 30 bpp ■ 4 layers, QSEED, Picture Adjust, SVI, CABL/FOSS, Q-sync, Rounded Corner
Camera support	
MIPI-CSI	MIPI CSI configurable in 4/4/4 configuration ■ D-PHY: 2.5 Gbps/lane ■ C-PHY: ~10 Gbps (3.42 Gbps/trio on three trios per port)
General camera features	Qualcomm Spectra Image Signal Processor: Triple ISP ■ Triple camera: 13 MP + 13 MP + 5 MP at 30 fps ZSL ■ Dual camera: 25 MP + 5 MP, 16 MP + 16 MP at 30 fps ZSL

Table 1-1 SM6225 features (cont.)

Feature	SM6225 capability
	■ Single camera: 32 MP at 30 fps ZSL ■ 64 MP for SM6225-AB and 108 MP for SM6225-AD non-ZSL
Video support	
Encode	1080p60 8-bit HEVC/H.264/H.265
Decode	1080p60 8-bit HEVC/H.264/H.265/VP9
Concurrency	1080p30 decode + 1080p30 encode
HFR Capture	720p at 120 fps
Graphics support	
Graphics	■ Adreno GPU ■ OpenGL ES 3.2, Vulkan 1.1 ■ OpenCL 2.0
Audio: Integrated Snapdragon Voice Activation WCD9370 codec	
Voice UI	■ Support for two voice activation engines ■ Integrated low power island for voice activation
Low power voice activation	Supported
Low-power audio	Low power; 7.1 surround sound
Voice Codec	■ EVS, EVRC, EVRC-B, EVRC-WB ■ G.711 and G.729A/AB ■ GSM-FR, GSM-EFR, and GSM-HR ■ AMR-NB, AMR-WB
Voice processing	Qualcomm Noise and Echo Cancellation and Qualcomm Voice Suite
Audio Codec support	MP3; AAC; HE AAC v1, v2; FLAC; APE; ALAC; AIFF
Enhanced Audio	DSP-offload for low power audio playback
Sensor support	
Sensors	■ Integrated low power island for sensor ■ QUP (4x in LPI) dedicated for sensors
Connectivity	
Qualcomm universal peripheral (QUP) ports	10 serial engines
UART	UART interface; six on top GPIO and two on LPI GPIO
I^2C	I^2C interface; six on top GPIO for touch, sensors, and NFC; three on LPI GPIO; dedicated controller for each port
I3C	I3C interface; one on top GPIO and two on LPI GPIO
SPI	SPI interfaces; six on top GPIO
CCI I^2C	Two dedicated I^2C interfaces for camera.
UIM	Two – dual voltages (1.8 V and 2.95 V)
USB	USB 3.1 Type-C
Secure digital interfaces	■ 8-bit port SDC1 and 4-bit port SDC2; eMMC5.1 and SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card
Audio interfaces	SLIMbus: WCN BT/FM SLIMbus

Table 1-1 SM6225 features (cont.)

Feature	SM6225 capability
	SWR: SoundWire interface (two Tx and two Rx data lines) for codec Digital Mic: Four DMICs (through four DMIC PDM interfaces) 4x MI^{2}S: ■ Three MI^{2}S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application ■ One MI^{2}S supports four data lanes for up to eight channels Tx/Rx application
Wireless connectivity	WCN3950: WLAN 1 × 1 802.11a/b/g/n/ac, Bluetooth 5.0, and FM WCN3988: WLAN 1 × 1 802.11a/b/g/n/ac, 802.11ax ready, Bluetooth 5.1, and FM
Touchscreen support	Capacitive panels via ext IC (I^{2}C, SPI, and interrupts)
Configurable GPIOs	
Number of GPIO ports	98
Number of LPI GPIO ports	27
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	Secure boot, Secure Debug, Secure Key Provisioning, TrustZone, Qualcomm® Trusted Execution Environment, Hardware Supported KeyStore
Crypto engines	Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), Inline Crypto Engine (FIPS-compliant)
TrustZone services	Secure File System, Fast Trusted Storage
DRM support in hardware	Widevine level 1, CPZ for DSP
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, QDSS, and Embedded USB Debug (EUD)
Others	Thermal sensors, modes and resets, and peripheral subsystem
Chipset interface features	
RF transceivers	WTR3925 and WTR2965 ■ Tx: One diferential I/Q Pair ■ Rx for WTR3925: Four single-ended I/Q pairs (two each for PRx and DRx) ■ Rx for WTR2965: Two single-ended I/Q pairs (one each for PRx and DRx) ■ GNSS Baseband data: One single-ended I/Q Rx pair ■ FBRx: One Single-ended I/Q pair
Power management	PM6225, PM7250B, PM8008
	2-line SPMI; plus other lines, as needed, via GPIOs, I^{2}C
Wireless connectivity	
WLAN Baseband data	I/Q Differential Pair Interface
Bluetooth	UART interface

Table 1-1 SM6225 features (cont.)

Feature	SM6225 capability
Fabrication technology and package	
Non-PoP – small, thermally efficient package	807 PSP: 10.5 mm × 11.1 mm × 0.89 mm; 0.35 mm pitch

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
LTE paired with WTR3925	
Category	Downlink: LTE CAT 13 up to 390 Mbps Uplink: LTE CAT 13 up to 150 Mbps
Carrier aggregation	Downlink: 2x 20 MHz carrier aggregation, 256-QAM Uplink: Contiguous (intra-band) 2x 20 MHz carrier aggregation, 64-QAM
LTE paired with WTR2965	
Category	Downlink: LTE CAT 4 up to 150 Mbps Uplink: LTE CAT 5 up to 75 Mbps
Carrier aggregation	Downlink: 2x 10 MHz, **contiguous (intra-band) only** Uplink: Contiguous (intra-band) carrier aggregation 64-QAM
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	▪ 1x SLTE and 1x SRLTE ▪ hVoLTE and hSRLTE
Multi-SIM	
3G	3G + 3G DSDS (in 3G mode)
4G	4G + 4G DSDS (in 4G mode)
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
CnE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Table 1-3 Position location and navigation summary

Standard	Feature description
Qualcomm® Location Suite with global navigation satellite system (GNSS) support	
Gen 9 VT-V4	L1/L5 (WTR3925) L1 (WTR2965)

Table 1-3 Position location and navigation summary (cont.)

Standard	Feature description
Qualcomm® Location Suite	■ GNSS: Concurrent support for GPS/Glonass/BeiDou/Galileo/QZSS/SBAS. NavIC (IRNSS) with WTR3925. QZSS is supported with WTR3925. ■ Dual-frequency (L1/L5) GNSS with WTR3925 ■ Qualcomm® GNSS Assistance Service (formerly known as XTRA) ■ Standards-based Assisted-GNSS (Control Plane and User Plane, all 3GPP Protocols) ■ Emergency Services (including LPP/LPPe protocols in support of OTDOA, Device-Based Hybrid, Uncompensated Barometric Pressure) ■ Qualcomm® Location Services (Global Terrestrial Positioning for WWAN) on non-GMS devices
Qualcomm® Location Suite Engine	Integrated Gen 9 VT.v4 engine
Qualcomm® Premium Location Suite	Qualcomm® Sensor-Assisted Positioning (INS and PDR) v.4.5

Table 1-4 Wireless connectivity summary by standard

Standard	Feature description
WLAN	
With WCN3988	WLAN 1 × 1 802.11a/b/g/n/ac, 802.11ax ready
With WCN3950	WLAN 1 × 1 802.11a/b/g/n/ac
Bluetooth	
With WCN3988	Bluetooth 5.1
With WCN3950	Bluetooth 5.0
FM	
With WCN3988	Rx, RDS, RBDS
With WCN3950	Rx, RDS, RBDS

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX0	Power for pad group 0
PX1	Power for pad group 1
PX2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX3	Pad group 3 (most peripherals); 1.8 V
PX5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX7	Pad group 7 (eMMC); tied to VDD_PX7 pins (1.8 V only)
PX10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_A_CSI_X_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_A_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SM6225 is available in the PSP807. See Chapter 4 for package details. A high-level view of the pin assignments is shown in the following figure. The text within the figure is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM6225 Pin Assignment and GPIO Configuration Spreadsheet* (80-26896-1A). This Microsoft Excel spreadsheet lists all SM6225 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the pin assignment spreadsheet (80-26896-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-26896-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

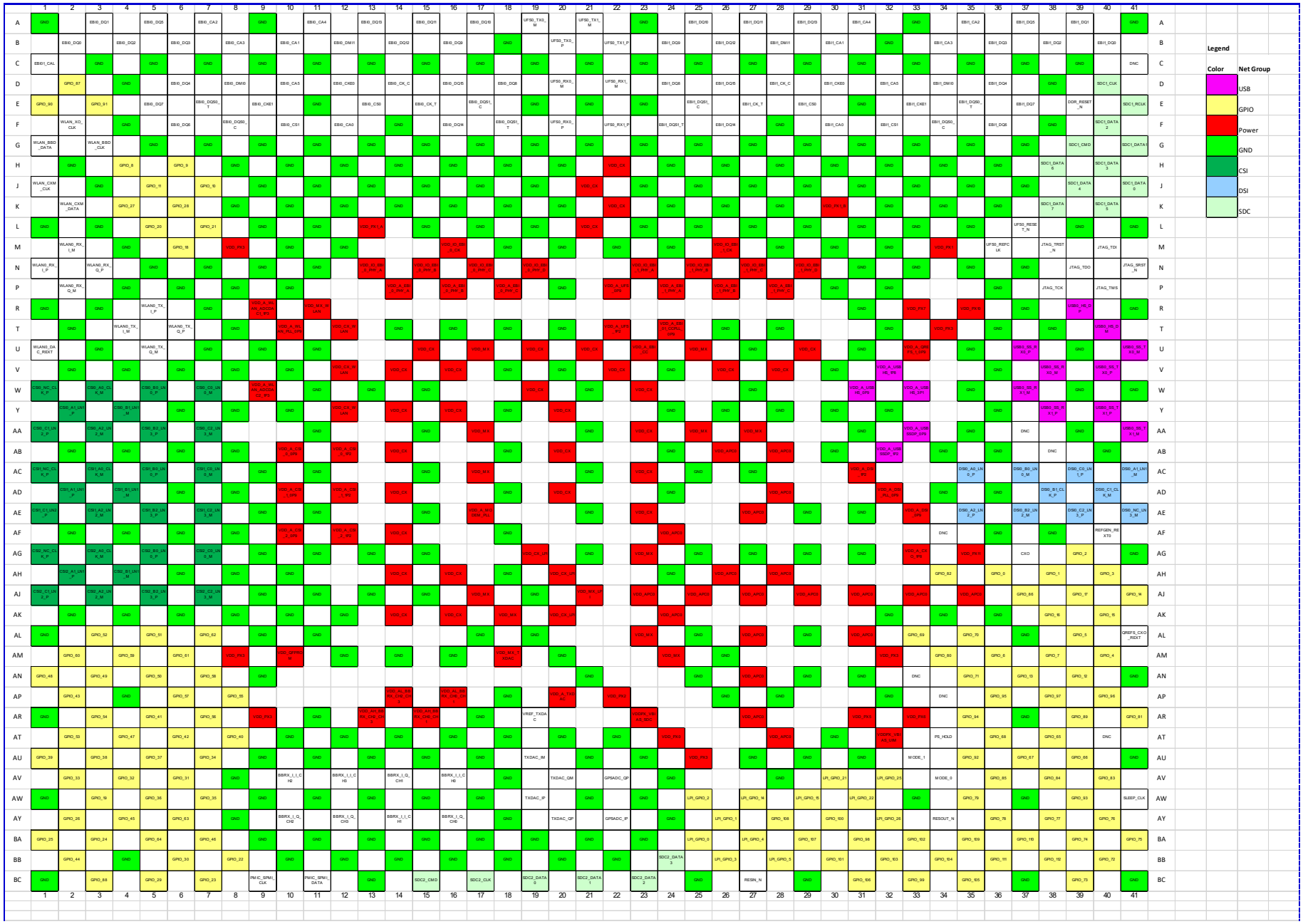


Figure 2-1 SM6225 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AV16	BBRX_I_I_CH0	–	AI	Baseband receiver input, channel 0, in-phase
AY14	BBRX_I_I_CH1	–	AI	Baseband receiver input, channel 1, in-phase
AV10	BBRX_I_I_CH2	–	AI	Baseband receiver input, channel 2, in-phase
AV12	BBRX_I_I_CH3	–	AI	Baseband receiver input, channel 3, in-phase
AY16	BBRX_I_Q_CH0	–	AI	Baseband receiver input, channel 0, quadrature-phase
AV14	BBRX_I_Q_CH1	–	AI	Baseband receiver input, channel 1, quadrature-phase
AY10	BBRX_I_Q_CH2	–	AI	Baseband receiver input, channel 2, quadrature-phase
AY12	BBRX_I_Q_CH3	–	AI	Baseband receiver input, channel 3, quadrature-phase
W3	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock - minus MIPI CSI 0 (CPHY), trio lane 0 – A
Y2	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 - plus MIPI CSI 0 (CPHY), trio lane 1 – A
AA3	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 - minus MIPI CSI 0 (CPHY), trio lane 2 – A
W5	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 - plus MIPI CSI 0 (CPHY), trio lane 0 – B
Y4	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 - minus MIPI CSI 0 (CPHY), trio lane 1 – B
AA5	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 - plus MIPI CSI 0 (CPHY), trio lane 2 – B
W7	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 - minus MIPI CSI 0 (CPHY), trio lane 0 – C
AA1	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 - plus MIPI CSI 0 (CPHY), trio lane 1 – C
AA7	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 - minus MIPI CSI 0 (CPHY), trio lane 2 – C
W1	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – P - plus MIPI CSI 0 (CPHY), no connect
AC3	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock - minus MIPI CSI 1 (CPHY), trio lane 0 – A
AD2	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 - plus MIPI CSI 1 (CPHY), trio lane 1 – A
AE3	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 - minus MIPI CSI 1 (CPHY), trio lane 2 – A
AC5	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 - plus MIPI CSI 1 (CPHY), trio lane 0 – B

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AD4	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 - minus MIPI CSI 1 (CPHY), trio lane 1 – B
AE5	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 - plus MIPI CSI 1 (CPHY), trio lane 2 – B
AC7	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 - minus MIPI CSI 1 (CPHY), trio lane 0 – C
AE1	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 - plus MIPI CSI 1 (CPHY), trio lane 1 – C
AE7	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 - minus MIPI CSI 1 (CPHY), trio lane 2 – C
AC1	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – P - plus MIPI CSI 1 (CPHY), no connect
AG3	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock - minus MIPI CSI 2 (CPHY), trio lane 0 – A
AH2	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 - plus MIPI CSI 2 (CPHY), trio lane 1 – A
AJ3	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 - minus MIPI CSI 2 (CPHY), trio lane 2 – A
AG5	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 - plus MIPI CSI 2 (CPHY), trio lane 0 – B
AH4	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 - minus MIPI CSI 2 (CPHY), trio lane 1 – B
AJ5	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 - plus MIPI CSI 2 (CPHY), trio lane 2 – B
AG7	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 - minus MIPI CSI 2 (CPHY), trio lane 0 – C
AJ1	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 - plus MIPI CSI 2 (CPHY), trio lane 1 – C
AJ7	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 - minus MIPI CSI 2 (CPHY), trio lane 2 – C
AG1	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – P - plus MIPI CSI 2 (CPHY), no connect
AG37	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
E39	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
AC35	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 - plus MIPI DSI 0 (CPHY), trio lane 0 – A
AC41	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 - minus MIPI DSI 0 (CPHY), trio lane 1 – A
AE35	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 - plus MIPI DSI 0 (CPHY), trio lane 2 – A
AC37	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 - minus MIPI DSI 0 (CPHY), trio lane 0 – B
AD38	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – P - plus MIPI DSI 0 (CPHY), trio lane 1 – B
AE37	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 - minus MIPI DSI 0 (CPHY), trio lane 2 – B

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AC39	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 - plus MIPI DSI 0 (CPHY), trio lane 0 – C
AD40	DSI0_C1_CLK_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – M - minus MIPI DSI 0 (CPHY), trio lane 1 – C
AE39	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 - plus MIPI DSI 0 (CPHY), trio lane 2 – C
AE41	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 - minus MIPI DSI 0 (CPHY), no connect
F12	EBI0_CA0	EBI	DO	EBI0 LPDDR4X command/address bit 0
B10	EBI0_CA1	EBI	DO	EBI0 LPDDR4X command/address bit 1
A7	EBI0_CA2	EBI	DO	EBI0 LPDDR4X command/address bit 2
B8	EBI0_CA3	EBI	DO	EBI0 LPDDR4X command/address bit 3
A11	EBI0_CA4	EBI	DO	EBI0 LPDDR4X command/address bit 4
D10	EBI0_CA5	EBI	DO	EBI0 LPDDR4X command/address bit 5
C1	EBI01_CAL	EBI	DO	EBI calibration resistor
D12	EBI0_CKE0	EBI	DO	EBI0 LPDDR4X clock enable 0
E9	EBI0_CKE1	EBI	DO	EBI0 LPDDR4X clock enable 1
D14	EBI0_CK_C	EBI	DO	EBI0 LPDDR4X differential clock - minus
E15	EBI0_CK_T	EBI	DO	EBI0 LPDDR4X differential clock - plus
E13	EBI0_CS0	EBI	DO	EBI0 LPDDR4X chip select 0
F10	EBI0_CS1	EBI	DO	EBI0 LPDDR4X chip select 1
D8	EBI0_DMI0	EBI	B	EBI0 LPDDR4X (and LPDDR5) data mask for byte 0
B12	EBI0_DMI1	EBI	B	EBI0 LPDDR4X (and LPDDR5) data mask for byte 1
B2	EBI0_DQ0	EBI	B	EBI0 LPDDR4X data bit 0
A3	EBI0_DQ1	EBI	B	EBI0 LPDDR4X data bit 1
A17	EBI0_DQ10	EBI	B	EBI0 LPDDR4X data bit 10
A15	EBI0_DQ11	EBI	B	EBI0 LPDDR4X data bit 11
B14	EBI0_DQ12	EBI	B	EBI0 LPDDR4X data bit 12
A13	EBI0_DQ13	EBI	B	EBI0 LPDDR4X data bit 13
F16	EBI0_DQ14	EBI	B	EBI0 LPDDR4X data bit 14
D16	EBI0_DQ15	EBI	B	EBI0 LPDDR4X data bit 15
B4	EBI0_DQ2	EBI	B	EBI0 LPDDR4X data bit 2
B6	EBI0_DQ3	EBI	B	EBI0 LPDDR4X data bit 3
D6	EBI0_DQ4	EBI	B	EBI0 LPDDR4X data bit 4
A5	EBI0_DQ5	EBI	B	EBI0 LPDDR4X data bit 5
F6	EBI0_DQ6	EBI	B	EBI0 LPDDR4X data bit 6
E5	EBI0_DQ7	EBI	B	EBI0 LPDDR4X data bit 7
D18	EBI0_DQ8	EBI	B	EBI0 LPDDR4X data bit 8

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B16	EBI0_DQ9	EBI	B	EBI0 LPDDR4X data bit 9
F8	EBI0_DQS0_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 - minus
E7	EBI0_DQS0_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 - plus
E17	EBI0_DQS1_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 - minus
F18	EBI0_DQS1_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 - plus
F30	EBI1_CA0	EBI	DO	EBI1 LPDDR4X command/address bit 0
B30	EBI1_CA1	EBI	DO	EBI1 LPDDR4X command/address bit 1
A35	EBI1_CA2	EBI	DO	EBI1 LPDDR4X command/address bit 2
B34	EBI1_CA3	EBI	DO	EBI1 LPDDR4X command/address bit 3
A31	EBI1_CA4	EBI	DO	EBI1 LPDDR4X command/address bit 4
D32	EBI1_CA5	EBI	DO	EBI1 LPDDR4X command/address bit 5
D30	EBI1_CKE0	EBI	DO	EBI1 LPDDR4X clock enable 0
E33	EBI1_CKE1	EBI	DO	EBI1 LPDDR4X clock enable 1
D28	EBI1_CK_C	EBI	DO	EBI1 LPDDR4X differential clock - minus
E27	EBI1_CK_T	EBI	DO	EBI1 LPDDR4X differential clock - plus
E29	EBI1_CS0	EBI	DO	EBI1 LPDDR4X chip select 0
F32	EBI1_CS1	EBI	DO	EBI1 LPDDR4X chip select 1
D34	EBI1_DMI0	EBI	B	EBI1 LPDDR4X (and LPDDR5) data mask for byte 0
B28	EBI1_DMI1	EBI	B	EBI1 LPDDR4X (and LPDDR5) data mask for byte 1
B40	EBI1_DQ0	EBI	B	EBI1 LPDDR4X data bit 0
A39	EBI1_DQ1	EBI	B	EBI1 LPDDR4X data bit 1
A25	EBI1_DQ10	EBI	B	EBI1 LPDDR4X data bit 10
A27	EBI1_DQ11	EBI	B	EBI1 LPDDR4X data bit 11
B26	EBI1_DQ12	EBI	B	EBI1 LPDDR4X data bit 12
A29	EBI1_DQ13	EBI	B	EBI1 LPDDR4X data bit 13
F26	EBI1_DQ14	EBI	B	EBI1 LPDDR4X data bit 14
D26	EBI1_DQ15	EBI	B	EBI1 LPDDR4X data bit 15
B38	EBI1_DQ2	EBI	B	EBI1 LPDDR4X data bit 2
B36	EBI1_DQ3	EBI	B	EBI1 LPDDR4X data bit 3
D36	EBI1_DQ4	EBI	B	EBI1 LPDDR4X data bit 4
A37	EBI1_DQ5	EBI	B	EBI1 LPDDR4X data bit 5
F36	EBI1_DQ6	EBI	B	EBI1 LPDDR4X data bit 6
E37	EBI1_DQ7	EBI	B	EBI1 LPDDR4X data bit 7
D24	EBI1_DQ8	EBI	B	EBI1 LPDDR4X data bit 8

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B24	EBI1_DQ9	EBI	B	EBI1 LPDDR4X data bit 9
F34	EBI1_DQS0_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 - minus
E35	EBI1_DQS0_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 - plus
E25	EBI1_DQS1_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 - minus
F24	EBI1_DQS1_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 - plus
AY22	GPSADC_IP	PX_3	AI	GPS receive ADC input, in-phase
AV22	GPSADC_QP	PX_3	AI	GPS receive ADC input, quadrature phase
AV34	MODE_0	PX_3	DI	Mode control bit 0 – unconnected for native mode
AU33	MODE_1	PX_3	DI	Mode control bit 1 – unconnected for native mode
BC9	PMIC_SPMI_CLK	PX_0	B	Slave and PBUS interface for PMICs – clock
BC11	PMIC_SPMI_DATA	PX_0	B	Slave and PBUS interface for PMICs – data
AT34	PS_HOLD	PX_3	Z	Power-supply hold signal to PMIC
AL41	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-die clocking
AF40	REFGEN_REXT0		AI, AO	[Insert direction]-side high-speed interface – external resistor
BC27	RESIN_N	PX_0	DI	Reset input
AY34	RESOUT_N	PX_3	DO	Reset output
D40	SDC1_CLK	PX_7	B	Secure digital controller 1 clock
G39	SDC1_CMD	PX_7	B	Secure digital controller 1 command
J41	SDC1_DATA0	PX_7	B	Secure digital controller 1 data bit 0
G41	SDC1_DATA1	PX_7	B	Secure digital controller 1 data bit 1
F40	SDC1_DATA2	PX_7	B	Secure digital controller 1 data bit 2
H40	SDC1_DATA3	PX_7	B	Secure digital controller 1 data bit 3
J39	SDC1_DATA4	PX_7	B	Secure digital controller 1 data bit 4
K40	SDC1_DATA5	PX_7	B	Secure digital controller 1 data bit 5
H38	SDC1_DATA6	PX_7	B	Secure digital controller 1 data bit 6
K38	SDC1_DATA7	PX_7	B	Secure digital controller 1 data bit 7
E41	SDC1_RCLK	PX_7	B	Secure digital controller 1 return clock
BC17	SDC2_CLK	PX_2	B	Secure digital controller 2 clock
BC15	SDC2_CMD	PX_2	B	Secure digital controller 2 command
BC19	SDC2_DATA0	PX_2	B	Secure digital controller 2 data bit 0
BC21	SDC2_DATA1	PX_2	B	Secure digital controller 2 data bit 1
BC23	SDC2_DATA2	PX_2	B	Secure digital controller 2 data bit 2
BB24	SDC2_DATA3	PX_2	B	Secure digital controller 2 data bit 3

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AW41	SLEEP_CLK	PX_3	DI	Sleep clock
N41	JTAG_SRST_N	PX_3	DI	JTAG reset for debug
P38	JTAG_TCK	PX_3	DI	JTAG clock input
M40	JTAG_TDI	PX_3	DI	JTAG data input
N39	JTAG_TDO	PX_3	Z	JTAG data output
P40	JTAG_TMS	PX_3	B	JTAG mode select input
M38	JTAG_TRST_N	PX_3	DI	JTAG reset
AU19	TXDAC_IM	–	AO	TXDAC in-phase – minus
AW19	TXDAC_IP	–	AO	TXDAC in-phase – plus
AV20	TXDAC_QM	–	AO	TXDAC quadrature-phase – minus
AY20	TXDAC_QP	–	AO	TXDAC quadrature-phase – plus
D20	UFS0_RX0_M	–	AI	UFS receive lane 0 - minus
F20	UFS0_RX0_P	–	AI	UFS receive lane 0 - plus
A19	UFS0_TX0_M	–	AO	UFS transmit lane 0 - minus
B20	UFS0_TX0_P	–	AO	UFS transmit lane 0 - plus
D22	UFS0_RX1_M	–	AI	UFS receive lane 1 - minus
F22	UFS0_RX1_P	–	AI	UFS receive lane 1 - plus
A21	UFS0_TX1_M	–	AO	UFS transmit lane 1 - minus
B22	UFS0_TX1_P	–	AO	UFS transmit lane 1 - plus
M36	UFS0_REFCLK	PX_10	DO	UFS reference clock
L37	UFS0_RESET_N	PX_10	DO	UFS reset
T40	USB0_HS_DM	–	AI, AO	USB 0 high-speed data - minus
R39	USB0_HS_DP	–	AI, AO	USB 0 high-speed data - plus
V38	USB0_SS_RX0_M	–	AI	USB super-speed receive 0 - minus
U37	USB0_SS_RX0_P	–	AI	USB super-speed receive 0 - plus
W37	USB0_SS_RX1_M	–	AI	USB super-speed receive 0 - minus
Y38	USB0_SS_RX1_P	–	AI	USB super-speed receive 0 - plus
U41	USB0_SS_TX0_M	–	AO	USB super-speed transmit 0 - minus
V40	USB0_SS_TX0_P	–	AO	USB super-speed transmit 0 - plus
AA41	USB0_SS_TX1_M	–	AO	USB super-speed transmit 0 - minus
Y40	USB0_SS_TX1_P	–	AO	USB super-speed transmit 0 - plus
AR19	VREF_TXDAC	–	AI, AO	Transmitter DAC voltage reference
U1	WLAN0_DAC_REXT	–	AI, AO	WLAN chain 0 external resistor
G3	WLAN_BBD_CLK	–	DO	WLAN baseband command clock
G1	WLAN_BBD_DATA	–	B	WLAN baseband command data
J1	WLAN_CXM_CLK	–	DO	WLAN coexistence module command clock
K2	WLAN_CXM_DATA	–	B	WLAN coexistence module command data

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
M2	WLAN0_RX_I_M	–	AI	WLAN receive in-phase – minus
N1	WLAN0_RX_I_P	–	AI	WLAN receive in-phase – plus
P2	WLAN0_RX_Q_M	–	AI	WLAN receive quadrature – minus
N3	WLAN0_RX_Q_P	–	AI	WLAN receive quadrature – plus
T4	WLAN0_TX_I_M	–	AO	WLAN transmit in-phase – minus
R5	WLAN0_TX_I_P	–	AO	WLAN transmit in-phase – plus
U5	WLAN0_TX_Q_M	–	AO	WLAN transmit quadrature – minus
T6	WLAN0_TX_Q_P	–	AO	WLAN transmit quadrature – plus
F2	WLAN_XO_CLK	–	DI	WLAN reference clock

[a] See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function - carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM6225 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the pin assignment spreadsheet (80-26896-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-26896-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
AH36	GPIO_0	–	Y		PX_3	B PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE0, lane 0: I2C_SDA
				I3C_SDA		B	QUP 0 SE0, lane 0: I3C_SDA
				QDSS_GPIO_TRACEDATA_LOCB[8]		DO	QDSS trace data bit 8 B
AH38	GPIO_1	–	–		PX_3	B- PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE0, lane 1: I2C_SCL
				I3C_SCL		DO	QUP 0 SE0, lane 1: I3C_SCL
				QDSS_GPIO_TRACEDATA_LOCB[9]		DO	QDSS trace data bit 9 B
AG39	GPIO_2	–	–		PX_3	B- PD:nppukp	Configurable I/O
				SPI_SCLK		DO	QUP 0 SE0, lane 2: SPI_SCLK
				UART_TX		DO	QUP 0 SE0, lane 2: UART_TX
				QDSS_GPIO_TRACEDATA_LOCB[10]		DO	QDSS trace data bit 10 B
AH40	GPIO_3	–	Y		PX_3	B- PD:nppukp	Configurable I/O
				SPI_CS_N_0		DO	QUP 0 SE0, lane 3:SPI_CS_N
				UART_RX		DI	QUP 0 SE0, lane 3: UART_RX
				QDSS_GPIO_TRACEDATA_LOCB[11]		DO	QDSS trace data bit 11 B
AM40	GPIO_4	–	Y		PX_3	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE1, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE1, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE1, lane 0: I2C_SDA

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
AL39	GPIO_5	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE1, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE1, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE1, lane 1: I2C_SCL
AM36	GPIO_6	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE2, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE2, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE2, lane 0: I2C_SDA
AM38	GPIO_7	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE2, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE2, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE2, lane 1: I2C_SCL
H4	GPIO_8	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE3, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE3, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE3, lane 0: I2C_SDA
				QDSS_GPIO_TRACECLK_LOCA		DO	QDSS trace clock
H6	GPIO_9	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE3, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE3, lane1: UART_RFR
				I2C_SCL		DO	QUP 0 SE3, lane1: I2C_SCL
				QDSS_GPIO_TRACECTL_LOCA		DO	QDSS trace control A
J7	GPIO_10	–	–		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				SPI_SCLK		DO	QUP 0 SE3, lane 2: SPI_SCLK
				UART_TX		DO	QUP 0 SE3, lane 2: UART_TX
				QDSS_GPIO_TRACEDATA_LOCA[0]		DO	QDSS trace data bit 0 A
J5	GPIO_11	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_CS_N		DO	QUP 0 SE3, lane 3: SPI_CS_N
				UART_RX		DI	QUP 0 SE3, lane 3: UART_RX
				QDSS_GPIO_TRACEDATA_LOCA[1]		DO	QDSS trace data bit 1 A
AN39	GPIO_12	–	–		PX_3	B-PD:nppukp	Configurable I/O
				UART_TX		B	QUP 0 SE4, lane 2: UART_TX
				SPI_SCLK		DO	QUP 0 SE4, lane 2: SPI_SCLK
AN37	GPIO_13	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				UART_RX		B	QUP 0 SE4, lane 3: UART_RX
				SPI_CS_N		DO	QUP 0 SE4, lane 3: SPI_CS_N
AJ41	GPIO_14	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE5, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE5, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE5, lane 0: I2C_SDA
				QDSS_GPIO_TRACEDATA_LOCB[4]		DO	QDSS trace data bit 4B
AK40	GPIO_15	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE5, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE5, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE5, lane1: I2C_SCL
				QDSS_GPIO_TRACEDATA_LOCB[5]		DO	QDSS trace data bit 5 B

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
AK38	GPIO_16	–	–		PX_3	B-PD:nppukp	Configurable I/O
				UART_TX		B	QUP 0 SE5, lane 2: UART_TX
				SPI_SCLK		DO	QUP 0 SE5, lane 2: SPI_SCLK
				QDSS_GPIO_TRACEDATA_LOCB[6]		DO	QDSS trace data bit 6 B
AJ39	GPIO_17	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				UART_RX		B	QUP 0 SE5, lane 3: UART_RX
				SPI_CS_N		DO	QUP 0 SE5, lane 3: SPI_CS_N
				QDSS_GPIO_TRACEDATA_LOCB[7]		DO	QDSS trace data bit 7 B
M6	GPIO_18	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCA[2]		DO	QDSS trace data bit 2 A
AW3	GPIO_19	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCA[3]		DO	QDSS trace data bit 3 A
L5	GPIO_20	–	–		PX_3	B-PD:nppukp	Configurable I/O
				CAM_MCLK0		DO	Camera master clock 0
				QDSS_GPIO_TRACEDATA_LOCA[4]		DO	QDSS trace data bit 4 A
L7	GPIO_21	–	–		PX_3	B-PD:nppukp	Configurable I/O
				CAM_MCLK1		DO	Camera master clock 1
				QDSS_GPIO_TRACEDATA_LOCA[5]		DO	QDSS trace data bit 5 A
BB8	GPIO_22	–	–		PX_3	B-PD:nppukp	Configurable I/O
				CCI_I2C_SDA0		B	Dedicated camera control interface I2C 0 serial data
				QDSS_GPIO_TRACEDATA_LOCA[6]		DO	QDSS trace data bit 6 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
BC7	GPIO_23	–	–		PX_3	B-PD:nppukp	Configurable I/O
				CCI_I2C_SCL0		DO	Dedicated camera control interface I2C 0 clock
				QDSS_GPIO_TRACEDATA_LOCA[7]		DO	QDSS trace data bit 7 A
BA3	GPIO_24	–	Y		PX_3	B-PD:nppukp	
				CCI_TIMER1		DO	Camera control interface timer 1
				GCC_GP1_CLK_MIRA		DO	Global general-purpose clock 1
				QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data bit 8 A
BA1	GPIO_25	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				CCI_ASYNC_IN0		DI	Camera control interface async 0
				CCI_TIMER0		DO	Camera control interface timer 0
				QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data bit 9 A
AY2	GPIO_26	–	–		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCA[10]		DO	QDSS trace data bit 10 A
K4	GPIO_27	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				CAM_MCLK2		DO	Camera master clock 2
				QDSS_CTI_TRIG0_IN_MIRB		DI	QDSS trigger input 0 B
K6	GPIO_28	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				CAM_MCLK3		DO	Camera master clock 3
				CCI_TIMER2		DO	Camera control interface timer 2
				QDSS_CTI_TRIG0_OUT_MIRB		DO	QDSS trigger output 0 B
BC5	GPIO_29	–	–		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				CCI_I2C_SDA1		B	Dedicated camera control interface I2C 1 serial data
BB6	GPIO_30	–	–		PX_3	B-PD:nppukp	Configurable I/O
				CCI_I2C_SCL1		DO	Dedicated camera control interface I2C 1 clock
AV6	GPIO_31	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				GP_PDM_MIRB[0]		B	General-purpose PDM_Mirror_B 0
AV4	GPIO_32	Y	Y		PX_3	B-PD:nppukp DO	Configurable I/O
				CCI_TIMER3		DO	Camera control interface timer 3
				GP_PDM_MIRB[1]		B	General-purpose PDM_Mirror_B 1
AV2	GPIO_33	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				GP_PDM_MIRB[2]		B	General-purpose PDM_Mirror_B 2
AU7	GPIO_34	Y	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AW7	GPIO_35	Y	Y	QDSS_GPIO_TRACEDATA_LOCA[14]	PX_3	B-PD:nppukp	Configurable I/O
AW5	GPIO_36	Y	Y	QDSS_GPIO_TRACEDATA_LOCA[15]	PX_3	B-PD:nppukp	Configurable I/O
AU5	GPIO_37	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC0		DO	Generic RF controller bit 0
AU3	GPIO_38	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC1		DO	Generic RF controller bit 1
AU1	GPIO_39	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				GRFC2		DO	Generic RF controller bit 2

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
AT8	GPIO_40	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC3		DO	Generic RF controller bit 3
AR5	GPIO_41	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC4		DO	Generic RF controller bit 4
AT6	GPIO_42	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC5		DO	Generic RF controller bit 5
				NAV_GPIO_1_MIRA		B	Generic I/O for GNSS
AP2	GPIO_43	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC6		DO	Generic RF controller bit 6
				BOOT_CONFIG[8]		DI	Boot configuration control bit 8
BB2	GPIO_44	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC7		DO	Generic RF controller bit 7
				BOOT_CONFIG[9]		DI	Boot configuration control bit 9
AY4	GPIO_45	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC8		DO	Generic RF controller bit 8
				BOOT_CONFIG[10]		DI	Boot configuration control bit 10
BA7	GPIO_46	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				GRFC9		DO	Generic RF controller bit 9
				BOOT_CONFIG[11]		DI	Boot configuration control bit 11
AT4	GPIO_47	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC10		DO	Generic RF controller bit 10
				NAV_GPIO_0_MIRA		B	Generic I/O for GNSS

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
AN1	GPIO_48	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC11		DO	Generic RF controller bit 11
				BOOT_CONFIG[0]		DI	Boot configuration control bit 0
AN3	GPIO_49	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC12		DO	Generic RF controller bit 12
				PA_INDICATOR_OR		DO	PA transmit indicator
AN5	GPIO_50	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC13		DO	Generic RF controller bit 13
				BOOT_CONFIG[1]		DI	Boot configuration control bit 1
AL5	GPIO_51	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC14		DO	Generic RF controller bit 14
				BOOT_CONFIG[2]		DI	Boot configuration control bit 2
AL3	GPIO_52	–	–		PX_3	B-PD:nppukp	Configurable I/O
				GRFC15		DO	Generic RF controller bit 15
				NAV_GPIO_2_MIRA		B	Generic I/O for GNSS
AT2	GPIO_53	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE1_DATA		B	RF front-end 1 interface data
				GSM1_TX_PHASE_D		B	GSM 1 transmit phase adjust data bit
				BOOT_CONFIG[3]		DI	Boot configuration control bit 3
AR3	GPIO_54	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE1_CLK		Z	RF front-end 1 interface clock
AP8	GPIO_55	–	–		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				RFFE2_DATA		B	RF front-end 2 interface data
				BOOT_CONFIG[4]		DI	Boot configuration control bit 4
AR7	GPIO_56	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE2_CLK		Z	RF front-end 2 interface clock
AP6	GPIO_57	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE3_DATA		B	RF front-end 3 interface data
				BOOT_CONFIG[5]		DI	Boot configuration control bit 5
AN7	GPIO_58	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE3_CLK		Z	RF front-end 3 interface clock
AM4	GPIO_59	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE4_DATA		B	RF front-end 4 interface data
				SSBI_WTR1_TX		B	Single serial bus interface transmiter
				BOOT_CONFIG[6]		DI	Boot configuration control bit 6
AM2	GPIO_60	–	–		PX_3	B-PD:nppukp	Configurable I/O
				RFFE4_CLK		Z	RF front-end 4 interface clock
				SSBI_WTR1_RX		B	Single serial bus interface receiver
AM6	GPIO_61	–	–		PX_3	B-PD:nppukp B	Configurable I/O
				RFFE5_DATA		B	RF front-end 5 interface data
				BOOT_CONFIG[7]		DI	Boot configuration control bit 7
AL7	GPIO_62	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				RFFE5_CLK		DO-Z	RF front-end 5 interface clock
AY6	GPIO_63	–	Y	–	PX_3	PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
BA5	GPIO_64	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				GSM0_TX_PHASE_D		B	GSM 0 transmit phase adjust data bit
AT38	GPIO_65	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AU39	GPIO_66	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AU37	GPIO_67	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AT36	GPIO_68	–	–	–	PX_3	B-PD:nppukp	Configurable I/O
AL33	GPIO_69	–	Y		PX_3	B-PU:nppukp	Configurable I/O
				SPI_SCLK		DO	QUP 0 SE1, lane 2: SPI_SCLK
				UART_TX		DO	QUP 0 SE1, lane 2: UART_TX
				GCC_GP2_CLK_MIRA		DO	Global general purpose clock 2 A
				QDSS_GPIO_TRACEDATA_LOCB[12]		DO	QDSS trace data bit 12 B
AL35	GPIO_70	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_CS_N		DO	QUP 0 SE1, lane 3: SPI_CS_N
				UART_RX		DO	QUP 0 SE1, lane 3: UART_RX
				GCC_GP3_CLK_MIRA		DO	Global general purpose clock 3 A
				QDSS_GPIO_TRACEDATA_LOCB[13]		DO	QDSS trace data bit 13 B
AN35	GPIO_71	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_SCLK		DO	QUP 0 SE2, lane 2: SPI_SCLK
				UART_TX		DO	QUP 0 SE 2, lane 2: UART_TX
BB40	GPIO_72	–	Y		PX_6	B-PD:nppukp	Configurable I/O
				UIM2_DATA		DO	UIM2 data (dual voltage)

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				QDSS_CTI_TRIG1_IN_MIRB		DI	QDSS trigger input 1 B
BC39	GPIO_73	–	–		PX_6	B-PD:nppukp	Configurable I/O
				UIM2_CLK		DO	UIM2 clock (dual voltage)
				QDSS_CTI_TRIG1_OUT_MIRB		DO	QDSS trigger output 1 B
BA39	GPIO_74	–	–		PX_6	B-PD:nppukp	Configurable I/O
				UIM2_RESET		DO	UIM2 reset (dual voltage)
BA41	GPIO_75	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				UIM2_PRESENT		DI	UIM2 presence detection
AY40	GPIO_76	–	–		PX_5	B-PD:nppukp	Configurable I/O
				UIM1_DATA		DO	UIM1 data (dual voltage)
AY38	GPIO_77	–	–		PX_5	B-PD:nppukp	Configurable I/O
				UIM1_CLK		DO	UIM1 clock (dual voltage)
AY36	GPIO_78	–	–		PX_5	B-PD:nppukp	Configurable I/O
				UIM1_RESET		DO	UIM1 reset (dual voltage)
AW35	GPIO_79	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				UIM1_PRESENT		DI	UIM1 presence detection
AM34	GPIO_80	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_CS_N		DO	QUP 0 SE2, lane 3: SPI_CS_N
				UART_RX		DI	QUP 0 SE2, lane 3: UART_RX
AR41	GPIO_81	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				MDP_VSYNC_OUT_0		DO	MDP vertical sync – output 0

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				MDP_VSYNC_OUT_1		DO	MDP vertical sync – output 1
				MDP_VSYNC_P		DI	MDP vertical sync – primary
AH34	GPIO_82	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_CS_N_1		DO	QUP 0 SE0, lane 4: SPI_CS_N_1
AV40	GPIO_83	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AV38	GPIO_84	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AV36	GPIO_85	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AJ37	GPIO_86	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SPI_CS_N_2		DO	QUP 0 SE0, lane 5: SPI_CS_N_2
				GCC_GP1_CLK_MIRB		DO	Global general purpose clock 1 B
D2	GPIO_87	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCA[11]		DO	QDSS trace data bit 11 A
BC3	GPIO_88	–	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AR39	GPIO_89	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				USB_PHY_PS		DI	USB PHY port select
E1	GPIO_90	–	–		PX_3	B-PD:nppukp	Configurable I/O
				MSS_LTE_COXM_TXD		DO	UART Tx for LTE coex
				QDSS_GPIO_TRACEDATA_LOCA[12]		DO	QDSS trace data bit 12 A
E3	GPIO_91	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				MSS_LTE_COXM_RXD		DI	UART Rx for LTE coex

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				QDSS_GPIO_TRACEDATA_LOCA[13]		DO	QDSS trace data bit 13 A
AU35	GPIO_92	–	–	–	PX_3	B-PD:nppukp	Configurable I/O
AW39	GPIO_93	Y	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AR35	GPIO_94	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				GP_MN		DO	General-purpose M/N: D counter output
				QDSS_GPIO_TRACEDATA_LOCB[14]		DO	QDSS trace data bit 14 A
				FORCED_USB_BOOT_POL_SEL		DI	Forced USB boot polarity select
AP36	GPIO_95	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				NAV_GPIO_0_MIRC		B	Generic I/O for GNSS
				GP_PDM_MIRA[0]		B	General-purpose PDM_Mirror_A 0
				QDSS_GPIO_TRACEDATA_LOCB[15]		DO	QDSS trace data bit 15 A
				FORCED_USB_BOOT		DI	Forced USB boot
AP40	GPIO_96	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE4, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE4, lane 0: UART_CTS
				I2C_SDA		DI	QUP 0 SE4, lane 0: I2C_SDA
				NAV_GPIO_1_MIRC		B	Generic I/O for GNSS
				MDP_VSYNC_E		DI	MDP vertical sync – external
				GP_PDM_MIRA[1]		B	General-purpose PDM_Mirror_A 1
				SD_WRITE_PROTECT		DI	SD card write protect
				QDSS_CTI_TRIG0_IN_MIRA		DI	QDSS trigger input 0 A
				QDSS_CTI_TRIG1_OUT_MIRA		DO	QDSS trigger output 1 A
AP38	GPIO_97	Y	Y		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				SPI_MOSI		DO	QUP 0 SE4, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE4, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE4, lane1: I2C_SCL
				NAV_GPIO_2_MIRC		B	Generic I/O for GNSS
				MDP_VSYNC_S		DI	MDP vertical sync – secondary
				GP_PDM_MIRA[2]		B	General-purpose PDM_Mirror_A 2
				QDSS_CTI_TRIG0_OUT_MIRA		DO	QDSS trigger output 0 A
				QDSS_CTI_TRIG1_IN_MIRA		DI	QDSS trigger input 1 A
BA31	GPIO_98	–	–		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_6:LPI_DMIC1_CLK		DO	LPI_Digital MIC 1 clock
				LPI_GPIO_6:LPI_MI2S1_CLK		DO	LPI_MI2S 1 clock
BC33	GPIO_99	–	Y		PX_3	B-PD:nppukp DI	Configurable I/O
				LPI_GPIO_7:LPI_DMIC1_DATA		DI	LPI_Digital MIC 1 data
				LPI_GPIO_7:LPI_MI2S1_WS		B	LPI_MI2S 1 word select
AY30	GPIO_100	–	–		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_8:LPI_DMIC2_CLK		DO	LPI_Digital MIC 2 clock
				LPI_GPIO_8:LPI_MI2S1_DATA0		B	LPI_MI2S 1 data 0
BB30	GPIO_101	–	–		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_9:LPI_DMIC2_DATA		DI	LPI_Digital MIC 2 data
				LPI_GPIO_9:LPI_MI2S1_DATA1		B	LPI_MI2S 1 data 1
				LPI_GPIO_9:MI2S_MCLK1_B		B	Master Clock 1 B
BA33	GPIO_102	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_10:LPI_MI2S2_CLK		B	LPI_MI2S 2 clock

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
BB32	GPIO_103	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_11:LPI_MI2S2_WS		B	LPI_MI2S 2 word select
BB34	GPIO_104	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCB[1]		DO	QDSS trace data bit 1 B
				LPI_GPIO_12:LPI_MI2S2_DATA0		B	LPI_MI2S 2 data 0
BC35	GPIO_105	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACECLK_LOCB		DO	QDSS trace clock B
				LPI_GPIO_13:LPI_MI2S2_DATA1		B	LPI_MI2S 2 data 1
				LPI_GPIO_13:MI2S_MCLK0_A		B	MI2S Master clock 0 A
BC31	GPIO_106	–	Y		PX_3	B-PD:nppukp	Configurable I/O
				NAV_GPIO_0_MIRB		B	Generic I/O for GNSS
				GCC_GP3_CLK_MIRB		DO	Global general purpose clock 3 B
				QDSS_GPIO_TRACECTL_LOCB		DO	QDSS trace control B
				LPI_GPIO_16:LPI_MI2S3_DATA0		B	LPI_MI2S 3 data 0
BA29	GPIO_107	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				NAV_GPIO_1_MIRB		B	Generic I/O for GNSS
				GCC_GP2_CLK_MIRB		DO	Global general purpose clock 2 B
				QDSS_GPIO_TRACEDATA_LOCB[0]		DO	QDSS trace data bit 0 B
				LPI_GPIO_17:LPI_MI2S3_DATA1		B	LPI_MI2S 3 data 1
				LPI_GPIO_17:MI2S_MCLK1_C		B	MI2S Master clock 1 C
AY28	GPIO_108	–	–		PX_3	B-PD:nppukp	Configurable I/O
				NAV_GPIO_2_MIRB		B	Generic I/O for GNSS
				LPI_GPIO_18:MI2S_MCLK1_A		B	MI2S Master clock 1 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				LPI_GPIO_18:SWR_TX_DATA2		B	SoundWire transmit data 2
BA35	GPIO_109	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCB[2]		DO	QDSS trace data bit 2 B
				LPI_GPIO_19:I2C_SDA		B	LPI_ QUP 0 SE0, lane 0: I2C_SDA
				LPI_GPIO_19:I3C_SDA		B	LPI_ QUP 0 SE0, lane 0: I3C_SDA
BA37	GPIO_110	–	–		PX_3	B-PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACEDATA_LOCB[3]		DO	QDSS trace data bit 3 B
				LPI_GPIO_20:I2C_SCL		DO	LPI_ QUP 0 SE0, lane 1: I2C_SCL
				LPI_GPIO_20:I3C_SCL		DO	LPI_ QUP 0 SE0, lane 1: I3C_SCL
BB36	GPIO_111	–	–		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_23:I2C_SDA		B	LPI_QUP 0 SE5, lane 0: I2C_SDA
				LPI_GPIO_23:UART_TX		DO	LPI_ QUP 0 SE5, lane 2: UART_TX
BB38	GPIO_112	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				LPI_GPIO_24:I2C_SCL		DO	LPI_ QUP 0 SE5, lane1: I2C_SCL
				LPI_GPIO_24:UART_RX		DI	LPI_ QUP 0 SE5, lane 3: UART_RX
BA25	LPI_GPIO_0	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SWR_TX_CLK		DO	SoundWire transmit clock
				LPI_QUA_MI2S_SCK		B	LPI_QUA_MI2S clock
AY26	LPI_GPIO_1	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				SWR_TX_DATA0		B	SoundWire transmit data 0
				LPI_QUA_MI2S_WS		B	LPI_QUA_MI2S word select
AW25	LPI_GPIO_2	–	–		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				SWR_TX_DATA1		B	SoundWire transmit data 1
				LPI_QUA_MI2S_DATA0		B	LPI_QUA_MI2S data 0
BB26	LPI_GPIO_3	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SWR_RX_CLK		DO	SoundWire receive clock
				LPI_QUA_MI2S_DATA1		B	LPI_QUA_MI2S data 1
BA27	LPI_GPIO_4	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				SWR_RX_DATA0		B	SoundWire receive data 0
				LPI_QUA_MI2S_DATA2		B	LPI_QUA_MI2S Data 2
BB28	LPI_GPIO_5	–	–		PX_3	B-PD:nppukp	Configurable I/O
				SWR_RX_DATA1		B	SoundWire receive data 1
				MI2S_MCLK0_B		B	MI2S Master clock 0 B
				LPI_QUA_MI2S_DATA3		B	LPI_QUA_MI2S data 3
AW27	LPI_GPIO_14	–	–		PX_3	B-PD:nppukp	Configurable I/O
				LPI_MI2S3_CLK		B	LPI_MI2S 3 clock
				BTFM_SLIMBUS_CLK		DO	Bluetooth/FM SLIMbus clock
AW29	LPI_GPIO_15	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				LPI_MI2S3_WS		B	LPI_MI2S 3 word select
				BTFM_SLIMBUS_DATA		B	Bluetooth/FM SLIMbus data
AV30	LPI_GPIO_21	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				I2C_SDA		B	LPI_QUP 0 SE1, lane 0: I2C_SDA
				I3C_SDA		B	LPI_QUP 0 SE1, lane 0: I3C_SDA
AW31	LPI_GPIO_22	–	–		PX_3	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad no.	Pad name	Wake-up function		Configurable functions	Pad characteristics		Functional description
		LPI	MPM		Voltage	Type	
				I2C_SCL		DO	LPI_QUP 0 SE1, lane 1: I2C_SCL
				I3C_SCL		DO	LPI_QUP 0 SE1, lane 1: I3C_SCL
AV32	LPI_GPIO_25	–	–		PX_3	B-PD:nppukp	Configurable I/O
				UART_TX		DO	LPI_QUP 0 SE6, lane 2: UART_TX
AY32	LPI_GPIO_26	Y	Y		PX_3	B-PD:nppukp	Configurable I/O
				UART_RX		DI	LPI_QUP 0 SE6, lane 3: UART_RX

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad no.	Pad name	Functional description
AA37, AB38, AN33, AP34, C41, AT40, AF34	DNC	Do not connect; connected internally, do not connect externally.
A1, A9, A23, A33, A41, AA11, AA15, AA21, AA31, AA35, AA39, AB2, AB4, AB6, AB8, AB18, AB24, AB30, AB34, AB36, AB40, AC9, AC11, AC15, AC21, AC25, AC27, AD6, AD8, AD18, AD24, AD34, AD36, AE9, AE11, AE15, AE21, AE29, AE31, AF2, AF4, AF6, AF8, AF18, AF36, AF38, AG9, AG11, AG13, AG15, AG21, AG25, AG27, AG29, AG31, AG41, AH6, AH8, AH10, AH18, AH24, AJ9, AJ11, AJ13, AJ15, AJ19, AK2, AK4, AK6, AK8, AK10, AK12, AK32, AK34, AK36, AL1, AL9, AL11, AL17, AL19, AL25, AL29, AL37, AM12, AM14, AM16, AM20, AM26, AN9, AN21, AN25, AN29, AN31, AN41, AP4, AP18, AP26, AP28, AP32, AR1, AR11, AR17, AR37, AT10, AT12, AT14, AT16, AT18, AT20, AT22, AT30, AU9, AU11, AU13, AU15, AU17, AU21, AU23, AU27, AU29, AU31, AU41, AV8, AV18, AV24, AV28, AW1, AW9, AW11, AW13, AW15, AW17, AW21, AW23, AW33, AW37, AY8, AY18, AY24, B18, B32, BA9, BA11, BA13, BA15, BA17, BA19, BA21, BA23, BB4, BB10, BB12, BB14, BB16, BB18, BB20, BB22, BC1, BC13, BC25, BC29, BC37, BC41, C3, C5, C7, C9, C11, C13, C15, C17, C19, C21, C23, C25, C27, C29, C31, C33, C35, C37, C39, D4, D38, E11, E19, E21, E23, E31, F4, F14, F28, F38, G5, G7, G9, G11, G13, G15, G17, G19, G21, G23, G25, G27, G29, G31, G33, G35, G37, H2, H8, H10, H12, H14, H16, H18, H20, H24, H26, H28, H30, H32, H34, H36, J3, J9, J11, J13, J15, J17, J19, J23, J25, J27, J29, J31, J33, J35, J37, K8, K10, K12, K14, K16, K18, K20, K24, K26, K28, K32, K34, K36, L1, L3, L9, L11, L15, L17, L19, L23, L25, L27, L29, L31, L33, L35, L39, L41, M4, M10, M12, M18, M20, M22, M24, M28, M30, M32, N5, N7, N9, N11, N31, N33, N35, N37, P4, P6, P8, P10, P20, P30, P32, P36, R1, R3, R7, R31, R37, R41, T2, T8, T14, T16, T18, T20, T26, T28, T32, T36, T38, U3, U7, U9, U11, U27, U31, U35, U39, V2, V4, V6, V8, V10, V18, V20, V24, V30, V36, W11, W13, W15, W21, W27, W35, W39, W41, Y6, Y8, Y10, Y18, Y24, Y26, Y28, Y30, Y32, Y36	GND	Ground
AR23	VDDPX_VBIAS_SDC	Reference voltage for SDC
AT32	VDDPX_VBIAS_UIM	Reference voltage for UIM
AR15	VDD_AH_BBRX_CH0_CH1	Power for modem high-voltage Rx circuits
AR13	VDD_AH_BBRX_CH2_CH3	Power for modem high-voltage Rx circuits
AP16	VDD_AL_BBRX_CH0_CH1	Power for modem low-voltage Rx circuits
AP14	VDD_AL_BBRX_CH2_CH3	Power for modem low-voltage Rx circuits
AB26, AB28, AD28, AE27, AF24, AH26, AH28, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AK24, AL27, AL31, AN27, AR27, AT28	VDD_APC0	Power for the Kryo Silver application processor

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad no.	Pad name	Functional description
AB10	VDD_A_CSI_0_0P9	Power for MIPI CSI0 0.9 V analog circuits
AB12	VDD_A_CSI_0_1P2	Power for MIPI CSI0 1.2 V analog circuits
AD10	VDD_A_CSI_1_0P9	Power for MIPI CSI1 0.9 V analog circuits
AD12	VDD_A_CSI_1_1P2	Power for MIPI CSI1 1.2 V analog circuits
AF10	VDD_A_CSI_2_0P9	Power for MIPI CSI2 0.9 V analog circuits
AF12	VDD_A_CSI_2_1P2	Power for MIPI CSI2 1.2 V analog circuits
AG33	VDD_A_CXO_1P8	Power for the digital core circuits
AE33	VDD_A_DSI_0P9	Power for MIPI DSI 0.9 V analog circuits
AC31	VDD_A_DSI_1P2	Power for MIPI DSI 1.2 V analog circuits
AD32	VDD_A_DSI_PLL_0P9	Power for MIPI DSI PLL 0.9 V analog circuits
T24	VDD_A_EBI_01_CCPLL_0P9	
P14	VDD_A_EBI_0_PHY_A	Power for EBI PHY circuit
P16	VDD_A_EBI_0_PHY_B	Power for EBI PHY circuit
P18	VDD_A_EBI_0_PHY_C	Power for EBI PHY circuit
P24	VDD_A_EBI_1_PHY_A	Power for EBI PHY circuit
P26	VDD_A_EBI_1_PHY_B	Power for EBI PHY circuit
P28	VDD_A_EBI_1_PHY_C	Power for EBI PHY circuit
U23	VDD_A_EBI_CC	Power for EBI clock circuit
AE17	VDD_A_MODEM_PLL	Power for modem PLL circuit
U33	VDD_A_QREFS_1_0P9	Reference voltage for QREFS
AP20	VDD_A_TXDAC	Power for modem circuit
P22	VDD_A_UFS_0P9	Power for UFS 0.9 V circuits
T22	VDD_A_UFS_1P2	Power for UFS 1.2 V circuits
W31	VDD_A_USBHS_0P9	Power for the USB high-speed 0.9 V analog circuits
V32	VDD_A_USBHS_1P8	Power for the USB high-speed 1.8 V analog circuits
W33	VDD_A_USBHS_3P1	Power for the USB high-speed 3.1 V analog circuits
AA33	VDD_A_USBSSDP_0P9	Power for USB SS 0.9 V circuit
AB32	VDD_A_USBSSDP_1P2	Power for USB SS 1.2 V circuit
R9	VDD_A_WLAN_ADCDAC1_1P3	Power for WLAN ADC and DAC 1 - 1.3 V circuit
W9	VDD_A_WLAN_ADCDAC2_1P3	Power for WLAN ADC and DAC 2 - 1.3 V circuit
T10	VDD_A_WLAN_PLL_0P9	Power for the WLAN PLL 0.9 V analog circuits
AA23, AB14, AB20, AC23, AD14, AD20, AE23, AF14, AH14, AH16, AK14, AK16, H22, J21, K22, L21, U15, U19, U21, U29, V14, V16, V22, V26, V28, W19, W23, Y14, Y16, Y20	VDD_CX	Power for digital core circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad no.	Pad name	Functional description
AG19, AH20, AK20	VDD_CX_LPI	Power for low-power island digital core circuits
T12, V12, Y12	VDD_CX_WLAN	Power for WLAN digital core circuits
M16	VDD_IO_EBI_0_CK	Power for the EBI0 I/O clock circuits
N13	VDD_IO_EBI_0_PHY_A	Power for the EBI0 I/O PHY circuits
N15	VDD_IO_EBI_0_PHY_B	Power for the EBI0 I/O PHY circuits
N17	VDD_IO_EBI_0_PHY_C	Power for the EBI0 I/O PHY circuits
N19	VDD_IO_EBI_0_PHY_D	Power for the EBI0 I/O PHY circuits
M26	VDD_IO_EBI_1_CK	Power for the EBI0 I/O clock circuits
N23	VDD_IO_EBI_1_PHY_A	Power for the EBI0 I/O PHY circuits
N25	VDD_IO_EBI_1_PHY_B	Power for the EBI0 I/O PHY circuits
N27	VDD_IO_EBI_1_PHY_C	Power for the EBI0 I/O PHY circuits
N29	VDD_IO_EBI_1_PHY_D	Power for the EBI0 I/O PHY circuits
AA17, AA25, AA27, AC17, AG23, AJ17, AK18, AL23, AM24, U17, U25	VDD_MX	Power for on-chip memory
AJ21	VDD_MX_LPI	Power for low-power island memory circuits
AM18	VDD_MX_TXDAC	Power for modern circuits
R11	VDD_MX_WLAN	Power for WLAN circuits
AT24	VDD_PX0	Power for pad group 0
M34	VDD_PX1	Power for pad group 1
R35	VDD_PX10	Power for pad group 10
AG35	VDD_PX11	Power for pad group 11
L13	VDD_PX1_A	Power for the EBI I/O circuits
K30	VDD_PX1_B	Power for the EBI I/O circuits
AP22	VDD_PX2	Power for pad group 2
AM8, AM32, AR9, AU25, M8, T34	VDD_PX3	Power for pad group 3
AR31	VDD_PX5	Power for pad group 5
AR33	VDD_PX6	Power for pad group 6
R33	VDD_PX7	Power for pad group 7
AM10	VDD_QFPROM	Power for programming the QFPROM

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Gold and Silver application processor	-0.3	1.25	V
VDD_CX_LPI	Low-power island digital core circuits	-0.3	1.04	V
VDD_MX_LPI	Low-power island memory circuits	-0.3	1.00	V
VDD_CX	Digital core circuits	-0.3	1.13	V
VDD_MX	On-chip memory	-0.3	1.05	V
VDD_MX_WLAN	WLAN circuits	-0.3	1.05	V
VDD_MX_TXDAC	Modem circuits	-0.3	1.05	V
VDD_A_WLAN_PLL_0P9	WLAN PLL 0.9 V analog circuits	-0.3	1.05	V
VDD_A_EBI_0_PHY_A	EBI0 PHY circuit	-0.3	1.05	V
VDD_A_EBI_0_PHY_B	EBI0 PHY circuit	-0.3	1.05	V
VDD_A_EBI_0_PHY_C	EBI0 PHY circuit	-0.3	1.05	V
VDD_A_EBI_1_PHY_A	EBI1 PHY circuit	-0.3	1.05	V
VDD_A_EBI_1_PHY_B	EBI1 PHY circuit	-0.3	1.05	V
VDD_A_EBI_1_PHY_C	EBI1 PHY circuit	-0.3	1.05	V
VDD_A_EBI_CC	EBI clock circuit	-0.3	1.05	V
VDD_A_MODEM_PLL	Modem PLL circuit	-0.3	1.05	V
VDD_CX_WLAN	WLAN digital core circuits	-0.3	0.94	V
VDD_A_USBHS_0P9	USB high speed 0.9 V analog circuits	-0.3	1.01	V
VDD_A_UFS_0P9	UFS 0.9 V circuits	-0.3	1.01	V
VDD_A_DSI_0P9	MIPI DSI 0.9 V analog circuits	-0.3	1.01	V
VDD_A_DSI_PLL_0P9	MIPI DSI PLL 0.9 V analog circuits	-0.3	1.01	V
VDD_A_EBI_01_CCPLL_0P9	EBI clock PLL 0.9 V analog circuits	-0.3	1.01	V
VDD_A_QREFS_1_0P9	Reference voltage for the QREFS	-0.3	1.16	V
VDD_A_CSI_0_0P9	MIPI CSI0 0.9 V analog circuits	-0.3	1.01	V
VDD_A_CSI_1_0P9	MIPI CSI1 0.9 V analog circuits	-0.3	1.01	V
VDD_A_CSI_2_0P9	MIPI CSI2 0.9 V analog circuits	-0.3	1.01	V
VDD_A_USBHS_1P8	USB high speed 1.8 V analog circuits	-0.3	2.15	V
VDD_A_CXO_1P8	Digital core circuits	-0.3	2.15	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_AH_BBRX_CH0_CH1	Modem high-voltage Rx circuit	-0.3	2.15	V
VDD_AH_BBRX_CH2_CH3	Modem high-voltage Rx circuit	-0.3	2.15	V
VDD_PX11	Pad group 11	-0.3	2.15	V
VDD_QFPROM	Programming the QFPROM	-0.3	2.15	V
VDD_A_TXDAC	Modem circuit	-0.3	2.15	V
VDD_IO_EBI_0_PHY_A	EBI0 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_0_PHY_B	EBI0 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_0_PHY_C	EBI0 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_0_PHY_D	EBI0 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_1_PHY_A	EBI1 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_1_PHY_B	EBI1 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_1_PHY_C	EBI1 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_1_PHY_D	EBI1 I/O PHY circuits	-0.3	0.72	V
VDD_IO_EBI_0_CK	EBI0 I/O clock circuits	-0.3	0.72	V
VDD_IO_EBI_1_CK	EBI1 I/O clock circuits	-0.3	0.72	V
VDD_A_CSI_0_1P2	MIPI CSI0 1.2 V analog circuits	-0.3	1.39	V
VDD_A_CSI_1_1P2	MIPI CSI1 1.2 V analog circuits	-0.3	1.39	V
VDD_A_CSI_2_1P2	MIPI CSI2 1.2 V analog circuits	-0.3	1.39	V
VDD_A_DSI_1P2	MIPI DSI 1.2 V analog circuits	-0.3	1.39	V
VDD_AL_BBRX_CH0_CH1	Modem low-voltage Rx circuit	-0.3	1.39	V
VDD_AL_BBRX_CH2_CH3	Modem low-voltage Rx circuit	-0.3	1.39	V
VDD_A_UFS_1P2	UFS 1.2 V circuits	-0.3	1.38	V
VDD_A_USBSSDP_1P2	USB SS 1.2 V circuit	-0.3	1.39	V
VDD_PX10	Pad group 10	-0.3	1.39	V
VDD_A_USBHS_3P1	USB high speed 3.1 V analog circuits	-0.3	3.99	V
VDD_A_USBSSDP_0P9	USB SS 0.9 V circuit	-0.3	1.01	V
VDD_A_WLAN_ADCDAC1_1P3	WLAN ADC and DAC 1 - 1.3 V circuit	-0.3	1.45	V
VDD_A_WLAN_ADCDAC2_1P3	WLAN ADC and DAC 2 - 1.3 V circuit	-0.3	1.45	V
VDD_PX0	Pad group 0	-0.3	2.15	V
VDD_PX1	Pad group 1 - EBI	-0.3	1.29	V
VDD_PX1_A				
VDD_PX1_B				
VDD_PX2	Pad group 2	-0.3	3.36	V
	Low voltage			
	High voltage			
VDD_PX3	Pad group 3	-0.3	2.15	V
VDD_PX5	Pad group 5	-0.3	3.36	V
	Low voltage			
	High voltage			

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_PX6	Pad group 6	-0.3	3.36	V
	Low voltage			
	High voltage			
VDD_PX7	Pad group 7	-0.3	2.15	V
VDDPX_VBIAS_SDC	SDC Reference Voltage	-0.3	1.51	V
VDDPX_VBIAS_UIM	UIM Reference Voltage	-0.3	1.51	V
T_s	Storage temperature [a] [b]	-55	150	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-3). The SM6225 meets all performance specifications listed in this chapter, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver + Gold application processor			
	Turbo_L3	0.796	1.132	V
	Turbo_L1	0.764	1.027	V
	Turbo	0.764	0.952	V
	Nominal	0.624	0.878	V
	SVS_L1	0.576	0.860	V
	SVS	0.532	0.785	V
	Low_SVS	0.484	0.719	V
VDD_CX_LPI	LPI core			
	Turbo	0.66	0.948	V
	Nominal	0.605	0.878	V
	SVS_L1	0.56	0.856	V
	SVS	0.515	0.790	V
	Low-SVS	0.47	0.719	V
VDD_MX_LPI	LPI core memory			
	Turbo	0.740	0.913	V
	Nominal	0.695	0.878	V
	SVS_L1	0.695	0.856	V
	SVS	0.695	0.807	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter		Min	Max	Unit
	Low-SVS	0.695	0.807	V
VDD_CX	Digital core circuits			
	Turbo-L1	0.700	1.027	V
	Turbo	0.660	0.952	V
	Nominal	0.605	0.878	V
	SVS-L1	0.560	0.856	V
	SVS	0.515	0.785	V
	Low-SVS	0.470	0.719	V
VDD_MX	On-chip memory			
VDD_MX_WLAN VDD_MX_TXDAC VDD_A_WLAN_PLL_0P9 VDD_A_EBI_0_PHY_A VDD_A_EBI_0_PHY_B VDD_A_EBI_0_PHY_C VDD_A_EBI_1_PHY_A VDD_A_EBI_1_PHY_B VDD_A_EBI_1_PHY_C VDD_A_EBI_CC VDD_A_MODEM_PLL	Turbo_L1	0.740	0.952	V
	Turbo	0.740	0.917	V
	Nominal	0.695	0.878	V
	SVS_L1	0.695	0.856	V
	SVS	0.695	0.807	V
	Low_SVS	0.695	0.807	V
VDD_CX_WLAN	WLAN core circuits			
	SVS_L1	0.560	0.851	V
	SVS	0.515	0.790	V

Table 3-3 Operating conditions

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_USBHS_0P9	USB high speed 0.9 V analog circuits	0.72	0.88	0.95	V
VDD_A_UFS_0P9	UFS 0.9 V circuits	0.83	0.88	0.92	V
VDD_A_DSI_0P9	MIPI DSI 0.9 V analog circuits				
VDD_A_DSI_PLL_0P9	MIPI DSI PLL 0.9 V analog circuits				
VDD_A_EBI_01_CCPLL_0P9	EBI clock PLL 0.9 V analog circuits				
VDD_A_QREFS_1_0P9	Reference voltage for the QREFS				
VDD_A_CSI_0_0P9	MIPI CSI0 0.9 V analog circuits				
VDD_A_CSI_1_0P9	MIPI CSI1 0.9 V analog circuits				
VDD_A_CSI_2_0P9	MIPI CSI2 0.9 V analog circuits				
VDD_A_USBHS_1P8	USB high speed 1.8 V analog circuits	1.7	1.8	1.9	V
VDD_A_CXO_1P8	Digital core circuits				
VDD_AH_BBRX_CH0_CH1	Modem high-voltage Rx circuit				
VDD_AH_BBRX_CH2_CH3	Modem high-voltage Rx circuit				
VDD_PX11	Pad group 11				

Table 3-3 Operating conditions (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
VDD_QFPROM	Programming the QFPROM				
VDD_A_TXDAC	Modem circuit				
VDD_IO_EBI_0_PHY_A	EBI0 I/O PHY circuits	0.57	0.6	0.65	V
VDD_IO_EBI_0_PHY_B	EBI0 I/O PHY circuits				
VDD_IO_EBI_0_PHY_C	EBI0 I/O PHY circuits				
VDD_IO_EBI_0_PHY_D	EBI0 I/O PHY circuits				
VDD_IO_EBI_1_PHY_A	EBI1 I/O PHY circuits				
VDD_IO_EBI_1_PHY_B	EBI1 I/O PHY circuits				
VDD_IO_EBI_1_PHY_C	EBI1 I/O PHY circuits				
VDD_IO_EBI_1_PHY_D	EBI1 I/O PHY circuits				
VDD_IO_EBI_0_CK	EBI0 I/O clock circuits				
VDD_IO_EBI_1_CK	EBI1 I/O clock circuits				
VDD_A_CSI_0_1P2	MIPI CSI0 1.2 V analog circuits	1.15	1.2	1.25	V
VDD_A_CSI_1_1P2	MIPI CSI1 1.2 V analog circuits				
VDD_A_CSI_2_1P2	MIPI CSI2 1.2 V analog circuits				
VDD_A_DSI_1P2	MIPI DSI 1.2 V analog circuits				
VDD_AL_BBRX_CH0_CH1	Modem low-voltage Rx circuit				
VDD_AL_BBRX_CH2_CH3	Modem low-voltage Rx circuit				
VDD_A_UFS_1P2	UFS 1.2 V circuits				
VDD_A_USBSSDP_1P2	USB SS 1.2 V circuit				
VDD_PX10	Pad group 10				
VDD_A_USBHS_3P1	USB high speed 3.1 V analog circuits	2.98	3.08	3.3	V
VDD_A_USBSSDP_0P9	USB SS 0.9 V circuit	0.83	0.88	0.92	V
VDD_A_WLAN_ADCDAC1_1P3	WLAN ADC and DAC 1 - 1.3 V circuit	1.25	1.304	1.32	V
VDD_A_WLAN_ADCDAC2_1P3	WLAN ADC and DAC 2 - 1.3 V circuit				
VDD_PX0	Pad group 0	1.65	1.8	1.95	V
VDD_PX1	Pad group 1 - EBI	1.06	1.1	1.17	V
VDD_PX1_A					
VDD_PX1_B					
VDD_PX2	Pad group 2 - SDC2				
	Low voltage	1.7	1.8	1.9	V
	High voltage	2.7	2.96	3.05	V
VDD_PX3	Pad group 3	1.7	1.8	1.9	V
VDD_PX5	Pad group 5 - UIM1 dual-voltage				V
	Low voltage	1.7	1.8	1.9	V
	High voltage	2.7	2.95	3.05	V
VDD_PX6	Pad group 6 - UIM2 dual-voltage				

Table 3-3 Operating conditions (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
	Low voltage	1.7	1.8	1.9	V
	High voltage	2.7	2.95	3.05	V
VDD_PX7	Pad group 7	1.7	1.8	1.9	V
VDDPX_VBIAS_SDC	SDC Reference Voltage	1.125	1.25	1.375	V
VDDPX_VBIAS_UIM	UIM Reference Voltage	1.125	1.25	1.375	V
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.

3.2.1 Core and memory voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE and VDD_MEM retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization.

Table 3-4 Core voltage in retention mode

VDD_CORE	Bit 31 (MSB)	Bit 30	Bit 29 (LSB)
0.352 V	0	0	1
0.384 V	0	1	0
0.416 V	0	1	1
0.448 V	1	0	0
0.48 V	1	0	1

NOTE
1. The VDD_CORE voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x1B40184.

Table 3-5 Memory voltage in retention mode

VDD_MEM	Bit 19 (MSB)	Bit 18	Bit 17 (LSB)
0.540 V	0	0	1
0.564 V	0	1	0
0.616 V	0	1	1
0.668 V	1	0	0

NOTE
1. The VDD_MEM voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x1B40198.

3.3 Power delivery network (PDN)

A detailed power delivery network specification is available in the *SM6225 Chipset Power Delivery Network Specification* (80-26896-1P) document.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the document *SM6225 Linux Android Current Consumption Data* (80-26896-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-6 Dhrystone and rock bottom maximum power

SDM version	Octa core – 4X Gold at 2.4 GHz for SM6225-AB, 2.8 GHz for SM6225-AD and 4X Silver at 1.9 GHz, Dhrystone (W) at +95°C (Tj) [a b c]	Rock bottom (mW) at 30°C (Tj) [d]
SM6225-AB	4.8	12.11
SM6225-AD	7.4	12.11

[a] Temperature reading is from the SM6225 device's internal temperature sensor.
[b] Dhrystone power should be measured on the VDD_APC rail, right before PDN capacitors (with a small serial sampling resistor inserted, if necessary).
[c] Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and the average window should be > 1 ms (or > 1250 samples).
[d] Rock bottom (VDDCX and VDDMX) power should be measured at VDDCX and VDDMX rails when VDDCX and VDDMX are at retention voltage. See AIR1 in Table 3.1 (Test definitions) in the *SM6225 Linux Android Current Consumption Data* (80-26896-7) document for the test setup.

3.5 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire SM6225 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. See the appropriate PMIC device specification, such as the *PM6225/PM6375 Power Management IC Device Specification* (80-27912-1).

A high-level summary of the required default power-on sequence is:

1. VDD_PX0 (pad group 0)
2. VDD_MX (on-chip memory, VDD_MX_WLAN (WLAN circuits), VDD_MX_TXDAC (modem circuits), VDD_A_WLAN_PLL_0P9 (WLAN PLL 0.9 V analog circuits, VDD_A_EBI_0_PHY_A, VDD_A_EBI_0_PHY_B, VDD_A_EBI_0_PHY_C, VDD_A_EBI_1_PHY_A, VDD_A_EBI_1_PHY_B, VDD_A_EBI_1_PHY_C (EBI0/EBI1 PHY circuits), VDD_A_EBI_CC (EBI clock circuit), VDD_A_MODEM_PLL (modem PLL circuit)
3. VDD_MX_LPI (LPI memory circuit)
4. VDD_CX (digital core circuit)
5. VDD_CX_LPI (LPI digital core circuit)
6. VDD_PX3 (pad group 3), VDD_PX7 (pad group 7)
7. VDD_CX_WLAN (WLAN digital core circuit)
8. VDDPX_VBIAS_SDC (SDC reference voltage), VDDPX_VBIAS_UIM (UIM reference voltage)
9. VDD_A_CSI_0_1P2, VDD_A_CSI_1_1P2, VDD_A_CSI_2_1P2, VDD_A_DSI_1P2 (MIPI CSI0/CSI1/CSI2/DSI 1.2 V analog circuits), VDD_AL_BBRX_CH0_CH1, VDD_AL_BBRX_CH2_CH3 (modem low-voltage Rx circuit), VDD_A_UFS_1P2 (UFS 1.2 V circuits), VDD_A_USBSSDP_1P2 (USB SS 1.2 V circuit), VDD_PX10 (pad group 10)
10. VDD_PX1, VDD_PX1_A, VDD_PX1_B (pad group 1 – EBI)

11. VDD_IO_EBI_0_PHY_A, VDD_IO_EBI_0_PHY_B, VDD_IO_EBI_0_PHY_C, VDD_IO_EBI_0_PHY_D, VDD_IO_EBI_1_PHY_A, VDD_IO_EBI_1_PHY_B, VDD_IO_EBI_1_PHY_C, VDD_IO_EBI_1_PHY_D (EBI0/EBI1 I/O PHY circuits), VDD_IO_EBI_0_CK, VDD_IO_EBI_1_CK (EBI0/EBI1 I/O clock circuits)
12. VDD_A_USBHS_0P9 (USB high speed 0.9 V analog circuits), VDD_A_UFS_0P9 (UFS 0.9 V circuits), VDD_A_DSI_0P9 (MIPI DSI 0.9 V analog circuits), VDD_A_DSI_PLL_0P9 (MIPI DSI PLL 0.9 V analog circuits), VDD_A_EBI_01_CCPLL_0P9 (EBI clock PLL 0.9 V analog circuits), VDD_A_QREFS_1_0P9 (QREFS reference voltage), VDD_A_CSI_0_0P9, VDD_A_CSI_1_0P9, VDD_A_CSI_2_0P9 (MIPI CSI0/CSI1/CSI2 0.9 V analog circuits)
13. VDD_A_USBHS_1P8 (USB high speed 1.8 V analog circuits), VDD_A_CXO_1P8 (digital core circuits), VDD_AH_BBRX_CH0_CH1, VDD_AH_BBRX_CH2_CH3 (modem high voltage Rx circuits), VDD_PX11 (pad group 11), VDD_QFPROM (programming the QFPROM), VDD_A_TXDAC (modem circuit)
14. VDD_A_USBHS_3P1 (USB high speed 3.1 V analog circuits)
15. VDD_PX2 (SDC2 pads)
16. VDD_APC0 (Kryo Gold and Silver application processor)

Comments regarding this sequence include:

- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up.

3.6 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM6225 device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-7 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDPX	VDDPX + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDPX	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDPX	VDDPX + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDPX	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [a]	–	1.0	µA
I_{IL}	Input low leakage current [a]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
$R_{PULL-UP}$	For GPIO on pads BA25, AY26, AW25, BB26, BA27, BB28, AW27, AW29, AY28 and GPIO_53 through GPIO_62	10	50	kΩ

Table 3-7 DC specification of 1.8 V GPIOs and WCSS WSI I/Os (cont.)

Parameter	Description	Min	Max	Units
$R_{PULL-DOWN}$	For GPIO on pads BA25, AY26, AW25, BB26, BA27, BB28, AW27, AW29, AY28 and GPIO_53 through GPIO_62	10	50	kΩ
I_{OZH}	High-level, tri-state leakage current [a]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [a]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [b]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [c]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage, CMOS	VDDPX - 0.45	VDDPX	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

[a] I_{IH}, I_{IL}, I_{OZH}, and I_{OZL} values are based on nominal PVT (TT/25°C).
[b] Pin voltage = VDDPX maximum. For keeper pins, pin voltage = VDDPX maximum - 0.45 V.
[c] Pin voltage = GND and supply = VDDPX maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX maximum.

Table 3-8 SDC 2.96 V mode DC specifications (VDDPX_2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_PX2	–	VDD_PX2	V
V_{OL}	Low-level output voltage	0	–	0.125 × VDD_PX2	V

Table 3-9 SDC2 1.8 V mode DC specifications (VDDPX_2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA

Table 3-9 SDC2 1.8 V mode DC specifications (VDDPX_2) (cont.)

Parameter	Description	Min	Typ	Max	Units
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-10 SDC1 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	0.65 × VDD_PX7	–	VDD_PX7 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.35 × VDD_PX7	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	2	µA
I_{IL}	Input low leakage current	-2	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	2	µA
I_{OZL}	Low-level, tri-state leakage current	-2	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	50	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	50	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	50	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	50	kΩ
V_{OH}	High-level output voltage	VDD_PX7 - 0.45	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-11 UIM 2.95 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [a]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage [a]	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage [b]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ

Table 3-11 UIM 2.95 V mode DC specifications (VDDPX_5 and VDDPX_6) (cont.)

Parameter	Description	Min	Typ	Max	Units
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [c]	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage [d]	0	–	0.4	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal.
[b] V_{HYS} is not a required specification for UICC.
[c] UIM specifies V_{OH} = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case V_{OH} is used in this table.
[d] UIM specifies V_{OL} = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O). The worse-case V_{OL} is used in this table.

Table 3-12 UIM 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [a]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage [a]	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage [b]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [c]	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage [d]	0	–	0.4	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal.
[b] V_{HYS} is not a required specification for UICC.
[c] UIM specifies V_{OH} = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case V_{OH} is used in this table.
[d] UIM specifies V_{OL} = 0.2 × VDD_Px (RST, CLK) and 0.3 V (I/O). The worse-case V_{OL} is used in this table.

Table 3-13 Digital I/O characteristics for VDDPX_10 nominal (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDDPX_10	V
V_{OH}	Output high-level voltage	0.75 × VDDPX_10	VDDPX_10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1), with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

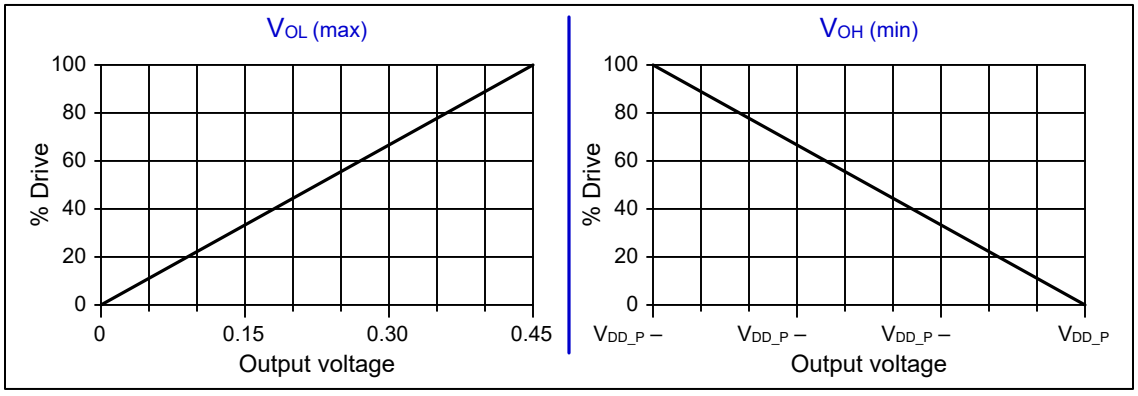


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all VDDPX)

3.7 Timing characteristics

NOTE All SM6225 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.2.

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the figure below.

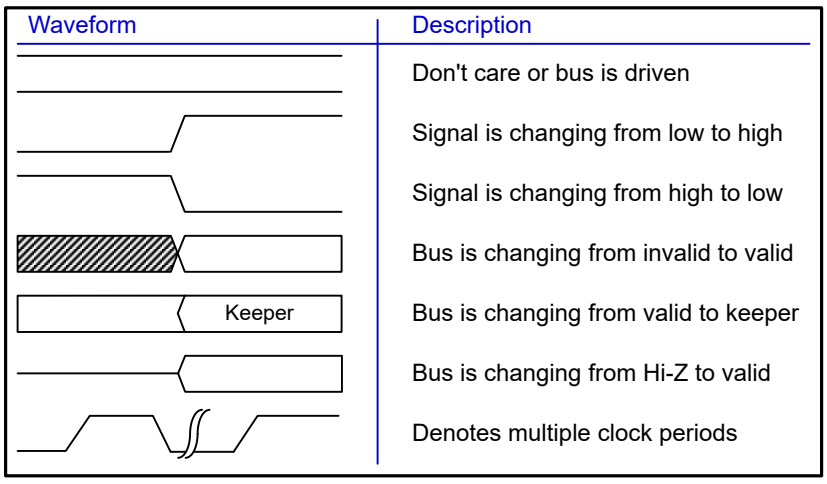


Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.7.2 Rise and fall time specifications

The testers that characterize SM6225 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the figure below.

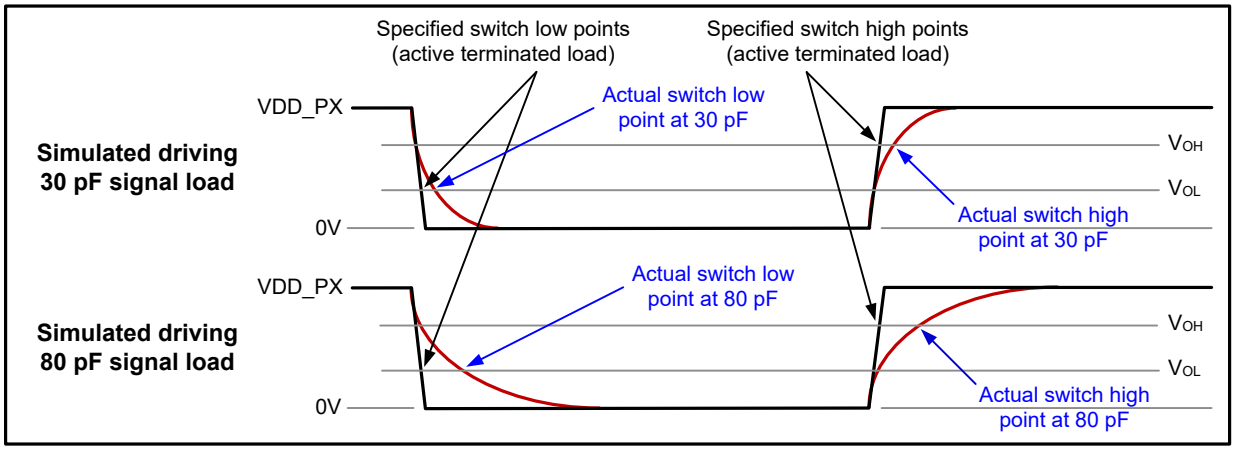


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM6225 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The SM6225device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated V_{DD_PX} supply Figure 3-4. The input switch point for pure input-only pads is designed to be $V_{DD\_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_IL and 65% of V_{DD_PX} for V_{IH}.

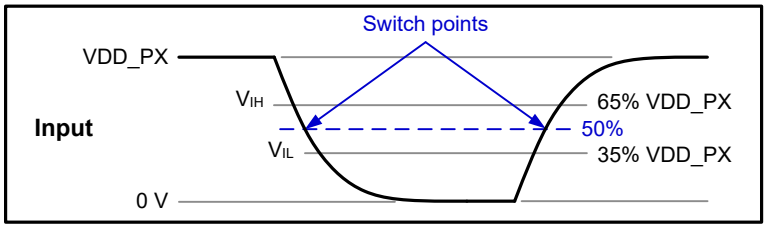


Figure 3-4 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- V_{OH} ~ V_{DD_PX} - 50 mV or more
- V_{OL} ~ 50 mV or less

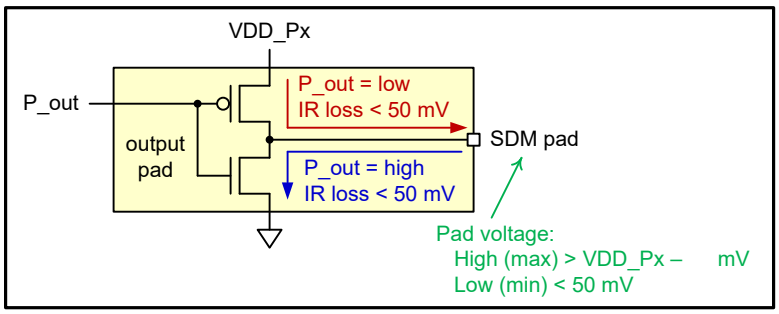


Figure 3-5 Output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of ISC is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading.

Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both the input and output behaviors were described above.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.8.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4X SDRAM memory that is attached to the SM6225 chipset.

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.10.1 for secure digital interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SM6225 device supports three 4-lane D-PHY or C-PHY camera interfaces.

Table 3-14 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.0	None

3.9.2 Audio support

The SM6225 supports the WCD9370 audio codec IC through SoundWire interface to provide the system's audio functions.

Other audio-related interface options include:

- I^2S – Section 3.10.5
- Digital microphone –Section 3.10.7
- SoundWire – Section 3.10.8
- I^2C – Section 3.10.10

See the *Qualcomm Aqstic WCD9370 Device Specification* (80-PG244-1) for performance characteristics.

3.9.3 Display support

The SM6225 device supports one 4-lane MIPI DSI port.

Table 3-15 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None

3.10 Connectivity

The connectivity functions supported by the SM6225 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power interchip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections

- Dedicated I^2C interfaces for camera (CCI I2C)
- Through proper configuration of the 10 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - I3C interface for sensor support

Pertinent specifications for these functions are detailed in the following subsections.

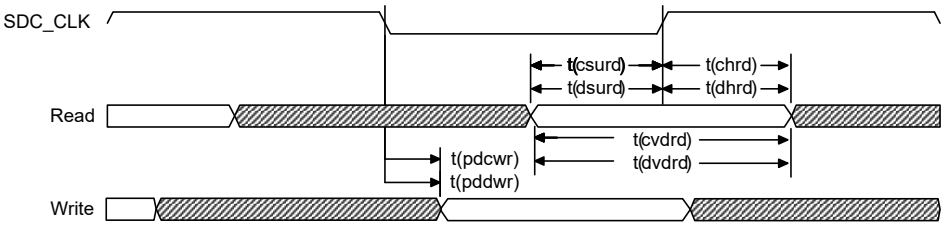
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

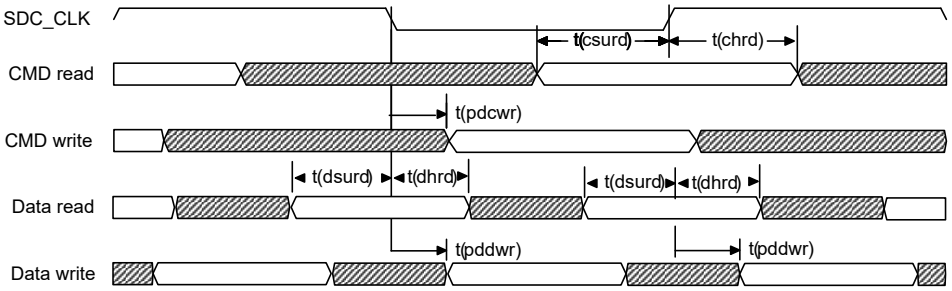
Table 3-16 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Multimedia Card Host Specification, version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

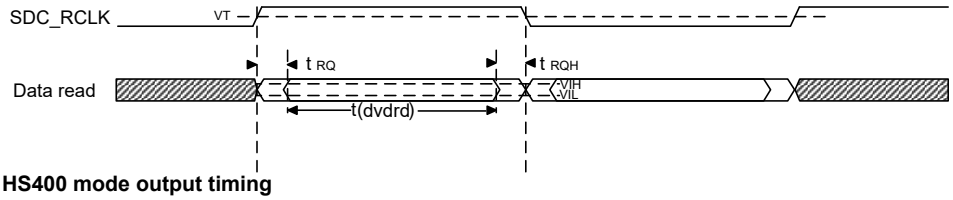
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

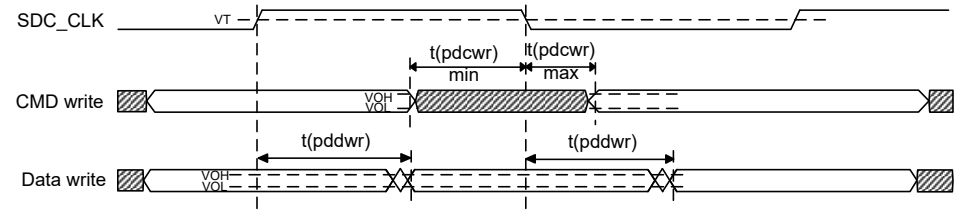


Figure 3-6 SD interface timing

3.10.2 USB interfaces

Table 3-17 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	Low speed is not supported in device mode
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 A or later)	Supports the host mode aspect of OTG only

3.10.3 UFS interface

Table 3-18 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 2.1	None

3.10.4 UIM interface

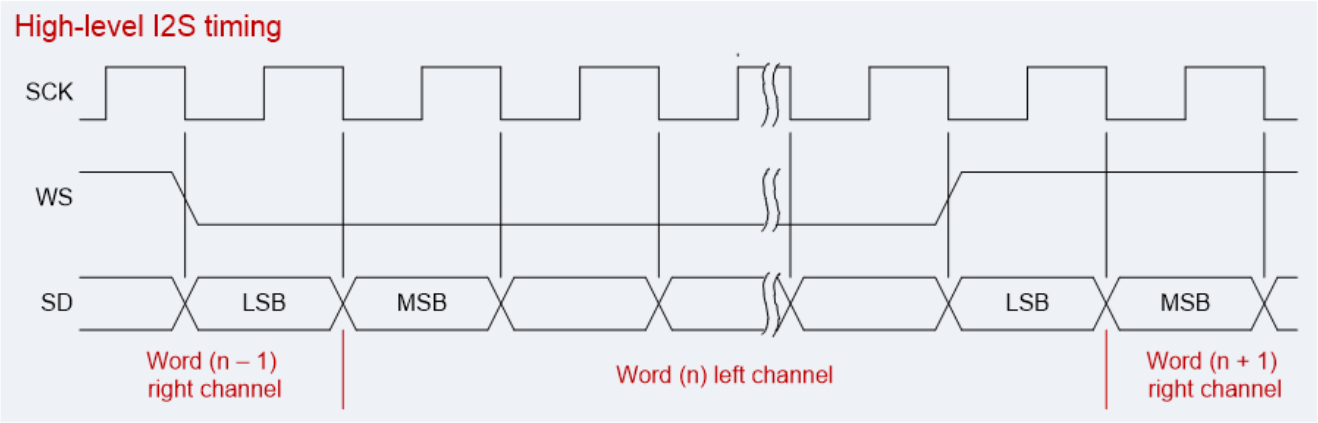
Table 3-19 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	None

3.10.5 I^2S interfaces

Table 3-20 Supported I^2S standards and exceptions

Applicable standards	Feature exceptions
Philips I^2S Bus Specifications revised June 5, 1996 (Available for free download.)	None



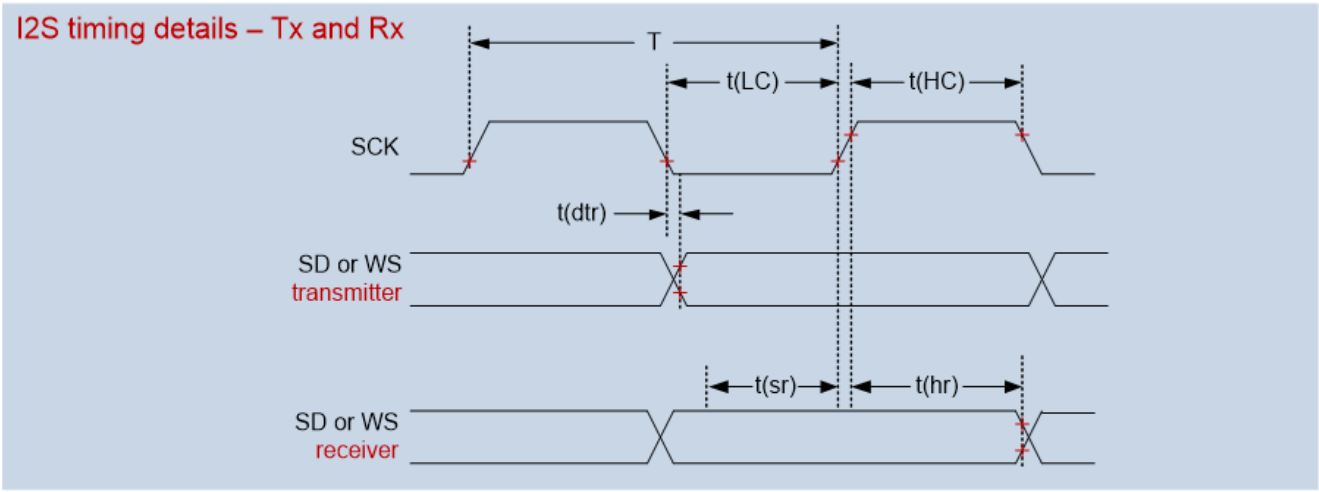


Figure 3-7 I²S timing diagram

Table 3-21 I²S interface timing – MI²S interface 1 and 2 (primary and secondary MI²S)

Parameter		Min	Typ	Max	Unit
Using internal SCK					
	Frequency	–	–	24.576	MHz
T	Clock period	40.69	–	–	ns
t(HC)	Clock high	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	8.14	–	–	ns
t(hr)	SD and WS input hold time	0	–	–	ns
t(dtr)	SD and WS output delay	-	–	8.14	ns
Using external SCK					
	Frequency	-	–	24.576	MHz
T	Clock period	40.69	–	–	ns
t(HC)	Clock high	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	8.14	–	–	ns
t(hr)	SD and WS input hold time	0	–	–	ns

Table 3-21 I²S interface timing – MI²S interface 1 and 2 (primary and secondary MI²S) (cont.)

Parameter		Min	Typ	Max	Unit
t(dtr)	SD and WS output delay	-	–	8.14	ns
NOTE I²S slave support of 24.576 MHz is available only with I²S1.					

3.10.6 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

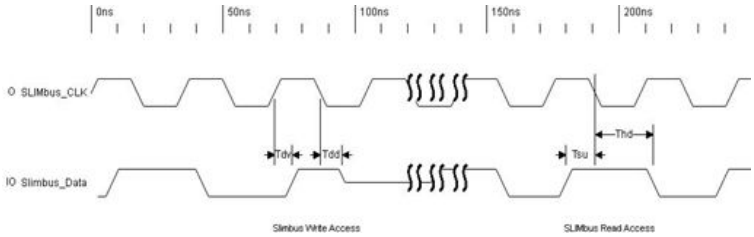


Figure 3-8 SLIMbus timing diagram

Table 3-23 SLIMbus timing parameters

Parameter		Min	Max	Units
Tdv	Prop delay from clock to data	–	10.5	ns
Tdd	Driver disable time	–	10	ns
Tsu	Setup time	3.5	–	ns
Thd	Hold time	2	–	ns

3.10.7 Digital microphone PDM interface

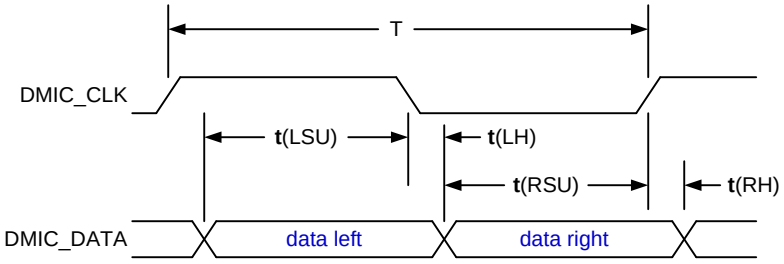


Figure 3-9 Digital microphone PDM interface timing

Table 3-24 Digital microphone timing

Parameter		Comments	Min	Typ	Max	Unit
T	DMIC clock period	–	163	–	1666	ns
t(LSU)	Data left setup time to clock falling edge	–	5	–	–	ns

Table 3-24 Digital microphone timing (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(LH)	Data left hold time to clock falling edge	–	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	–	5	–	–	ns
t(RH)	Data right hold time to clock falling edge	–	0	–	–	ns

3.10.8 SoundWire

SM6225 SoundWire PHY timing parameters, as specified in the following table, are compliant to clock and data specifications, as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04. See the following figures.

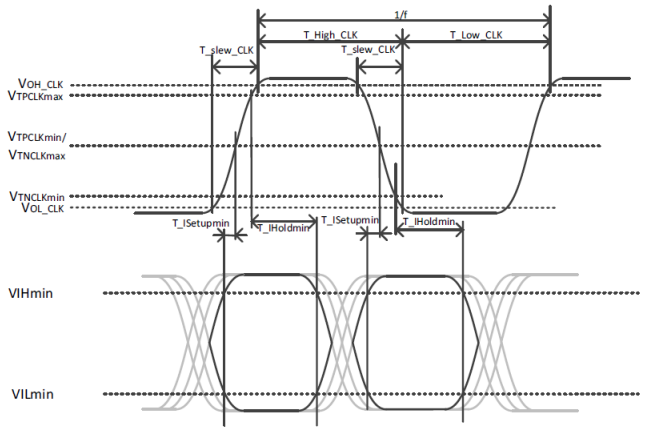


Figure 3-10 PHY timing – clock output/input and data input

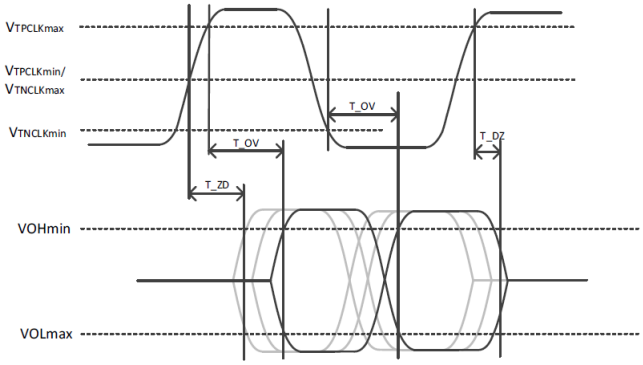


Figure 3-11 PHY timing – clock output and data output

Table 3-25 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Unit
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	kHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of low half-period on clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns

Table 3-25 PHY timing parameters (1.8 V systems) (cont.)

Name	Description	Min	Max	Unit
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	%
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	4	–	ns
t_IHold_min_Data_1V8	Input hold time	–	5	ns
DC_Out_Clock	Duty cycle generated at clock output signal calculated from t_Low_Clock/(t_Low_Clock + t_ High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.10.9 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.10.10) and GPIOs configured as discrete digital inputs (Section 3.6).

3.10.10 I^{2}C interface

Table 3-26 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions
I^{2}C Specification, version 3.0	HS mode, slave mode, and 10-bit addressing are not supported.

3.10.11 I3C interface

Table 3-27 Supported I3C standards and exceptions

Applicable standard	Feature exceptions
I3C Specification, version 1.0	None

3.10.12 Serial peripheral interface

The SM6225 supports SPI as a master only. Only six out of 10 QUP ports can be configured as an SPI master.

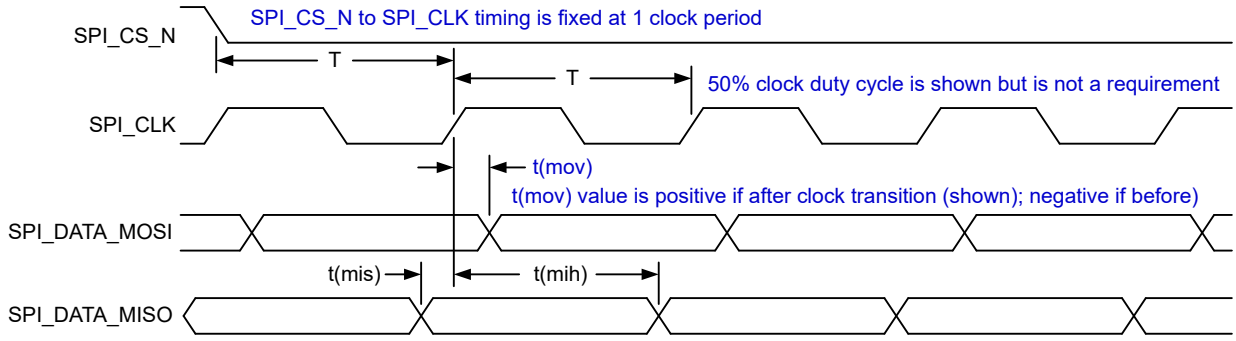


Figure 3-12 SPI master timing diagram

Table 3-28 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	9	–	–	ns
t(cl)	Clock low	9	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz CXO input

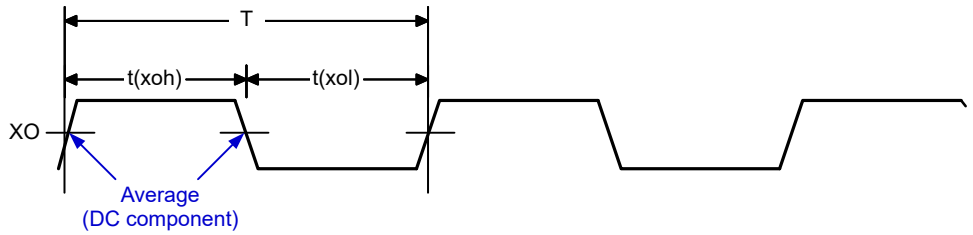


Figure 3-13 XO timing parameters

Table 3-29 XO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used	–	19.2	–	MHz

[a] See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal, and TH + Xtal Mini-Specification* (80-V9690-24) document for more details.

3.11.1.2 Sleep clock

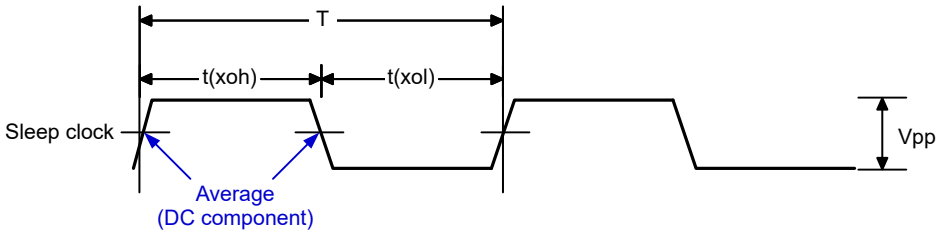


Figure 3-14 Sleep clock timing parameters

Table 3-30 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F= 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

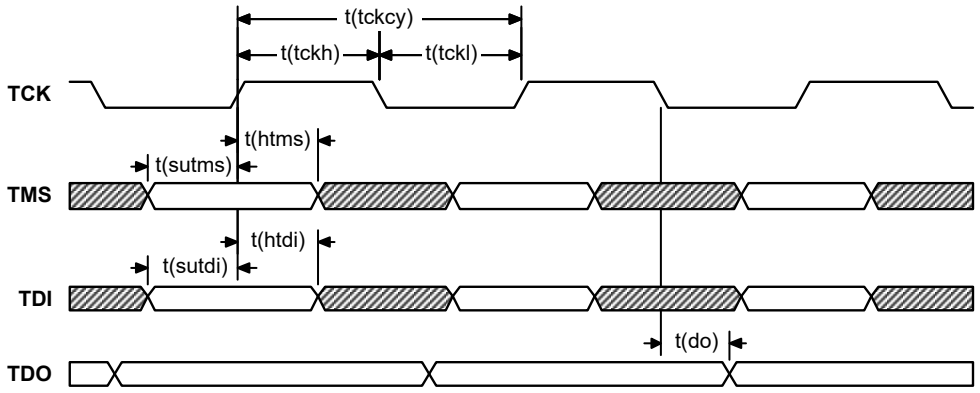


Figure 3-15 JTAG interface timing diagram

Table 3-31 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.12 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-3. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 RF front end (RFFE)

Table 3-32 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None

3.12.2 System power management interface (SPMI)

Table 3-33 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM6225 device is available in the PSP807 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The PSP807 has a 11.1 mm by 10.5 mm body, with a maximum height of 0.89 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in the following figure.

NOTE Click the following link to download the *Package Outline Drawing PSP807, 11.1 × 10.5 × 0.89 mm, M530, S140* (NT90-27087-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-27087-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

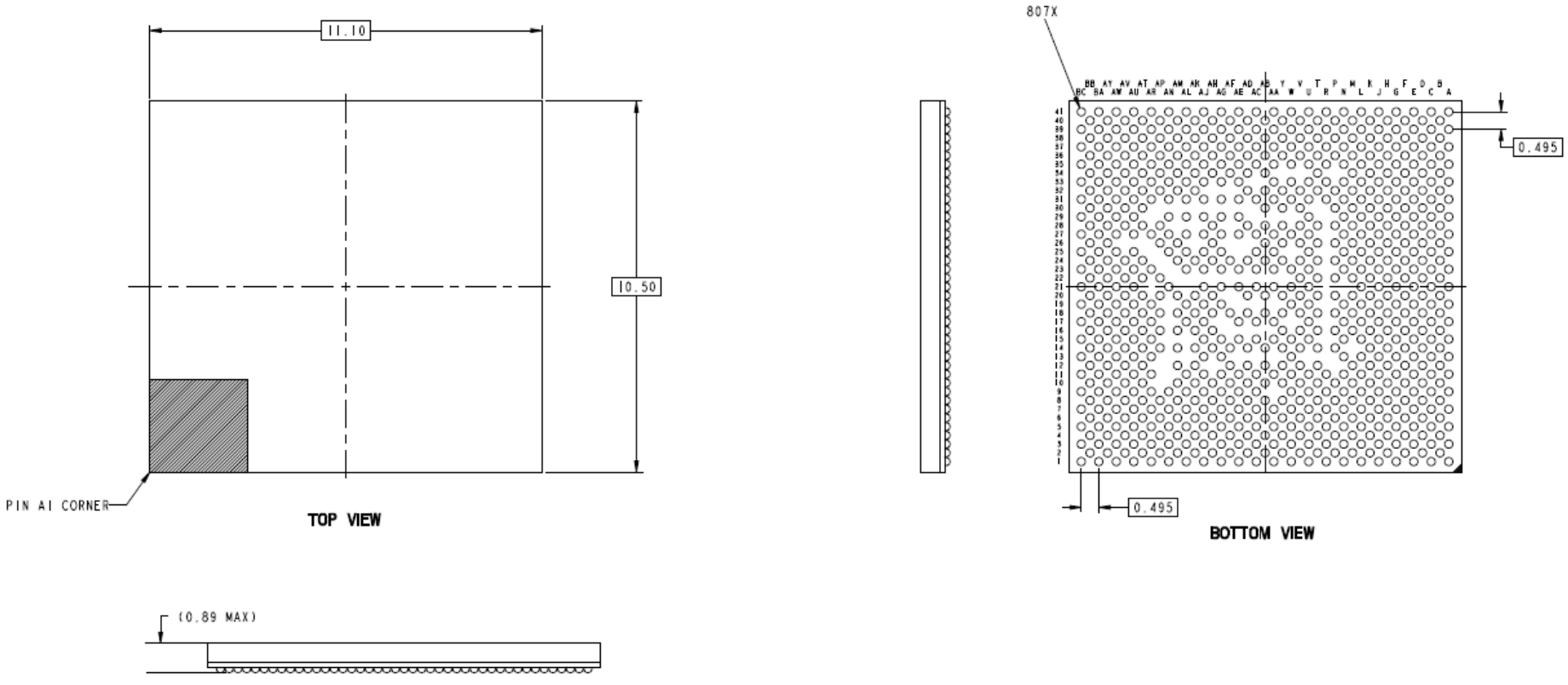


Figure 4-1 PSP807 outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

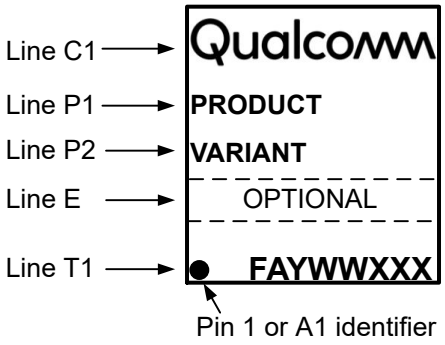


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	[PRODUCT]	Qualcomm Technologies, Inc. (QTI) product name ▪ SM6225
P2	[VARIANT]	Device variant information ▪ See Table 4-4 for the assigned values.
E	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ▪ F = F (TSMC) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = U (Amkor, China) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Ball A1 indicator

NOTE For complete marking definitions of all SM6225 variants and revisions, see the *SM6225 Device Revision Guide* (80-26896-4).

Table 4-2 QFPROM_CORR_PTE_ROW0_LSB

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants (see Table 4-4).
bits [19:0]	JTAG_ID	These bits map to bits of the hardware revision number (see Table 4-4).

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in the following table.

Table 4-3 Device identification code

Device ID code	AA-AAAA	-P	-TTT	NNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	SM-6225	-0	-PSP	807			-MT	-00	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/ program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example: SM-6225-0-PSP807-MT-00-0-AB

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	FEATURE_ID (see Table 4-2) [b]	Hardware revision number (JTAG_ID see Table 4-2)	Hardware version	Source configuration code (S) [c]	Comments	Sample date
SM6225	ES	000-AB	0x0	0x0 01B8 0E1	1.0	0	SM6225 Gold CPU at 2.4 GHz, Silver CPU at 1.9 GHz, FHD+ 90 Hz, triple ISP, GPU at 1115 MHz, dual HVX at 614 MHz	08/10/2021
SM6225	CS	000-AB	0x0	0x0 01B8 0E1	1.0	0	SM6225 Gold CPU at 2.4 GHz, Silver CPU at 1.9 GHz, FHD+ 90 Hz, triple ISP, GPU at 1115 MHz, dual HVX at 614 MHz	10/10/2021

Table 4-4 Device identification details (cont.)

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	FEATURE_ID (see Table 4-2) [b]	Hardware revision number (JTAG_ID see Table 4-2)	Hardware version	Source configuration code (S) [c]	Comments	Sample date
		CS date codes are as follows: ■ SPIL: 138 ■ ASE: 139 ■ Amkor: 138						
SM6225	CS	000-AD CS date codes are as follows: ■ SPIL: 227 ■ ASE: 227	0x9	0x0 01B8 0E1	1.0	0	SM6225 Gold CPU at 2.8 GHz, Silver CPU at 1.9 GHz, FHD+ 120 Hz, triple ISP, GPU at 1260 MHz, dual HVX at 614 MHz	30/06/2022

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
[b] The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-5.

Table 4-5 Source configuration code

S value	F value = F	A value = E	A value = U	A value = K
0	TSMC	ASE, Taiwan	Amkor, China	SPIL, Taiwan

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH **SM6225 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory baking before use. After baking, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM6225 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SM6225 Package Thermal Model Icepak* (HS11-26896-5HW) and the *SM6225 Package Thermal Model FloTHERM* (HS11-26896-6HW) from the CreatPoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-26896-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-26896-6HW

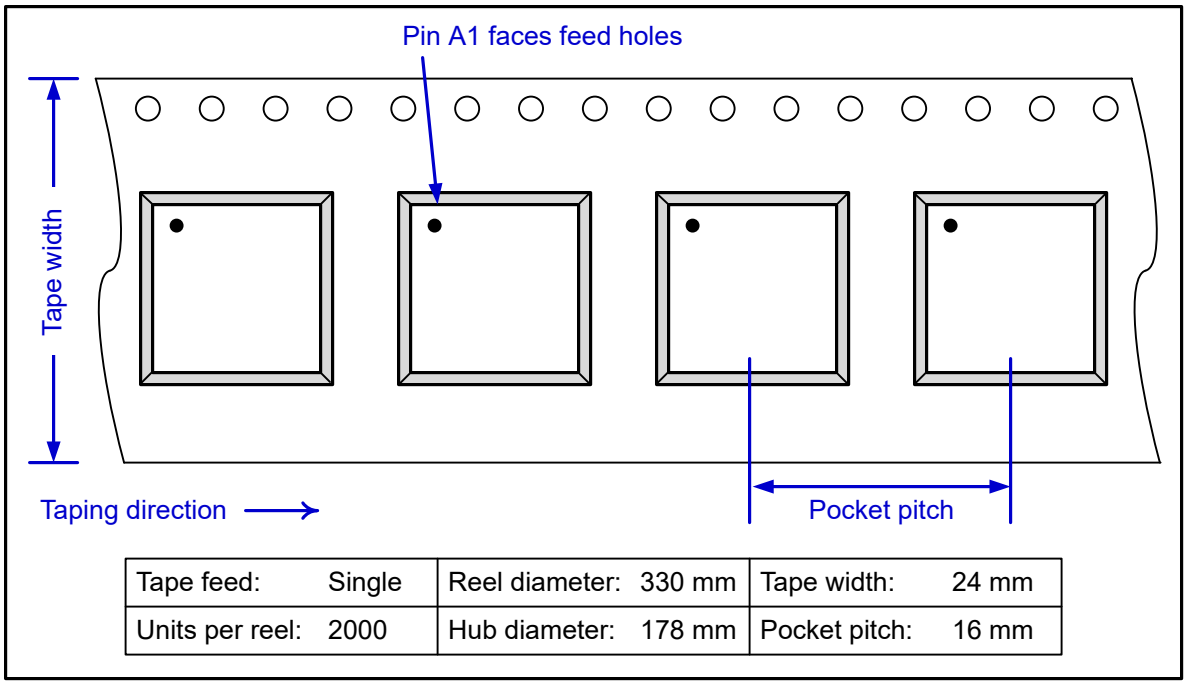
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM6225 tape carrier is shown in the following figure, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in the following figure.

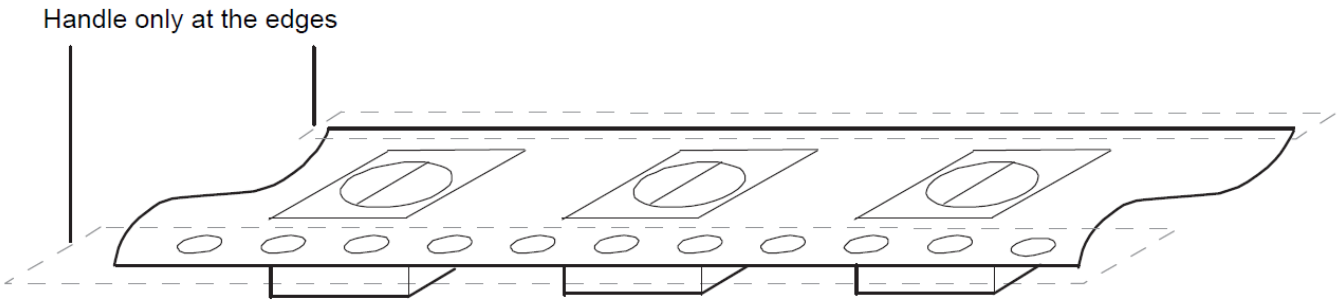


Figure 5-2 Tape handling

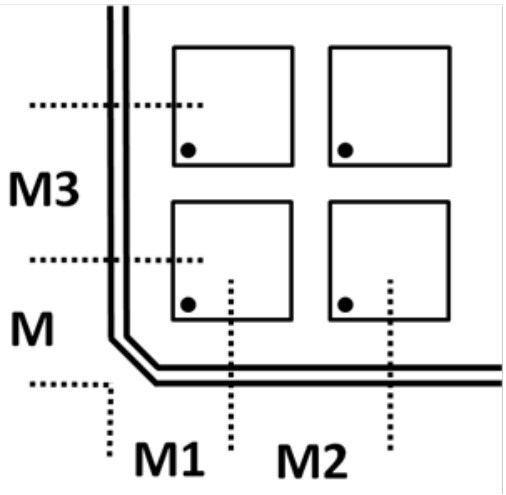
5.1.2 Matrix tray information

Matrix tray media is available for sampling only.

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See the following figure for matrix-tray key attributes and dimensions.



Key dimensions (mm)	
Array	8 × 21 (168)
M	11.95
M1	11.00
M2	14.65
M3	16.00

Figure 5-3 Matrix tray orientation

5.2 Storage

5.2.1 Bagged storage conditions

SM6225 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM6225 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is necessary to bake the SM6225 if any condition specified in Section 5.2.1 or Section 5.2.2 has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80- VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the SM6225 ESD ratings.

5.3.3 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualifications summary

SM6225 reliability evaluation report for PSP807 device.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (total samples from three different wafer lots). See reliability report shared earlier.	1004	Pass[a] DPPM < 1000
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (total samples from three different wafer lots)	1004	Pass[a] FIT < 100
Mean time to failure (MTTF) t = 1/λ in million hours (total samples from three different wafer lots)	1004	Pass[a] > 10
ESD – human-body model (HBM) rating JS001-2017 (total samples from one wafer lot)	21	Pass ±1000V
ESD – charged-device model (CDM) rating JS-002-2014 (total samples from one wafer lot)	6	Pass ± 250 V
Latch-up (I-test): EIA/JESD78E Trigger current: ±100 mA; temperature: 85°C (total samples from one wafer lot)	6	Pass Class II, Level A
Latch-up (Vsupply overvoltage): EIA/JESD78E Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 85°C (total samples from one wafer lot)	6	Pass Class II, Level A

[a] SM6225 HTOL data 0F/95, additional data leveraged from other 6FF of the same process technology node process products (0F/909).

Table 7-2 Package reliability results

Tests, standards, and conditions	ASE sample size	SPIL sample size	ATC sample size	Result
Moisture resistance test (MRT): J-STD-020C MSL 3, reflow at 260 +0/-5°C (total samples from three different assembly lots)	719	720	715	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 500,1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (cph)	240	240	240	Pass

Table 7-2 Package reliability results (cont.)

Tests, standards, and conditions	ASE sample size	SPIL sample size	ATC sample size	Result
Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (total samples from three different assembly lots)				
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (total samples from three different assembly lots)	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (total samples from three different assembly lots)	120	120	120	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (total samples from three different assembly lots)	240	240	240	Pass
Flammability Note: Flammability test – not required UL-STD-94 Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	–	–
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (total samples from three different assembly lots at each SAT)	30	30	30	Pass
Solder bump shear (total samples from three different assembly lots at each SAT)	30	30	30	Pass[a]
Solder ball shear: JESD22-B117 (total samples from three different assembly lots at each SAT)	30	30	30	Pass[a]
Internal/external visual (total samples from three different assembly lots at each SAT)	30	30	30	Pass

[a] Data is leveraged from other previously qualified PSP packages that are similar to this configuration.

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	SM6225
Package type	PSP807
Package body size	11.1 × 10.5 × 0.89 mm

Table 7-3 Device characteristics (cont.)

Category	Definition
Ball count	807
Ball composition	SAC125/Ni
Fab process	6 nm
Supply sources (fab sites)	TSMC
Assembly sites	■ ASE, Taiwan ■ Amkor, China ■ SPIL, Taiwan
Solder ball pitch	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	June 2021	Initial release
AB	August 2021	■ Table 1-1 *SM6225 features*: Updated the GNSS and SPI capabilities ■ Table 1-3 *Position location and navigation summary*: Updated the GNSS capability ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Updated the table ■ Section 4.2 *Part marking*: Added new section ■ Section 4.3 *Device ordering information*: Added new section ■ Section 4.4 *Daisy chain devices*: Added new section
AC	September 16, 2021	■ Table 1-1 *SM6225 features*: Updated audio interfaces capability ■ Figure 2-1 *SM6225 pin assignments*: Updated the figure ■ Table 2-2 *Pin descriptions – general pins*: Removed AA37 and AB38 pins ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Removed functions that are not supported for GPIO_102–GPIO_105 ■ Table 2-4 *Pin descriptions – DNC, ground, and power-supply pins*: Added AA37 and AB38 to DNC pins list
AD	October 2021	■ Added the following chapters and sections: □ Chapter 3 *Electrical specifications* □ Section 4.4 *Device moisture sensitivity level* □ Section 4.5 *Thermal characteristics* □ Chapter 5 *Carrier, storage, and handling information* □ Chapter 6 *PCB mounting guidelines* ■ Table 4-4 *Device identification details*: Updated the table
AE	November 2021	Added the following chapters and sections: ■ Section 3.4.2 *Dhrystone and rock bottom maximum power* ■ Section 3.5 *Power sequencing* ■ Section 3.6 *Digital-logic characteristics* ■ Section 3.7 *Timing characteristics* ■ Chapter 7 *Part reliability*
AF	November 19, 2021	■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Updated the table ■ Added the following sections: Section 3.8 *Memory support* through Section 3.12 *RF and power management interfaces*
AG	December 2021	■ Table 7-3 *Device characteristics*: Updated the solder ball pitch
AH	January 2022	■ Table 2-2 *Pin descriptions – general pins*: Updated the pad characteristics ■ Table 3-7 *DC specification of 1.8 V GPIOs and WCSS WSI I/Os*: Updated the table ■ Table 3-13 *Digital I/O characteristics for VDDPX_10 nominal (UFS)*: Updated the table
Revision AI was omitted in accordance with QTI document conventions.		
AJ	May 2022	Table 3-3 *Operating conditions*: Updated the values for VDD_A_USBHS_0P9
AK	June 2022	■ Cover page *Device description*: Updated for SM6225-AD information ■ Cover page *Key features*: Updated for SM6225-AD information ■ Table 1-1 *SM6225 features*: Updated for SM6225-AD information

Revision	Date	Description
		■ Table 3-6 *Dhrystone and rock bottom maximum power*: Updated for SM6225-AD information ■ Table 4-4 *Device identification details*: Added SM6225-AD sample information
AL	July 2022	Table 4-4 *Device identification details*: Added the CS date codes

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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