Device description

SM6350 includes the next generation of the Qualcomm® Snapdragon™ 600 series processor with integrated 5G modem. It implements the 5G NR standard for sub-6 GHz bands.

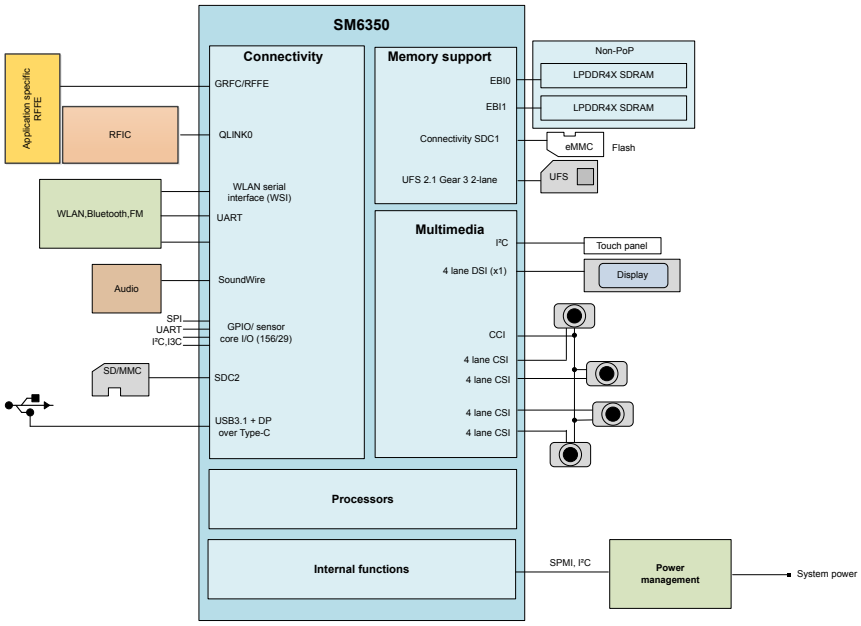
Key processor and memory characteristics include:

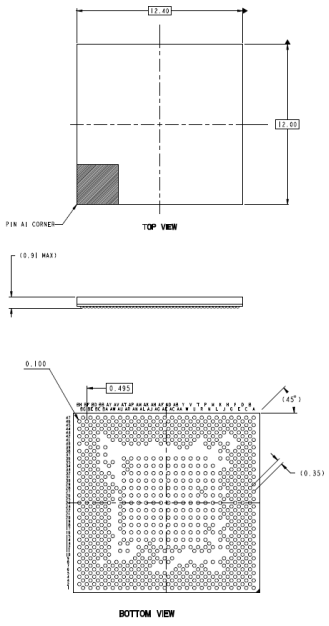
- 8 nm process for lower active power dissipation and faster CPU performance
- Non package-on-package (non-PoP), 0.35 mm pitch
- A customized 64-bit Arm v8 compliant applications processor Qualcomm® Kryo™ CPU 560
  - Kryo Gold: dual high-performance cores with 2.0 GHz
  - Kryo Silver: hexa low-power cores with 1.7 GHz
- Qualcomm® Adreno™ GPU 619 at 565 MHz
- Dedicated compute DSP for computer vision and video post processing. Qualcomm® Hexagon™ DSP with dual Hexagon Vector eXtensions (HVX) 512 processor
- Low-power island (LPI) – contains DSP shared between Snapdragon sensor core and low-power audio subsystem. The Snapdragon sensor supports always-on use cases
- Dual-channel non-PoP high-speed memory, LPDDR4X SDRAM designed for clock (2 × 16 bit) at 1866 MHz
- Qualcomm® Universal Bandwidth Compression (UBWC) 2.0 compression with camera, DSP, and display

Key features

- Always-on subsystem with RPMh for hardware-based resource and power management
- More RF operating bands and advanced techniques with SDR735:
  - 3G/4G/5G modem– sub-6 GHz bands (Rel. 15 integrated modem)
  - Uplink 256 QAM and downlink 256 QAM support for sub-6
  - Downlink 4 × 4 MIMO and uplink 2 × 2 MIMO support for sub-6
  - Uplink 256 QAM and downlink 256 QAM support for LTE
  - WCDMA, CDMA up to 1x advanced, and 1xEV-DOrA
- Display support: FHD+ 10-bit, 60/90/120 Hz support, eight hardware layers, improved HDR10, wide color gamut, Qualcomm® Low-Power Picture Enhancement display feature, and DisplayPort support
- One 4-lane DSI supports D-PHY 1.2 and C-PHY 1.0
- Triple 14-bit image signal processing (ISP) + 1 lite ISP: 16 + 16 + 16 MP, 32 MP at 30 fps ZSL
- Four 4-lane CSIs (4/4/4/4) D-PHY 1.2 at 2.5 Gbps per lane or C-PHY 1.0 at 17 Gbps (5.71 Gbps/trio on three trios per port)
- Support for USB 3.1 Gen1 Type-C with DisplayPort 1.4 and USB 2.0
- WCN3991: WLAN 2 × 2 802.11a/b/g/n/ac, no DBS support, Bluetooth 5.1 compliant, and FM

SM6350 high-level block diagram and 837 PSP drawing





Contents

Tables

Figures

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

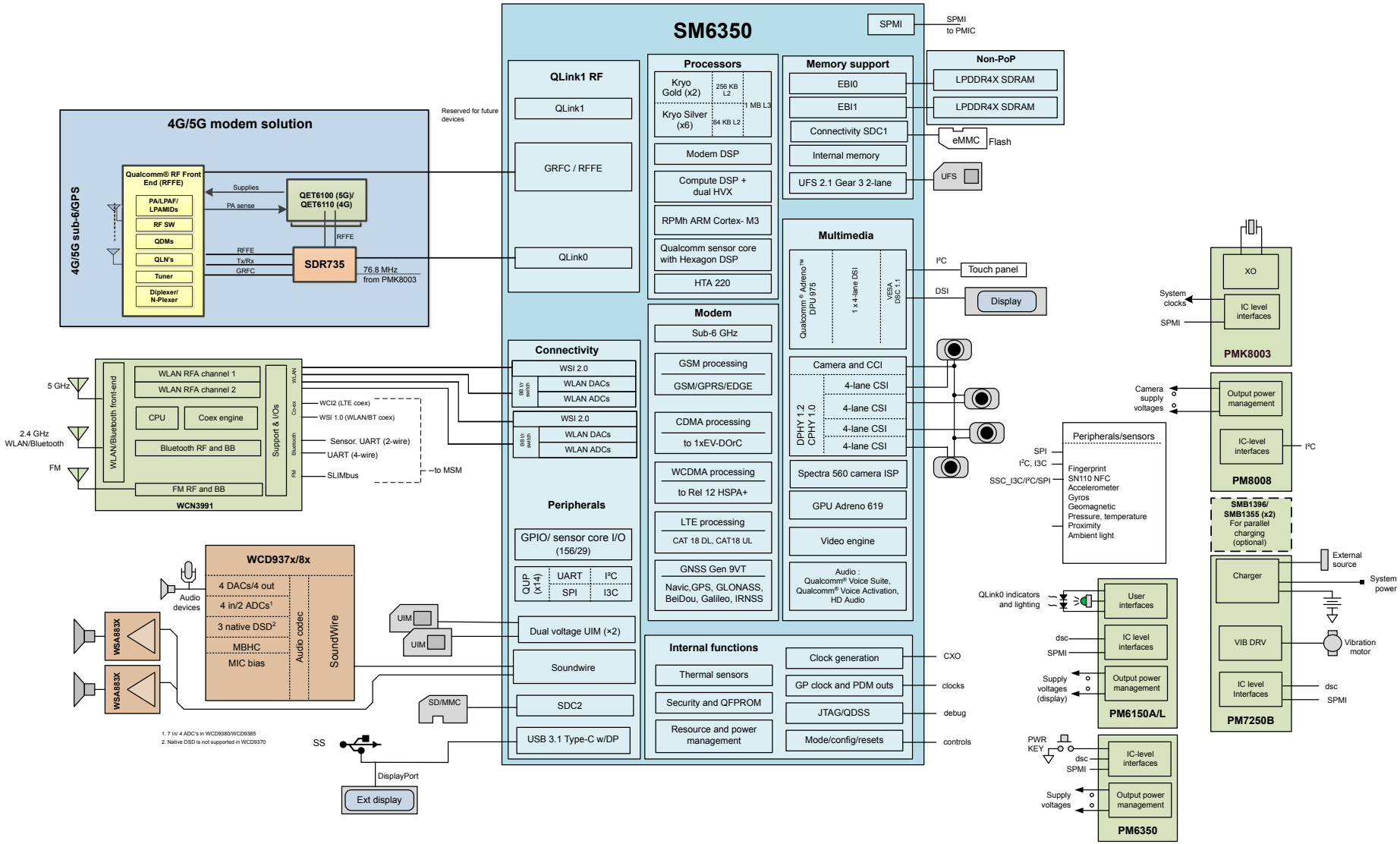


Figure 1-1 SM6350 functional block diagram

1.2 SM6350 features

NOTE Some of the hardware features integrated within the SM6350 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM6350 features.

Table 1-1 SM6350 features

Feature	SM6350 capability
Processors	
Applications	64 bit applications processor (Kryo) with 1 MB L3 cache ■ Dual high-performance Kryo cores – Gold cluster with 256 KB L2 cache per core at 2.0 GHz ■ Hexa low-power Kryo cores – Silver cluster with 64 KB L2 cache per core at 1.7 GHz
Digital signal processing	Compute DSP dual HVX 512; Hexa low-power Kryo cores – Silver cluster with 512 KB L2 cache per core
Always-on system	Always-on subsystem with always-on processor RPMh with hardware accelerators for voltage control and regulation, clock management, and resource communication
Artificial intelligence	Qualcomm hexagon tensor accelerator (HTA) 220 with deep learning BW compression (DLBC) for performance and always-on neural network (NN) use cases. It incorporates a neural network matrix engine to ensure efficient execution of various neural networks and their parameters. The HTA may be used for typical imaging, video, audio, and data-based NN use cases and will be used in conjunction with the compute Hexagon DSP subsystem.
Memory support	
System memory via EBI	Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM (2 × 16 bit) at 1866 MHz 768 KB system cache
Other internal memory	184 KB IMEM 512 KB GMEM for graphics
External memory Via	UFS 2.1 gear 3 (two-lane), eMMC 5.1, and SD 3.0 Note: eMMC requires external LDO if UFS is used. Simultaneous use of e-MMC and UFS is not supported by PMIC.
RF support	
RF operating bands	Defined by the RF transceiver SDR device
Air interfaces 5G GSM CDMA WCDMA TD-SCDMA LTE WLAN/Bluetooth GNSS – Integrated Qualcomm® Location Suite engine	 Yes (Sub-6 and 5G NR) Yes Yes Yes Yes Yes (Cat18 DL, Cat18 UL) Yes (with WCN3991) Gen 9; GPS, GLONASS, BeiDou, Galileo, NavIC, and IRNSS
Multimedia Display support	

Table 1-1 SM6350 features (cont.)

Feature	SM6350 capability
MIPI-DSI	One 4-lane; DSI D-PHY 1.2, C-PHY 1.0
DisplayPort	DisplayPort 1.4. Split link not supported
Mobile display processor	Adreno DPU 975
Example combinations	2520 × 1080 60 fps + QHD60 via DisplayPort
General display features	Color depth – 30-bit per pixel; TFT, LTPS, CSTN, and OLED panels
Camera interfaces	3 × ISP, 1 × ISP-lite, 16 + 16 + 16 MP ZSL, MCTF
MIPI-CSI	MIPI combination D-PHY 1.2 /C-PHY 1.0 configurable in 4/4/4/4, 32 MP, 30 fps 4 × 4-lane CSI ■ D-PHY: 2.1 Gbps/lane ■ C-PHY: ~17 Gbps (5.7 Gbps per trio)
Performance	■ Real-time sensor input resolution: 16 + 16 + 16 MP ■ 32 MP, 30 ZSL with dual ISP
Video applications performance	
Encode	4K30 8-bit: H.265
Decode	4K30 10-bit: H.265, VP9
Concurrency	4K30 playback + 1080p30 encode
Graphics	■ Adreno 619 GPU ■ OpenGL ES 3.2, Vulkan, DX12.2 ■ OpenCL2.0
Audio Option 1: WCD9370 codec + WSA8830/WSA8835 speaker amplifier Option 2: WCD9375 codec + WSA8830/WSA8835 speaker amplifier Option 3: WCD9380 codec + WSA8830/WSA8835 speaker amplifier Option 4: WCD9385 codec + WSA8830/WSA8835 speaker amplifier	
Voice codec support	■ EVRC, EVRC-B, and EVRC-WB ■ G.711 and G.729A/AB ■ GSM-FR, GSM-EFR, and GSM-HR ■ AMR-NB, AMR-WB, AMR-eAMR, and AMR-BeAMR
Audio codec support	■ MP3 ■ AAC ■ HE AACv1, v2 ■ WMA 9/Pro ■ Dolby AC-3 ■ eAC-3 ■ DTS-HD ■ FLAC ■ APE ■ ALAC ■ AIFF
Enhanced audio	■ Surround sound: Dolby Digital and Dolby Atmos ■ Qualcomm® Audio Post-processing ■ Qualcomm® Noise and Echo Cancellation v7 and Qualcomm Voice Suite v3
Connectivity	

Table 1-1 SM6350 features (cont.)

Feature	SM6350 capability
Qualcomm universal peripheral (QUP) ports	14 QUP ports, multiplexed serial interface functions (eights ports on GPIO and six ports on LPI GPIO)
UART	UART interface; eight on GPIO and two on LPI GPIO
I^2C	I^2C interface; eight on GPIO and four on LPI GPIO
I3C	I3C interface; one on GPIO and two on LPI GPIO
SPI	SPI interfaces; four on GPIO and two on LPI GPIO
CCI I^2C	CCI I^2C interface: four dedicated I^2C interfaces for camera
UIM	Two – dual voltages (1.8 V and 2.95 V)
USB	USB 3.1, and DisplayPort support over Type-C (split link not supported)
Secure digital interfaces	■ 8 bit port SDC1 for eMMC 5.1-bit and 4-bit port SDC2 for SD3.0 ■ SDC2 is dual-voltage ■ SD/MMC card; UFS
Audio interfaces	
USB	Audio over USB Type-C
I^2S	Four MI^{2}S ports, two I^2S ports
SWR	SoundWire interface
Wireless connectivity	WCN3991 2 × 2 802.11ac RF
Touchscreen support	Capacitive panels via ext IC (I^2C)
Configurable GPIOs	
Number of GPIO ports	156 (including 29 for Sensor I/O)
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment (TEE), hardware supported KeyStore
Crypto engines	Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), inline crypto engine (FIPS-compliant)
TrustZone services	Secure file system, fast trusted storage
DRM support in hardware	PlayReady SL2000/SL3000, Widevine level 1, ISDB-T, and CPZ for GPU and DSP
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, QDSS, embedded USB debug (EUD), and ETM
Others	Thermal sensors, modes and resets, and peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
SDR RF transceivers	
QLink0 digital interface	Five QLink pairs (SDR735)
QLink1 digital interface	Seven QLink pairs. (Reserved for future devices. Do not connect SDR735 with QLINK1)
Power management	PM6350, PM6150A/PM6150L, PM7250B, PM8008 (camera), SMB1396/SMB1355, and PMK8003

Table 1-1 SM6350 features (cont.)

Feature	SM6350 capability
Wireless connectivity	
WLAN baseband data	I/Q differential pair interface
Bluetooth	UART interface
Fabrication technology and package	
Digital die	8 nm process for lower active power dissipation
Non-PoP – small, thermally efficient package	837 PSP: 12.4 × 12.0 × 0.91 mm; 0.35 mm pitch

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
3GPP 5G Rel.15	■ Sub-6 GHz, 5G NR - FDD < 3 GHz, TDD frequencies + n41, n70, n77, n78, and n79 ■ Standalone mode (SA) and non-standalone mode (NSA) support for TDD ■ 256 QAM for uplink and downlink ■ DL 4 × 4 MIMO SA/NSA mode and UL 2 × 2 MIMO SA mode support for sub-6 ■ FR1 UL (2 × 2) MIMO in SA TDD mode ■ UL and DL bandwidth - 100 MHz ■ SRS 1T4R for NSA, 1T4R and 2T4R for SA ■ HPUE support for power class three ■ SCS - 30 KHz (TDD), 15 KHz (FDD) ■ LTE reframe band support for 5G (both SA and NSA, FDD)
3GPP LTE Rel.15	■ Cat18 download and upload ■ TM9 ■ Four-way Rx diversity ■ 4 × 4 MIMO using single LTE-TRx ■ HPUE support for power class three ■ UL bandwidth - 40 MHz, DL bandwidth - 80 MHz ■ 64 QAM for uplink and 256 QAM for downlink
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1x SLTE and 1x SRLTE ■ hVoLTE and hSRLTE
Multi-SIM	
5G + 4G	5G/4G/3G/2G (SIM1) + 4G/3G/2G (SIM2)
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/5G - Wi-Fi selection

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite with global navigation satellite system (GNSS) support	
Gen 9	GPS, GLONASS, BeiDou, Galileo, NavIC, and IRNSS

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN3991	802.11ac, 2 × 2 MIMO
Bluetooth	
With WCN3991	Bluetooth 5.1 compliant
FM	
With WCN3991	Rx

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX_2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX_6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX_7	Pad group 7 (eMMC); tied to VDD_P7 pins (1.8 V only)
PX_10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.2 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_A_CSI_X_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_A_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SM6350 is available in the 837 PSP. See Mechanical information for package details. A high-level view of the pin assignments is shown in the Figure 2-1. The text within the figure is difficult to read when viewing an

8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM6350 Pin Assignment and GPIO Configuration Spreadsheet* (80-PT056-1A). This Microsoft Excel spreadsheet lists all SM6350 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the pin assignment spreadsheet (80-PT056-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PT056-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

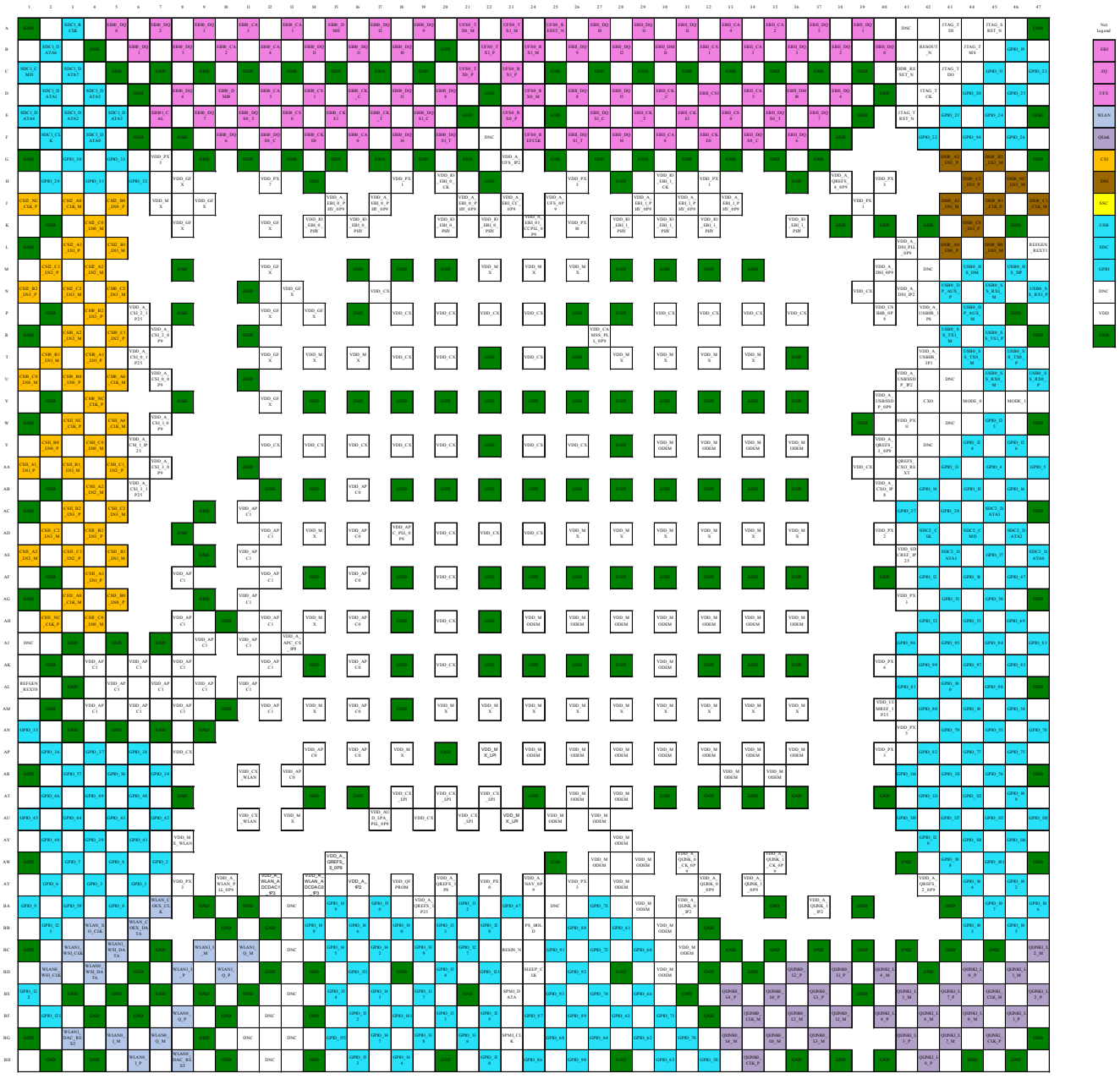


Figure 2-1 SM6350 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions - general pins

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
U5	CSI0_A0_CLK_M	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
T4	CSI0_A1_LN1_P	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
R3	CSI0_A2_LN2_M	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
U3	CSI0_B0_LN0_P	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY). trio lane 0 – B
T2	CSI0_B1_LN1_M	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
P4	CSI0_B2_LN3_P	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
U1	CSI0_C0_LN0_M	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
R5	CSI0_C1_LN2_P	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
N5	CSI0_C2_LN3_M	–	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
V4	CSI0_NC_CLK_P	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
W5	CSI1_A0_CLK_M	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A
AA1	CSI1_A1_LN1_P	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A
AB4	CSI1_A2_LN2_M	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A
Y2	CSI1_B0_LN0_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
AA3	CSI1_B1_LN1_M	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B
AC3	CSI1_B2_LN3_P	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B
Y4	CSI1_C0_LN0_M	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
AA5	CSI1_C1_LN2_P	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C
AC5	CSI1_C2_LN3_M	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C
W3	CSI1_NC_CLK_P	–	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
J3	CSI2_A0_CLK_M	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential clock – negative MIPI CSI 2 (C-PHY), trio lane 0 – A
L3	CSI2_A1_LN1_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 1– positive MIPI CSI 2 (C-PHY), trio lane 1 – A
M4	CSI2_A2_LN2_M	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – negative MIPI CSI 2 (C-PHY), trio lane 2 – A
J5	CSI2_B0_LN0_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
L5	CSI2_B1_LN1_M	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 – negative MIPI CSI 2 (C-PHY), trio lane 1 – B
N1	CSI2_B2_LN3_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – positive MIPI CSI 2 (C-PHY), trio lane 2 – B
K4	CSI2_C0_LN0_M	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – negative MIPI CSI 2 (C-PHY), trio lane 0 – C
M2	CSI2_C1_LN2_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – positive MIPI CSI 2 (C-PHY), trio lane 1 – C
N3	CSI2_C2_LN3_M	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – negative MIPI CSI 2 (C-PHY), trio lane 2 – C
J1	CSI2_NC_CLK_P	–	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential clock – positive MIPI CSI 2 (C-PHY), trio lane – no connect
AG3	CSI3_A0_CLK_M	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A
AF4	CSI3_A1_LN1_P	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 1– positive MIPI CSI 3 (C-PHY), trio lane 1 – A
AE1	CSI3_A2_LN2_M	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A
AG5	CSI3_B0_LN0_P	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B
AE5	CSI3_B1_LN1_M	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B
AD4	CSI3_B2_LN3_P	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
AH4	CSI3_C0_LN0_M	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C
AE3	CSI3_C1_LN2_P	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C
AD2	CSI3_C2_LN3_M	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C
AH2	CSI3_NC_CLK_P	–	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), trio lane – no connect
V42	CXO	–	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
C41	DDR_RESET_N	–	PX_1	DO	LPDDR4X reset (shared by EBI0 and EBI1)
L43	DSI0_A0_LN0_P	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – positive MIPI DSI 0 (C-PHY), trio lane 0 – A
J43	DSI0_A1_LN1_M	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – negative MIPI DSI 0 (C-PHY), trio lane 1 – A
G43	DSI0_A2_LN2_P	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – positive MIPI DSI 0 (C-PHY), trio lane 2 – A
L45	DSI0_B0_LN0_M	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – negative MIPI DSI 0 (C-PHY), trio lane 0 – B
J45	DSI0_B1_CLK_P	–	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – positive MIPI DSI 0 (C-PHY), trio lane 1 – B
G45	DSI0_B2_LN2_M	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – negative MIPI DSI 0 (C-PHY), trio lane 2 – B
K44	DSI0_C0_LN1_P	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – positive MIPI DSI 0 (C-PHY), trio lane 0 – C
J47	DSI0_C1_CLK_M	–	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – negative MIPI DSI 0 (C-PHY), trio lane 1 – C
H44	DSI0_C2_LN3_P	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3 – positive MIPI DSI 0 (C-PHY), trio lane 2 – C
H46	DSI0_NC_LN3_M	–	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3 – negative MIPI DSI 0 (C-PHY), no connect
F16	EBI0_CA0	–	EBI	DO	EBI1 LPDDR4X command/address bit 0
A13	EBI0_CA1	–	EBI	DO	EBI1 LPDDR4X command/address bit 1
B10	EBI0_CA2	–	EBI	DO	EBI1 LPDDR4X command/address bit 2
A11	EBI0_CA3	–	EBI	DO	EBI1 LPDDR4X command/address bit 3
B12	EBI0_CA4	–	EBI	DO	EBI1 LPDDR4X command/address bit 4
D12	EBI0_CA5	–	EBI	DO	EBI1 LPDDR4X command/address bit 5
E7	EBI01_CAL	–	EBI	AL	EBI0 LPDDR4X calibration resistor
F14	EBI0_CKE0	–	EBI	DO	EBI0 LPDDR4X clock enable 0
E15	EBI0_CKE1	–	EBI	DO	EBI0 LPDDR4X clock enable 1

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
D16	EBI0_CK_C	–	EBI	DO	EBI0 LPDDR4X differential clock (C)
E17	EBI0_CK_T	–	EBI	DO	EBI0 LPDDR4X differential clock (T)
E13	EBI0_CS0	–	EBI	DO	EBI0 LPDDR4X chip select 0
D14	EBI0_CS1	–	EBI	DO	EBI0 LPDDR4X chip select 1
D10	EBI0_DMI0	–	EBI	DO	EBI0_DMI0 data mask byte 0
A15	EBI0_DMI1	–	EBI	DO	EBI0_DMI0 data mask byte 1
A5	EBI0_DQ0	–	EBI	B	EBI0 LPDDR4X data bit 0
B6	EBI0_DQ1	–	EBI	B	EBI0 LPDDR4X data bit 1
B18	EBI0_DQ10	–	EBI	B	EBI0 LPDDR4X data bit 10
B16	EBI0_DQ11	–	EBI	B	EBI0 LPDDR4X data bit 11
A17	EBI0_DQ12	–	EBI	B	EBI0 LPDDR4X data bit 12
B14	EBI0_DQ13	–	EBI	B	EBI0 LPDDR4X data bit 13
F18	EBI0_DQ14	–	EBI	B	EBI0 LPDDR4X data bit 14
D18	EBI0_DQ15	–	EBI	B	EBI0 LPDDR4X data bit 15
A7	EBI0_DQ2	–	EBI	B	EBI0 LPDDR4X data bit 2
A9	EBI0_DQ3	–	EBI	B	EBI0 LPDDR4X data bit 3
D8	EBI0_DQ4	–	EBI	B	EBI0 LPDDR4X data bit 4
B8	EBI0_DQ5	–	EBI	B	EBI0 LPDDR4X data bit 5
F10	EBI0_DQ6	–	EBI	B	EBI0 LPDDR4X data bit 6
E9	EBI0_DQ7	–	EBI	B	EBI0 LPDDR4X data bit 7
D20	EBI0_DQ8	–	EBI	B	EBI0 LPDDR4X data bit 8
A19	EBI0_DQ9	–	EBI	B	EBI0 LPDDR4X data bit 9
F12	EBI0_DQS0_C	–	EBI	B	EBI0 LPDDR4X data strobe 0 (C)
E11	EBI0_DQS0_T	–	EBI	B	EBI0 LPDDR4X data strobe 0 (T)
E19	EBI0_DQS1_C	–	EBI	B	EBI0 LPDDR4X data strobe 1 (C)
F20	EBI0_DQS1_T	–	EBI	B	EBI0 LPDDR4X data strobe 1 (T)
F30	EBI1_CA0	–	EBI	DO	EBI1 LPDDR4X command/address bit 0
B32	EBI1_CA1	–	EBI	DO	EBI1 LPDDR4X command/address bit 1
A35	EBI1_CA2	–	EBI	DO	EBI1 LPDDR4X command/address bit 2
B34	EBI1_CA3	–	EBI	DO	EBI1 LPDDR4X command/address bit 3
A33	EBI1_CA4	–	EBI	DO	EBI1 LPDDR4X command/address bit 4
D34	EBI1_CA5	–	EBI	DO	EBI1 LPDDR4X command/address bit 5
F32	EBI1_CKE0	–	EBI	DO	EBI1 LPDDR4X clock enable 0
E31	EBI1_CKE1	–	EBI	DO	EBI1 LPDDR4X clock enable 1
D30	EBI1_CK_C	–	EBI	DO	EBI1 LPDDR4X differential clock (C)
E29	EBI1_CK_T	–	EBI	DO	EBI1 LPDDR4X differential clock (T)
E33	EBI1_CS0	–	EBI	DO	EBI1 LPDDR4X chip select 0

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
D32	EBI1_CS1	–	EBI	DO	EBI1 LPDDR4X chip select 1
D36	EBI1_DMI0	–	EBI	DO	EBI1 LPDDR4X data mask for byte 0
B30	EBI1_DMI1	–	EBI	DO	EBI1 LPDDR4X data mask for byte 1
B40	EBI1_DQ0	–	EBI	B	EBI1 LPDDR4X data bit 0
A39	EBI1_DQ1	–	EBI	B	EBI1 LPDDR4X data bit 1
A27	EBI1_DQ10	–	EBI	B	EBI1 LPDDR4X data bit 10
A29	EBI1_DQ11	–	EBI	B	EBI1 LPDDR4X data bit 11
B28	EBI1_DQ12	–	EBI	B	EBI1 LPDDR4X data bit 12
A31	EBI1_DQ13	–	EBI	B	EBI1 LPDDR4X data bit 13
F28	EBI1_DQ14	–	EBI	B	EBI1 LPDDR4X data bit 14
D28	EBI1_DQ15	–	EBI	B	EBI1 LPDDR4X data bit 15
B38	EBI1_DQ2	–	EBI	B	EBI1 LPDDR4X data bit 2
B36	EBI1_DQ3	–	EBI	B	EBI1 LPDDR4X data bit 3
D38	EBI1_DQ4	–	EBI	B	EBI1 LPDDR4X data bit 4
A37	EBI1_DQ5	–	EBI	B	EBI1 LPDDR4X data bit 5
F36	EBI1_DQ6	–	EBI	B	EBI1 LPDDR4X data bit 6
E37	EBI1_DQ7	–	EBI	B	EBI1 LPDDR4X data bit 7
D26	EBI1_DQ8	–	EBI	B	EBI1 LPDDR4X data bit 8
B26	EBI1_DQ9	–	EBI	B	EBI1 LPDDR4X data bit 9
F34	EBI1_DQS0_C	–	EBI	B	EBI1 LPDDR4X data strobe 0 (C)
E35	EBI1_DQS0_T	–	EBI	B	EBI1 LPDDR4X data strobe 0 (T)
E27	EBI1_DQS1_C	–	EBI	B	EBI1 LPDDR4X data strobe 1 (C)
F26	EBI1_DQS1_T	–	EBI	B	EBI1 LPDDR4X data strobe 1 (T)
V44	MODE_0	–	PX_3	DIS-PD:nppukp	Mode control bit 0 – unconnected for native mode
V46	MODE_1	–	PX_3	DIS-PD:nppukp	Mode control bit 1 – unconnected for native mode
BB24	PS_HOLD	–	PX_3	DO	Power-supply hold signal to PMIC
BF34	QLINK0_CLK_M	–	–	AI,AO	QLink clock – negative
BH34	QLINK0_CLK_P	–	–	AI,AO	QLink clock – positive
BF36	QLINK0_L2_M	–	–	AI,AO	QLink lane 2 – negative
BD36	QLINK0_L2_P	–	–	AI,AO	QLink lane 2 – positive
BG33	QLINK0_L4_M	–	–	AI,AO	QLink lane 4 – negative
BE33	QLINK0_L4_P	–	–	AI,AO	QLink lane 4 – positive
BG37	QLINK0_L3_M	–	–	AI,AO	QLink lane 3 – negative
BE37	QLINK0_L3_P	–	–	AI,AO	QLink lane 3 – positive

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
BG35	QLINK0_L0_M	–	–	AI,AO	QLink lane 0 – negative
BE35	QLINK0_L0_P	–	–	AI,AO	QLink lane 0 – positive
BF38	QLINK0_L1_M	–	–	AI,AO	QLink lane 1 – negative
BD38	QLINK0_L1_P	–	–	AI,AO	QLink lane 1 – positive
BE45	QLINK1_CLK_M	–	–	AI,AO	QLink clock – negative
BG45	QLINK1_CLK_P	–	–	AI,AO	QLink clock – positive
BG43	QLINK1_L7_M	–	–	AI,AO	QLink lane 7 – negative
BE43	QLINK1_L7_P	–	–	AI,AO	QLink lane 7 – positive
BD46	QLINK1_L1_M	–	–	AI,AO	QLink lane 1 – negative
BF46	QLINK1_L1_P	–	–	AI,AO	QLink lane 1 – positive
BC47	QLINK1_L2_M	–	–	AI,AO	QLink lane 2 – negative
BE47	QLINK1_L2_P	–	–	AI,AO	QLink lane 2 – positive
BF42	QLINK1_L8_M	–	–	AI,AO	QLink lane 8 – negative
BH42	QLINK1_L8_P	–	–	AI,AO	QLink lane 8 – positive
BF44	QLINK1_L0_M	–	–	AI,AO	QLink lane 0 – negative
BD44	QLINK1_L0_P	–	–	AI,AO	QLink lane 0 – positive
BE41	QLINK1_L3_M	–	–	AI,AO	QLink lane 3 – negative
BG41	QLINK1_L3_P	–	–	AI,AO	QLink lane 3 – positive
BD40	QLINK1_L4_M	–	–	AI,AO	QLink lane 4 – negative
BF40	QLINK1_L4_P	–	–	AI,AO	QLink lane 4 – positive
AA41	QREFS_CXO_REXT	–	PX_11	–	External resistor for on-die clocking
AL1	REFGEN_REXT0	–	PX_3	–	East-side high-speed interface – external resistor
L47	REFGEN_REXT1	–	PX_3	–	West-side high-speed interface – external resistor
BC23	RESIN_N	–	PX_0	DI	Reset input
B42	RESOUT_N	–	PX_3	DO	Reset output
F2	SDC1_CLK	–	PX_7	B-NP: pdpukp	Secure digital controller 1 clock
C1	SDC1_CMD	–	PX_7	B-NP: pdpukp	Secure digital controller 1 command
F4	SDC1_DATA0	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 0
D2	SDC1_DATA1	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 1
E3	SDC1_DATA2	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 2
E5	SDC1_DATA3	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 3

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
E1	SDC1_DATA4	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 4
D4	SDC1_DATA5	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 5
B2	SDC1_DATA6	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 6
C3	SDC1_DATA7	–	PX_7	B-NP: pdpukp	Secure digital controller 1 data bit 7
A3	SDC1_RCLK	–	PX_7	DI-PD: pdpukp	Secure digital controller 1 return clock
AD42	SDC2_CLK	–	PX_2	BH-NP: dpukp	Secure digital controller 2 clock
AD44	SDC2_CMD	–	PX_2	BH-NP: dpukp	Secure digital controller 2 command
AE47	SDC2_DATA0	–	PX_2	BH-NP: dpukp	Secure digital controller 2 data bit 0
AE43	SDC2_DATA1	–	PX_2	BH-NP: dpukp	Secure digital controller 2 data bit 1
AD46	SDC2_DATA2	–	PX_2	BH-NP: dpukp	Secure digital controller 2 data bit 2
AC45	SDC2_DATA3	–	PX_2	BH-NP: dpukp	Secure digital controller 2 data bit 3
BD24	SLEEP_CLK	–	PX_3	DI	Sleep clock
BG23	SPMI_CLK	–	PX_0	DO	Slave and PBUS interface for PMICs – clock
BE23	SPMI_DATA	–	PX_0	B	Slave and PBUS interface for PMICs – data
A45	JTAG_SRST_N	–	PX_3	DI-PU:nppdkp	JTAG reset for debug
D42	JTAG_TCK	–	PX_3	DI-PU:nppdkp	JTAG clock input
A43	JTAG_TDI	–	PX_3	DI-PU:nppdkp	JTAG data input
C43	JTAG_TDO	–	PX_3	DO-Z	JTAG data output
B44	JTAG_TMS	–	PX_3	DI-PU:nppdkp	JTAG mode select input
E41	JTAG_TRST_N	–	PX_3	DI PD:nppukp	JTAG reset

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
F24	UFS0_REFCLK	–	PX_10	DO-Z- PD:nppukp	UFS reference clock
A25	UFS0_RESET_N	–	PX_10	DO-Z- PD:nppukp	UFS reset
D24	UFS0_RX0_M	–	–	AI, AO	UFS receive lane 0 – negative
E23	UFS0_RX0_P	–	–	AI, AO	UFS receive lane 0 – positive
B24	UFS0_RX1_M	–	–	AI, AO	UFS receive lane 1 – negative
C23	UFS0_RX1_P	–	–	AI, AO	UFS receive lane 1 – positive
A21	UFS0_TX0_M	–	–	AI, AO	UFS transmit lane 0 – negative
C21	UFS0_TX0_P	–	–	AI, AO	UFS transmit lane 0 – positive
A23	UFS0_TX1_M	–	–	AI, AO	UFS transmit lane 1 – negative
B22	UFS0_TX1_P	–	–	AI, AO	UFS transmit lane 1 – positive
P44	USB0_DP_AUX_M	–	–	AI, AO	DisplayPort auxiliary channel – negative
N43	USB0_DP_AUX_P	–	–	AI, AO	DisplayPort auxiliary channel – positive
M44	USB0_HS_DM	–	–	AI, AO	USB high-speed data - negative
M46	USB0_HS_DP	–	–	AI, AO	USB high-speed data - positive
U45	USB0_SS_RX0_M	–	–	AI, AO	USB super-speed receive – negative
U47	USB0_SS_RX0_P	–	–	AI, AO	USB super-speed receive – positive
N45	USB0_SS_RX1_M	–	–	AI, AO	USB super-speed receive – negative
N47	USB0_SS_RX1_P	–	–	AI, AO	USB super-speed receive – positive
T44	USB0_SS_TX0_M	–	–	AI, AO	USB super-speed transmit – negative
T46	USB0_SS_TX0_P	–	–	AI, AO	USB super-speed transmit – positive
R43	USB0_SS_TX1_M	–	–	AI, AO	USB super-speed transmit – negative
R45	USB0_SS_TX1_P	–	–	AI, AO	USB super-speed transmit – positive
BH8	WLAN0_DAC_REXT	–	–	AI, AO	WLAN chain 0 digital-to-analog converter external resistor
BG5	WLAN0_I_M	–	–	AI, AO	WLAN 0 in-phase - negative
BH6	WLAN0_I_P	–	–	AI, AO	WLAN 0 in-phase - positive
BG7	WLAN0_Q_M	–	–	AI, AO	WLAN 0 quadrature - negative
BF8	WLAN0_Q_P	–	–	AI, AO	WLAN 0 quadrature - positive
BD2	WLAN0_WSI_CLK	–	PX_3	DO	Power for WSI0 PHY clock
BD4	WLAN0_WSI_DATA	–	PX_3	B	Power for WSI0 PHY data
BG3	WLAN1_DAC_REXT	–	–	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
BC9	WLAN1_I_M	–	–	AI, AO	WLAN 1 in-phase - negative
BD8	WLAN1_I_P	–	–	AI, AO	WLAN 1 in-phase - positive
BC11	WLAN1_Q_M	–	–	AI, AO	WLAN 1 quadrature - negative

Table 2-2 Pin descriptions - general pins (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad characteristics [a]		Functional description
			Voltage	Type	
BD10	WLAN1_Q_P	–	–	AI, AO	WLAN 1 quadrature - positive
BC3	WLAN1_WSI_CLK	–	–	AO	Power for WSI1 PHY clock
BC5	WLAN1_WSI_DATA	–	–	B	Power for WSI1 PHY data
BA7	WLAN_COEX_CLK	–	–	DO	WLAN coexistence module command clock
BB6	WLAN_COEX_DATA	–	–	B	WLAN coexistence module command data
BB4	WLAN_XO_CLK	–	–	AI	WLAN reference clock

[a] See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function - carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM6350 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the *SM6350 Pin Assignment and GPIO Configuration Spreadsheet* (80-PT056-1A) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PT056-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BA5	GPIO_0		PX_3	PD:nppukp	Configurable I/O	Y
		I3C_SDA		B	QUP 0 SE0, lane 0: I3C_SDA	
		SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO	
		UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP 0 SE0, lane 0: I2C_SDA	
AY6	GPIO_1		PX_3	PD:nppukp	Configurable I/O	N
		I3C_SCL		DO	QUP 0 SE0, lane 1: I3C_SCL	
		SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI	
		UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP 0 SE0, lane 1: I2C_SCL	
AW7	GPIO_2		PX_3	PD:nppukp	Configurable I/O	N
		SPI_SCLK		DO	QUP 0 SE0, lane 2: SPI_SCLK	
		UART_TX		DO	QUP 0 SE0, lane 2: UART_TX	
		CCI_I2C_SDA3		B	Dedicated camera control interface I²C 3 serial data	
		QDSS_CTI_TRIG0_OUT_MIRA		DO	QDSS trigger output 0 A	
AY4	GPIO_3		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N		DO	QUP 0 SE0, lane 3: SPI_CS_N	
		UART_RX		DI	QUP 0 SE0, lane 3: UART_RX	
		CCI_I2C_SCL3		DO	Dedicated camera control interface I²C 3 clock	
		QDSS_CTI_TRIG0_IN_MIRA		DI	QDSS trigger input 0 A	
AA45	GPIO_4		PX_3	PD:nppukp	Configurable I/O	Y
		I2C_SDA		B	QUP 1 SE4, lane 0: I2C_SDA	
		UART_RX		DI	QUP 1 SE4, lane 3: UART_RX	
AA47	GPIO_5		PX_3	PD:nppukp	Configurable I/O	N
		I2C_SCL		DO	QUP 1 SE4, lane 1: I2C_SCL	
		UART_TX		DO	QUP 1 SE4, lane 2: UART_TX	
AY2	GPIO_6		PX_3	PU:nppdkp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		MDP_VSYNC_E		DI	MDP vertical sync – external	
		QDSS_CTI_TRIG1_OUT_MIRA		DO	QDSS trigger output 1 A	
AW3	GPIO_7		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG1_IN_MIRA		DI	QDSS trigger input 1 A	
AW5	GPIO_8		PX_3	PD:nppukp	Configurable I/O	Y
		GP_PDM_MIRB[1]		DO	General-purpose PDM_Mirror_B	
		QDSS_GPIO_TRACECLK_LOCA		DO	QDSS trace clock A	
BA1	GPIO_9		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACECTL_LOCA		DO	QDSS trace clock A	
AM44	GPIO_10	—	PX_3	PD:nppukp	Configurable I/O	N
C45	GPIO_11	—	PX_3	PD:nppukp	Configurable I/O	Y
AF42	GPIO_12		PX_3	PD:nppukp	Configurable I/O	Y
		DP_HOT_PLUG_DETECT_MIRA		DI	DisplayPort hot plug detect	
AA43	GPIO_13		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_MISO		DI	QUP 1 SE0, lane 0: SPI_MISO	
		UART_CTS		DI	QUP 1 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP 1 SE0, lane 0: I2C_SDA	
AB42	GPIO_14		PX_3	PD:nppukp	Configurable I/O	N
		SPI_MOSI		DO	QUP 1 SE0, lane 1: SPI_MOSI	
		UART_RFR		DO	QUP 1 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP 1 SE0, lane 1: I2C_SCL	
AB44	GPIO_15		PX_3	PD:nppukp	Configurable I/O	N
		SPI_SCLK		DO	QUP 1 SE0, lane 2: SPI_SCLK	
		UART_TX		DO	QUP 1 SE0, lane 2: UART_TX	
AB46	GPIO_16		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N_0		DO	QUP 1 SE0, lane 3: SPI_CS_N_0	
		UART_RX		DI	QUP 1 SE0, lane 3: UART_RX	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AE45	GPIO_17		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N_1		DO	QUP 1 SE0, lane 4: SPI_CS_N_1	
AF44	GPIO_18	—	PX_3	PD:nppukp	Configurable I/O	Y
B46	GPIO_19		PX_3	PD:nppukp	Configurable I/O	Y
		I2C_SDA		B	QUP 1 SE2, lane 0: I2C_SDA	
		UART_RX		DI	QUP 1 SE2, lane 3: UART_RX	
D44	GPIO_20		PX_3	PD:nppukp	Configurable I/O	N
		I2C_SCL		DO	QUP 1 SE2, lane 1: I2C_SCL	
		UART_TX		DO	QUP 1 SE2, lane 2: UART_TX	
E43	GPIO_21		PX_3	PD:nppukp	Configurable I/O	Y
		GCC_GP2_CLK_MIRB		DO	General-purpose clock	
F42	GPIO_22		PX_3	PD:nppukp	Configurable I/O	Y
		GCC_GP3_CLK_MIRB		DO	General-purpose clock	
C47	GPIO_23		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA		DI	MDP vertical sync – primary	
E45	GPIO_24		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA		DI	MDP vertical sync – secondary	
D46	GPIO_25		PX_3	PD:nppukp	Configurable I/O	Y
		I2C_SDA		B	QUP 1 SE3, lane 0: I2C_SDA	
		UART_RX		DI	QUP 1 SE3, lane 3: UART_RX	
F46	GPIO_26		PX_3	PD:nppukp	Configurable I/O	N
		I2C_SCL		DO	QUP 1 SE3, lane 1: I2C_SCL	
		UART_TX		DO	QUP 1 SE3, lane 2: UART_TX	
AC41	GPIO_27		PX_3	PD:nppukp	Configurable I/O	Y
		I2C_SDA		B	QUP 1 SE1, lane 0: I2C_SDA	
		UART_RX		DI	QUP 1 SE1, lane 3: UART_RX	
		MDP_VSYNC_P_MIRB		DI	MDP vertical sync – primary B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACEDATA_LOCB[14]		DO	QDSS trace data bit 14 B	
AC43	GPIO_28		PX_3	PD:nppukp	Configurable I/O	Y
		I2C_SCL		DO	QUP 1 SE1, lane 1: I2C_SCL	
		UART_TX		DO	QUP 1 SE1, lane 2: UART_TX	
		MDP_VSYNC_S_MIRB		DI	MDP vertical sync – secondary	
		QDSS_GPIO_TRACEDATA_LOCB[15]		DO	QDSS trace data bit 15 A	
H2	GPIO_29		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK0		DO	Camera master clock 0	
G3	GPIO_30		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK1		DO	Camera master clock 1	
H4	GPIO_31		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK2		DO	Camera master clock 2	
H6	GPIO_32		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK3		DO	Camera master clock 3	
G5	GPIO_33		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK4		DO	Camera master clock 4	
AR7	GPIO_34		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER0		DO	Camera control interface timer 0	
		QDSS_GPIO_TRACEDATA_LOCA[12]		DO	QDSS trace data bit 12 A	
AN1	GPIO_35		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER1		DO	Camera control interface timer 1	
		CCI_ASYNC_IN1		DI	Camera control interface async	
		QDSS_GPIO_TRACEDATA_LOCA[13]		DO	QDSS trace data bit 13 A	
AP2	GPIO_36		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER2		DO	Camera control interface timer	
		CCI_ASYNC_IN2		DI	Camera control interface async	
		QDSS_GPIO_TRACEDATA_LOCA[14]		DO	QDSS trace data bit 14 A	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AP4	GPIO_37		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3		DO	Camera control interface timer	
		GP_PDM_MIRB[0]		DO	General-purpose PDM output	
		QDSS_GPIO_TRACEDATA_LOCA[15]		DO	QDSS trace data bit 15 A	
AP6	GPIO_38		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER4		DO	Camera control interface timer	
		QDSS_GPIO_TRACEDATA_LOCB[2]		DO	QDSS trace data bit 2 B	
AV4	GPIO_39		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0		B	Dedicated camera control interface I²C serial data	
		QDSS_GPIO_TRACEDATA_LOCA[0]		DO	QDSS trace data bit 0 A	
AV2	GPIO_40		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0		DO	Dedicated camera control interface I²C clock	
		QDSS_GPIO_TRACEDATA_LOCA[1]		DO	QDSS trace data bit 1 A	
AV6	GPIO_41		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1		B	Dedicated camera control interface I²C serial data	
		QDSS_GPIO_TRACEDATA_LOCA[2]		DO	QDSS trace data bit 2 A	
AU7	GPIO_42		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1		DO	Dedicated camera control interface I²C clock	
		QDSS_GPIO_TRACEDATA_LOCA[3]		DO	QDSS trace data bit 3 A	
AU5	GPIO_43		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2		B	Dedicated camera control interface I²C serial data	
		QDSS_GPIO_TRACEDATA_LOCA[4]		DO	QDSS trace data bit 4 A	
AU3	GPIO_44		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2		DO	Dedicated camera control interface I²C clock	
		QDSS_GPIO_TRACEDATA_LOCA[5]		DO	QDSS trace data bit 5 A	
AU1	GPIO_45		PX_3	PD:nppukp	Configurable I/O	N
		SPI_MISO		DI	QUP 0 SE2, lane 0: SPI_MISO	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		UART_CTS		DI	QUP 0 SE2, lane 0: UART_CTS	
		I2C_SDA		B	QUP 0 SE2, lane 0: I2C_SDA	
AT2	GPIO_46		PX_3	PD:nppukp	Configurable I/O	N
		SPI_MOSI		DO	QUP 0 SE2, lane 1: SPI_MOSI	
		UART_RFR		DO	QUP 0 SE2, lane 1: UART_RFR	
		I2C_SCL		DO	QUP 0 SE2, lane 1: I2C_SCL	
AF46	GPIO_47		PX_3	PD:nppukp	Configurable I/O	N
		MDP_VSYNC0_OUT		DO	MDP vertical sync 0 output	
		QDSS_GPIO_TRACEDATA_LOCB[3]		DO	QDSS trace data bit 3 B	
AT6	GPIO_48		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N_1		DO	QUP 0 SE2, lane 4: SPI_CS_N_1	
		CCI_ASYNC_IN0		DI	Camera control interface async	
		MDP_VSYNC1_OUT		DO	MDP vertical sync 1 output	
		GCC_GP1_CLK_MIRA		DO	General-purpose clock	
		QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data bit 8 A	
AT4	GPIO_49		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data bit 9 A	
AG45	GPIO_50		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[10]		DO	QDSS trace data bit 10 B	
		BOOT_CONFIG[11]		DI	Boot configuration control bit 11	
AG43	GPIO_51		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[11]		DO	QDSS trace data bit 11 B	
		BOOT_CONFIG[10]		DI	Boot configuration control bit 10	
AH42	GPIO_52		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN3		DI	Camera control interface async 3	
		GP_PDM_MIRA[1]		DO	General-purpose PDM_Mirror_A 1	
		QDSS_GPIO_TRACEDATA_LOCB[12]		DO	QDSS trace data bit 12 B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AH44	GPIO_53		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN4		DI	Camera control interface async 4	
		QDSS_GPIO_TRACEDATA_LOCB[13]		DO	QDSS trace data bit 13 B	
AM46	GPIO_54	—	PX_3	PD:nppukp	Configurable I/O	Y
AN45	GPIO_55	—	PX_3	PD:nppukp	Configurable I/O	Y
AR5	GPIO_56		PX_3	PD:nppukp	Configurable I/O	N
		SPI_SCLK		DO	QUP 0 SE2, lane 2: SPI_SCLK	
		UART_TX		DO	QUP 0 SE2, lane 2: UART_TX	
		MDP_VSYNC2_OUT		DO	MDP vertical sync 2 output	
		QDSS_GPIO_TRACEDATA_LOCA[10]		DO	QDSS trace data bit 10 A	
AR3	GPIO_57		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N_0		DO	QUP 0 SE2, lane 3: SPI_CS_N_0	
		UART_RX		DI	QUP 0 SE2, lane 3: UART_RX	
		MDP_VSYNC3_OUT		DO	MDP vertical sync 3 output	
		GP_PDM_MIRA[2]		DO	General-purpose PDM_Mirror_A 2	
		QDSS_GPIO_TRACEDATA_LOCA[11]		DO	QDSS trace data bit 11 A	
BH32	GPIO_58		PX_3	PD:nppukp	Configurable I/O	Y
		GCC_GP1_CLK_MIRB		DO	Global general purpose clock 1 B	
BA3	GPIO_59	—	PX_3	PD:nppukp	Configurable I/O	Y
BC29	GPIO_60		PX_3	PD:nppukp	Configurable I/O	Y
		AUDIO_REF_CLK		DI	Audio reference clock	
		MI2S_2_DATA1		B	MI²S serial data channel	
BB28	GPIO_61		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_MISO		DI	QUP 0 SE1, lane 0: SPI_MISO	
		UART_CTS		DI	QUP 0 SE1, lane 0: UART_CTS	
		I2C_SDA		B	QUP 0 SE1, lane 0: I2C_SDA	
		QDSS_CTI_TRIG1_OUT_MIRB		DO	QDSS trigger output 1 B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BG29	GPIO_62		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_MOSI		DO	QUP 0 SE1, lane 1: SPI_MOSI	
		UART_RFR		DO	QUP 0 SE1, lane 1: UART_RFR	
		I2C_SCL		B	QUP 0 SE1, lane 1: I2C_SCL	
		QDSS_CTI_TRIG1_IN_MIRB		DI	QDSS trigger input 1 B	
BF28	GPIO_63		PX_3	PD:nppukp	Configurable I/O	N
		SPI_SCLK		DO	QUP 0 SE1, lane 2: SPI_SCLK	
		UART_TX		DO	QUP 0 SE1, lane 2: UART_TX	
		QDSS_GPIO_TRACECLK_LOCB		DO	QDSS trace clock B	
BG27	GPIO_64		PX_3	PD:nppukp	Configurable I/O	Y
		SPI_CS_N		DO	QUP 0 SE1, lane 3: SPI_CS_N	
		UART_RX		DI	QUP 0 SE1, lane 3: UART_RX	
		QDSS_GPIO_TRACECTL_LOCB		DO	QDSS trace control B	
BH30	GPIO_65		PX_3	PD:nppukp	Configurable I/O	N
		MSS_LTE_COXM_TXD		DO	UART Tx for LTE coex	
		QDSS_GPIO_TRACEDATA_LOCB[0]		DO	QDSS trace data bit 0 B	
BE29	GPIO_66		PX_3	PD:nppukp	Configurable I/O	Y
		MSS_LTE_COXM_RXD		DI	UART Rx for LTE coex	
		QDSS_GPIO_TRACEDATA_LOCB[1]		DO	QDSS trace data bit 1 B	
BA23	GPIO_67		PX_3	PD:nppukp	Configurable I/O	Y
		BTFM_SLIMBUS_CLK		DO	Bluetooth/FM SLIMbus clock	
		MI2S_1_SCK		B	MI²S clock	
BG25	GPIO_68		PX_3	PD:nppukp	Configurable I/O	N
		BTFM_SLIMBUS_DATA0		B	Bluetooth/FM SLIMbus data	
		MI2S_1_WS		B	MI²S serial data word select	
		GP_PDM_MIRA[0]		DO	General-purpose PDM_Mirror_A 0	
AH46	GPIO_69	—	PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BG31	GPIO_70	—	PX_3	PD:nppukp	Configurable I/O	N
BF30	GPIO_71	—	PX_3	PD:nppukp	Configurable I/O	N
BC27	GPIO_72	MI2S_2_SCK	PX_3	PD:nppukp B	Configurable I/O MI²S clock	N
BA27	GPIO_73	MI2S_2_DATA0	PX_3	PD:nppukp B	Configurable I/O MI²S data 0	Y
BE27	GPIO_74	MI2S_2_WS	PX_3	PD:nppukp B	Configurable I/O MI²S serial data word select	N
AP46	GPIO_75	UIM2_DATA	PX_6	PD:nppukp B	Configurable I/O UIM2 data (dual voltage)	N
AR45	GPIO_76	UIM2_CLK	PX_6	PD:nppukp DO	Configurable I/O UIM2 clock (dual voltage)	N
AP44	GPIO_77	UIM2_RESET	PX_6	PD:nppukp DO	Configurable I/O UIM2 reset (dual voltage)	N
AN47	GPIO_78	UIM2_PRESENT	PX_3	PD:nppukp DI	Configurable I/O UIM2 presence detection	Y
AN43	GPIO_79	UIM1_DATA	PX_5	PD:nppukp B	Configurable I/O UIM1 data (dual voltage)	N
AM42	GPIO_80	UIM1_CLK	PX_5	PD:nppukp DO	Configurable I/O UIM1 clock (dual voltage)	N
AL41	GPIO_81	UIM1_RESET	PX_5	PD:nppukp DO	Configurable I/O UIM1 reset (dual voltage)	N
AP42	GPIO_82	UIM1_PRESENT	PX_3	PD:nppukp DI	Configurable I/O UIM1 presence detection	Y
AJ47	GPIO_83	—	PX_3	PD:nppukp	Configurable I/O	Y
AJ45	GPIO_84	—	PX_3	PD:nppukp	Configurable I/O	Y
AK46	GPIO_85		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SD_WRITE_PROTECT		DO	SD card write protect	
BH24	GPIO_86		PX_3	PD:nppukp	Configurable I/O	N
		BTFM_SLIMBUS_DATA1		B	Bluetooth/FM SLIMbus data 1	
		MI2S_1_DATA0		B	MI²S 1 data 0	
		QDSS_CTI_TRIG0_IN_MIRB		DO	QDSS trigger input 0 B	
BF24	GPIO_87		PX_3	PD:nppukp	Configurable I/O	Y
		BTFM_SLIMBUS_DATA2		B	Bluetooth/FM SLIMbus data 2	
		MI2S_1_DATA1		B	MI²S 1 data 1	
		QDSS_CTI_TRIG0_OUT_MIRB		DO	QDSS trigger output 0 B	
BB26	GPIO_88		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S_0_SCK		DO	MI²S 0 clock	
		QDSS_GPIO_TRACEDATA_LOCB[4]		DO	QDSS trace data bit 4 B	
BF26	GPIO_89		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S_0_WS		B	MI²S 0 Word Select	
		QDSS_GPIO_TRACEDATA_LOCB[5]		DO	QDSS trace data bit 5 B	
BH26	GPIO_90		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S_0_DATA0		B	MI²S 0 data 0	
		QDSS_GPIO_TRACEDATA_LOCB[6]		DO	QDSS trace data bit 6 B	
BC25	GPIO_91		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S_0_DATA1		B	MI²S 0 data 1	
		QDSS_GPIO_TRACEDATA_LOCB[7]		DO	QDSS trace data bit 7 B	
BD26	GPIO_92		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[8]		DO	QDSS trace data bit 8 B	
		BOOT_CONFIG[2]		DI	Boot configuration control bit 2	
BE25	GPIO_93		PX_3	PD:nppukp	Configurable I/O	Y
		MCLK		DO	Master Clock	
		LPASS_EXT_MCLK0		DO	Low-power audio external master clock 0	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACEDATA_LOCB[9]		DO	QDSS trace data bit 9 B	
F44	GPIO_94	—	PX_3	PD:nppukp	Configurable I/O	Y
AJ43	GPIO_95	—	PX_3	PD:nppukp	Configurable I/O	Y
AJ41	GPIO_96	—	PX_3	PD:nppukp	Configurable I/O	Y
AK44	GPIO_97	—	PX_3	PD:nppukp	Configurable I/O	Y
AL45	GPIO_98	—	PX_3	PD:nppukp	Configurable I/O	Y
AK42	GPIO_99	—	PX_3	PD:nppukp	Configurable I/O	Y
AL43	GPIO_100	—	PX_3	PD:nppukp	Configurable I/O	Y
AW45	GPIO_101		PX_3	PD:nppukp	Configurable I/O	N
		NAV_GPIO_0		B	GPS control signal	
		GPS_TX_AGGRESSOR_D			Tx level may degrade GNSS receiver D	
AY46	GPIO_102		PX_3	PD:nppukp	Configurable I/O	N
		NAV_GPIO_1		B	GPS control signal	
		GPS_TX_AGGRESSOR_C		DI	Tx level may degrade GNSS receiver C	
BB44	GPIO_103		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_WMSS_RESET_N		DO	SDR modem subsystem reset output	
		BOOT_CONFIG[7]		DI	Boot configuration bit 7	
AY44	GPIO_104		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK0_REQUEST		DI	QLink0 request	
BB46	GPIO_105		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_ENABLE		DO	QLink0 enable	
BA47	GPIO_106		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_WMSS_RESET_N		DO	Modem subsystem reset output	
		BOOT_CONFIG[8]		DI	Boot configuration control bit 8	
BA45	GPIO_107		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK1_REQUEST		DI	QLink1 request	
		GPS_TX_AGGRESSOR_B			Tx level may degrade GNSS receiver B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AW43	GPIO_108		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_ENABLE		DO	QLink1 enable	
		GPS_TX_AGGRESSOR_A		DI	Tx level may degrade GNSS receiver A	
AT46	GPIO_109		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA		B	RF front end 0 interface data	
		GRFC1		DO	Generic RF controller bit 1	
		BOOT_CONFIG[0]		DI	Boot configuration control bit 0	
AU47	GPIO_110		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE0_CLK		DO	RF front end 0 interface clock	
		GRFC0		DO	Generic RF controller bit 0	
AR43	GPIO_111		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_DATA		B	RF front end 1 interface data	
		GRFC3		DO	Generic RF controller bit 3	
		BOOT_CONFIG[1]		DI	Boot configuration control bit 1	
AT44	GPIO_112		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE1_CLK		DO	RF front end 1 interface clock	
		GRFC2		DO	Generic RF controller bit 2	
AT42	GPIO_113		PX_3	PD:nppukp	Configurable I/O	N
		RFFE2_DATA		B	RF front end 2 interface data	
		GRFC5		DO	Generic RF controller bit 5	
		BOOT_CONFIG[9]		DI	Boot configuration control bit 9	
AR41	GPIO_114		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE2_CLK		DO	RF front end 2 interface clock	
		GRFC4		DO	Generic RF controller bit 4	
AU45	GPIO_115		PX_3	PD:nppukp	Configurable I/O	N
		RFFE3_DATA		B	RF front end 3 interface data	
		GRFC7		DO	Generic RF controller bit 7	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		BOOT_CONFIG[3]		DI	Boot configuration control bit 3	
AV46	GPIO_116		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE3_CLK		DO	RF front end 3 interface clock	
		GRFC6		DO	Generic RF controller bit 6	
AU43	GPIO_117		PX_3	PD:nppukp	Configurable I/O	N
		RFFE4_DATA		B	RF front end 4 interface data	
		GRFC9		DO	Generic RF controller bit 9	
		BOOT_CONFIG[4]		DI	Boot configuration control bit 4	
AV44	GPIO_118		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE4_CLK		DO	RF front end 4 interface clock	
		GRFC8		DO	Generic RF controller bit 8	
		PA_INDICATOR_1_OR_2		DO	PA transmit indicator	
		DP_HOT_PLUG_DETECT		DI	DisplayPort hot plug detect	
AU41	GPIO_119		PX_3	PD:nppukp	Configurable I/O	N
		GRFC10		DO	Generic RF controller bit 10	
		BOOT_CONFIG[5]		DI	Boot configuration control bit 5	
AV42	GPIO_120		PX_3	PD:nppukp	Configurable I/O	N
		GRFC11		DO	Generic RF controller bit 11	
		BOOT_CONFIG[6]		DI	Boot configuration control bit 6	
BF2	GPIO_121		PX_3	PD:nppukp	Configurable I/O	N
		GRFC12		DO	Generic RF controller bit 12	
BE1	GPIO_122		PX_3	PU:nppdkp	Configurable I/O	Y
		GRFC13		DO	Generic RF controller bit 13	
BB2	GPIO_123		PX_3	PD:nppukp	Configurable I/O	Y
		GRFC14		DO	Generic RF controller bit 14	
Y44	GPIO_124		PX_3	PD:nppukp	Configurable I/O	Y
		USB_PHY_PS		DI	USB PHY port select	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
W45	GPIO_125		PX_3	PD:nppukp	Configurable I/O	Y
		FORCE_USB_BOOT_POLARITY		DI	Forced USB boot polarity	
Y46	GPIO_126		PX_3	PD:nppukp	Configurable I/O	N
		FORCED_USB_BOOT		DI	Forced USB boot	
BC21	GPIO_127	LPI_GPIO_0	PX_3	PD:nppukp	Configurable I/O	N
		SWR_TX_CLK		DO	SoundWire transmit clock	
		LPI_QUA_MI2S_SCK		B	LPI_MI2S_ SCK	
BB22	GPIO_128	LPI_GPIO_1	PX_3	PD:nppukp	Configurable I/O	Y
		SWR_TX_DATA0		B	SoundWire transmit data 0	
		LPI_QUA_MI2S_WS		B	LPI_QUA_MI2S Word Select	
BF22	GPIO_129	LPI_GPIO_2	PX_3	PD:nppukp	Configurable I/O	Y
		SWR_TX_DATA1		B	SoundWire transmit data 1	
		LPI_QUA_MI2S_DATA0		B	LPI_QUA_MI2S Data 0	
BH22	GPIO_130	LPI_GPIO_3	PX_3	PD:nppukp	Configurable I/O	N
		SWR_RX_CLK		B	SoundWire receive clock	
		LPI_QUA_MI2S_DATA1		B	LPI_QUA_MI2S Data 1	
BD22	GPIO_131	LPI_GPIO_4	PX_3	PD:nppukp	Configurable I/O	Y
		SWR_RX_DATA0		B	SoundWire receive data 0	
		LPI_QUA_MI2S_DATA2		B	Quaternary MI²S Data 2	
BA21	GPIO_132	LPI_GPIO_5	PX_3	PD:nppukp	Configurable I/O	N
		SWR_RX_DATA1		B	SoundWire receive data 1	
		EXT_MCLK1_C		B	External master clock 1 C	
		LPI_QUA_MI2S_DATA3		B	LPI_QUA_MI2S Data 3	
BB20	GPIO_133	LPI_GPIO_6	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_DMIC1_CLK		DO	DMIC clock	
		LPI_I2S1_CLK		B	LPI I²S clock	
BD20	GPIO_134	LPI_GPIO_7	PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPI_DMIC1_DATA		DI	DMIC1 data	
		LPI_I2S1_WS		B	LPI MI²S serial data word select	
BF20	GPIO_135	LPI_GPIO_8	PX_3	PD:nppukp	Configurable I/O	N
		LPI_DMIC2_CLK		DO	DMIC 2 clock	
		LPI_I2S1_DATA0		B	LPI I²S 1 serial data channel	
BG21	GPIO_136	LPI_GPIO_9	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_DMIC2_DATA		DI	DMIC 2 data	
		LPI_I2S1_DATA1		B	LPI MI²S 1 serial data channel	
		EXT_MCLK1_B		B	External master clock 1 B	
BE19	GPIO_137	LPI_GPIO_10	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_I2S2_CLK		B	LPI MI²S 2 clock	
		WSA_SWR_CLK		B	SoundWire clock for WSA	
BG19	GPIO_138	LPI_GPIO_11	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_I2S2_WS		B	LPI MI²S 2 serial data word select	
		WSA_SWR_DATA		B	SoundWire data for WSA	
BC19	GPIO_139	LPI_GPIO_12	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_DMIC3_CLK		DO	DMIC 3 clock	
		LPI_I2S2_DATA0		B	LPI MI²S data	
BB18	GPIO_140	LPI_GPIO_13	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_DMIC3_DATA		DI	DMIC 3 data	
		LPI_I2S2_DATA1		B	LPI I²S2 serial data channel 1	
		EXT_MCLK1_A		B	External master clock 1 A	
BF18	GPIO_141	LPI_GPIO_14	PX_3	PD:nppukp	Configurable I/O	N
		SWR_TX_DATA2		B	SoundWire transmit data	
BC17	GPIO_142	LPI_GPIO_15	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_I3C_SDA		B	QUP 2 SE0; lane 0: I3C_SDA	
		LPI_I2C_SDA		B	QUP 2 SE0; lane 0: I2C_SDA	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SYNC_OUT_GPIO_0		DO	Sync out GPIO_0	
BE17	GPIO_143	LPI_GPIO_16	PX_3	PD:nppukp	Configurable I/O	N
		LPI_I3C_SCL		DO	QUP 2 SE0; lane 1: I3C_SCL	
		LPI_I2C_SCL		DO	QUP 2 SE0; lane 1: I2C_SCL	
		SYNC_OUT_GPIO_1		DO	Sync out GPIO_1	
BH18	GPIO_144	LPI_GPIO_17	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_SPI_MISO		DI	QUP2 SE2, lane 0: SPI MISO	
		LPI_I2C_SDA		B	QUP2 SE2, lane 0: I²C SDA	
		LPI_I3C_SDA		B	QUP2 SE2, lane 0: I3C SDA	
		SYNC_OUT_GPIO_2		DO	Sync out GPIO_2	
		SYNC_OUT_GPIO_4		DO	Sync out GPIO_4	
BC15	GPIO_145	LPI_GPIO_18	PX_3	PD:nppukp	Configurable I/O	N
		LPI_SPI_MOSI		DO	QUP2 SE2, lane 1: SPI MOSI	
		LPI_I2C_SCL		DO	QUP2 SE2, lane 1: I²C SCL	
		LPI_I3C_SCL		DO	QUP2 SE2, lane 1: I3C SCL	
		SYNC_OUT_GPIO_3		DO	Sync out GPIO_3	
		SYNC_OUT_GPIO_5		DO	Sync out GPIO_5	
BB16	GPIO_146	LPI_GPIO_19	PX_3	PD:nppukp	Configurable I/O	N
		LPI_SPI_SCK		DO	QUP2 SE2, lane 2: SPI SCK	
		SYNC_OUT_GPIO_6		DO	Sync out GPIO_6	
BG17	GPIO_147	LPI_GPIO_20	PX_3	PD:nppukp	Configurable I/O	Y
		LPI_SPI_CS_N		DO	QUP2 SE2, lane 3: SPI CS	
		SYNC_OUT_GPIO_7		DO	Sync out GPIO_7	
BB14	GPIO_148	LPI_GPIO_21	PX_3	PD:nppukp	Configurable I/O	N
		LPI_I2C_SDA		B	QUP2 SE3, lane 0: I²C SDA	
		LPI_SPI_MISO		DI	QUP2 SE6, lane 0: SPI MISO	
		SYNC_OUT_GPIO_8		DO	Sync out GPIO_8	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable functions	Pad characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BA15	GPIO_149	LPI_GPIO_22	PX_3	PD:nppukp	Configurable I/O	N
		LPI_I2C_SCL		DO	QUP2 SE3, lane 1: I²C SCL	
		LPI_SPI_MOSI		DO	QUP2 SE6, lane 1: SPI MOSI	
		SYNC_OUT_GPIO_9		DO	Sync out GPIO_9	
BA17	GPIO_150	LPI_GPIO_23	PX_3	PD:nppukp	Configurable I/O	N
		LPI_I2C_SDA		B	QUP2 SE4, lane 0: I²C SDA	
		SYNC_OUT_GPIO_10		DO	Sync out GPIO_10	
BD16	GPIO_151	LPI_GPIO_24	PX_3	PD:nppukp	Configurable I/O	N
		LPI_I2C_SCL		DO	QUP2 SE4, lane 1: I²C SCL	
		SYNC_OUT_GPIO_11		DO	Sync out GPIO_11	
BF16	GPIO_152	LPI_GPIO_25	PX_3	PD:nppukp	Configurable I/O	N
		LPI _UART_TX		DO	QUP2 SE5, lane 2: UART TX	
		SYNC_OUT_GPIO_12		DO	Sync out GPIO_11	
BH16	GPIO_153	LPI_GPIO_26	PX_3	PD:nppukp	Configurable I/O	Y
		LPI _UART_RX		DI	QUP2 SE5, lane 3:UART RX	
		SYNC_OUT_GPIO_13		DO	Sync out GPIO_13	
BE15	GPIO_154	LPI_GPIO_27	PX_3	PD:nppukp	Configurable I/O	N
		LPI _UART_TX		DO	QUP2 SE6, lane 2: UART TX	
		LPI_SPI_SCK		DO	QUP2 SE6, lane 2: SPI SCK	
BG15	GPIO_155	LPI_GPIO_28	PX_3	PD:nppukp	Configurable I/O	Y
		LPI _UART_RX		DI	QUP2 SE6, lane 3:UART RX	
		LPI_SPI_CS_N		DO	QUP2 SE6, lane 3: SPI CS	
		SYNC_OUT_GPIO_15		DO	Sync out GPIO_15	

[a] See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad #	Pad name	Functional description
AB16, AD16, AF16, AH16, AK16, AM16, AP14, AP16, AR13	VDD_APC0	Power for the Kryo Silver application processor
AC11, AD12, AE11, AF8, AF12, AG11, AH8, AH12, AJ9, AJ11, AK4, AK6, AK8, AK12, AL5, AL7, AL9, AL11, AM4, AM6, AM8, AM12	VDD_APC1	Power for the Kryo Gold application processor
AD18	VDD_APC_PLL_0P9	Power for application processor PLL 0.9 V circuits
AU17	VDD_AUD_LPA_PLL_0P9	Power for LPA audio PLL 0.9 V circuits
AJ13	VDD_A_APC_CS_1P8	Power for application processor current sensor circuits
U7	VDD_A_CSI_0_0P9	Power for MIPI CSI0 0.9 V circuits
T6	VDD_A_CSI_0_1P25	Power for MIPI CSI0 1.25 V circuits
W7	VDD_A_CSI_1_0P9	Power for MIPI CSI1 0.9 V circuits
Y6	VDD_A_CSI_1_1P25	Power for MIPI CSI1 1.25 V circuits
R7	VDD_A_CSI_2_0P9	Power for MIPI CSI2 0.9 V circuits
P6	VDD_A_CSI_2_1P25	Power for MIPI CSI2 1.25 V circuits
AA7	VDD_A_CSI_3_0P9	Power for MIPI CSI3 0.9 V circuits
AB6	VDD_A_CSI_3_1P25	Power for MIPI CSI3 1.25 V circuits
AB40	VDD_A_CXO_1P8	Power for 1.8 V clock circuits
M40	VDD_A_DSI_0P9	Power for MIPI DSI 0.9 V circuits
N41	VDD_A_DSI_1P2	Power for MIPI DSI 1.2 V circuits
L41	VDD_A_DSI_PLL_0P9	Power for MIPI DSI PLL 0.9 V circuits
J15, J17, J21	VDD_A_EBI_0_PHY_0P9	Power for EBI0 PHY 0.9 V circuits
J29, J31, J33	VDD_A_EBI_1_PHY_0P9	Power for EBI1 PHY 0.9 V circuits
K24	VDD_A_EBI_01_CCPLL_0P9	Power for EBI clock PLL 0.9 V circuits
J23	VDD_A_EBI_CC_0P9	Power for EBI clock 0.9 V circuits
AY24	VDD_A_NAV_0P9	Power for NAV circuits
AW15	VDD_A_QREFS_5_0P9	Reference voltage for the QREFS 0.9 V
AY16	VDD_A_1P2	Power for internal 1.2 V circuit
AY32	VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits
BA31	VDD_A_QLINK_0_1P2	Power for the QLink0 1.2 V circuits
AW31	VDD_A_QLINK_0_CK_0P9	Power for the QLink0 0.9 V clock circuits
AY34	VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits
BA37	VDD_A_QLINK_1_1P2	Power for the QLink1 1.2 V circuits
AW35	VDD_A_QLINK_1_CK_0P9	Power for the QLink1 0.9 V clock circuits
BA19	VDD_A_QREFS_1P25	Reference voltage for the QREFS 1.25 V circuits
AY20	VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits
AY42	VDD_A_QREFS_2_0P9	Reference voltage for the QREFS 0.9 V circuits
Y40	VDD_A_QREFS_3_0P9	Reference voltage for the QREFS 0.9 V circuits
H38	VDD_A_QREFS_4_0P9	Reference voltage for the QREFS 0.9 V circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
J25	VDD_A_UFS_0P9	Power for the UFS 0.9 V circuits
G23	VDD_A_UFS_1P2	Power for the UFS 1.2 V circuits
P42	VDD_A_USBHS_1P8	Power for the USB high speed 1.8 V circuits
T42	VDD_A_USBHS_3P1	Power for the USB high speed 3.1 V circuits
V40	VDD_A_USBSSDP_0P9	Power for USB SS and DisplayPort 0.9 V circuits
U41	VDD_A_USBSSDP_1P2	Power for USB SS and DisplayPort 1.2 V circuits
AY14	VDD_A_WLAN_ADCDAC0_1P3	Power for the WLAN ADC and DAC 0 1.3 V circuits
AY12	VDD_A_WLAN_ADCDAC1_1P3	Power for the WLAN ADC and DAC 1 1.3 V circuits
AY10	VDD_A_WLAN_PLL_0P9	Power for the WLAN PLL 0.9 V circuits
R27	VDD_CAMSS_PLL_0P9	Power for camera SS PLL 0.9 V circuits
AA39, AD20, AD22, AD24, AF20, AH20, AK20, AP8, AU19, N17, N39, P18, P20, P22, P24, P30, P32, P34, P36, T18, T20, T24, Y12, Y14, Y16, Y18, Y20, Y24, Y26	VDD_CX	Power for digital core circuits
AT18, AT20, AT22, AU21	VDD_CX_LPI	Power supply for LPI core
AR11, AU11	VDD_CX_WLAN	Power for WLAN core circuits
H8, J9, K8, K12, M12, N13, P12, P14, T12, V12	VDD_GFX	Power for graphics
H20	VDD_IO_EBI_0_CK	Power for the EBI0 I/O clock circuits
K14, K16, K20, K22	VDD_IO_EBI_0_PHY	Power for EBI I/O circuits
H30	VDD_IO_EBI_1_CK	Power for the EBI1 I/O clock circuits
K28, K30, K32, K36	VDD_IO_EBI_1_PHY	Power for EBI I/O circuits
AH24, AH26, AH28, AH30, AH32, AH34, AH36, AK30, AP24, AP26, AP28, AP30, AP32, AP34, AP36, AR33, AR35, AT26, AT28, AU25, AU27, AV28, AW27, AW29, AY28, BA29, BB30, BC31, BD30, Y30, Y32, Y34, Y36	VDD_MODEM	Power for modem circuits
AD14, AD26, AD28, AD30, AD32, AD34, AD36, AH14, AM14, AM20, AM22, AM24, AM26, AM28, AM30, AM32, AM34, AM36, AP18, AU13, J7, M22, M24, M26, T14, T16, T28, T30, T32, T34	VDD_MX	Power for on-chip memory
AP22, AU23	VDD_LPI_MX	Power for LPI core memory
AV8	VDD_MX_WLAN	Power for WCSS circuits
AY22	VDD_PX0	Power for pad group 0
K26	VDD_PX10	Power for pad group 10
W41	VDD_PX11	Power for pad group 11
H18	VDD_PX1	Power for pad group 1 - EBI
H32	VDD_PX1	Power for pad group 1 - EBI
J39	VDD_PX1	Power for pad group 1 - EBI

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AD40	VDD_PX2	Power for pad group 2
AG41, AP40, AY8, AY26, G7, H26, H40	VDD_PX3	Power for pad group 3
AN41	VDD_PX5	Power for pad group 5
AK40	VDD_PX6	Power for pad group 6
H12	VDD_PX7	Power for pad group 7
AY18	VDD_QFPROM	Power for programming the QFPROM
AE41	VDD_SDCREF_1P25	Power for SDC 1.25 Vcircuits
AM40	VDD_UIMREF_1P25	Power for UIM 1.25 V circuits
P40	VDD_USBHS_0P9	Power for the USB high speed 0.9 V circuits
A41, AJ1, F22, M42, Y42, W43, BA25, U43, BF12, BG11, BH12, BG13, BA13, BC13, BE13,	DNC	Do not connect; connected internally, do not connect externally
A1, A47, AA11, AB2, AB12, AB14, AB18, AB20, AB22, AB24, AB26, AB28, AB30, AB32, AB34, AB36, AC1, AC9, AC47, AD8, AE9, AF2, AF14, AF18, AF22, AF24, AF26, AF28, AF30, AF32, AF34, AF36, AF40, AG1, AG9, AG47, AH10, AH18, AH22, AJ3, AJ5, AJ7, AK2, AK14, AK18, AK22, AK24, AK26, AK28, AK32, AK34, AK36, AL3, AL47, AM2, AM10, AM18, AN3, AN5, AN7, AN9, AP20, AR1, AR47, AT8, AT14, AT16, AT24, AT30, AT32, AT34, AT36, AT40, AW1, AW25, AW41, AW47, B4, B20, BA9, BA11, BA35, BA39, BA43, BB10, BB12, BB32, BC1, BC7, BC33, BC35, BC37, BC39, BC41, BC43, BC45, BD6, BD12, BD14, BD18, BD28, BD32, BD34, BD42, BE3, BE5, BE7, BE9, BE11, BE21, BE31, BE39, BF4, BF6, BF10, BF14, BF32, BG1, BG9, BG47, BH2, BH4, BH10, BH14, BH20, BH28, BH36, BH38, BH40, BH44, BH46, C5, C7, C9, C11, C13, C15, C17, C19, C25, C27, C29, C31, C33, C35, C37, C39, D6, D22, D40, E21, E25, E39, E47, F6, F8, F38, G1, G9, G11, G13, G15, G17, G19, G21, G25, G27, G29, G31, G33, G35, G37, G47, H14, H22, H28, H36, K2, K38, K40, K42, K46, L1, M8, M16, M18, M20, M28, M30, M32, M34, N11, P2, P8, P16, P26, P28, P46, R1, R11, R47, T22, T26, T36, U11, V2, V8, V14, V16, V18, V20, V22, V24, V26, V28, V30, V32, V34, V36, W1, W39, W47, Y22, Y28	GND	Ground

3 Electrical specifications

3.1 Power delivery network specification

The design guidelines for the PDN are listed in the *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, contact QTI for assistance

(https://createpoint.qti.qualcomm.com).

The following tables list the PDN specifications:

Table 3-1 PDN specification core power rails

Power domain	Specifications			Port number	Pin number of positive port	Pin number of negative port
	Max DC resistance (mΩ)	Parameters for max impedence (Z_{spec}) [a]				
		R_{mid_freq} (mΩ)	Inductance L (pH)			
VDD_APC0	3	22	140	1	AB16, AD16, AF16, AH16, AK16, AM16, AP16, AP14, AP16, AR13	AF18, AH18, AK18, AM18, AB14, AF14, AK14, AT14
VDD_APC1	3	14	105	1	AJ9, AJ11, AK4, AK6, AK8, AK12, AL5, AL7, AL9, AL11, AM4, AM6, AM8, AM12, AC11, AD12, AE11, AF8, AF12, AG11, AH8, AH12	AJ3, AJ5, AJ7, AK2, AL3, AM2, AM10, AN3, AN5, AN7, AN9, AA11, AB12, AC9, AD8, AE9, AG9, AH10, AF14, AK14
VDD_CX (Distributed)	3	20	100	1	N17, P18, P20, P22, P24, T18, T20, T24, P30, P32, P34, P36, N39, Y24, Y26, Y14, Y16, Y18, Y20, Y12, AD20, AF20, AH20, AK20, AD22, AD24	M16, M18, M20, P16, T22, P26, P28, M28, M30, M32, M34, T36, V36, V28, V30, V32, V34, V22, V24, V26, V28, Y22, Y28, AB22, AB24, AB26, V14, V16, V18, V20, AA11, AB12, AB14, AF18, AH18, AK18, AM18, AB20, AF22, AH22, AK22, AF24, K38
	15	30	800	2	AA39	W39, V36, AB36
	15	30	800	3	AU19	AP20, AT24
	15	30	800	4	AP8	AN9, AN7
VDD_MX (Distributed)	6	15	130	1	M22, M24, M26, T28, T30, T32, T34, T14, T16	M20, M28, P28, P26, T22, V28, V30, V32, V34, V26, T36, V36, V14, V16, P16
	6	15	130	2	AD26, AD28, AD30, AD32, AD34, AD36, AM22, AM24, AM26, AM28, AM32, AM34, AM36, AM30, AM20, AP18	AB26, AB28, AB30, AB32, AB34, AB36, AF26, AF28, AF30, AF32, AF34, AF36, AK22, AK24, AK26, AK28, AK32, AK34, AK36, AM18, AP20, AT30
	6	15	150	3	AD14, AH14, AM14	AB14, AF14, AK14
	15	30	500	4	AU13	AT14
	15	30	500	5	J7	M8, G9
VDD_GFX	3	20	130	1	H8, J9, K8, K12, M12, P12, T12, V12, N13, P14	M16, P16, V14, N11, R11, U11, M8, F8, G9, G11, F6,

Table 3-1 PDN specification core power rails (cont.)

Power domain	Specifications			Port number	Pin number of positive port	Pin number of negative port
	Max DC resistance (mΩ)	Parameters for max impedence (Z_{spec}) [a]				
		R_{mid_freq} (mΩ)	Inductance L (pH)			
VDD_MODEM	3	15	100	1	Y30, Y32, Y34, Y36, AH24, AH26, AH28, AH30, AH32, AH34, AH36, AK30, AP24, AP26, AP28, AP30, AP32, AP34, AP36, AR33, AR35, AT26, AT28, AU25, AU27, AV28, AW27, AW29, AY28, BA29, BB30, BC31, BD30	V28, V30, V32, V34, V36, Y28, AB28, AB30, AB32, AB34, AB36, AF22, AF24, AF26, AF28, AF30, AF32, AF34, AF36, AH22, AK22, AK24, AK26, AK28, AK32, AK34, AK36, AT24, AT30, AT32, AT34, AT36, AW25, BE31, BD32, BC33, BB32
VDD_CX_WLAN	75	75	800	1	AU11, AR11	AT14, AN9, AM10, AT8
VDD_MX_WLAN	15	30	500	1	AV8	BA9, BA11
VDD_CX_LPI	100	100	700	1	AT18, AT20, AT22, AU21	AT14, AP20, AT24
VDD_LPI_MX	140	140	1000	1	AP22, AU23	AP20, AT24, AW25

[a] The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-freq resistance (R_{mid_freq}) and inductance (L) values from the core power rails table. Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) is ranging from 1 MHz to 200 MHz.

Table 3-2 PDN specification SerDes rails

Power rail	Power domain	Specifications			Port number	Pin number of positive port	Pin number of negative port
		Max DC resistance (mΩ)	Parameters for max effective impedence (Z_{spec}) [a]				
			R_{mid_freq} (mΩ)	Inductance L (pH)			
VREG_L16A	VDD_A_USBSSDP_0P9	125	138	880	1	V40	W47, V36, T36, W39
VREG_L18A	VDD_A_QREFS_5_0P9	170	118	750	1	AW15	AT14, BD14
	VDD_A_QLINK_0_CK_0P9	4000	118	750	2	AW31	AT30, AT32, BB32
	VDD_A_QLINK_1_CK_0P9	4000	118	750	3	AW35	AT34, AT36, BA35
	VDD_A_UFS_0P9	140	176	1125	4	J25	M28, M20, H28, H22
	VDD_USBHS_0P9	1500	235	1500	5	P40	T36, R47, P46
	VDD_A_CSI_0_0P9	550	235	1500	6	U7	V8, P8, AC9
	VDD_A_CSI_1_0P9	550	235	1500	7	W7	V8, P8, AC9

Table 3-2 PDN specification SerDes rails (cont.)

Power rail	Power domain	Specifications			Port number	Pin number of positive port	Pin number of negative port
		Max DC resistance (mΩ)	Parameters for max effective impedence (Z_{spec}) [a]				
			R_{mid_freq} (mΩ)	Inductance L (pH)			
	VDD_A_CSI_2_0P9	550	235	1500	8	R7	V8, P8, AC9
	VDD_A_CSI_3_0P9	550	235	1500	9	AA7	V8, P8, AC9
	VDD_A_QLINK_0_0P9	44	235	1500	10	AY32	AT30, AT32, BB32
	VDD_A_QLINK_1_0P9	33	235	1500	11	AY34	AT34, AT36, BA35
	VDD_A_DSI_PLL_0P9	900	170	1080	12	L41	K42, K40
VREG_L22A	VDD_A_DSI_1P2	440	157	1000	1	N41	T36, R47, P46, V36, W39
	VDD_A_1P2	845	235	1500	2	AY16	AT14, BD14
	VDD_A_USBSSDP_1P2	400	235	1500	3	U41	T36, R47, P46, V36, W39
	VDD_A_CSI_0_1P25	1300	235	1500	4	T6	V8, P8, AC9
	VDD_A_CSI_1_1P25	1300	235	1500	5	Y6	V8, P8, AC9
	VDD_A_CSI_2_1P25	1300	235	1500	6	P6	V8, P8, AC9
	VDD_A_CSI_3_1P25	1300	235	1500	7	AB6	V8, P8, AC9
	VDD_A_UFS_1P2	650	235	1500	8	G23	H22, G25, G21
	VDD_A_QLINK_0_1P2	2000	235	1500	9	BA31	AT36, AT40, BA35, BA39
	VDD_A_QLINK_1_1P2	2000	235	1500	10	BA37	AT36, AT40, BA35, BA39
VREG_L2A	VDD_A_USBHS_1P8	380	157	1000	1	P42	T36, R47, P46
VREG_L3A	VDD_A_USBHS_3P1	880	235	1500	1	T42	W47, V36, T36, R47, P46
VREG_S5A	VDD_A_DSI_0P9	215	170	1080	1	M40	K40, K38

[a] The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and inductance (L) values from the SerDes rails table. Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) is ranging from 1 MHz to 200 MHz.

Table 3-3 PDN specification DDR rails

Power domain	Specifications			Port number	Pin number of positive port	Pin number of negative port
	Max DC resistance (mΩ)	Parameters for max impedence (Z_{spec}) [a]				
		R_{mid_freq} (mΩ)	Inductance L (pH)			
VDD_A_EBI_0_PHY	12.7	12.9	215	1	J21, J17, J15	H22, H14
VDD_A_EBI_1_PHY	12.7	12.9	215	2	J33, J31, J29	H28, G33, G31, G29
VDD_IO_EBI_0_PHY	40	57.5	529	1	K22, K20, K16, K14, H20	M20, M18, M16, H22, H14
VDD_IO_EBI_1_PHY	40	57.5	529	2	K36, K32, K30, K28, H30	M34, M32, M30, M28, K38, H36, H28

[a] The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using mid-frequency resistance (R_{mid_freq}) and inductance (L) values from the DDR rails table. Where, $Z_{spec} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$ and frequency (f) is ranging from 1 MHz to 200 MHz.

4 Mechanical information

4.1 Device physical dimensions

The SM6350 device is available in the 837 PSP, a 12.4 × 12.0 × 0.91 mm non-PoP package. The package includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in the following figure.

NOTE Click the following link to download the *Package Outline Drawing 837 PSP, 12.4 × 12.0 × 0.91 mm, M530, S164* (NT90-PT438-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PT438-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

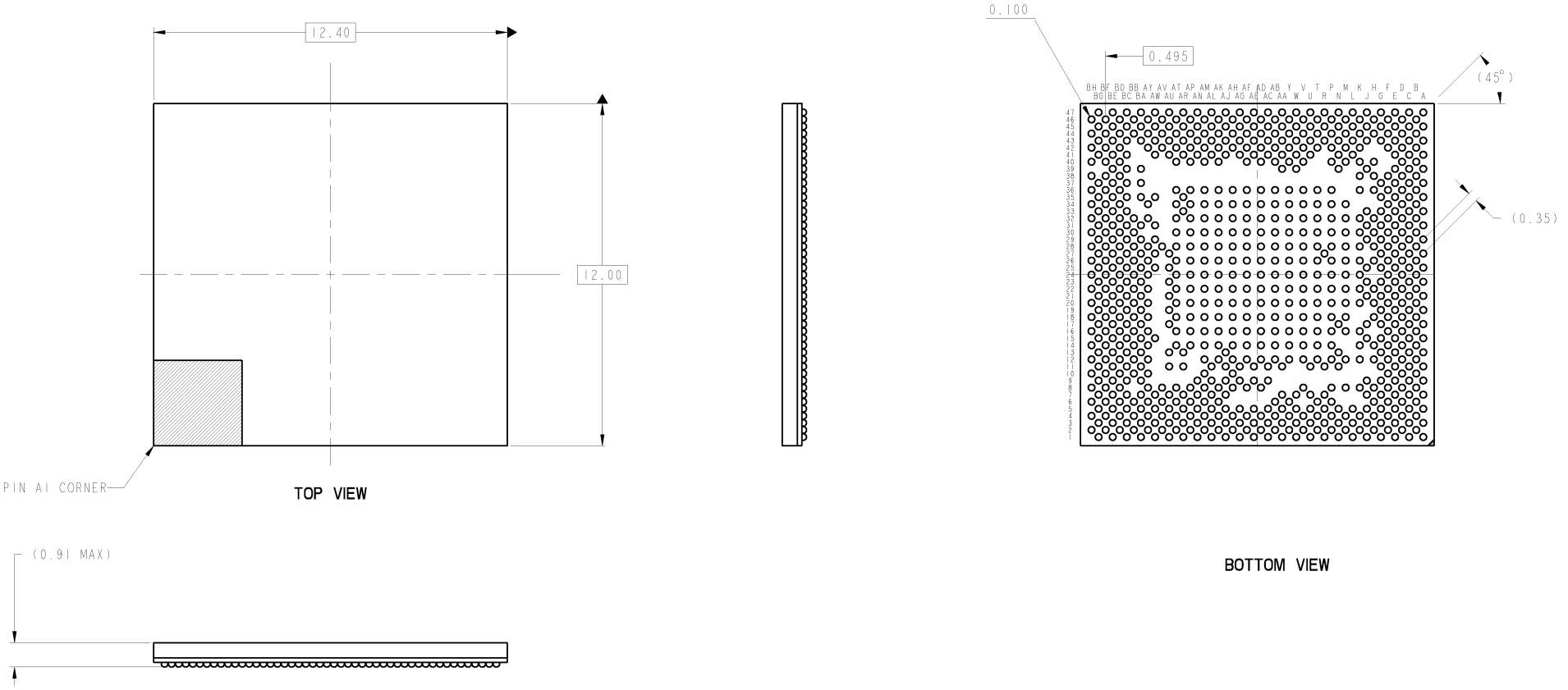


Figure 4-1 Simplified 837 PSP (12.4 × 12.0 × 0.91 mm) outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 SM6350 Part marking

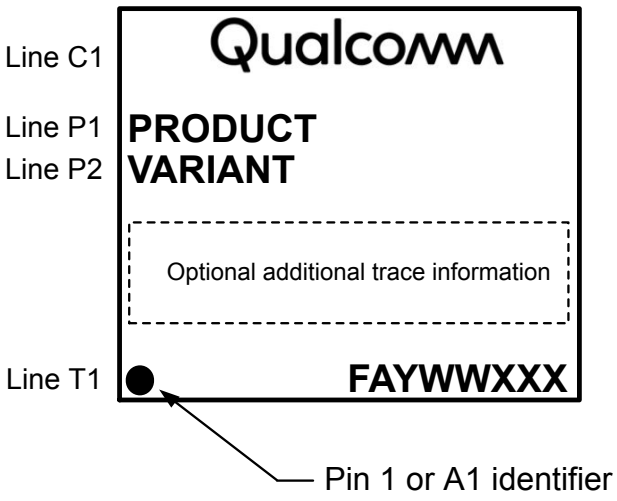


Figure 4-2 SM6350 device marking (top view, not to scale)

Table 4-1 SM6350 device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	[PRODUCT]	Qualcomm Technologies, Inc. (QTI) product name ▪ SM6350
P2	[VARIANT]	Device variant information ▪ See Table 4-4 for the assigned values.
	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ▪ F = J (Samsung) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = K (JCET StatsChipPAC, Korea) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE For complete marking definitions of all SM6350 variants and revisions, see the *SM6350 Device Revision Guide* (80-PT056-4)

Table 4-2 QFPROM_CORR_PTE_ROW0_LS

Bit location	Name	Description
[bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code as shown in the following table:

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example 1	SM-6350	-0	-PSP	837			-TR	-00	-0	-AA

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-6350-0-PSP837-TR-000-AA

Device identification details for all samples available to date are summarized in the following table:

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	Hardware revision number (JTAG_ID - see Table 4-2)	FEATURE_ID (see Table 4-2) [b]	Hardware version	Source configuration code (S) [c]	Comments	Sample date
SM6350	ES	000-AA	0x0 013F 0E1	0x0	v1.0	0	2X Gold CPU 2.0 GHz with 256 KB L2 cache, 6X Silver CPU 1.7 GHz with 64 KB L2 cache, 5G sub-6 GHz, UL, DL 256 QAM, FHD+, triple ISP, DDR -1866 MHz	3/30/2020

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
[b] The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-5.

Table 4-5 Source configuration code

S value	Die	F value = J
0	Digital	Samsung
Other columns and rows will be added in future revisions of this document, if needed.		

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in the following table:

NOTE The appropriate MSL rating is shaded in the table.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM6350 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM6350 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following link to download the SM6350 thermal package model from the CreatePoint website.

This link will be included in future revisions of this document.

After successfully logging in, the document is downloaded.

Make this document a favorite to be notified of any changes.

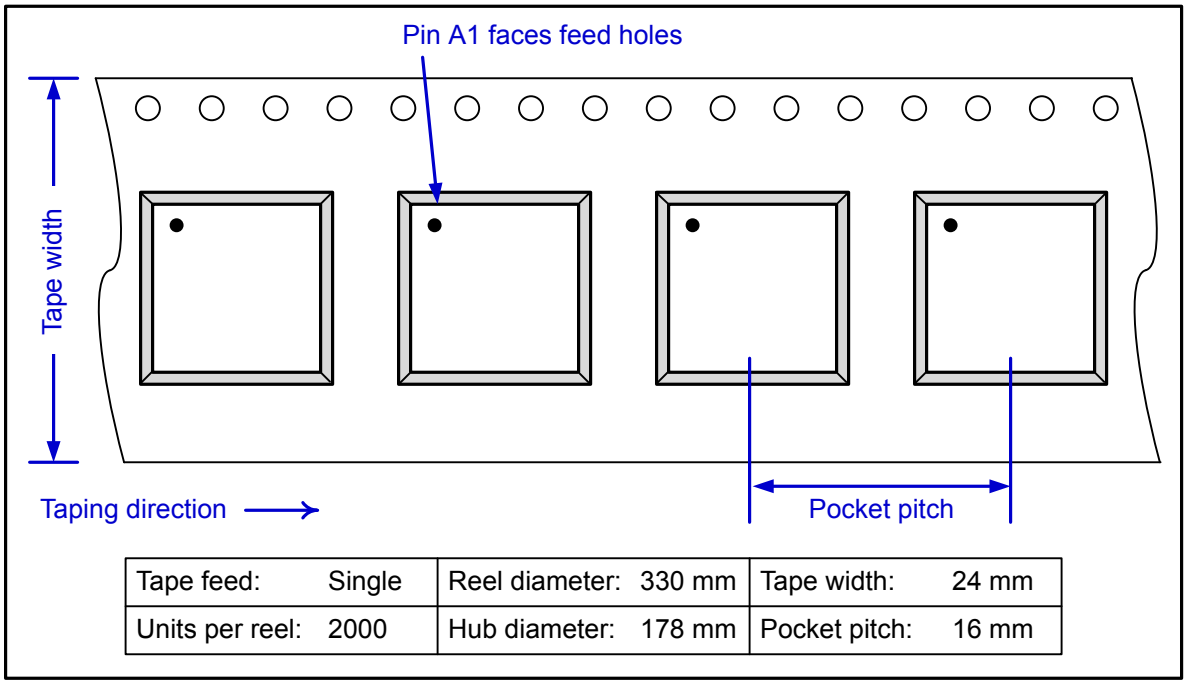
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM6350 tape carrier is shown in the following figure, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in the following figure.

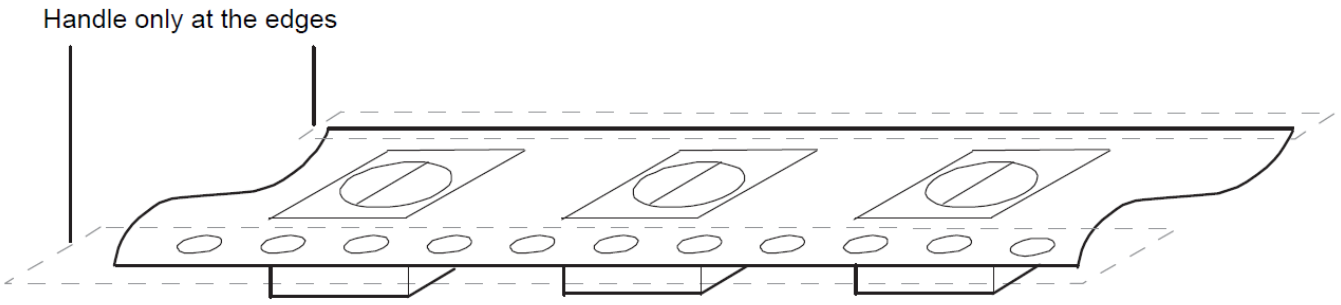


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

SM6350 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM6350 if the conditions specified in Bagged storage conditions and Out-of-bag duration have **not been exceeded**.

It is necessary to bake the SM6350 if any condition specified in Bagged storage conditions or Out-of-bag duration has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

This information will be included in a future revision of this document.

7 Part reliability

This information will be included in a future revision of this document.

8 Revision history

Revision	Date	Description
A	January 2020	Initial release
B	April 2020	■ Global: □ Updated the memory frequency □ Updated the HTA version to 220 □ Updated the gold and silver CPU frequencies ■ Figure 1-1 *Functional block diagram*: Added SMB1355 in the functional block diagram ■ *Pin map*: Updated the CreatePoint link for pin assignment spreadsheet ■ Table 1-1 *SM6350 features*: Added SMB1355 in the power management row ■ Table 2-3 *Pin descriptions*: Updated the functional description of SYNC_OUT_GPIO ■ *Electrical specifications*: Added PDN specification information ■ *Mechanical information*: Added the following sections: □ *SM6350 Part marking* □ *Device ordering information* □ *Device moisture sensitivity level* □ *Thermal characteristics* ■ *Carrier, storage, and handling information*: Added information

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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