Device description

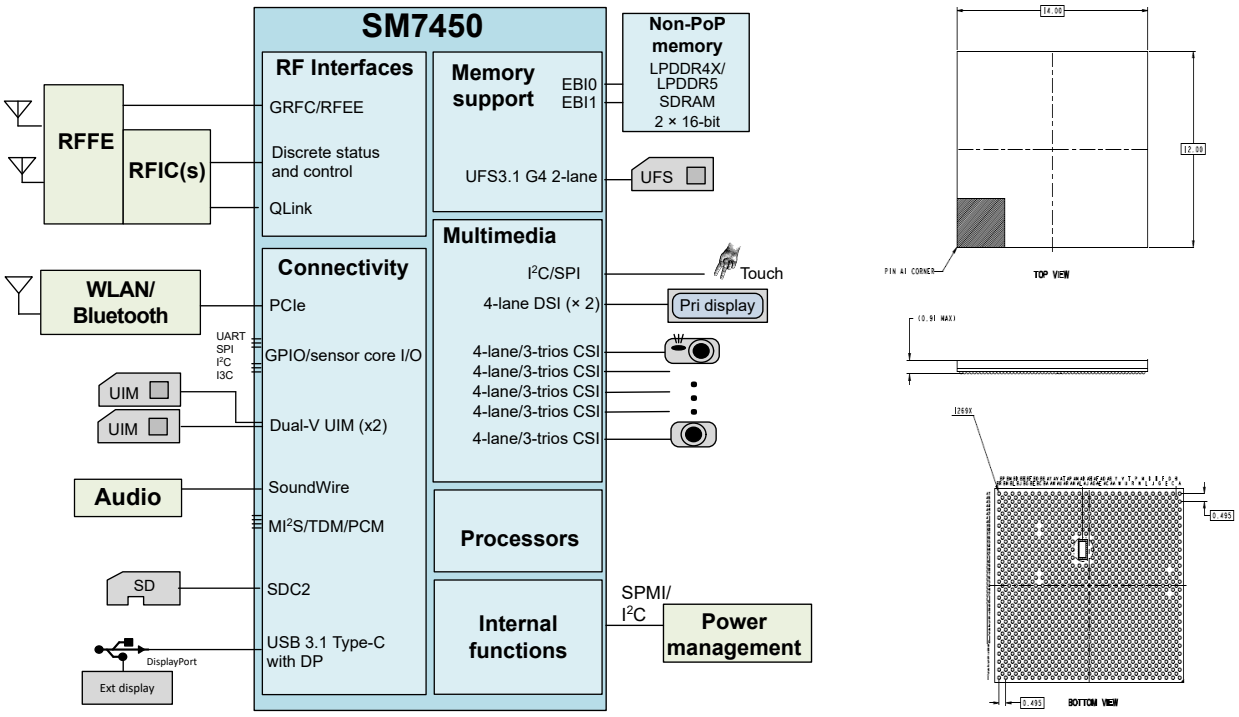
The SM7450 device is the new generation Qualcomm ® Snapdragon high-tier 5G SoC with an integrated modem. It is designed with the 4 nm process, for superior performance and power efficiency. SM7450 includes the following key components:

- Qualcomm® Kryo™ CPU built on Arm Cortex technology
  - Kryo Prime: One high performance core up to 2.4 GHz
  - Kryo Gold: Three High performance cores up to 2.36 GHz
  - Kryo Silver: Four low-power cores up to 1.8 GHz
- Qualcomm® Adreno™ GPU for better graphics performance and power efficiency
- Compute Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (HVX) and Hexagon Tensor Accelerator
- Qualcomm Spectra™ ISP image-processing engine for the ultimate photography and videography experiences
- VPU for high-quality, ultra HD video encode and decode
- DPU for on-device and external ultra HD display support
- Low-power island (LPI): contains DSP and embedded AI accelerator shared between the Snapdragon sensor core and low-power audio subsystem, supporting always-on use cases like sensors and keyword detection.
- Memory: dual-channel non-package-on-package (non-PoP) high-speed LPDDR5/LPDDR4X SDRAM
  - LPDDR5 SDRAM designed for 3200 MHz clock (2 × 16-bit)
  - LPDDR4X SDRAM designed for 2133 MHz clock (2 × 16-bit)

Key features

- Always-on subsystem with RPMh for hardware-based resource and power management.
- Qualcomm® Universal bandwidth compression (UBWC) with camera, display, GPU, video, and compute DSP
- More RF operating bands and advanced techniques with SDR735, QTM545, and SMR546:
  - 3GPP Rel. 16 5G NR
  - mmW and sub-6 GHz 5G NR
  - UL 256 QAM and DL 256 QAM support for sub-6 GHz
  - EN-DC mode support
  - 64 QAM uplink/downlink in mmW TDD
  - Rel. 16 LTE multimode modem
  - UL 256 QAM and DL 256 QAM support for LTE
  - DC-HSPA+, CDMA, WCDMA, and GSM
- Display support: FHD+, 10 bit DisplayPort, ten hardware layers, improved HDR10+, and wide color Gamut, Qualcomm® Low-Power Picture Enhancement display feature, and Qualcomm® True Palette Display feature, VESA DSC 1.2
- Two 4-lane DSI DSC1.2, D-PHY 1.2, or C-PHY 1.1
- Triple 14-bit image front end (IFE) + two lite IFE 25 + 25 + 25 MP, 84 MP/30 fps
- Five 4-lane CSIs (4/4/4/4/4) D-PHY 1.2 or C-PHY 1.2
- Support for UFS 3.1 Gear 4 (two-lane), SD 3.0
- Support for USB 3.1 Type-C with DisplayPort 1.4 and USB 2.0
- External WLAN 2 × 2 802.11a/b/g/n/ac/ax MU-MIMO, Bluetooth 5.2, and FM

SM7450 high-level block diagram and PSP1269B outline drawing



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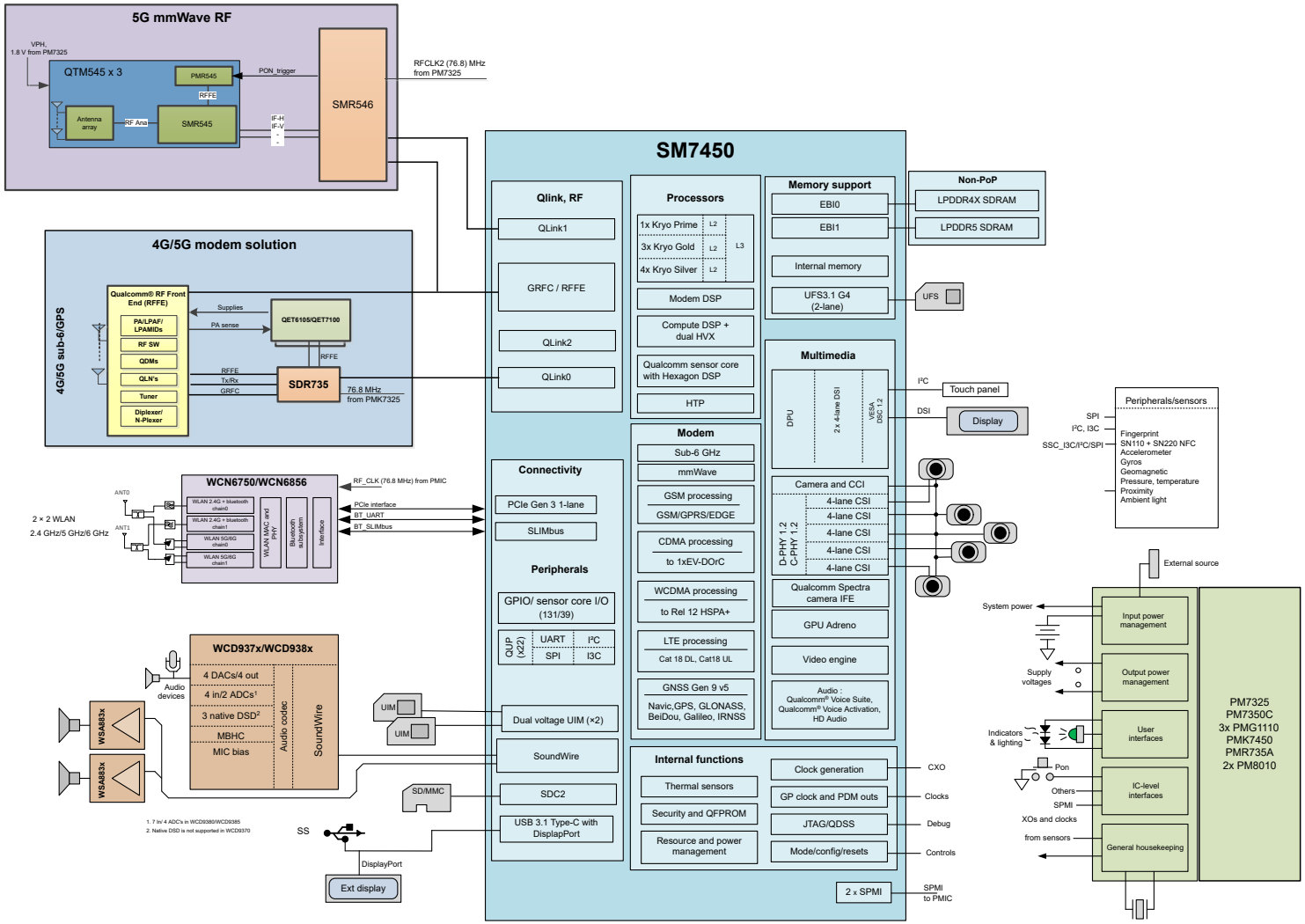
1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram



Note: SM7450-AB SKU will need 1x PMG1110. It is recommended to account for additional 2x PMG1110 to mitigate any future hardware redesign.

Figure 1-1 SM7450 functional block diagram

1.2 SM7450 features

NOTE Some of the hardware features integrated within the SM7450 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM7450 features.

Table 1-1 SM7450 features

Feature	SM7450 capability
Processors	
Applications	Kryo CPU built on Arm Cortex technology ■ Kryo Prime: One high performance core up to 2.4 GHz ■ Kryo Gold: Three high performance cores up to 2.36 GHz ■ Kryo Silver: Four low-power cores up to 1.8 GHz
Digital signal processing and artificial intelligence	Compute Hexagon DSP with dual HVX and Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Low power island (LPI)	LPI with Hexagon DSP consists of Snapdragon sensor core and lowpower audio subsystem
Modem	2G/3G/4G/5G – mmWave and sub-6 GHz bands (Rel. 16)
Qualcomm® Location™	Gen 9 VT v5
Memory support	
System memory via non-PoP and EBI	■ Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM designed for a 2133 MHz (2 × 16-bit) clock ■ LPDDR5 3200 MHz (2 × 16-bit) clock
External memory Via UFS Via SDC Other internal memory	 UFS3.1 G4 (2-lane) SD v3.0 4 bit for SD card 172 KB IMEM 1.5 MB GMEM for graphics
RF support	
RF operating bands	Defined by the RF transceiver SDR735 device
Air interfaces	
5G NR LTE CDMA, WCDMA, and GSM WLAN/Bluetooth Antenna sharing GNSS – Integrated Qualcomm® Location Suite engine	Yes, Rel. 16 Yes, Rel.16 LTE multimode modem Yes Yes with WCN6750/WCN6856 Antenna shared between Wi-Fi and WAN Gen 9VT; GPS, GLONASS, NavIC, BeiDou, Galileo, QZSS, and SBAS

Table 1-1 SM7450 features (cont.)

Feature	SM7450 capability
Multimedia	
Display support	DPU: ■ Maximum resolution for internal panel: FHD+ 144 fps ■ 2x DSI DPHY (4-lane); DSI D-PHY 1.2 or C-PHY 1.1; VESA DSC 1.2 ■ 4K60 DP1.4 (USB3 + DisplayPort concurrency)
Camera support	Qualcomm Spectra: 84 MP at 30 fps/3 × 25 MP 30 fps ZSL Qualcomm Spectra ISP supports connectivity to multiple cameras due to five C-PHY/D-PHY interfaces. ■ Real-time sensor input resolution: 25 + 25 + 25 ■ Three IFE + two IFE lite, up to eight sensors, five concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 configuration ■ 5x D-PHY v1.2 /C-PHY v1.2
Video processing unit (VPU)	VPU – fifth-generation UHD video processing unit ■ Video decode: Up to 4K30 for H.264/H.265/VP9 ■ Video encode: Up to 4K30 for H.264/H.265 ■ Video concurrency: 1080p60 decode and 1080p60 encode/ 4K30 decode + 1080p30 encode ■ HDR playback: Support for HDR10 and HDR10+ ■ HFR capture: 720p at 240 fps or 1080p at 120 fps
Adreno graphic processing unit (GPU)	Adreno GPU OpenGL ES 3.2, Vulkan 1.x OpenCL 2.0, DX FL12
Audio (Low power audio subsystem) Codec Speaker amplifier	LPI, improved voice UI concurrencies, ML hardware accelerator; V66M, LPI shared with Sensor SS ■ eNPU/AI accelerator: Embedded AI accelerator for LPI and low power use cases ■ Hardware adaptive filter enabled voice UI always by offloading echo cancellation processing ■ Hardware resampler ■ DSP offload for audio playback, including USB digital audio and Bluetooth audio WCD937x/WCD938x high fidelity audio codec WSA883x class-H, low noise smart amplifier
Audio interfaces	■ SLIMbus for WCN6750 and WCN6856 ■ SoundWire interface (two Tx and two Rx data for codec) ■ SoundWire MIC support ■ Dedicated SoundWire interface for smart speaker amplifier ■ Four DMIC ports in LPI ■ Five MI^{2}S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application ■ One MI^{2}S supports four data lanes for up to eight channels Tx/Rx application
Connectivity	
Qualcomm universal peripheral (QUP) ports	22: Multiplexed serial interface functions
USB	One USB 3.1 port: Gen 2, 10 Gbps (DisplayPort + data), support Type-C with DisplayPort v1.4
PCIe	PCIe Gen 3 1-lane

Table 1-1 SM7450 features (cont.)

Feature	SM7450 capability
Secure digital interfaces	■ SDC2 (SD3.0) ■ SDC2 is dual-voltage ■ SD card; UFS
Touchscreen support	Capacitive panels via ext IC (I^2C, SPI)
Configurable GPIOs	
Number of GPIO ports	170
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
Crypto	AES-GCM, hardware ECC and RSA (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP certifiable
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure Boot with Sec tools 2.0; easy to use tool set
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted
TrustZone	Qualcomm® Trusted Execution Environment (TEE) v5.4
DRM	Widevine V16 L1, HDCP v2.3
QTEE services	ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
Boot sequence	1. TME ROM FW+ Applications PBL 2. XBL 3. SHRM 4. AOP 5. HLOS 6. Rest of subsystems Emergency boot over USB 3.1
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Chipset interface features	
QLink	Three QLink0/1/2 ports for sub-6 and mmWave applications
Power management	2-channel 2-line SPMI; plus other lines, as needed, via GPIOs, I^2C PM7325 + PM7350C + 3x PMG1110 + PMK7450 + PMR735A + 2x PM8010
Wireless connectivity	
WLAN	PCIe interface
Bluetooth	SLIMbus/UART interface
Fabrication technology and package	

Table 1-1 SM7450 features (cont.)

Feature	SM7450 capability
Digital die	4 nm process
Non-PoP – small, thermally efficient package	14.0 × 12.0 × 0.91 mm

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
3GPP 5G Rel.16	■ Sub-6 GHz, 5G NR - FDD < 3 GHz, TDD frequencies n77, n78, and n79 ■ Standalone mode (SA) and non-standalone mode (NSA) support ■ 256 QAM for uplink and downlink ■ DL 4 × 4 MIMO and UL 2 × 2 UL MIMO support for sub-6 ■ EN-DC mode support ■ NR CA support
	■ mmW – n257, n258, n260, and n261 ■ TDD only ■ 64 QAM for uplink (UL)/downlink (DL)
3GPP LTE Rel.16	■ Cat18 download and upload ■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ Four-way Rx diversity ■ 4 × 4 MIMO using single LTE TRx, LTE-U, and LAA ■ UL: 256 QAM; DL: 256 QAM for LTE
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1x SLTE and 1x SRLTE ■ hVoLTE and hSRLTE ■ VoNR support
Multi-SIM	
MSIM	5G/4G/3G/2G (SIM1) + 5G/4G/3G/2G (SIM2)
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/5G - Wi-Fi selection

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite with global navigation satellite system (GNSS) support	
Gen 9VT	GPS, GLONASS, NavIC, BeiDou, Galileo, QZSS, and SBAS

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN6750/WCN6856	802.11ax, 2 × 2 MU-MIMO (Wi-Fi 6E)
Bluetooth	
With WCN6750/WCN6856	Bluetooth 5.2 (Milan) compliant

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX0	Power for pad group 0
PX1	Power for pad group 1
PX2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX3	Pad group 3 (most peripherals); 1.8 V
PX5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_A_CSI_X_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_A_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SM7450 is available in the PSP1269B package. See Mechanical information for package details. A high-level view of the pin assignments is shown in the following figure. The text within the figure is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM7450 Pin Assignment and GPIO Configuration Spreadsheet* (80-26135-1A). This Microsoft Excel spreadsheet lists all SM7450 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the pin assignment spreadsheet (80-26135-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-26135-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

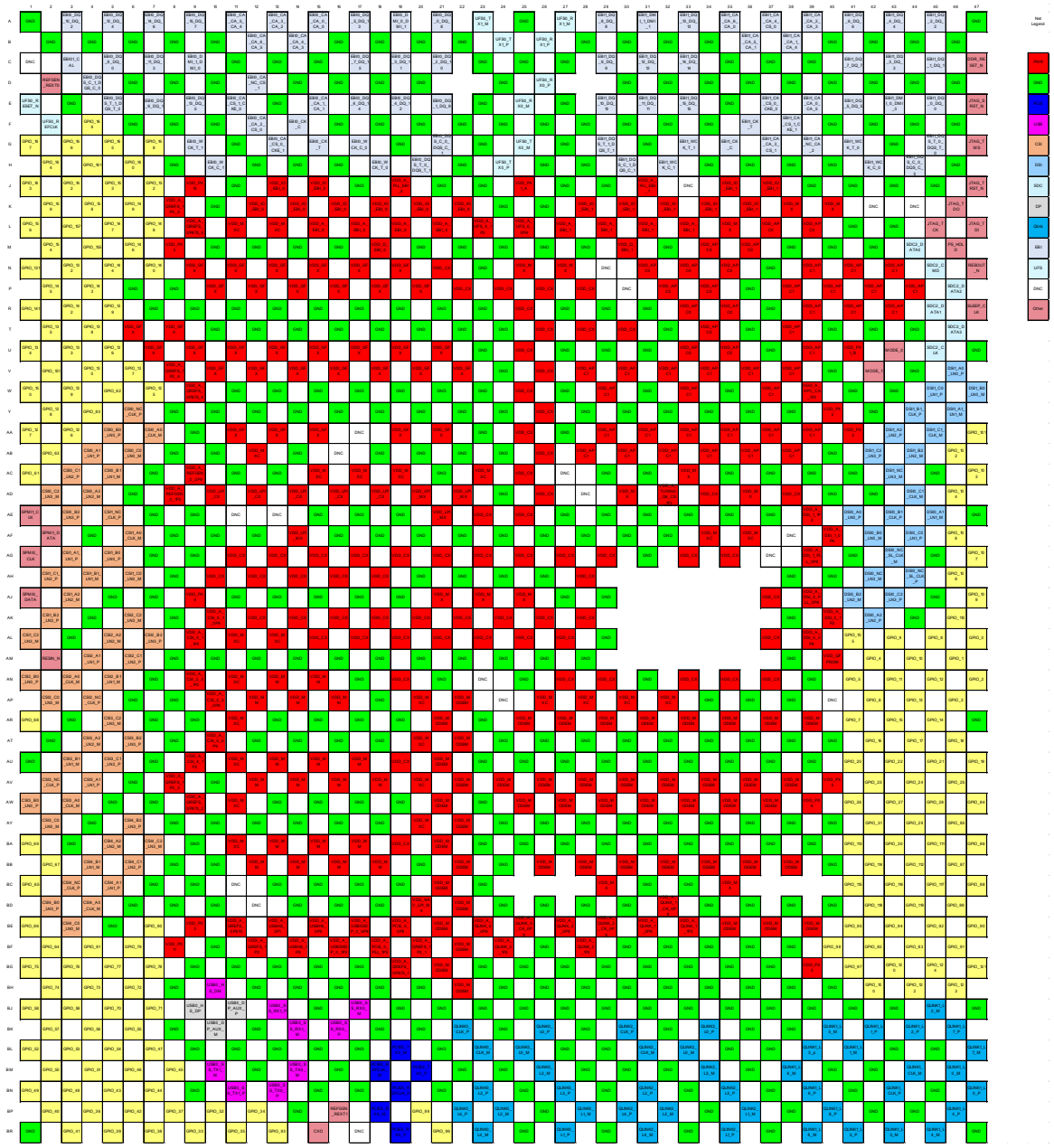


Figure 2-1 SM7450 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AA7	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
AB4	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
AD4	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
AA5	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY), trio lane 0 – B
AC5	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
AE3	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
AB6	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
AC3	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
AD2	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
Y6	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock – positive MIPI CSI 0 (C-PHY), no connect
AF6	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A
AG3	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A
AJ3	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A
AG5	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 – positive MIPI CSI 1 (C-PHY), trio lane 0 – B
AH4	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B
AK2	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B
AH6	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C
AH2	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AL1	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C
AE5	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
AN3	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock – negative MIPI CSI 2 (C-PHY), trio lane 0 – A
AM4	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 – positive MIPI CSI 2 (C-PHY), trio lane 1 – A
AL5	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – negative MIPI CSI 2 (C-PHY), trio lane 2 – A
AN1	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
AN5	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 – negative MIPI CSI 2 (C-PHY), trio lane 1 – B
AL7	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – positive MIPI CSI 2 (C-PHY), trio lane 2 – B
AP2	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – negative MIPI CSI 2 (C-PHY), trio lane 0 – C
AM6	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – positive MIPI CSI 2 (C-PHY), trio lane 1 – C
AK6	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – negative MIPI CSI 2 (C-PHY), trio lane 2 – C
AP4	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock – positive MIPI CSI 2 (C-PHY), no connect
AW3	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A
AV4	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A
AT4	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A
AW1	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B
AU3	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B
AT6	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B
AY2	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AU5	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C
AR5	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C
AV2	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect
BD4	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
BC5	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
BA5	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
BD2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY), trio lane 0 – B
BB4	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
AY6	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
BE3	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
BB6	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
BA7	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
BC3	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock – positive MIPI CSI 0 (C-PHY), no connect
BR15	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
C47	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
AE41	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - positive MIPI DSI 0 (C-PHY), trio lane 0 – A
AE45	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - negative MIPI DSI 0 (C-PHY), trio lane 1 – A
AK42	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - positive MIPI DSI 0 (C-PHY), trio lane 2 – A
AH42	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - negative
AF42	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - negative MIPI DSI 0 (C-PHY), trio lane 0 – B
AE43	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock - positive MIPI DSI 0 (C-PHY), trio lane1 – B

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AJ41	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - negative MIPI DSI 0 (C-PHY), trio lane 2 – B
AH44	DSI0_NC_SL_CLK_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), SL differential clock - positive
AF44	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - positive MIPI DSI 0 (C-PHY), trio lane 0 – C
AD44	DSI0_C1_CLK_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock - negative MIPI DSI 0 (C-PHY), trio lane 1 – C
AJ43	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - positive MIPI DSI 0 (C-PHY), trio lane 2 – C
AG43	DSI0_NC_SL_CLK_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), SL differential clock - negative
V46	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - positive MIPI DSI 1 (C-PHY), trio lane 0 – A
Y46	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - negative MIPI DSI 1 (C-PHY), trio lane 1 – A
AA43	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - positive MIPI DSI 1 (C-PHY), trio lane 2 – A
AC43	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - negative
W47	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - negative MIPI DSI 1 (C-PHY), trio lane 0 – B
Y44	DSI1_B1_CLK_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock - positive MIPI DSI 1 (C-PHY), trio lane1 – B
AB44	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - negative MIPI DSI 1 (C-PHY), trio lane 2 – B
W45	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - positive MIPI DSI 1 (C-PHY), trio lane 0 – C
AA45	DSI1_C1_CLK_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock - negative MIPI DSI 1 (C-PHY), trio lane 1 – C
AB42	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - positive MIPI DSI 1 (C-PHY), trio lane 2 – C
C3	EBI01_CAL	EBI	AI	EBI 0/1 LPDDRx calibration resistor
A15	EBI0_CA_CA_0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0 EBI0 LPDDR4X command/address bit 0
E15	EBI0_CA_CA_1_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1 EBI0 LPDDR4X command/address bit 1
F12	EBI0_CA_CA_2_CS_0	EBI	DO	EBI0 LPDDR5 command/address bit 2 EBI0 LPDDR4X chip select 0
A13	EBI0_CA_CA_3_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 3 EBI0 LPDDR4X command/address bit 2

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B14	EBI0_CA_CA_4_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 4 EBI0 LPDDR4X command/address bit 3
A11	EBI0_CA_CA_5_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 5 EBI0 LPDDR4X command/address bit 4
B12	EBI0_CA_CA_6_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 6 EBI0 LPDDR4X command/address bit 5
G13	EBI0_CA_CS_0_CKE_1	EBI	DO	EBI0 LPDDR5 chip select 0 EBI0 LPDDR4X clock enable 1
E11	EBI0_CA_CS_1_CKE_0	EBI	DO	EBI0 LPDDR5 chip select 1 EBI0 LPDDR4X clock enable 0
D12	EBI0_CA_NC_CS_1	EBI	DO	EBI0 LPDDR4 chip select 1
F14	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock – negative EBI0 LPDDR4X differential clock – negative
G15	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock – positive EBI0 LPDDR4X differential clock – positive
A19	EBI0_DMI_0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask inversion 0 EBI0 LPDDR4X data mask inversion 1
C9	EBI0_DMI_1_DMI_0	EBI	DO	EBI0 LPDDR5 data mask inversion 1 EBI0 LPDDR4X data mask inversion 0
G21	EBI0_DQS_C_0_DQS_C_1	EBI	B	EBI0 LPDDR5 differential data strobe for byte 0 negative EBI0 LPDDR4X differential data strobe for byte 1 negative
D4	EBI0_DQS_C_1_DQS_C_0	EBI	B	EBI0 LPDDR5 differential data strobe for byte 1 negative EBI0 LPDDR4X differential data strobe for byte 0 negative
H20	EBI0_DQS_T_0_DQS_T_1	EBI	B	EBI0 LPDDR5 differential data strobe for byte 0 positive EBI0 LPDDR4X differential data strobe for byte 1 positive
E5	EBI0_DQS_T_1_DQS_T_0	EBI	B	EBI0 LPDDR5 differential data strobe for byte 1 positive EBI0 LPDDR4X differential data strobe for byte 0 positive
A21	EBI0_DQ_0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 0 EBI0 LPDDR4X data bit 8
A3	EBI0_DQ_10_DQ_2	EBI	B	EBI0 LPDDR5 data bit 10 EBI0 LPDDR4X data bit 2
C7	EBI0_DQ_11_DQ_3	EBI	B	EBI0 LPDDR5 data bit 11 EBI0 LPDDR4X data bit 3
A5	EBI0_DQ_12_DQ_4	EBI	B	EBI0 LPDDR5 data bit 12 EBI0 LPDDR4X data bit 4
E9	EBI0_DQ_13_DQ_5	EBI	B	EBI0 LPDDR5 data bit 13 EBI0 LPDDR4X data bit 5

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
A7	EBI0_DQ_14_DQ_6	EBI	B	EBI0 LPDDR5 data bit 14 EBI0 LPDDR4X data bit 6
A9	EBI0_DQ_15_DQ_7	EBI	B	EBI0 LPDDR5 data bit 15 EBI0 LPDDR4X data bit 7
E21	EBI0_DQ_1_DQ_9	EBI	B	EBI0 LPDDR5 data bit 1 EBI0 LPDDR4X data bit 9
C21	EBI0_DQ_2_DQ_10	EBI	B	EBI0 LPDDR5 data bit 2 EBI0 LPDDR4X data bit 10
C19	EBI0_DQ_3_DQ_11	EBI	B	EBI0 LPDDR5 data bit 3 EBI0 LPDDR4X data bit 11
E19	EBI0_DQ_4_DQ_12	EBI	B	EBI0 LPDDR5 data bit 4 EBI0 LPDDR4X data bit 12
A17	EBI0_DQ_5_DQ_13	EBI	B	EBI0 LPDDR5 data bit 5 EBI0 LPDDR4X data bit 13
E17	EBI0_DQ_6_DQ_14	EBI	B	EBI0 LPDDR5 data bit 6 EBI0 LPDDR4X data bit 14
C17	EBI0_DQ_7_DQ_15	EBI	B	EBI0 LPDDR5 data bit 7 EBI0 LPDDR4X data bit 15
C5	EBI0_DQ_8_DQ_0	EBI	B	EBI0 LPDDR5 data bit 8 EBI0 LPDDR4X data bit 0
E7	EBI0_DQ_9_DQ_1	EBI	B	EBI0 LPDDR5 data bit 9 EBI0 LPDDR4X data bit 1
G17	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 negative
H10	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 negative
H18	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 positive
G9	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 positive
E39	EBI1_CA_CA_0_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 0 EBI1 LPDDR4X command/address bit 5
B38	EBI1_CA_CA_1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 1 EBI1 LPDDR4X command/address bit 4
A39	EBI1_CA_CA_2_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 2 EBI1 LPDDR4X command/address bit 3
G37	EBI1_CA_CA_3_CS_1	EBI	DO	EBI1 LPDDR5 command/address bit 3 EBI1 LPDDR4X chip select 1
A37	EBI1_CA_CA_4_CS_0	EBI	DO	EBI1 LPDDR5 command/address bit 4 EBI1 LPDDR4X chip select 0
B36	EBI1_CA_CA_5_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 5 EBI1 LPDDR4X command/address bit 1

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
A35	EBI1_CA_CA_6_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 6 EBI1 LPDDR4X command/address bit 0
E37	EBI1_CA_CS_0_CKE_0	EBI	DO	EBI1 LPDDR5 chip select 0 EBI1 LPDDR4X clock enable 0
F38	EBI1_CA_CS_1_CKE_1	EBI	DO	EBI1 LPDDR5 chip select 1 EBI1 LPDDR4X clock enable 1
G39	EBI1_CA_NC_CA_2	EBI	D	EBI1 LPDDR4X command/address bit 2
G35	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock – negative EBI1 LPDDR4X differential clock – negative
F36	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock – positive EBI1 LPDDR4X differential clock – positive
E43	EBI1_DMI_0_DMI_0	EBI	DO	EBI1 LPDDR5 data mask 0 EBI1 LPDDR4X data mask 0
A31	EBI1_DMI_1_DMI_1	EBI	DO	EBI1 LPDDR5 data mask 1 EBI1 LPDDR4X data mask 1
H44	EBI1_DQS_C_0_DQS_C_0	EBI	B	EBI1 LPDDR5 differential data strobe for byte 0 negative EBI1 LPDDR4X differential data strobe for byte 0 negative
H30	EBI1_DQS_C_1_DQS_C_1	EBI	B	EBI1 LPDDR5 differential data strobe for byte 1 negative EBI1 LPDDR4X differential data strobe for byte 1 negative
G45	EBI1_DQS_T_0_DQS_T_0	EBI	B	EBI1 LPDDR5 differential data strobe for byte 0 positive EBI1 LPDDR4X differential data strobe for byte 0 positive
G29	EBI1_DQS_T_1_DQS_T_1	EBI	B	EBI1 LPDDR5 differential data strobe for byte 1 positive EBI1 LPDDR4X differential data strobe for byte 1 positive
E45	EBI1_DQ_0_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0 EBI1 LPDDR4X data bit 0
E29	EBI1_DQ_10_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10 EBI1 LPDDR4X data bit 10
E31	EBI1_DQ_11_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11 EBI1 LPDDR4X data bit 11
C31	EBI1_DQ_12_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12 EBI1 LPDDR4X data bit 12
A33	EBI1_DQ_13_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13 EBI1 LPDDR4X data bit 13
C33	EBI1_DQ_14_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14 EBI1 LPDDR4X data bit 14
E33	EBI1_DQ_15_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15 EBI1 LPDDR4X data bit 15

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
C45	EBI1_DQ_1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1 EBI1 LPDDR4X data bit 1
A45	EBI1_DQ_2_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2 EBI1 LPDDR4X data bit 2
C43	EBI1_DQ_3_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3 EBI1 LPDDR4X data bit 3
A43	EBI1_DQ_4_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4 EBI1 LPDDR4X data bit 4
E41	EBI1_DQ_5_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5 EBI1 LPDDR4X data bit 5
A41	EBI1_DQ_6_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6 EBI1 LPDDR4X data bit 6
C41	EBI1_DQ_7_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7 EBI1 LPDDR4X data bit 7
A29	EBI1_DQ_8_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8 EBI1 LPDDR4X data bit 8
C29	EBI1_DQ_9_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9 EBI1 LPDDR4X data bit 9
H42	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 negative
H32	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 negative
G41	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 positive
G33	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 positive
E47	JTAG_SRST_N	PX_3	PU:nppdkp DI	JTAG reset for debug
L45	JTAG_TCK	PX_3	PU:nppdkp DI	JTAG clock input
L47	JTAG_TDI	PX_3	PU:nppdkp DI	JTAG data input
K46	JTAG_TDO	PX_3	DO:Z	JTAG data output
G47	JTAG_TMS	PX_3	PU:nppdkp B	JTAG mode select input
J47	JTAG_TRST_N	PX_3	PD:nppukp DI	JTAG reset
U43	MODE_0	PX_3	DI	Mode control bit 0 – unconnected for native mode
V42	MODE_1	PX_3	DI	Mode control bit 1 – unconnected for native mode
BM18	PCIE0_REFCLK_M	–	AI, AO	PCIe 0 Gen 3 reference clock – negative
BN19	PCIE0_REFCLK_P	–	AI, AO	PCIe 0 Gen 3 reference clock – positive
BP18	PCIE0_RX0_M	–	AI	PCIe 0 Gen 3 receive – negative
BR19	PCIE0_RX0_P	–	AI	PCIe 0 Gen 3 receive – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
BL19	PCIE0_TX0_M	–	AO	PCIe 0 Gen 3 transmit – negative
BM20	PCIE0_TX0_P	–	AO	PCIe 0 Gen 3 transmit – positive
M46	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
BL23	QLINK0_CLK_M	–	AI, AO	QLink0 clock – minus
BK22	QLINK0_CLK_P	–	AI, AO	QLink0 clock – positive
BP24	QLINK0_L2_M	–	AI, AO	QLink0 lane 2 – minus
BN23	QLINK0_L2_P	–	AI, AO	QLink0 lane 2 – positive
BM26	QLINK0_L3_M	–	AI, AO	QLink0 lane 3 – minus
BN27	QLINK0_L3_P	–	AI, AO	QLink0 lane 3 – positive
BR23	QLINK0_L4_M	–	AI, AO	QLink0 lane 4 – minus
BP22	QLINK0_L4_P	–	AI, AO	QLink0 lane 4 – positive
BL25	QLINK0_L0_M	–	AI, AO	QLink0 lane 0 – minus
BK26	QLINK0_L0_P	–	AI, AO	QLink0 lane 0 – positive
BP28	QLINK0_L1_M	–	AI, AO	QLink0 lane 1 – minus
BR27	QLINK0_L1_P	–	AI, AO	QLink0 lane 1 – positive
BM44	QLINK1_CLK_M	–	AI, AO	QLink1 clock – minus
BN43	QLINK1_CLK_P	–	AI, AO	QLink1 clock – positive
BR45	QLINK1_L4_M	–	AI, AO	QLink1 lane 4 – minus
BP46	QLINK1_L4_P	–	AI, AO	QLink1 lane 4 – positive
BL47	QLINK1_L7_M	–	AI, AO	QLink1 lane 7 – minus
BK46	QLINK1_L7_P	–	AI, AO	QLink1 lane 7 – positive
BR43	QLINK1_L5_M	–	AI, AO	QLink1 lane 5 – minus
BR41	QLINK1_L5_P	–	AI, AO	QLink1 lane 5 – positive
BM38	QLINK1_L6_M	–	AI, AO	QLink1 lane 6 – minus
BN39	QLINK1_L6_P	–	AI, AO	QLink1 lane 6 – positive
BR39	QLINK1_L8_M	–	AI, AO	QLink1 lane 8 – minus
BP40	QLINK1_L8_P	–	AI, AO	QLink1 lane 8 – positive
BM46	QLINK1_L0_M	–	AI, AO	QLink1 lane 0 – minus
BN47	QLINK1_L0_P	–	AI, AO	QLink1 lane 0 – positive
BJ45	QLINK1_L2_M	–	AI, AO	QLink1 lane 2 – minus
BK44	QLINK1_L2_P	–	AI, AO	QLink1 lane 2 – positive
BL41	QLINK1_L1_M	–	AI, AO	QLink1 lane 1 – minus
BK42	QLINK1_L1_P	–	AI, AO	QLink1 lane 1 – positive
BK40	QLINK1_L3_M	–	AI, AO	QLink1 lane 3 – minus
BL39	QLINK1_L3_P	–	AI, AO	QLink1 lane 3 – positive
BL31	QLINK2_CLK_M	–	AI, AO	QLink2 clock – minus
BK30	QLINK2_CLK_P	–	AI, AO	QLink2 clock – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
BP32	QLINK2_L2_M	–	AI, AO	QLink2 lane 2 – minus
BN31	QLINK2_L2_P	–	AI, AO	QLink2 lane 2 – positive
BM34	QLINK2_L3_M	–	AI, AO	QLink2 lane 3 – minus
BN35	QLINK2_L3_P	–	AI, AO	QLink2 lane 3 – positive
BR31	QLINK2_L4_M	–	AI, AO	QLink2 lane 4 – minus
BP30	QLINK2_L4_P	–	AI, AO	QLink2 lane 4 – positive
BL33	QLINK2_L0_M	–	AI, AO	QLink2 lane 0 – minus
BK34	QLINK2_L0_P	–	AI, AO	QLink2 lane 0 – positive
BP36	QLINK2_L1_M	–	AI, AO	QLink2 lane 1 – minus
BR35	QLINK2_L1_P	–	AI, AO	QLink2 lane 1 – positive
D2	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
BP16	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
AM2	RESIN_N	PX_0	DI	Reset input
N47	RESOUT_N	PX_3	DO	Reset output
U45	SDC2_CLK	PX_2	NP:pdpukp DO	Secure digital controller 2 clock
N45	SDC2_CMD	PX_2	NP:pdpukp B	Secure digital controller 2 command
M44	SDC2_DATA0	PX_2	NP:pdpukp B	Secure digital controller 2 data bit 0
R45	SDC2_DATA1	PX_2	NP:pdpukp B	Secure digital controller 2 data bit 1
P46	SDC2_DATA2	PX_2	NP:pdpukp B	Secure digital controller 2 data bit 2
T46	SDC2_DATA3	–	NP:pdpukp B	Secure digital controller 2 data bit 3
R47	SLEEP_CLK	PX_3	DI	Sleep clock
AG1	SPMI0_CLK	PX_0	PD:nppukp DO	Slave and PBUS interface for PMICs – clock 0
AJ1	SPMI0_DATA	PX_0	PD:nppukp B	Slave and PBUS interface for PMICs – data 0
AE1	SPMI1_CLK	PX_0	PD:nppukp DO	Slave and PBUS interface for PMICs – clock 1
AF2	SPMI1_DATA	PX_0	PD:nppukp B	Slave and PBUS interface for PMICs – data 1
F2	UFS0_REFCLK	PX_10	Z:PD:nppukp DO	UFS reference clock
E1	UFS0_RESET_N	PX_10	Z:PD:nppukp DO	UFS reset

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
E25	UFS0_RX0_M	–	AI	UFS lane 0 receiver – negative
D26	UFS0_RX0_P	–	AI	UFS lane 0 receiver – positive
A27	UFS0_RX1_M	–	AI	UFS lane 1 receiver – negative
B26	UFS0_RX1_P	–	AI	UFS lane 1 receiver – positive
G25	UFS0_TX0_M	–	AO	UFS lane 0 transmit – negative
H24	UFS0_TX0_P	–	AO	UFS lane 0 transmit – positive
A23	UFS0_TX1_M	–	AO	UFS lane 1 transmit – negative
B24	UFS0_TX1_P	–	AO	UFS lane 1 transmit – positive
BK10	USB0_DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – negative
BJ11	USB0_DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – positive
BH10	USB0_HS_DM	–	AI, AO	USB 2.0 high-speed data – negative
BJ9	USB0_HS_DP	–	AI, AO	USB 2.0 high-speed data – positive
BJ17	USB0_SS_RX0_M	–	AI	USB 3.0 Type-C PHY receiver 0 – negative
BK16	USB0_SS_RX0_P	–	AI	USB 3.0 Type-C PHY receiver 0 – positive
BK14	USB0_SS_RX1_M	–	AI	USB 3.0 Type-C PHY receiver 1 – negative
BJ13	USB0_SS_RX1_P	–	AI	USB 3.0 Type-C PHY receiver 1 – positive
BM14	USB0_SS_TX0_M	–	AO	USB 3.0 Type-C PHY transmit 0 – negative
BN13	USB0_SS_TX0_P	–	AO	USB 3.0 Type-C PHY transmit 0 – positive
BM10	USB0_SS_TX1_M	–	AO	USB 3.0 Type-C PHY transmit 1 – negative
BN11	USB0_SS_TX1_P	–	AO	USB 3.0 Type-C PHY transmit 1 – positive

[a] See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See the following table for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM7450 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the *SM7450 Pin Assignment and GPIO Configuration Spreadsheet* (80-26135-1A) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-26135-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AL47	GPIO_0		PD:nppuk	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP 0 SE0, lane 0: UART_CTS	
		I2C_SDA	B		QUP 0 SE0, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP 0 SE0, lane 0: SPI_MISO	
		I3C_SDA	B		QUP 0 SE0, lane 0: I3C_SDA	
AM46	GPIO_1		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP 0 SE0, lane 1: UART_RFR	
		I2C_SCL	DO		QUP 0 SE0, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP 0 SE0, lane 1: SPI_MOSI	
		I3C_SCL	DO		QUP 0 SE0, lane 1: I3C_SCL	
AN47	GPIO_2		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP 0 SE0, lane 2: UART_TX	
		SPI_SCLK	DO		QUP 0 SE0, lane 2: SPI_SCLK	
AP46	GPIO_3		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE0, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE0, lane 3: SPI_CS_0	
AM42	GPIO_4		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE1, lane 0 UART_CTS	
		I2C_SDA	B		QUP0 SE1, lane 0 I2C_SDA	
		SPI_MISO	DI		QUP0 SE1, lane 0 SPI_MISO	
		I3C_SDA	B		QUP 0 SE1, lane 0: I3C_SDA	
AN41	GPIO_5		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP0 SE1, lane 1:UART_RFR	
		I2C_SCL	B		QUP0 SE1, lane 1: I2C_SCL	
		SPI_MOSI	DI		QUP0 SE1, lane 1: SPI_MOSI	
		I3C_SCL	B		QUP 0 SE1, lane 1: I3C_SCL	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AP42	GPIO_6		PD:nppukp	PX_3	Configurable I/O	N
		SPI_CS_1	DO		QUP0 SE0, lane 4 : SPI_CS_1	
		UART_TX	DO		QUP0 SE1, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE1, lane 2: SPI_SCLK	
		DP0_HOT_PLUG_DETECT	DI		DisplayPort 0 hot plug detect	
AR41	GPIO_7		PD:nppukp	PX_3	Configurable I/O	Y
		SPI_CS_2	DO		QUP0 SE0, lane 5 : SPI_CS_2	
		UART_RX	DI		QUP0 SE1, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE1, lane 3: SPI_CS_0	
AL45	GPIO_8		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE2, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE2, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP0 SE2, lane 0: SPI_MISO	
AL43	GPIO_9		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP0 SE2, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE2, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP0 SE2, lane 1: SPI_MOSI	
AM44	GPIO_10		PD:nppukp	PX_3	Configurable I/O	Y
		UART_TX	DO		QUP0 SE2, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE2, lane 2: SPI_SCLK	
AN43	GPIO_11		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE2, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE2, lane 3: SPI_CS_0	
AN45	GPIO_12		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE3, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE3, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP0 SE3, lane 0: SPI_MISO	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AP44	GPIO_13		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP0 SE3, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE3, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP0 SE3, lane 1: SPI_MOSI	
AR45	GPIO_14		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP0 SE3, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE3, lane 2: SPI_SCLK	
AR43	GPIO_15		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE3, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE3, lane 3: SPI_CS_0	
		GCC_GP3_CLK_MIRA	DO		General purpose clock 3 A	
AT42	GPIO_16		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE4, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE4, lane 0: I2C_SDA	
		SPI_MISO	DO		QUP0 SE4, lane 0: SPI_MISO	
		GCC_GP1_CLK_MIRA			General purpose clock 1 A	
AT44	GPIO_17		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP0 SE4, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE4, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP0 SE4, lane 1: SPI_MOSI	
		GCC_GP2_CLK_MIRA	DO		General purpose clock 2 A	
AT46	GPIO_18		PD:nppukp	PX_3	Configurable I/O	Y
		UART_TX	DO		QUP0 SE4, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE4, lane 2: SPI_SCLK	
		BOOT_CONFIG[7]	DI		Boot configuration control bit 7	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AU47	GPIO_19		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE4, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE4, lane 3: SPI_CS_0	
		GP_PDM_MIRA[0]	DO		General purpose PDM output 0 A	
AU41	GPIO_20		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE5, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE5, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP0 SE5, lane 0: SPI_MISO	
		CCI_TIMER0	DO		Camera control interface timer 0	
		GP_PDM_MIRA[1]	DO		General purpose PDM output 1 A	
AU45	GPIO_21		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RFR	DO		QUP0 SE5, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE5, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP 0 SE5, lane 1: SPI_MOSI	
		CCI_TIMER1	DO		Camera control interface timer 1	
		GP_PDM_MIRA[2]	DO		General purpose PDM output 2 A	
AU43	GPIO_22		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP0 SE5, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE5, lane 2: SPI_SCLK	
AV42	GPIO_23		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE5, lane 3: UART_RX	
		SPI_CS_0	DO		QUP0 SE5, lane 3: SPI_CS_0	
AV44	GPIO_24		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE6, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE6, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP0 SE6, lane 0: SPI_MISO	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AV46	GPIO_25		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RFR	DO		QUP0 SE6, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE6, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP0 SE6, lane 1: SPI_MOSI	
AW41	GPIO_26		PD:nppukp	PX_3	Configurable I/O	Y
		UART_TX	DO		QUP0 SE6, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE6, lane 2: SPI_SCLK	
		SPI_CS	DO		QUP0 SE4, lane 4: SPI_CS_1	
AW43	GPIO_27		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE6, lane 3: UART_RX	
		SPI_CS	DO		QUP0 SE6, lane 3: SPI_CS_0	
		SPI_CS	DO		QUP0 SE4, lane 5: SPI_CS_2	
AW45	GPIO_28		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP0 SE7, lane 0: UART_CTS	
		I2C_SDA	B		QUP0 SE7, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP0 SE7, lane 0: SPI_MISO	
AY44	GPIO_29		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP0 SE7, lane 1: UART_RFR	
		I2C_SCL	DO		QUP0 SE7, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP0 SE7, lane 1: SPI_MOSI	
BA43	GPIO_30		PU:nppdkp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP0 SE7, lane 2: UART_TX	
		SPI_SCLK	DO		QUP0 SE7, lane 2: SPI_SCLK	
AY42	GPIO_31		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP0 SE7, lane 3: UART_RX	
		SPI_CS	DO		QUP0 SE7, lane 3: SPI_CS_0	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BP10	GPIO_32		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE0, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE0, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE0, lane 0: I3C_SDA	
		I3C_SDA	B		QUP1 SE0, lane 0: SPI_MISO	
BR9	GPIO_33		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP1 SE0, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE0, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE0, lane 1: SPI_MOSI	
		I3C_SCL	DO		QUP1 SE0, lane 1: I3C_SCL	
BP12	GPIO_34		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP1 SE0, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE0, lane 2: SPI_SCLK	
BR11	GPIO_35		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE0, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE0, lane 3: SPI_CS_0	
BP4	GPIO_36		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE1, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE1, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE1, lane 0: SPI_MISO	
		I3C_SDA	B		QUP1 SE1, lane 0: I3C_SDA	
BP8	GPIO_37		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP1 SE1, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE1, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE1, lane 1: SPI_MOSI	
		I3C_SCL	DO		QUP 1SE1, lane 1: I3C_SCL	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BR7	GPIO_38		PU:nppukp	PX_3	Configurable I/O	Y
		UART_TX	DO		QUP1 SE1, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE1, lane 2: SPI_SCLK	
		SPI_CS_1	DO		QUP1 SE2, lane 4: SPI_CS 1	
		QDSS_CTI_TRIG0_IN_MIRA	DO		QDSS trigger input 0 A	
BR5	GPIO_39		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE1, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE1, lane 3: SPI_CS 0	
		SPI_CS_2	DO		QUP1 SE2, lane 5: SPI_CS 2	
		QDSS_CTI_TRIG1_IN_MIRA	DO		QDSS trigger input 1 A	
BP2	GPIO_40		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE2, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE2, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE2, lane 0: SPI_MISO	
		GCC_GP1_CLK_MIRB	DO		Global general purpose clock 1 B	
BR3	GPIO_41		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RFR	DO		QUP1 SE2, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE2, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE2, lane 1: SPI_MOSI	
		GCC_GP2_CLK_MIRB	DO		General purpose clock 2 B	
BP6	GPIO_42		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP1 SE2, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE2, lane 2: SPI_SCLK	
		GCC_GP3_CLK_MIRB	DO		General purpose clock 3 B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BN5	GPIO_43		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE2, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE2, lane 3: SPI_CS_0	
		GP_PDM_MIRB[0]	DO		General purpose PDM output 0 B	
BN7	GPIO_44		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE3, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE3, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE3, lane 0: SPI_MISO	
		GP_PDM_MIRB[1]	DO		General purpose PDM output 1 B	
BM8	GPIO_45		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RFR	DO		QUP1 SE3, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE3, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE3, lane 1: SPI_MOSI	
		MDP_VSYNC_E	DI		MDP vertical sync – external	
BM6	GPIO_46		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP1 SE3, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE3, lane 2: SPI_SCLK	
		SD_WRITE_PROTECT	DI		Secure digital card write protection	
BL7	GPIO_47		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE3, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE3, lane 3: SPI_CS_0	
BN3	GPIO_48		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE4, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE4, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE4, lane 0: SPI_MISO	
		MDP_VSYNC_P_MIRB	DI		MDP vertical sync – primary B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BN1	GPIO_49		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP1 SE4, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE4, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE4, lane 1: SPI_MOSI	
		MDP_VSYNC_S_MIRB	DO		MDP vertical sync – secondary B	
BM2	GPIO_50		PD-nppukp	PX_3	Configurable I/O	Y
		UART_TX	DO		QUP1 SE4, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE4, lane 2: SPI_SCLK	
		BOOT_CONFIG[6]	DI		Boot configuration control bit 6	
BM4	GPIO_51		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE4, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE4, lane 3: SPI_CS_0	
BL1	GPIO_52		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE5, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE5, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE5, lane 0: SPI_MISO	
		QDSS_CTI_TRIG0_OUT_MIRA	DO		QDSS trigger output 0 A	
BL3	GPIO_53		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RFR	DO		QUP1 SE5, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE5, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE5, lane 1: SPI_MOSI	
		QDSS_CTI_TRIG1_OUT_MIRA	DO		QDSS trigger output 1 A	
BL5	GPIO_54		PD:nppukp	PX_3	Configurable I/O	Y
		SPI_CLK	DO		QUP1 SE5, lane 2: SPI_CLK	
		UART_TX	DO		QUP1 SE5, lane 2: UART_TX	
		BOOT_CONFIG[8]	DI		Boot configuration control bit 8	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BK6	GPIO_55		PD:nppukp	PX_3	Configurable I/O	Y
		SPI_CS_0	DO		QUP1 SE5, lane 3: SPI_CS_0	
		UART_RX	DI		QUP1 SE5, lane 3: UART_RX	
BK4	GPIO_56		PD:nppukp	PX_3	Configurable I/O	Y
		UART_CTS	DI		QUP1 SE6, lane 0: UART_CTS	
		I2C_SDA	B		QUP1 SE6, lane 0: I2C_SDA	
		SPI_MISO	DI		QUP1 SE6, lane 0: SPI_MISO	
BK2	GPIO_57		PD:nppukp	PX_3	Configurable I/O	N
		UART_RFR	DO		QUP1 SE6, lane 1: UART_RFR	
		I2C_SCL	DO		QUP1 SE6, lane 1: I2C_SCL	
		SPI_MOSI	DO		QUP1 SE6, lane 1: SPI_MOSI	
BJ1	GPIO_58		PD:nppukp	PX_3	Configurable I/O	N
		UART_TX	DO		QUP1 SE6, lane 2: UART_TX	
		SPI_SCLK	DO		QUP1 SE6, lane 2: SPI_SCLK	
BJ3	GPIO_59		PD:nppukp	PX_3	Configurable I/O	Y
		UART_RX	DI		QUP1 SE6, lane 3: UART_RX	
		SPI_CS_0	DO		QUP1 SE6, lane 3: SPI_CS_0	
Y4	GPIO_60		PD:nppukp	PX_3	Configurable I/O	N
		MI2S2_SCK	B		MI²S 2 clock	
AC1	GPIO_61		PD:nppukp	PX_3		Y
		MI2S2_DATA0	B		MI²S 2 serial data channel 0	
		QDSS_GPIO_TRACEDATA_LOCB[15]	DO		QDSS trace data bit 15 B	
W5	GPIO_62		PD:nppukp	PX_3	Configurable I/O	N
		MI2S2_WS	B		MI²S 2 serial data word select	
AB2	GPIO_63		PD:nppukp	PX_3	Configurable I/O	Y
		MI2S2_DATA1	B		MI²S 2 serial data channel 1	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BF2	GPIO_64		PD:nppukp	PX_3	Configurable I/O	N
		CAM_MCLK0	DO		Camera master clock 0	
		QDSS_GPIO_TRACEDATA_LOCA(0)	DO		QDSS trace data bit 0 A	
BC1	GPIO_65		PD:nppukp	PX_3	Configurable I/O	N
		CAM_MCLK1	DO		Camera master clock 1	
		QDSS_GPIO_TRACEDATA_LOCA(1)	DO		QDSS trace data bit 1 A	
BE1	GPIO_66		PD:nppukp	PX_3	Configurable I/O	N
		CAM_MCLK2	DO		Camera master clock 2	
		QDSS_GPIO_TRACEDATA_LOCA(2)	DO		QDSS trace data bit 2 A	
BB2	GPIO_67		PD:nppukp	PX_3	Configurable I/O	N
		CAM_MCLK3	DO		Camera master clock 3	
		QDSS_GPIO_TRACEDATA_LOCA(3)	DO		QDSS trace data bit 3 A	
AR1	GPIO_68		PD:nppukp	PX_3	Configurable I/O	N
		CAM_MCLK4	DO		Camera master clock 4	
		QDSS_GPIO_TRACEDATA_LOCA(4)	DO		QDSS trace data bit 4 A	
BA1	GPIO_69		PD:nppukp	PX_3	Configurable I/O	Y
		CAM_MCLK5	DO		Camera master clock 5	
		QDSS_GPIO_TRACEDATA_LOCA(5)	DO		QDSS trace data bit 5 A	
BJ5	GPIO_70		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SDA0	B		Dedicated Camera control interface I²C 0	
		QDSS_GPIO_TRACEDATA_LOCA(6)	DO		Serial Data QDSS trace data bit 6 A	
BJ7	GPIO_71		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SCL0	DO		Dedicated camera control interface 0 I²C	
		QDSS_GPIO_TRACEDATA_LOCA(7)	DO		Serial clock QDSS trace data bit 7 A	
BH6	GPIO_72		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SDA1	B		Dedicated camera control interface I²C	
		QDSS_GPIO_TRACECLK_LOCA	DO		Serial data QDSS trace clock A	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BH4	GPIO_73		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SCL1	B		Dedicated camera control interface I²C 1	
		QDSS_GPIO_TRACECTL_LOCA	DO		Serial clock QDSS trace control A	
BH2	GPIO_74		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SDA2	B		Dedicated camera control interface I²C 2	
		QDSS_GPIO_TRACEDATA_LOCA(8)	DO		Serial data QDSS trace data bit 8 A	
BG1	GPIO_75		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SCL2	DO		Dedicated camera control interface I²C 2	
		QDSS_GPIO_TRACEDATA_LOCA(9)	DO		Serial clock QDSS trace data bit 9 A	
BG3	GPIO_76		PD:nppukp	PX_3	Configurable I/O	N
		CCI_I2C_SDA3	B		Dedicated camera control interface I²C 3	
		QDSS_GPIO_TRACEDATA_LOCA(10)	DO		Serial data QDSS trace data bit 10 A	
BG5	GPIO_77		PD:nppukp	PX_3	Configurable I/O	Y
		CCI_I2C_SCL3	DO		Dedicated camera control interface I²C 3	
		QDSS_GPIO_TRACEDATA_LOCA(11)	DO		Serial clock QDSS trace data bit 11 A	
BG7	GPIO_78		PD:nppukp DO	PX_3	Configurable I/O	N
		CCI_TIMER2	DO		Camera control interface timer 2	
		QDSS_GPIO_TRACEDATA_LOCA(12)	DO		QDSS trace data bit 12 A	
BF6	GPIO_79		PD:nppukp	PX_3	Configurable I/O	N
		CCI_TIMER3	DO		Camera control interface timer 3	
		CCI_ASYNC_IN2	DI		Camera control interface async 2	
		QDSS_GPIO_TRACEDATA_LOCA(13)	DO		QDSS trace data bit 13 A	
BE7	GPIO_80		PD:nppukp	PX_3	Configurable I/O	N
		CCI_TIMER4	DO		Camera control interface timer 4	
		CCI_ASYNC_IN1	DI		Camera control interface async 1	
		QDSS_GPIO_TRACEDATA_LOCA(14)	DO		QDSS trace data bit 14 A	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BF4	GPIO_81		PD:nppukp	PX_3	Configurable I/O	Y
		CCI_ASYNC_IN0	DI		Camera control interface async 0	
		MDP_VSYNC_S_MIRA	DI		MDP vertical sync – secondary	
		MDP_VSYNC2_OUT	DO		MDP vertical sync 2 output	
BF42	GPIO_82		PD:nppukp	PX_3	Configurable I/O	Y
		MDP_VSYNC_P_MIRA	DI		MDP vertical sync – primary	
BF44	GPIO_83		PD:nppukp	PX_3	Configurable I/O	Y
AW47	GPIO_84		PD:nppukp	PX_5	Configurable I/O	N
		UIM0_DATA	B		UIM0 data (dual voltage)	
AY46	GPIO_85		PD:nppukp	PX_5	Configurable I/O	N
		UIM0_CLK	DO		UIM0 clock (dual voltage)	
BA47	GPIO_86		PD:nppukp	PX_5	Configurable I/O	N
		UIM0_RESET	DO		UIM0_RESET	
BB46	GPIO_87		PD:nppukp	PX_3	Configurable I/O	Y
		UIM0_PRESENT	DI		UIM0 presence detection	
BC47	GPIO_88		PD:nppukp	PX_6	Configurable I/O	N
		UIM1_DATA	B		UIM1 data (dual voltage)	
BD46	GPIO_89		PD:nppukp	PX_6	Configurable I/O	N
		UIM1_CLK	DO		UIM1 clock (dual voltage)	
BE47	GPIO_90		PD:nppukp	PX_6	Configurable I/O	N
		UIM1_RESET	DO		UIM1_RESET	
BF46	GPIO_91		PD:nppukp	PX_3	Configurable I/O	Y
		UIM1_PRESENT	DI		UIM1 presence detection	
BE45	GPIO_92		PD:nppukp	PX_3	Configurable I/O	Y
		QLINK0_REQUEST	DI		QLink0 request	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BR13	GPIO_93		PD:nppukp	PX_3	Configurable I/O	N
		QLINK0_ENABLE	DO		QLink0 enable	
BE43	GPIO_94		PD:nppukp	PX_3	Configurable I/O	N
		QLINK0_WMSS_RESET_N	DO		QLINK0 reset output	
BE41	GPIO_95		PD:nppukp	PX_3	Configurable I/O	Y
		QLINK1_REQUEST	DI		QLink1 request	
BR21	GPIO_96		PD:nppukp	PX_3	Configurable I/O	N
		QLINK1_ENABLE	DO		QLink1 enable	
BG41	GPIO_97		PD:nppukp	PX_3	Configurable I/O	N
		QLINK1_WMSS_RESET_N	DO		QLink1 reset output	
		BOOT_CONFIG[5]	DI		Boot configuration control bit 5	
BF40	GPIO_98		PD:nppukp	PX_3	Configurable I/O	Y
		QLINK2_REQUEST	DI		QLink2 request	
BP20	GPIO_99		PD:nppukp	PX_3	Configurable I/O	N
		QLINK2_ENABLE	DO		QLink2 enable	
BH42	GPIO_100		PD:nppukp	PX_3	Configurable I/O	N
		QLINK2_WMSS_RESET_N	DO		QLink2 reset output	
		BOOT_CONFIG[10]	DI		Boot configuration control bit 10	
AA47	GPIO_101		PD:nppukp	PX_3	Configurable I/O	N
		RFFE0_CLK	DO		RF front end interface clock	
		GRFC0	DO		Generic RF controller bit 0	
AB46	GPIO_102		PD:nppukp	PX_3	Configurable I/O	N
		RFFE0_DATA	B		RF front end 0 interface data	
		GRFC1	DO		Generic RF controller bit 1	
		BOOT_CONFIG[0]	DI		Boot configuration control bit 0	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AC47	GPIO_103		PD:nppukp	PX_3	Configurable I/O	N
		RFFE1_CLK	DO		RF front end 1 interface clock	
		GRFC2	DO		Generic RF controller bit 2	
AD46	GPIO_104		PD:nppukp	PX_3	Configurable I/O	N
		RFFE1_DATA	B		RF front end 1 interface data	
		GRFC3	DO		Generic RF controller bit 3	
		BOOT_CONFIG[1]	DI		Boot configuration control bit 1	
AL41	GPIO_105		PD:nppukp	PX_3	Configurable I/O	N
		RFFE2_CLK	DO		RF front end 1 interface clock	
		GRFC4	DO		Generic RF controller bit 4	
AF46	GPIO_106		PD:nppukp	PX_3	Configurable I/O	N
		RFFE2_DATA	B		RF front end 1 interface data	
		GRFC5	DO		Generic RF controller bit 3	
		BOOT_CONFIG[2]	DI		Boot configuration control bit 2	
AG47	GPIO_107		PD:nppukp	PX_3	Configurable I/O	N
		RFFE3_CLK	DO		RF front end 3 interface clock	
		GRFC6	DO		Generic RF controller bit 6	
AH46	GPIO_108		PD:nppukp	PX_3	Configurable I/O	N
		RFFE3_DATA	B		RF front end 3 interface data	
		GRFC7	DO		Generic RF controller bit 7	
		BOOT_CONFIG[3]	DI		Boot configuration control bit 3	
AJ47	GPIO_109		PD:nppukp	PX_3	Configurable I/O	N
		RFFE4_CLK	DO		RF front end 4 interface clock	
		GRFC8	DO		Generic RF controller bit 8	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AK46	GPIO_110		PD:nppukp	PX_3	Configurable I/O	N
		RFFE4_DATA	B		RF front end 4 interface data	
		GRFC9	DO		Generic RF controller bit 9	
		BOOT_CONFIG[4]	DI		Boot configuration control bit 4	
BA45	GPIO_111		PD:nppukp	PX_3	Configurable I/O	N
		WLAN_COEX_UART1_TX	DO		Interface between WCN and SM7450	
		GRFC10	DO		Generic RF controller bit 10	
		BOOT_CONFIG[9]	DI		Boot configuration control bit 9	
BB44	GPIO_112		PD:nppukp	PX_3	Configurable I/O	N
		WLAN_COEX_UART1_RX	DI		Interface between WCN and SM7450	
		GRFC11	DO		Generic RF controller bit 11	
BA41	GPIO_113		PD:nppukp	PX_3	Configurable I/O	Y
		NAV_GPIO_0	B		Generic input/output 0 for GNSS	
BB42	GPIO_114		PD:nppukp	PX_3	Configurable I/O	Y
		NAV_GPIO_1	B		Generic input/output 1 for GNSS	
BC41	GPIO_115		PD:nppukp	PX_3	Configurable I/O	Y
		GRFC12	DO		Generic RF controller bit 12	
		NAV_GPIO_2	B		Generic input/output 2 for GNSS	
BC43	GPIO_116		PD:nppukp	PX_3	Configurable I/O	N
		GRFC0_MIRA	DO		Generic RF controller bit 0 A	
		BOOT_CONFIG[11]	DI		Boot configuration control bit 11	
BC45	GPIO_117		PD:nppukp	PX_3	Configurable I/O	N
		PCIE0_RESET_N	DO		PCIe 0 reset	
BD42	GPIO_118		PU:nppdkp	PX_3	Configurable I/O	Y
		PCIE0_CLK_REQ_N	DI		PCIe 0 clock request	
BD44	GPIO_119		PD:nppukp	PX_3	Configurable I/O	Y
		PCIE0_WAKE_N	DO		PCIe 0 wake up	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BG43	GPIO_120	FORCED_USB_BOOT_POLARITY	PD:nppukp DI	PX_3	Configurable I/O Forced USB boot parity select	N
BG47	GPIO_121	FORCED_USB_BOOT	PD:nppukp DI	PX_3	Configurable I/O Forced USB boot	Y
BH44	GPIO_122	USB0_PHY_PS	PD:nppukp DI	PX_3	Configurable I/O USB0 PHY port select	Y
BH46	GPIO_123	USB0_HS_AC_EN	PD:nppukp DO	PX_3	Configurable I/O USB0 HS AC coupling 0 control	Y
BG45	GPIO_124	HOST2WLAN_SOL	PD:nppukp DO		Configurable I/O WLAN control	N
W7	GPIO_125	MI2S_MCLK 1 AUDIO_REF_CLK	PD:nppukp DO DI	PX_3	Configurable I/O MI²S master clock 1 Audio reference clock	Y
AA3	GPIO_126	MI2S_MCLK 0	PD:nppukp DO	PX_3	Configurable I/O MI²S master clock 0	N
AA1	GPIO_127	MI2S0_SCK QDSS_CTI_TRIG0_IN_MIRB	PD:nppukp DO DI	PX_3	Configurable I/O MI²S 0 clock QDSS trigger input 0 B	Y
Y2	GPIO_128	MI2S0_DATA0 QDSS_CTI_TRIG1_IN_MIRB	PD:nppukp B DI	PX_3	Configurable I/O MI²S 0 serial data channel 0 QDSS trigger input 1 B	Y
W3	GPIO_129	MI2S0_DATA1 QDSS_CTI_TRIG1_OUT_MIRB	PD:nppukp B DO	PX_3	Configurable I/O MI²S 0 serial data channel 1 QDSS trigger output 1 B	N
V4	GPIO_130	MI2S0_WS QDSS_CTI_TRIG0_OUT_MIRB	PD:nppukp B DO	PX_3	Configurable I/O MI²S 0 serial data word select QDSS trigger output 0 B	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
N1	GPIO_131		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_0	B		LPI GPIO 0	
		SWR_TX_CLK	DO		SoundWire transmit clock	
		LPI_QUA_MI2S_SCK	B		LPI quaternary MI²S clock 0	
N3	GPIO_132		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_1	B		LPI GPIO 1	
		SWR_TX_DATA0	DO		SoundWire transmit data 0	
		LPI_QUA_MI2S_WS	B		LPI quaternary MI²S word select	
U3	GPIO_133		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_2	B		LPI GPIO 2	
		SWR_TX_DATA1	DO		SoundWire transmit data 1	
		LPI_QUA_MI2S_DATA0	B		LPI quaternary MI²S data 0	
U1	GPIO_134		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_3	B		LPI GPIO 3	
		SWR_RX_CLK	DI		SoundWire receive clock	
		LPI_QUA_MI2S_DATA1	B		LPI quaternary MI²S data 1	
T2	GPIO_135		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_4	B		LPI GPIO 4	
		SWR_RX_DATA0	DI		SoundWire receive data 0	
		LPI_QUA_MI2S_DATA2	B		LPI quaternary MI²S data 2	
U5	GPIO_136		PD:nppuk	PX_3	Configurable I/O	N
		LPI_GPIO_5	B		LPI GPIO 5	
		SWR_RX_DATA1	DI		SoundWire receive data 1	
		EXT_MCLK1_C	DO		External master clock 1 C	
		LPI_QUA_MI2S_DATA3	B		LPI quaternary MI²S data 3	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
V6	GPIO_137		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[0]	DO		QDSS trace data bit 0 A	
		LPI_GPIO_6	B		LPI GPIO 6	
		LPI_DMIC1_CLK	DO		LPI DMIC 1	
		LPI_I2S1_CLK	B		Clock LPI I2S 1 clock	
T4	GPIO_138		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[1]	DO		QDSS trace data bit 1 A	
		LPI_GPIO_7	B		LPI GPIO 7	
		LPI_DMIC1_DATA	DI		LPI DMIC 1	
		LPI_I2S1_WS	B		Data LPI I2S 1 word select	
R5	GPIO_139		PD:nppukp	PX_3	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCA[2]	DO		QDSS trace data bit 2 A	
		LPI_GPIO_8	B		LPI GPIO 8	
		LPI_DMIC2_CLK	DO		LPI DMIC 2 clock	
		LPI_I2S1_DATA0	B		LPI I2S 1 Data 0	
N7	GPIO_140		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[3]	DO		QDSS trace data bit 3 B	
		LPI_GPIO_9	B		LPI GPIO 9	
		LPI_DMIC2_DATA	DI		LPI DMIC 2 data	
		LPI_I2S1_DATA1	B		LPI I2S 1 Data 1	
		EXT_MCLK1_B	DO		External master clock 1 B	
R1	GPIO_141		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_10	B		LPI GPIO 10	
		LPI_I2S2_CLK	B		LPI MI²S 2 clock	
		WSA_SWR_CLK	DO		SoundWire clock for WSA	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
R3	GPIO_142		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_11	B		LPI GPIO 11	
		LPI_I2S2_WS	B		LPI I2S 2 Word select	
		WSA_SWR_DATA	B		SoundWire data for WSA	
P4	GPIO_143		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[4]	DO		QDSS trace data bit 4 B	
		LPI_GPIO_12	B		LPI_GPIO 12	
		LPI_DMIC3_CLK	DO		LPI_DMIC 3 clock	
N5	GPIO_144		PD:nppukp	PX_3	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCB[5]	DO		QDSS trace data bit 5 B	
		LPI_GPIO_13	B		LPI GPIO 13	
		LPI_DMIC3_DATA	DI		LPI DMIC 3 data	
		EXT_MCLK1_A	DO		External master clock 1 A	
P2	GPIO_145		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_3	B		LPI GPIO 3	
		SWR_TX_DATA2	DO		SoundWire transmitt data 2	
		EXT_MCLK1_D	DO		External master clock 1 D	
M6	GPIO_146		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_4	B		LPI GPIO 4	
		WSA2_SWR_CLK	DO		SoundWire clock for WSA 2	
		LPI_I2S2_DATA0	B		LPI I2S 2 Data 0	
L5	GPIO_147		PD:nppuk	PX_3	Configurable I/O	Y
		LPI_GPIO_5	B		LPI GPIO 5	
		LPI_I2S2_DATA1	B		LPI I2S 2 data 1	
		WSA2_SWR_DATA	B		SoundWire data for WSA 2	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
L7	GPIO_148		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[6]	DO		QDSS trace data bit 6 A	
		LPI_GPIO_17	B		LPI GPIO 17	
		LPI_DMIC4_CLK	DO		LPI DMIC 4 Clock	
K6	GPIO_149		PD:nppukp	PX_3	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[7]	DO		QDSS trace data bit 7 A	
		LPI_GPIO_18	B		LPI GPIO 18	
		LPI_DMIC4_DATA	DI		LPI DMIC 4 data	
W1	GPIO_150		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_19	B		LPI GPIO 19	
		LPI_I2S3_CLK	B		LPI I2S 3 clock	
		SLIMBUS_CLK	B		Low-power audio SLIMbus clock	
V2	GPIO_151		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_20	B		LPI GPIO 20	
		LPI_I2S3_WS	B		LPI I2S 3 word select	
		SLIMBUS_DATA	B		Low-power audio SLIMbus data	
J7	GPIO_152		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_21	B		LPI GPIO 21	
		QDSS_GPIO_TRACECTL_LOCB	DO		QDSS trace control B	
		LPI_I2S3_DATA0	B		LPI I2S 3 data 0	
J5	GPIO_153		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_22	B		LPI GPIO 22	
		QDSS_GPIO_TRACECLK_LOCB	DO		QDSS trace clock B	
		LPI_I2S3_DATA1	B		LPI I2S 3 data 1	
		EXT_MCLK1_E	DO		External master clock 1 E	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
M2	GPIO_154		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_23	B		LPI GPIO 23	
		LPI_I2C0_SDA	B		LPI_QUP SE0, lane 0: I2C_SDA 0	
		LPI_I3C0_SDA	B		LPI_QUP SE0, lane 0: I3C_SDA 0	
		SYNC_OUT_GPIO_0	DO		Sync out GPIO 0	
M4	GPIO_155		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_24	B		LPI GPIO 24	
		LPI_I2C0_SCL	DO		LPI_QUP SE0, lane 1: I2C_SCL 0	
		LPI_I3C0_SCL	DO		LPI_QUP SE0, lane 1: I3C_SCL 0	
		SYNC_OUT_GPIO_1	DO		Sync out GPIO 1	
L1	GPIO_156		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_25	B		LPI GPIO 25	
		LPI_I2C1_SDA	B		LPI_QUP SE1, lane 0: I2C_SDA 1	
		LPI_I3C1_SDA	B		LPI_QUP SE1, lane 0: I3C_SDA1	
		SYNC_OUT_GPIO_2	DO		Sync out GPIO 2	
L3	GPIO_157		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_26	B		LPI GPIO 26	
		LPI_I2C1_SCL	DO		LPI_QUP0 SE1, lane 1: I2C_SCL1	
		LPI_I3C1_SCL	DO		LPI_QUP0 SE1, lane 1: I3C_SCL 1	
		SYNC_OUT_GPIO_3	DO		Sync out GPIO 3	
K4	GPIO_158		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_27	B		LPI GPIO 27	
		SPI_MISO	DI		LPI_QUP SE2, lane 0 : SPI_MISO	
		LPI_I2C2_SDA	B		LPI_QUP SE2, lane 0: I2C_SDA 2	
		LPI_I3C2_SDA	B		LPI_QUP SE2, lane 0: I3C_SDA 2	
		SYNC_OUT_GPIO_4	DO		Sync out GPIO 4	
K2	GPIO_159		PD:nppukp	PX_3	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_GPIO_28	B		LPI GPIO 28	
		SPI_MOSI	DO		LPI_QUP SE2, lane 1: SPI_MOSI	
		LPI_I2C2_SCL	DO		LPI_QUP SE2, lane 1: I2C_SCL 2	
		LPI_I3C2_SCL	DO		LPI_QUP SE2, lane 1: I3C_SCL 2	
		SYNC_OUT_GPIO_5	DO		Sync out GPIO 5	
H6	GPIO_160		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_29	B		LPI GPIO 29 QDSS trace data bit 8 B	
		QDSS_GPIO_TRACEDATA_LOCB[8]	DO		LPI_QUP SE2, lane 2: SPI_CLK	
		SPI_CLK SPI_CLK	DO		LPI_QUP SE4, lane 2: SPI_CLK	
		SYNC_OUT_GPIO_6	DO		Sync out GPIO 6	
H4	GPIO_161		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_30	B		LPI GPIO 30 QDSS trace data bit 9 B	
		QDSS_GPIO_TRACEDATA_LOCB[9]	DO		LPI_QUP SE2, lane 3: SPI_CS	
		SPI_CS	DO		LPI_QUP SE4, lane 3: SPI_CS	
		SYNC_OUT_GPIO_7	DO		Sync out GPIO 7	
J3	GPIO_162		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_31	B		LPI GPIO 31	
		QDSS_GPIO_TRACEDATA_LOCB[10]	DO		QDSS trace data bit 10 B	
		I2C_SDA	B		LPI_QUP SE3, lane 0 : I2C_SDA 3	
		SPI_MISO	DI		LPI_QUP SE3, lane 0 : SPI_MISO	
		UART_CTS	DO		LPI_QUP SE6, lane 0 : UART_CTS	
		SYNC_OUT_GPIO_8	DO		Sync out GPIO 8	
J1	GPIO_163		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_32	B		LPI GPIO 32	
		QDSS_GPIO_TRACEDATA_LOCB[11]	DO		QDSS trace data bit 11 B	
		I2C_SCL	DO		LPI_QUP SE3, lane 1: I2C_SCL 3	
		SPI_MOSI	DO		LPI_QUP SE3, lane 1 : SPI_MOSI	
		UART_RTS	DO		LPI_QUP SE6, lane 1 : UART_RTS	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		SYNC_OUT_GPIO_9	DO		Sync out GPIO 9	
H2	GPIO_164		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_33	B		LPI GPIO 33	
		SPI_CLK	DO		LPI_QUP SE3, lane 2: SPI_CLK	
		I2C_SDA	B		LPI_QUP SE4, lane 0: I2C_SDA 4	
		SPI_MISO	DI		LPI_QUP SE4, lane 0 : SPI_MISO	
		SYNC_OUT_GPIO_10	DO		Sync out GPIO 10	
G5	GPIO_165		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_34	B		LPI GPIO 34	
		QDSS_GPIO_TRACEDATA_LOCB[12]	DO		QDSS trace data bit 12 B	
		SPI_CS	DO		LPI_QUP SE3, lane 3: SPI_CS 0	
		I2C_SCL	DO		LPI_QUP SE4, lane 1: I2C_SCL 4	
		SPI_MOSI	DO		LPI_QUP SE4, lane 1: SPI_MOSI	
		SYNC_OUT_GPIO_11	DO		Sync out GPIO 11	
G3	GPIO_166		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_35	B		LPI GPIO 35	
		UART_TX	DO		LPI_QUP SE5, lane 2: UART_TX	
		I2C_SDA	B		LPI_QUP SE5, lane 0: I2C_SDA	
		SYNC_OUT_GPIO_12	DO		Sync out GPIO 12	
G1	GPIO_167		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_36	B		LPI GPIO 36	
		UART_RX	DI		LPI_QUP SE5, lane 3: UART_RX	
		I2C_SCL	DO		LPI_QUP SE5, lane 1: I2C_SCL	
		QDSS_GPIO_TRACEDATA_LOCB[13]	DO		QDSS trace data bit 13 B	
		SYNC_OUT_GPIO_13	DO		Sync out GPIO 13	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
G7	GPIO_168		PD:nppukp	PX_3	Configurable I/O	N
		LPI_GPIO_37	B		LPI GPIO 37	
		UART_TX	DO		LPI_QUP SE6, lane 2: UART_TX	
		SYNC_OUT_GPIO_14	DO		Sync out GPIO 14	
F4	GPIO_169		PD:nppukp	PX_3	Configurable I/O	Y
		LPI_GPIO_38	B		LPI GPIO 38	
		QDSS_GPIO_TRACEDATA_LOCB[14]	DO		QDSS trace data bit 14 B	
		UART_RX	DI		LPI_QUP SE6, lane 3: UART_RX	
		SYNC_OUT_GPIO_15	DO		Sync out GPIO 15	

[a] See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad number	Pad name	Functional description
C1, J33, K42, K44, N29, P30, AA17, AB16, AC27, AD28, AE11, AE13, AF38, AG37, AN23, AP24, AP40, BC11, BD12, BR17	DNC	Do not connect; connected internally, do not connect externally.
A1, A25, A47, AA23, AA27, AA9, AB10, AB14, AB18, AB20, AB22, AB24, AB40, AB8, AC11, AC13, AC21, AC29, AC31, AC35, AC37, AC39, AC41, AC45, AC7, AD24, AD40, AD42, AD6, AE15, AE17, AE19, AE27, AE29, AE31, AE33, AE35, AE37, AE47, AE7, AE9, AF10, AF12, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF32, AF4, AF8, AG31, AG41, AG45, AG7, AG9, AH20, AH22, AH24, AH26, AH38, AH40, AH8, AJ11, AJ13, AJ15,AJ17, AJ19, AJ27, AJ29, AJ45, AJ5, AJ7, AK38, AK4, AK44, AK8, AL29, AL3, AM10, AM12, AM14, AM16, AM18, AM20, AM22, AM24, AM26, AM28, AM38, AM8, AN17, AN21, AN25, AN31, AN39, AN7, AP18, AP34, AP36, AP38, AP6, AP8, AR13, AR15, AR17, AR19, AR23, AR3, AR47, AR7, AR9, AT12, AT14, AT16, AT18, AT2, AT24, AT26, AT28, AT30, AT32, AT34, AT36, AT38, AT40, AT8, AU1, AU23, AU25, AU27, AU29, AU31, AU33, AU35, AU37, AU39, AU7, AV10, AV6, AW13, AW15, AW17, AW19, AW23, AW5, AW7, AY10, AY12, AY14, AY16, AY18, AY24, AY26, AY28, AY30, AY32, AY34, AY36, AY38, AY4, AY40, AY8, B10, B16, B18, B2, B20, B22, B28, B30, B32, B34, B4, B40, B42, B44, B46, B6, B8, BA23, BA25, BA27, BA29, BA3, BA31, BA33, BA35, BA37, BA39, BA9, BB10, BB20, BB24, BB40, BB8, BC13, BC15, BC17, BC19, BC23, BC31, BC33, BC7, BC9, BD10, BD14, BD16, BD18, BD24, BD26, BD28, BD30, BD34, BD36, BD38, BD40, BD6, BD8, BE5, BF10, BF26, BF30, BF32, BF34, BF36, BF38, BG11, BG13, BG15, BG17, BG23, BG25, BG27, BG29, BG31, BG33, BG35, BG37, BG9, BH12, BH14, BH16, BH18, BH20, BH24, BH26, BH28, BH30, BH32, BH34, BH36, BH38, BH40, BH8, BJ15, BJ19, BJ21, BJ23, BJ25, BJ27, BJ29, BJ31, BJ33, BJ35, BJ37, BJ39, BJ41, BJ43, BJ47, BK12, BK18, BK20, BK24, BK28, BK32, BK36, BK38, BK8, BL11, BL13, BL15, BL17, BL21, BL27, BL29, BL35, BL37, BL43, BL45, BL9, BM12, BM16, BM22, BM24, BM28, BM30, BM32, BM36, BM40, BM42, BN15, BN17, BN21, BN25, BN29, BN33, BN37, BN41, BN45, BN9, BP14, BP26, BP34, BP38, BP42, BP44, BR1, BR25, BR29, BR33, BR37, BR47, C11, C13, C15, C23, C25, C27, C35, C37, C39, D10, D14, D16, D18, D20, D24, D30, D32, D34, D36, D38, D40, D42, D44, D46, D6, D8, E13, E23, E27, E3, E35, F10, F16, F18, F20, F22, F24, F26, F28, F30, F32, F34, F40, F42, F44, F46, F6, F8, G11, G19, G23, G27, G31, G43, H12, H14, H16, H22, H26, H28, H34, H36, H38, H40, H46, H8, J11, J17, J21, J23, J27, J29, J39, J41, J43, J45, K10, K24, K26, L41, L43, M10, M12, M14, M16, M20, M22, M24, M26, M28, M32, M38, M40, M42, N23, N37, P36, P6, P8, R11, R13, R15, R17, R19, R21, R23, R27, R29, R31, R37, R7, R9, T10, T12, T14, T16, T18, T20, T22, T24, T32, T36, T40, T42, T44, U23, U27, U29, U31, U37, U47, V24, V40, V44, W11, W13, W15, W17, W19, W21, W23, W27, W31, W35, W41, W43, Y10, Y12, Y14, Y16, Y18, Y20, Y22, Y24, Y28, Y30, Y32, Y34, Y36, Y38, Y42, Y8	GND	Ground
W39	VDD_A_APC_CS_1P2	Power for application processor current sensor; 1.2 V circuits
AK10	VDD_A_CSI_0_1_0P9	Power for CSI 0, 1: 0.9 V circuits
AL9	VDD_A_CSI_0_1_1P2	Power for CSI 0, 1: 1.2 V circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
AP10	VDD_A_CSI_2_3_0P9	Power for CSI 2, 3: 0.9 V circuits
AN9	VDD_A_CSI_2_3_1P2	Power for CSI 2, 3: 1.2 V circuits
AT10	VDD_A_CSI_4_0P9	Power for CSI 4: 0.9 V circuits
AU9	VDD_A_CSI_4_1P2	Power for CSI 4: 1.2 V circuits
AL39	VDD_A_DSI_0_0P9	Power for the DSI0 0.9 V circuits
AK40	VDD_A_DSI_0_1P2	Power for the DSI0 1.2 V circuits
AJ39	VDD_A_DSI_0_PLL_0P9	Power for the DSI0 0.9 V PLL circuits
AF40	VDD_A_DSI_1_0P9	Power for the DSI1 0.9 V circuits
AE39	VDD_A_DSI_1_1P2	Power for the DSI1 1.2 V circuits
AG39	VDD_A_DSI_1_PLL_0P9	Power for the DSI1 0.9 V PLL circuits
BE19	VDD_A_PCIE_0_0P9	Power for the PCIe0 PLL
BF18	VDD_A_PCIE_0_PLL_1P2	Power for PCIe0 core circuits
J19	VDD_A_PLL_EBI_0	Power for EBI0 PLL circuits
J31	VDD_A_PLL_EBI_1	Power for EBI1 PLL circuits
BE23	VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits
BF24	VDD_A_QLINK_0_1P2	Power for the QLink0 1.2 V clock circuits
BE25	VDD_A_QLINK_0_CK_0P9	Power for the QLink0 0.9 V clock circuits
BE31	VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits
BE33	VDD_A_QLINK_1_1P2	Power for the QLink1 0.9 V clock circuits
BD32	VDD_A_QLINK_1_CK_0P9	Power for the QLink1 1.2 V clock circuits
BE27	VDD_A_QLINK_2_0P9	Power for the QLink2 0.9 V circuits
BF28	VDD_A_QLINK_2_1P2	Power for the QLink2 0.9 V clock circuits
BE29	VDD_A_QLINK_2_CK_0P9	Power for the QLink2 1.2 V clock circuits
BE11, BG19, AW9, W9, L9	VDD_A_QREFS_0P875	Reference voltage for the QREFS 0.875 V circuits
BF12, BF20, AV8, V8, K8	VDD_A_QREFS_1P2	Reference voltage for the QREFS 1.2V circuits
AC9	VDD_A_REFGEN_0_0P9	Voltage for the REFGEN 0.9 V circuits
AD8	VDD_A_REFGEN_0_1P2	Voltage for the REFGEN 1.2 V circuits
AD32	VDD_A_TURING_Q6_CS_1P2	Voltage for the TURING 1.2 V circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
L25	VDD_A_UFS_0_0P9	Power for the UFS 0.9V core circuits
L23	VDD_A_UFS_0_1P2	Power for the UFS 1.2 V circuits
BE15	VDD_A_USBHS_0P9	Power for the USB high speed 0.9 V circuits
BF14	VDD_A_USBHS_1P8	Power for the USB high speed1.8 V circuits
BE13	VDD_A_USBHS_3P1	Power for the USB high speed3.1 V circuits
BE17	VDD_A_USBSSDP_0_0P9	Power for the USB SS and DisplayPort 0P9V circuits
BF16	VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort 1.2 V circuits
AA25, AB26, AC25, AD26, AD34, AD38, AE23, AE25, AG11, AG13, AG15 , AG17, AG19, AG21, AG23, AG25, AG27, AG29, AG33, AG35, AH10, AH12 , AH14, AH16, AH18, AH28, AJ37, AK12, AK14, AK16, AK18, AK20, AK22 , AK24, AK26, AK28, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL37 , AN19, AN27, AN29, AN33, AN35, AN37, AU19, BA19, N21, P22, P24, P26 , P28, R25, T26, T28, T30, U25, V26, W25, Y26,	VDD_CX	Power for digital core circuits
M18	VDD_D_EBI_0	Power for EBI0 digital circuits
M30	VDD_D_EBI_1	Power for EBI1 digital circuits
AA11, AA13, AA15, AA19, AA21, N11, N13, N15, N17, N19, N9, P10 , P12, P14, P16, P18, P20, T6, T8, U11, U13, U15, U17, U19, U21, U7 , U9, V10, V12, V14, V16, V18, V20, V22	VDD_GFX	Power for graphics
J13, J15, K12, K14, K16, K18, K20, K22	VDD_IO_EBI_0	Power for EBI0 I/O circuits
J35, J37, K28, K30, K32, K34, K36,	VDD_IO_EBI_1	Power for EBI1 I/O circuits
AD10, AD12, AD14, AD16, AD18,	VDD_LPI_CX	Power for LPI digital core circuits
AD20, AD22, AE21, AF14,	VDD_LPI_MX	Power for LPI memory circuits
AN13, AN15, AP12, AP14, AP16, AU13, AU15, AU17, AV12, AV14, AV16 , AV18, BA13, BA15, BA17, BB12, BB14, BB16, BB18,	VDD_MM	Power for multimedia subsystem circuits
AP22, AR21, AR25, AR27, AR29, AR31, AR33, AR35, AR37, AR39, AT22 , AU21, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, AV38, AW21 , AW25, AW27, AW29, AW31, AW33, AW35, AW37, AY22, BA21, BB22, BB26 , BB28, BB30, BB32, BB34, BB36, BB38, BC21, BD22, BE21, BE35, BE37 , BE39, BF22, BG21, BH22	VDD_MODEM	Power for modem circuits
AC33, AD30, AD36, AJ21, AJ23, AJ25, BC29, BC35, K38, K40, L35 , N25, N27	VDD_MX	Power for on-chip memory
AB12, AC15, AC17, AC19, AC23, AF34, AF36, AL11, AL13, AN11, AP20 , AP26, AP28, AP30, AP32, AR11, AT20, AU11, AV20, AW11, AY20, BA11 , L11, L13,	VDD_MXC	
BD20	VDD_NAV_LPI_MX	Power for LPI on chip memory – NAV

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
AJ9	VDD_PX0	Power for pad group 0 – control signals
J9	VDD_PX10	Power for pad group 10 – UFS
BF8	VDD_PX11	Power for pad group 11 – CXO pad
J25	VDD_PX1_A	Power for pad group 1
U41	VDD_PX1_B	Power for pad group 1
Y40	VDD_PX2	Power for pad group 2 – SDC2 pads
AA41, BE9, BG39, M8,	VDD_PX3	Power for pad group 3 – most I/O pads
AV40	VDD_PX5	Power for pad group 5 – UIM1 pads
AW39	VDD_PX6	Power for pad group 6 – UIM2 pads
AM40	VDD_QFPROM	Power for programming the QFPROM
L37, L39, M34, M36, N31, N33, N35, P32, P34, R33, R35, T34, U33, U35	VDD_APC0	Power for the Kryo Silver application processor
AA29, AA31, AA33, AA35, AA37, AA39, AB28, AB30, AB32, AB34, AB36, AB38, N39, N41, N43, P38, P40, P42, P44, R39, R41, R43, T38, U39, V28, V30, V32, V34, V36, V38, W29, W33, W37	VDD_APC1	Power for the Kryo Gold application processor
L15, L17, L19, L21	VDD_A_EBI_0	Power for EBI0 PHY analog circuits
L27, L29, L31, L33	VDD_A_EBI_1	Power for EBI1 PHY analog circuits

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings shown in the following table reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Power supply	Description	Min	Max	Unit
VDD_A_CSI_0_1_0P9	Power for CSI 0, 1: 0.9 V circuits	-0.3	1.012	V
VDD_A_CSI_2_3_0P9	Power for CSI 2, 3: 0.9 V circuits			V
VDD_A_CSI_4_0P9	Power for CSI 4: 0.9 V circuits			V
VDD_A_DSI_0_0P9	Power for the DSI0 0.9 V circuits			V
VDD_A_DSI_1_0P9	Power for the DSI1 0.9 V circuits			V
VDD_A_DSI_0_PLL_0P9	Power for the DSI0 0.9 V PLL circuits			V
VDD_A_DSI_1_PLL_0P9	Power for the DSI1 0.9 V PLL circuits			V
VDD_A_PCIE_0_0P9	Power for the PCIe0 PLL			V
VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits			V
VDD_A_QLINK_2_0P9	Power for the QLink2 0.9 V circuits			V
VDD_A_QLINK_0_CK_0P9	Power for the QLink0 0.9 V clock circuits			V
VDD_A_QLINK_2_CK_0P9	Power for the QLink2 1.2 V clock circuits			V
VDD_A_REFGEN_0_0P9	Voltage for the REFGEN 0.9 V circuits			V
VDD_A_UFS_0_0P9	Power for the UFS 0.9 V core circuits			V
VDDA_QREF_0P85	Reference voltage for the QREFS 0.875 V circuits			V
VDD_A_USBHS_0P9	Power for the USB high speed 0.9 V circuits			V
VDD_A_USBHS_1P8	Power for the USB high speed 1.8 V circuits	-0.3	1.98	V
VDD_QFPROM	Power for programming the QFPROM			V
VDD_IO_EBI_x (LP4)	Power for EBIx I/O circuits	-0.3	0.715	V
VDD_IO_EBI_x (LP5)	Power for EBIx I/O circuits	-0.3	0.627	V
VDD_A_USBHS_3P1	Power for the USB high speed 3.1 V circuits	-0.3	3.52	V
VDD_PX5	Power for pad group 5 – UIM1 pads	-0.3	3.52	V
VDD_PX6	Power for pad group 6 – UIM2 pads	-0.3	3.52	V
VDD_PX2	Power for pad group 2 – SDC2 pads	-0.3	3.52	V
VDD_PX3	Power for pad group 3 – most I/O pads	-0.3	2.09	V
VDD_PX0	Power for pad group 0 – control signals			V
VDD_PX1	Power for pad group 1	-0.3	1.287	V
VDD_PX10	Power for pad group 10 – UFS	-0.3	1.43	V
VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits	-0.3	1.045	V
VDD_A_QLINK_1_CK_0P9	Power for the QLink1 1.2 V clock circuits			V

Table 3-1 Absolute maximum ratings (cont.)

Power supply	Description	Min	Max	Unit
VDD_A_USBSSDP_0_0P9	Power for the USB SS and DisplayPort 0P9V circuits	-0.3	1.045	V
VDD_A_QREFS_1P2	Reference voltage for the QREFS 1.2V circuits	-0.3	1.386	V
VDD_A_TURING_Q6_CS_1P2	Voltage for the TURING 1.2 V circuits			V
VDD_A_APC_CS_1P2	Power for application processor current sensor; 1.2 V circuits			V
VDD_A_CSI_0_1_1P2	Power for CSI 0, 1: 1.2 V circuits			V
VDD_A_CSI_2_3_1P2	Power for CSI 2, 3: 1.2 V circuits			V
VDD_A_CSI_4_1P2	Power for CSI 4: 1.2 V circuits			V
VDD_A_DSI_0_1P2	Power for the DSI0 1.2 V circuits			V
VDD_A_DSI_1_1P2	Power for the DSI1 1.2 V circuits			V
VDD_A_PCIE_0_PLL_1P2	Power for PCIe0 core circuits			V
VDD_A_QLINK_0_1P2	Power for the QLink0 1.2 V clock circuits			V
VDD_A_QLINK_1_1P2	Power for the QLink1 0.9 V clock circuits			V
VDD_A_QLINK_2_1P2	Power for the QLink2 0.9 V clock circuits			V
VDD_A_REFGEN_0_1P2	Voltage for the REFGEN 1.2 V circuits			V
VDD_A_UFS_0_1P2	Power for the UFS 1.2 V circuits			V
VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort 1.2 V circuits			V
VDD_APC0	Power for the Kryo Silver application processor	-0.3	1.133	V
VDD_APC1	Power for the Kryo Gold application processor	-0.3	1.243	V
VDD_CX	Power for digital core circuits	-0.3	1.133	V
VDD_MODEM	Modem circuits	-0.3	1.133	V
VDD_GFX	Power for graphics	-0.3	1.133	V
VDD_MX	Power for on-chip memory	-0.3	1.133	V
VDD_PX11	Power for pad group 11 – CXO pad	-0.3	1.43	V
VDD_LPI_CX	Power for LPI digital core circuits	-0.3	1.133	V
VDD_A_EBI_x	Power for EBIx PHY analog circuits	-0.3	1.133	V
VDD_LPI_MX	Power for LPI memory circuits	-0.3	1.133	V
VDD_MXC		-0.3	1.133	V
VDD_MM	Power for on-chip memory	-0.3	1.133	V
T_s	Storage temperature [a] [b]	-55	150	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [-35°C to +15°C] and relative humidity (RH) < 90%. QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions. The SM7450 meets all performance specifications listed in the following table, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

NOTE Customers should keep the thermal mitigation algorithm enabled with default limits to ensure that the operating temperature range is kept within the specification.

Table 3-2 Operating conditions for voltage rails

Parameter [a]		Min	Typ [b]	Max	Unit
Power-supply voltages					
VDD_APC0	Power for the Kryo Silver application processor	0.485	–	1.135	V
VDD_APC1	Power for the Kryo Gold application processor	0.5	–	1.13	V
VDD_CX	Power for digital core circuits	0.485	–	1.03	V
VDD_MODEM	Power for modem circuits	0.485	–	1.03	V
VDD_GFX	Power for graphics	0.485	–	1.03	V
VDD_MX	Power for on-chip memory	0.695	–	1.03	V
VDD_LPI_CX	Power for LPI digital core circuits	0.485	–	1.03	V
VDDA_EBI		0.65	–	1.03	V
VDD_LPI_MX VDD_LPI_MX_NAV		0.695	–	1.03	V
VDD_MXC		0.695	–	1.03	V
VDD_MM	Power for multimedia subsystem circuits	0.485	–	1.03	V
VDD_A_CSI_0_1_0P9	Power for CSI 0, 1: 0.9 V circuits	0.85	0.88	0.92	V
VDD_A_CSI_2_3_0P9	Power for CSI 2, 3: 0.9 V circuits				V
VDD_A_CSI_4_0P9	Power for CSI 4: 0.9 V circuits				V
VDD_A_DSI_0_0P9	Power for the DSI0 0.9 V circuits				V
VDD_A_DSI_1_0P9	Power for the DSI1 0.9 V circuits				V
VDD_A_DSI_0_PLL_0P9	Power for the DSI0 0.9 V PLL circuits				V
VDD_A_DSI_1_PLL_0P9	Power for the DSI1 0.9 V PLL circuits				V
VDD_A_PCIE_0_0P9	Power for the PCIe0 PLL				V
VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits				V
VDD_A_QLINK_2_0P9	Power for the QLink2 0.9 V circuits				V
VDD_A_QLINK_0_CK_0P9	Power for the QLink0 0.9 V clock circuits				V
VDD_A_QLINK_2_CK_0P9	Power for the QLink2 1.2 V clock circuits				V
VDD_A_REFGEN_0_0P9	Voltage for the REFGEN 0.9 V circuits				V
VDD_A_UFS_0_0P9	Power for the UFS 0.9V core circuits				V
VDD_A_QREFS_0P875	Reference voltage for the QREFS 0.875 V circuits				V
VDD_A_USBHS_0P9	Power for the USB high speed 0.9 V circuits				V
VDD_A_USBHS_1P8	Power for the USB high speed1.8 V circuits	1.7	1.75	1.8	V

Table 3-2 Operating conditions for voltage rails (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
VDD_QFPROM	Power for programming the QFPROM				V
VDD_IO_EBI_x (LP4)	Power for EBIx I/O circuits	0.57	0.6	0.65	V
VDD_IO_EBI_x (LP5)	Power for EBIx I/O circuits	0.47	0.5	0.57	V
VDD_A_USBHS_3P1	Power for the USB high speed 3.1 V circuits	2.97	3.072	3.2	V
VDD_PX5	Power for pad group 5 – UIM1 pads				
Low voltage		1.7	1.8	1.9	V
High voltage		2.72	2.96	3.2	
VDD_PX6	Power for pad group 6 – UIM2 pads				
Low voltage		1.7	1.8	1.9	V
High voltage		2.72	2.96	3.2	
VDD_PX2	Power for pad group 2 – SDC2 pads				
Low voltage		1.7	1.8	1.9	V
High voltage		2.72	2.96	3.2	
VDD_PX3	Power for pad group 3 – most I/O pads	1.7	1.8	1.9	V
VDD_PX0	Power for pad group 0 – control signals				V
VDD_PX1	Power for pad group 1	1.05	1.128	1.17	V
VDD_PX10	Power for pad group 10 – UFS	1.12	1.2	1.3	V
VDD_PX11	Power for pad group 11 – CXO pad	1.1	1.2	1.3	V
VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits	0.866	0.912	0.95	V
VDD_A_QLINK_1_CK_0P9	Power for the QLink1 1.2 V clock circuits				V
VDD_A_USBSSDP_0_0P9	Power for the USB SS and DisplayPort 0P9V circuits	0.86	0.88	0.95	V
VDD_A_QREFS_1P2	Reference voltage for the QREFS 1.2V circuits	1.14	1.2	1.26	V
VDD_A_TURING_Q6_CS_1P2	Voltage for the TURING 1.2 V circuits				V
VDD_A_APC_CS_1P2	Power for application processor current sensor; 1.2 V circuits				V
VDD_A_CSI_0_1_1P2	Power for CSI 0, 1: 1.2 V circuits				V
VDD_A_CSI_2_3_1P2	Power for CSI 2, 3: 1.2 V circuits				V
VDD_A_CSI_4_1P2	Power for CSI 4: 1.2 V circuits				V
VDD_A_DSI_0_1P2	Power for the DSI0 1.2 V circuits				V
VDD_A_DSI_1_1P2	Power for the DSI1 1.2 V circuits				V
VDD_A_PCIE_0_PLL_1P2	Power for PCIe0 core circuits				V
VDD_A_QLINK_0_1P2	Power for the QLink0 1.2 V clock circuits				V
VDD_A_QLINK_1_1P2	Power for the QLink1 0.9 V clock circuits				V
VDD_A_QLINK_2_1P2	Power for the QLink2 0.9 V clock circuits				V
VDD_A_REFGEN_0_1P2	Voltage for the REFGEN 1.2 V circuits				V
VDD_A_UFS_0_1P2	Power for the UFS 1.2 V circuits				V
VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort 1.2 V circuits				V
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.

3.3 Power delivery network specification

A detailed power delivery network specification is available in the *SM7450 Chipset Power Delivery Network Specification* (80-19448-1P) document.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the *SM7325 Linux Android Current Consumption Data Application Note* (80-19448-7) document.

3.5 Power sequencing

The PMIC includes poweron circuits that provide the proper power sequencing for the entire SM7450 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of certain PMIC pins. See the appropriate PMIC data sheet for details.

A high-level summary of the required default power-on sequence is as follows:

1 VDD_PX5 (UICC1), VDD_PX6 (UICC2),

2 VDD_MX (on-chip memory)

3 VDD_MX

4 VDD_LPI_MX (LPI core memory), VDD_NAV_LPI_MX

5 VDD_A_EBI_0/1 (EBI 0.9 V), VDD_A_PLL_EBI_0/1
VDD_CX (digital core), VDD_D_EBI

6 VDD_LPI_CX (LPI core)

7 VDD_PX0 (pad group0), VDD_PX3 (peripheral)

8 VDD_PX1 (pad group1)

9 VDDA_QREF_1P2, VDD_A_TURING_Q6_CS_1P2, VDD_A_APC_CS_1P2, VDD_A_CSI_0_1_1P2, VDD_A_CSI_2_3_1P2, VDD_A_CSI_4_1P2, VDD_A_DSI_0_1P2, VDD_A_DSI_1_1P2, VDD_A_PCIE_0_PLL_1P2, VDD_A_QLINK_0_1P2, VDD_A_QLINK_1_1P2, VDD_A_QLINK_2_1P2, VDD_A_REFGEN_0_1P2, VDD_A_UFS_0_1P2, VDD_A_USBSSDP_0_1P2

10 VDD_A_CSI_0_1_0P9, VDD_A_CSI_2_3_0P9, VDD_A_CSI_4_0P9, VDD_A_DSI_0_0P9, VDD_A_DSI_1_0P9, VDD_A_DSI_0_PLL_0P9, VDD_A_DSI_1_PLL_0P9, VDD_A_PCIE_0_0P9, VDD_A_QLINK_0_0P9, VDD_A_QLINK_2_0P9, VDD_A_QLINK_0_CK_0P9, VDD_A_QLINK_2_CK_0P9, VDD_A_REFGEN_0_0P9, VDD_A_UFS_0_0P9, VDDA_QREF_0P85, VDD_A_USBHS_0P9

11 VDD_A_USBSSDP_0_0P9

12 VDD_PX11 (CXO pad group)

13 VDD_A_USBHS_1P8,VDD_QFPROM

14 VDD_IO_EBI_0, VDD_IO_EBI_0

15 VDDA_USB_HS_3P1 (USB HS 3.1 V)

16 VDD_PX10 (UFS reference clock, UFS reset)

17 VDD_APC0 (Silver application processor)

Comments regarding this sequence include:

- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up.

3.6 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage.

- Some are dedicated for interconnections between the SM device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-3 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDD_PX3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDD_PX3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	100	—	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	—	mV
I_{IH}	Input high leakage current [a]	—	1.0	µA
I_{IL}	Input low leakage current	-1.0	—	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current	—	1.0	µA
I_{OZL}	Low-level, tri-state leakage current	-1.0	—	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	97.5 (20)	27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [b]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [c]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage, CMOS	VDD_PX3 - 0.45	VDD_PX3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

[a] I_{IH}, I_{IL}, I_{OZH}, and I_{OZL} values are based on nominal PVT (TT/25°C).
[b] Pin voltage = VDD_PX3 maximum. For keeper pins, pin voltage = VDD_PX3 maximum - 0.45 V.
[c] Pin voltage = GND and supply = VDD_PX3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_PX3 maximum.

Table 3-4 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_PX2	–	VDD_PX2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDD_PX2	V

Table 3-5 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-6 UICC 3 V mode DC specifications for (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
VDDPX	Supply voltage	2.7	2.95	3.05	V
V_{IH}	High-level input voltage [a]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage [b]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA

Table 3-6 UICC 3 V mode DC specifications for (VDD_PX5 and VDD_PX6) (cont.)

Parameter	Description	Min	Typ	Max	Unit
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10K	–	100K	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10K	–	100K	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10K	–	100K	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10K	–	100K	kΩ
V_{OH}	High-level output voltage [c]	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage [d]	0.0	–	0.4	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal. V_{HYS} is not a required specification for UICC.
[b] V_{HYS} is not a required specification for UICC.
[c] UICC specifies V_{OH} = 0.8 × VDDPx (RST) and 0.7 × VDDPx (CLK, I/O). The worse-case V_{OH} is used in this table.
[d] UICC specifies V_{OL} = 0.2 × VDDPx (RST, CLK) and 0.4 V (I/O). The worse-case V_{OL} is used in this table.

Table 3-7 UICC 1.8 V mode DC specifications for (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
VDDPX	Supply voltage [a]	1.65	1.8	1.95	V
V_{IH}	High-level input voltage [b]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10K	–	100K	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10K	–	100K	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10K	–	100K	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10K	–	100K	kΩ
V_{OH}	High-level output voltage	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage	0.0	–	0.4	V

[a] UICC supply range for class C is 1.62 V 1.98 V.
[b] V_{IH}, V_{IL}, are only applicable for I/O signal. V_{HYS} is not required specification for UICC.

Table 3-8 Digital I/O characteristics for VDD_PX10 nominal (UFS)

Parameter	Description	Min	Max	Unit
V_{OL}	Output low-level voltage	0	0.25 × VDD_PX10	V
V_{OH}	Output high-level voltage	0.75 × VDD_PX10	VDD_PX10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM7450 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Rise and fall time specifications.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the following figure.

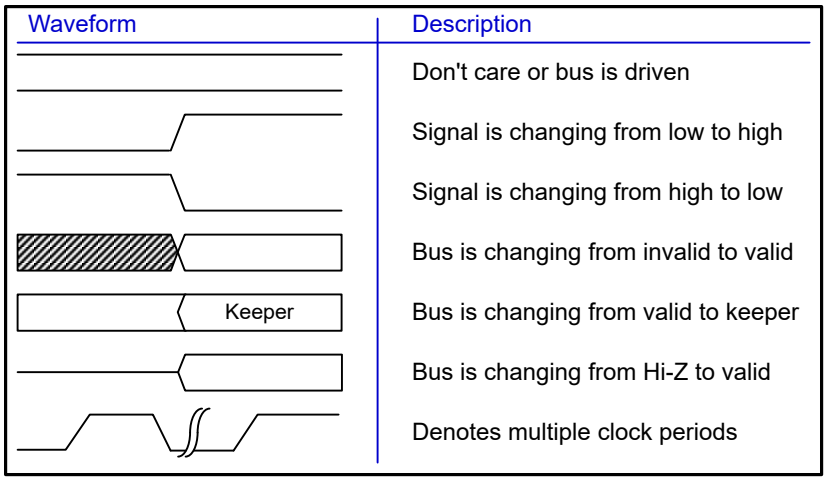


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize SM7450 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the following figure.

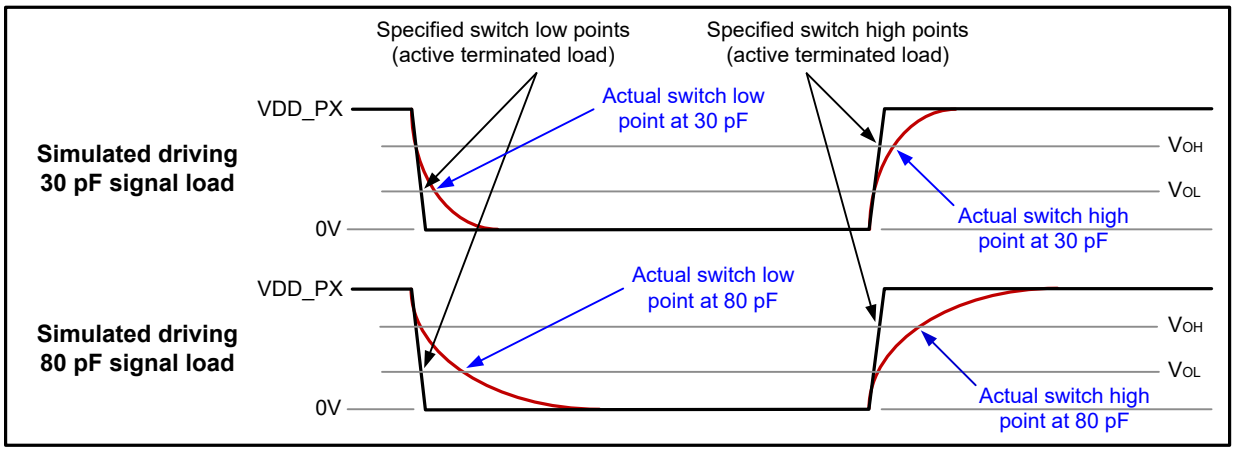


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM7450 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The SM7450 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated $V_{DD\_PXDD\_PX}/2$ (or 50% of V supply. The input switch point for pure input-only pads is designed to be V_{DD_PX} supply. The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

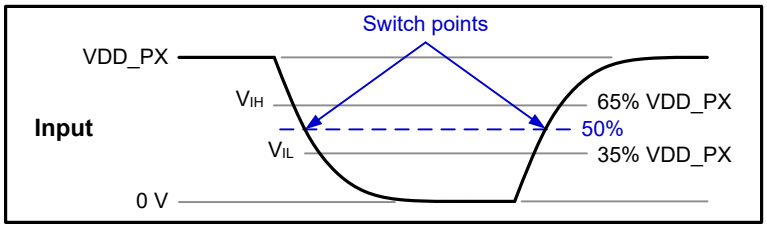


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented VOH (min) and VOL(max) levels over worst-case process/voltage/temperature. Because the pad output structures are essentially CMOS drivers that possibly have a small amount of

IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX} - 50 mV or more
- V_{OL} ~ 50 mV or less

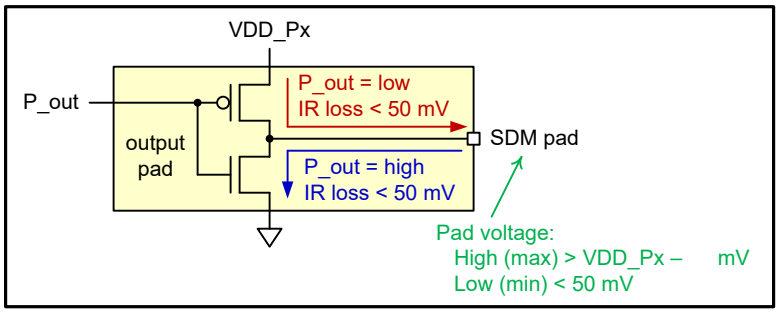


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) provides approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) provides approximately 1.25 mA or more at ½ × [V_{DDPX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.8.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4X/LPDDR5 SDRAM memory that is attached to the SM7450 chipset.

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Secured digital interfaces for details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SM7450 device supports four 4-lane MIPI_CSIs: CSI0, CSI1, CSI2, and CSI3.

Table 3-9 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.0	None

3.9.2 Audio support

- A dedicated audio codec, such as the WCD9370/WCD9375/WCD9380/WCD9385, uses the industry standard SoundWire interface.

Other audio-related interface options include:

- Digital microphone: Digital microphone PDM interface
- SWR: SoundWire (SWR) interface
- SLIMbus: SLIMbus interface
- I^2S: I^2S interfaces
- I^2C/I3C: I^2C/I3C interface
- SPI: Serial peripheral interface

See the *Qualcomm Aqstic WCD9370 Device Specification* (80-PG244-1), *Qualcomm Aqstic WCD9375 Device Specification* (80-PG245-1), and *Qualcomm Aqstic WCD9380/WCD9385 Device Specification* (80-PL335-1) for performance characteristics.

3.9.3 Display support

The SM7450 device supports up to one D-PHY display.

Table 3-10 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

3.9.4 DMB support

The SM7350 supports an external DMB solution using the following interface options:

- SPI: Serial peripheral interface
- SD: Secured digital interfaces

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

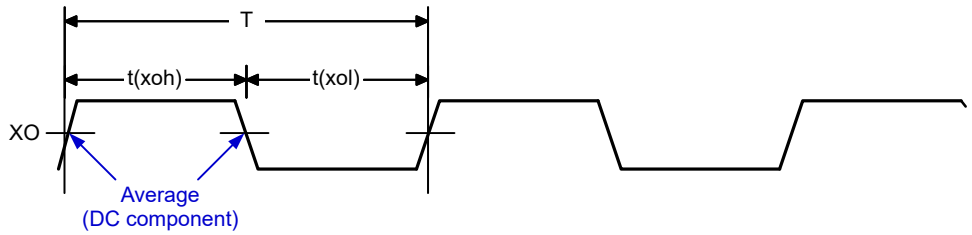


Figure 3-5 XO timing parameters

Table 3-11 XO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	–	–	ns
1/T	Frequency	19.2 MHz must be used.	–	–	–	MHz

[a] See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.10.1.2 Sleep clock

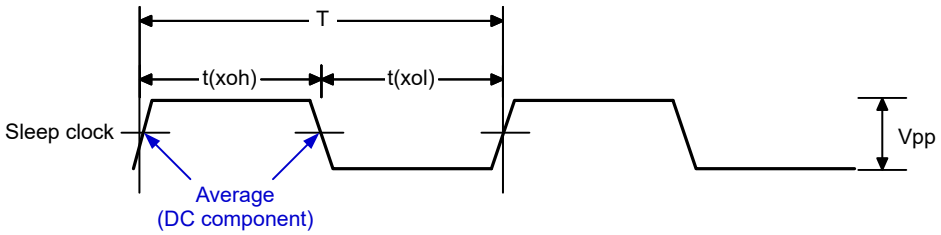


Figure 3-6 Sleep-clock timing parameters

Table 3-12 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs

Table 3-12 Sleep-clock timing parameters (cont.)

Parameter		Comments	Min	Typ	Max	Unit
F	Sleep-clock frequency	F= 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Digital-logic characteristics.

3.10.3 JTAG

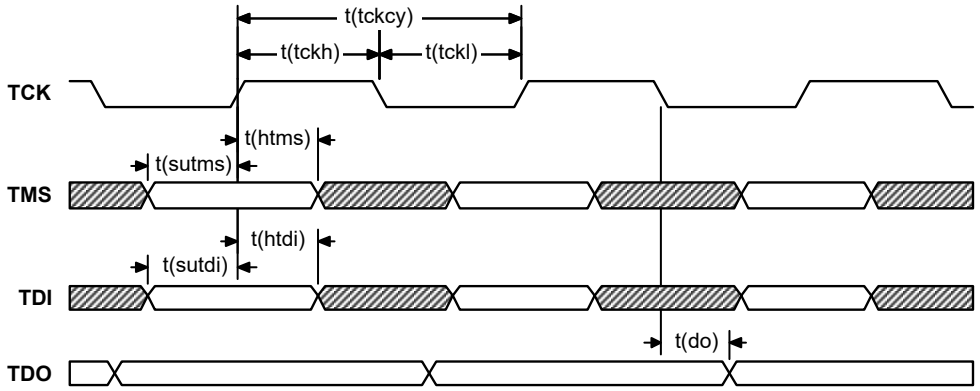


Figure 3-7 JTAG interface timing diagram

Table 3-13 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

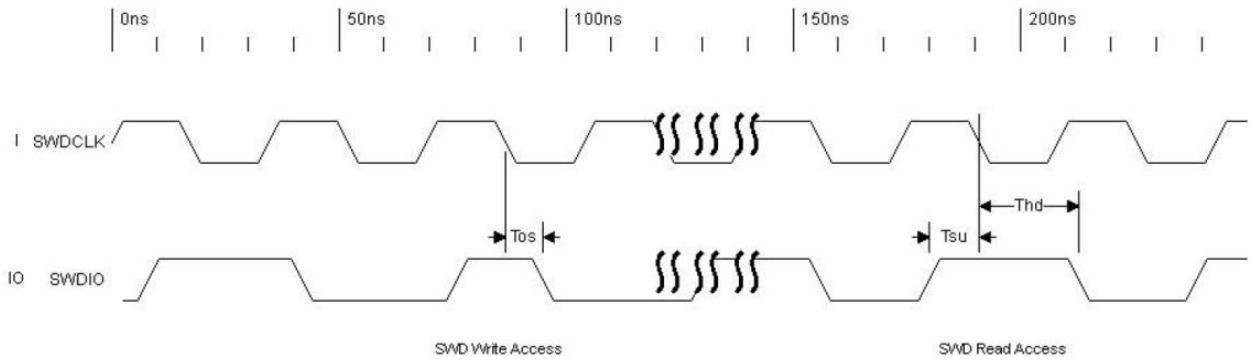


Figure 3-8 SWD write and read AC timing diagram

Table 3-14 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	s	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

NOTE SWDCLK runs at 20 MHz or lower.

3.11 RF and power management interfaces

3.11.1 RF front end (RFFE)

Table 3-15 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 2.0	None

3.11.2 System power management interface (SPMI)

Table 3-16 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

3.12 Connectivity

The connectivity functions supported by the SM7450 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Universal integrated circuit card (UICC) interface
- DisplayPort support over USB Type-C
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power interchip media bus (SLIMbus) interface for Bluetooth, FM
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Dedicated I^2C interfaces for camera (CCI I^2C)
- Through proper configuration of QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

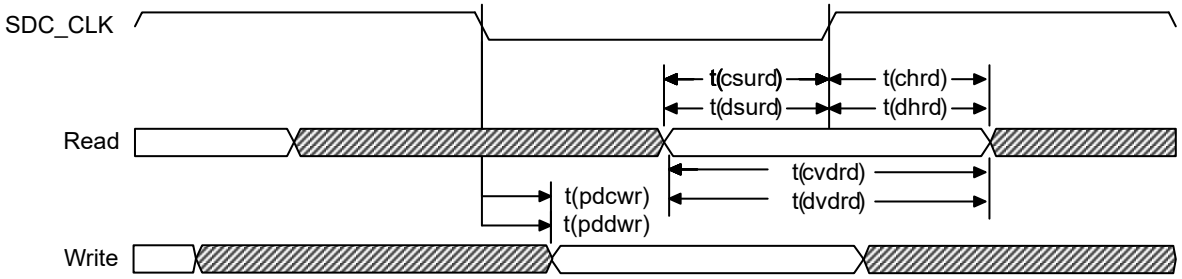
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.12.1 Secured digital interfaces

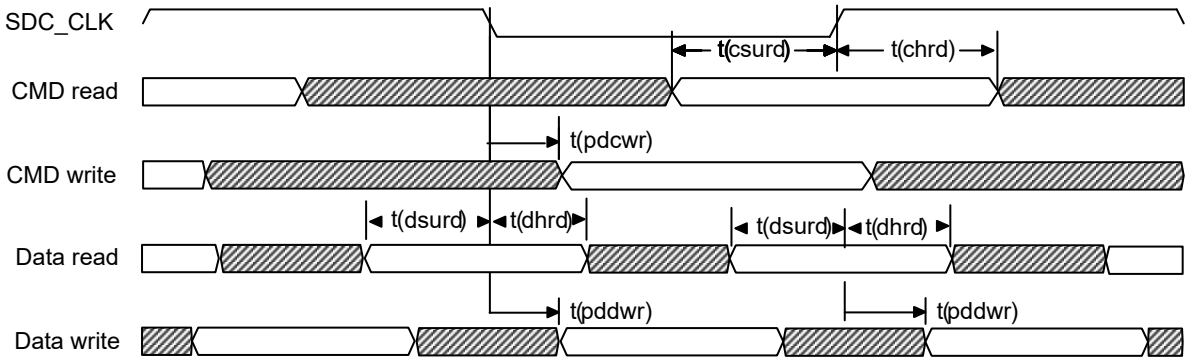
Table 3-17 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

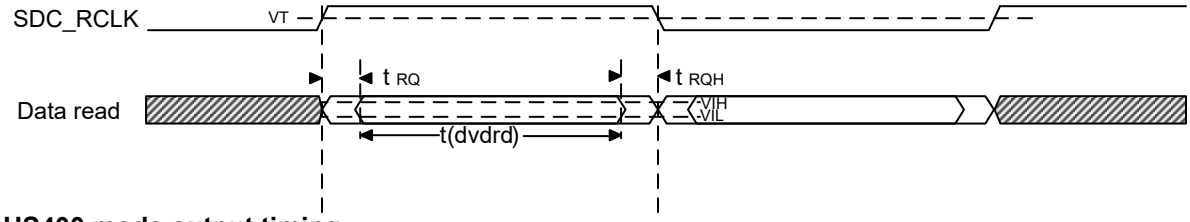
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

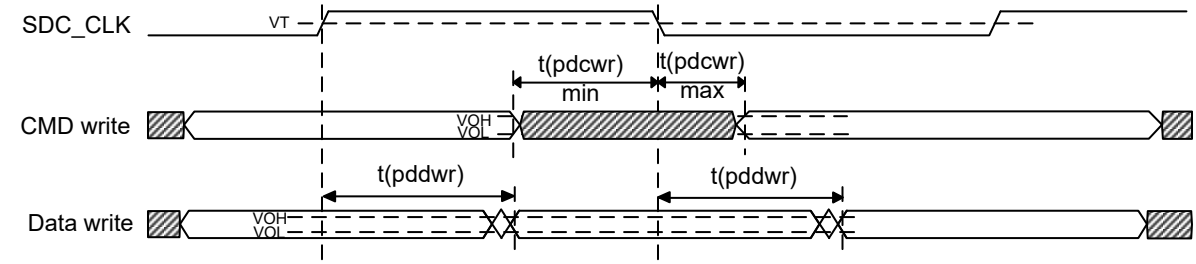


Figure 3-9 Secured digital interface timing

3.12.2 USB interfaces

Table 3-18 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 1
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.12.3 UICC interface

Table 3-19 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.12.4 DisplayPort

Table 3-20 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.12.5 PCIe interface

Table 3-21 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link upconfigure capability

3.12.6 UFS interface

Table 3-22 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None
Universal Flash Storage (UFS), Version 2.1	None

3.12.7 Digital microphone PDM interface

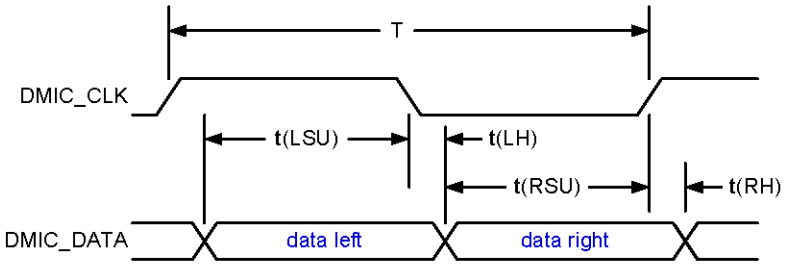


Figure 3-10 Digital microphone PDM interface timing

Table 3-23 Digital microphone timing

Parameter		Min	Typ	Max	Unit
1/T	DMIC clock frequency	0.6	–	6.144	ns
	DMIC clock duty cycle	45	–	55	
t(LSU)	Data left setup time to clock falling edge	–	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	

3.12.8 SoundWire (SWR) interface

SM7450 SoundWire PHY timing parameters, as specified in the following table, are compliant to clock and data specifications, as specified in the *MIPI Alliance Specification for SoundWire Version 0.8, Revision 04*.

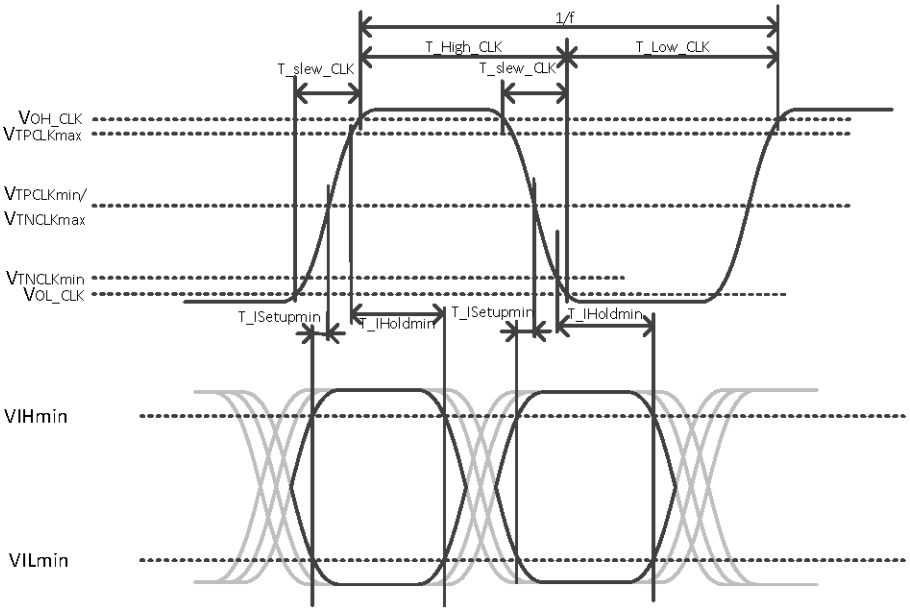


Figure 3-11 PHY timing – clock output/input and data input

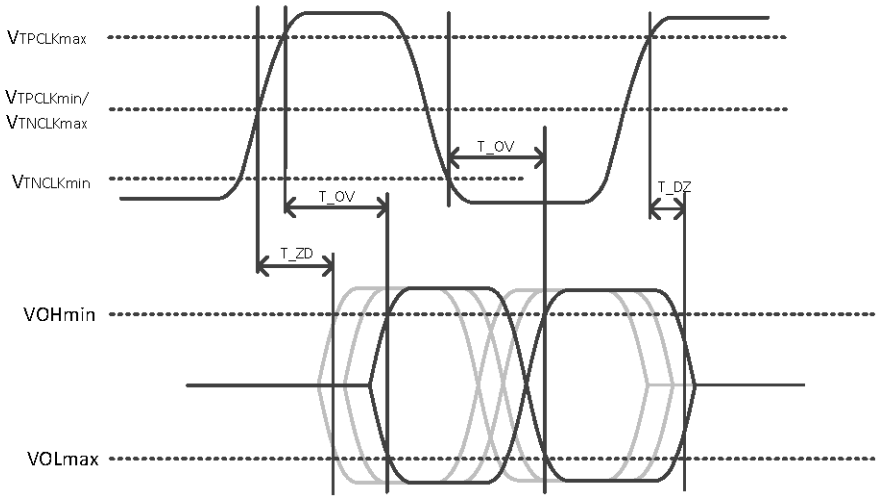


Figure 3-12 PHY timing – clock output and data output

Table 3-24 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Unit
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	ns
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	4	–	ns
t_IHold_min_Data_1V8	Input hold time	–	5	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.12.9 SLIMbus interface

Table 3-25 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.12.10 I²S interfaces

There are two I²S interface types supported by the SM7325:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI²S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-26 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

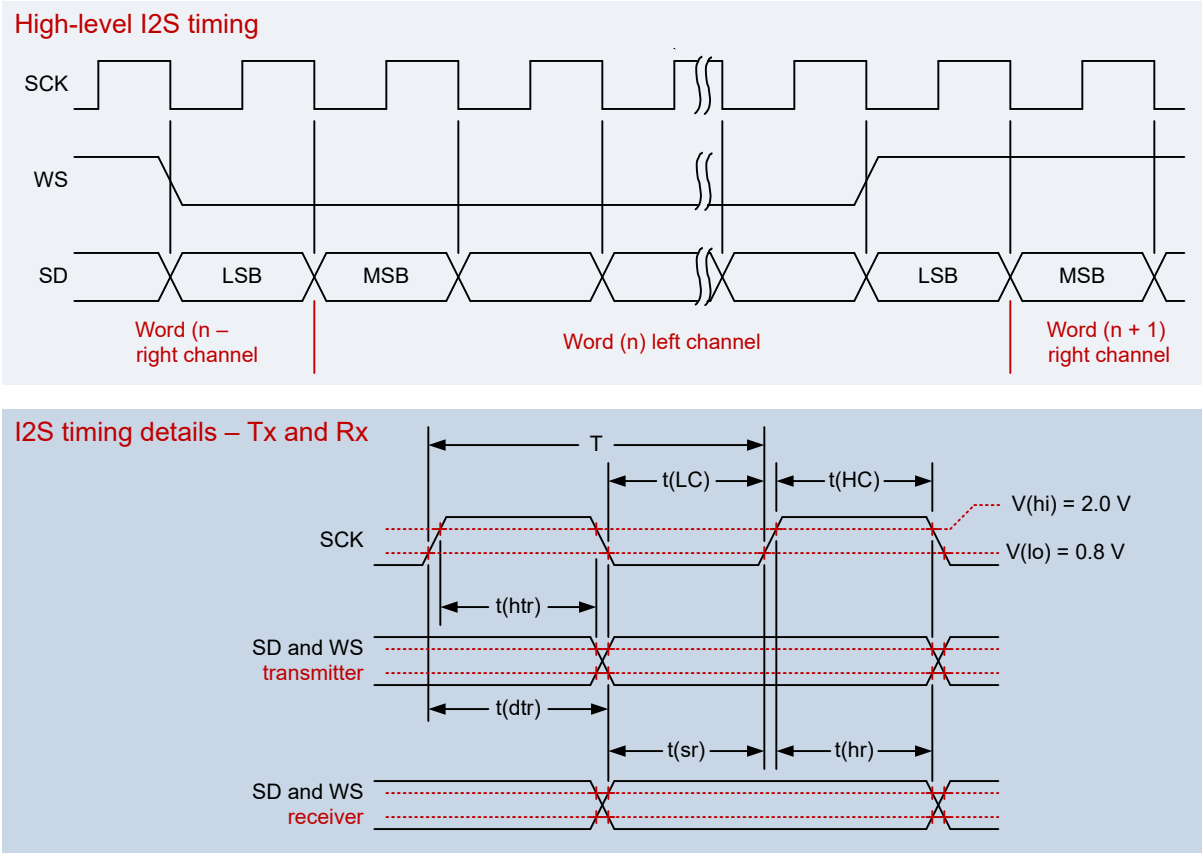


Figure 3-13 I²S timing diagram

Table 3-27 I²S interface timing interface

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency [a]		–	–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns

Table 3-27 I²S interface timing interface (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.1	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60 × T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.1	ns

[a] Load capacitance is between 10 and 40 pF.

3.12.11 Touchscreen connections

Touchscreen panels are supported using I²C buses (I²C/I3C interface) and GPIOs configured as discrete digital inputs (Digital-logic characteristics). Additional specifications are not required.

3.12.12 I²C/I3C interface

Table 3-28 Supported I²C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C Specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.12.13 Serial peripheral interface

The SM7450 supports SPI as a master only.

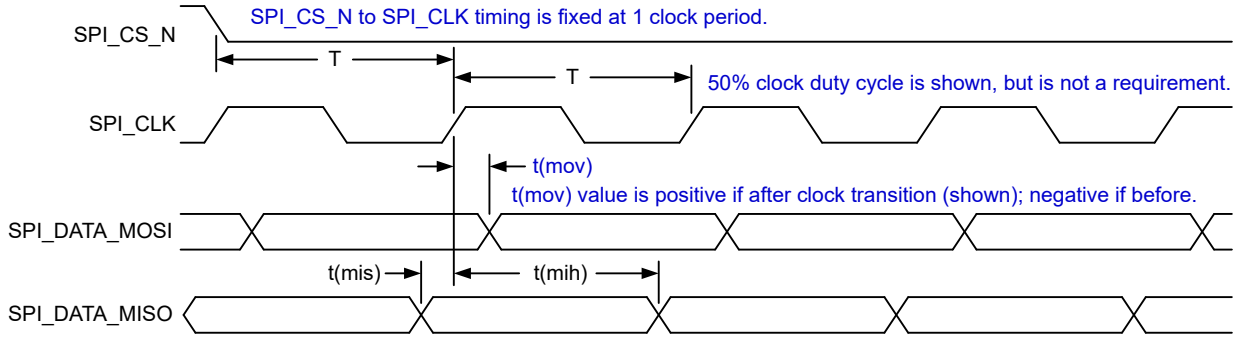


Figure 3-14 SPI master timing diagram

Table 3-29 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clockperiod) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

4 Mechanical information

4.1 Device physical dimensions

The SM7450 device is available in the PSP1269B that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The PSP1269B has a 14 mm by 12 mm body, with a maximum height of 0.91 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in the following figure.

NOTE Click the following link to download the *Package Outline Drawing PSP1269B, 14.0 × 12.0 × 0.91 mm, M530, S164* (NT90-29856-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-29856-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

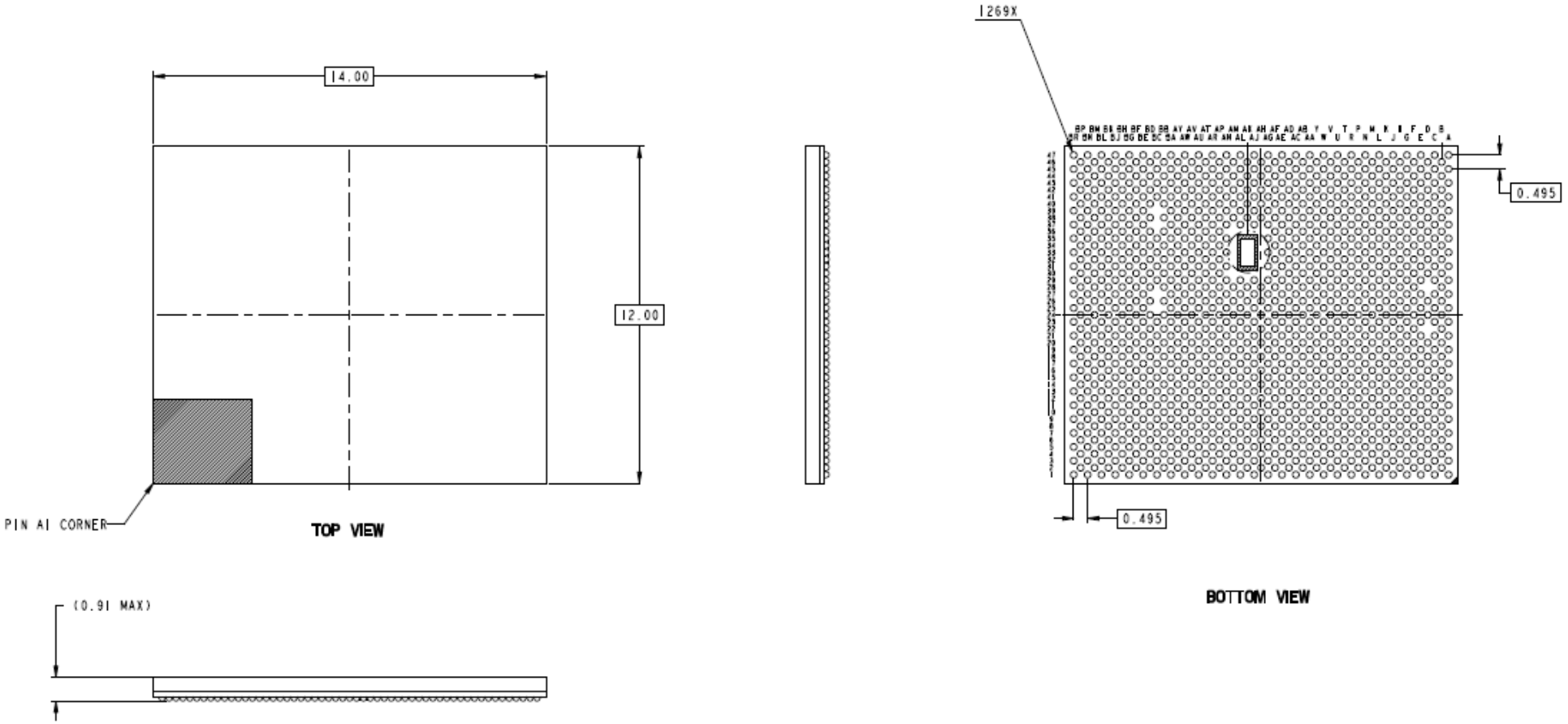


Figure 4-1 PSP1269B outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

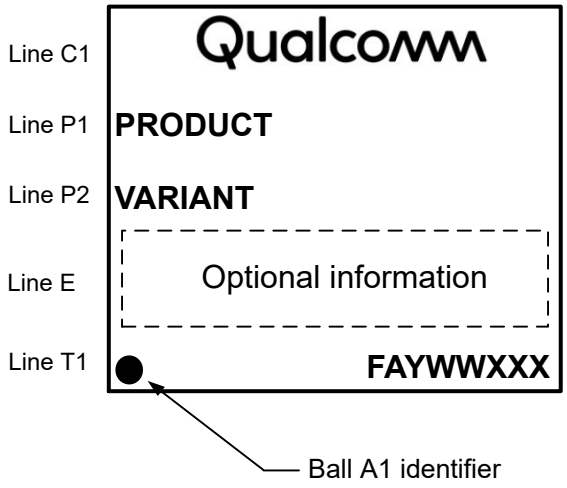


Figure 4-2 SM7450 device marking (top view, not to scale)

Table 4-1 SM7450 device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ SM7450
P2	VARIANT	Device variant information ▪ See Table 4-4 for the assigned values.
E	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ▪ F = J (Samsung) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE For complete marking definitions of all SM7450 variants and revisions, see the *SM7450 Device Revision Guide* (80-26135-4).

Table 4-2 QFPROM_CORE_PTE_ROW0_LS

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various features variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code as shown in the following table:

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	SM-7450	-0	-PSP	1269	B		-TR	-00	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example: SM-7450-0-PSP1269B-TR-00-0-AB

Device identification details for all samples available to date are summarized in the following table:

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	Hardware revision number (JTAG_ID - see Table 4-2)	FEATURE_ID (see Table 4-2) [b]	Hardware version	Source configuration code (S) [c]	Comments	Sample date
SM7450	ES	000-AB	0x0 01D3 0E1	0x0	v1.0	0	CPU 4 × 2.35 GHz, 4 × 1.8 GHz; GPU 443 M; LPDDR5/4X; C/G/W/L/5G sub-6 140 MHz/mmW 400 MHz	12/24/2021
SM7450	CS	000-AB CS date codes are as follow: ■ SPIL: 215 ■ ASE: 216	0x0 01D3 0E1	0x0	v1.0	0	CPU 1 × 2.4 GHz, 3 × 2.36 GHz, 4 × 1.8 GHz; GPU 443 M; LPDDR4X; C/G/W/L/5G sub-6 140 MHz/mmW 400 MHz	4/30/2022
SM7450	CS2	000-AB CS date codes are as follow: ■ SPIL: 220 ■ ASE: 220	0x0 01D3 0E1	0x0	v1.0	0	CPU 1 × 2.4 GHz, 3 × 2.36 GHz, 4 × 1.8 GHz; GPU 443 M; LPPDR5/4X; C/G/W/L/5G sub-6 140 MHz/mmW 400 MHz	6/30/2022

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
[b] The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-5.

Table 4-5 Source configuration code

S value	Die	F value = J
0	Digital	Samsung
Other columns and rows will be added in future revisions of this document, if needed.		

4.3.1 Daisy chain devices

For daisy chain part information, contact QTI Sales team.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in the following table:

NOTE The appropriate MSL rating is shaded in the table.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM7450 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM7450 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SM7450 Package Thermal Model Icepak* (HS11-26135-5HW) and the *SM7450 Package Thermal Model FloTHERM* (HS11-26135-6HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-26135-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-26135-6HW

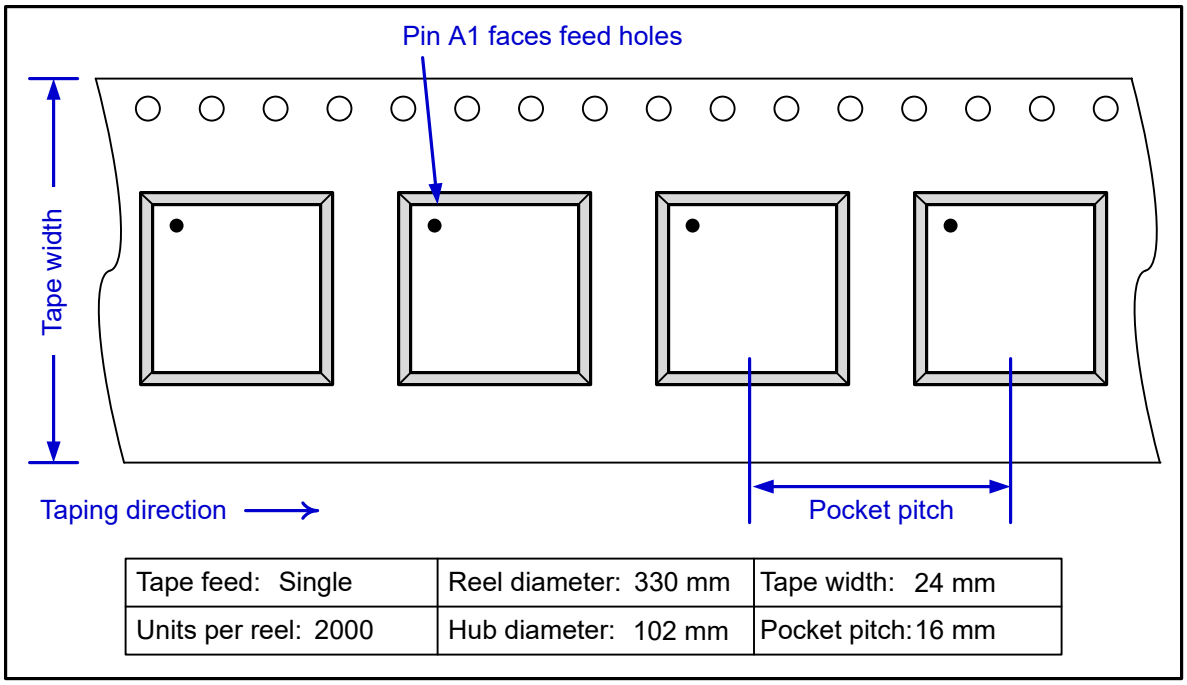
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM7450 tape carrier is shown in the following figure, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed: Single	Reel diameter: 330 mm	Tape width: 24 mm
Units per reel: 2000	Hub diameter: 102 mm	Pocket pitch: 16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in the following figure.

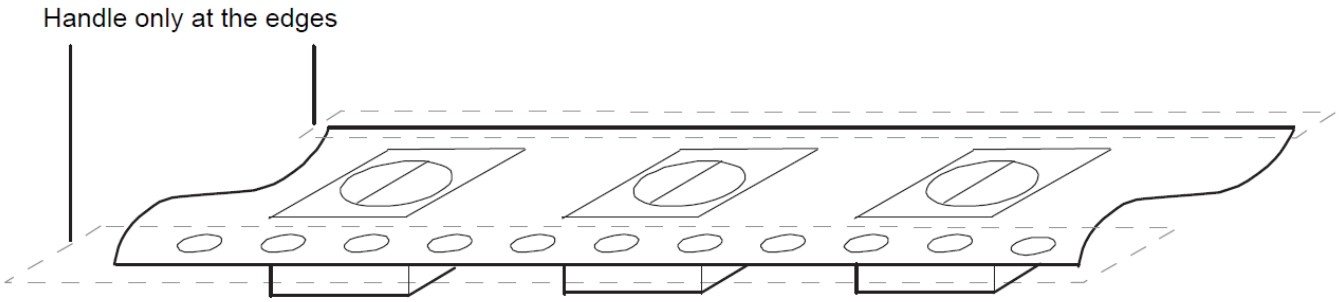


Figure 5-2 Tape handling

5.1.2 Matrix tray information

Table 5-1 Matrix tray key dimensions

Array	Key dimensions
M	15.45
M1	15.10
M2	17.80
M3	15.00
Units per tray	8 × 17 (136)

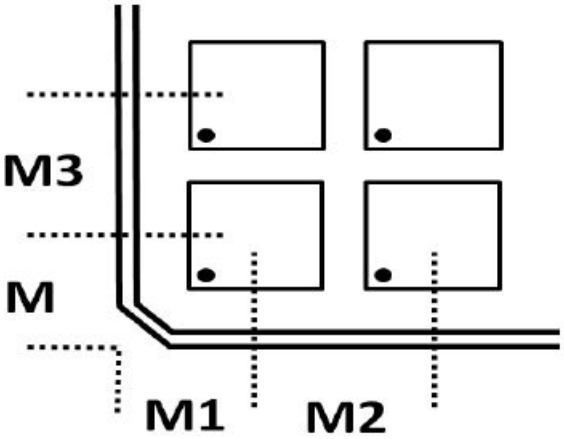


Figure 5-3 Matrix tray orientation

5.2 Storage

5.2.1 Bagged storage conditions

SM7450 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM7450 if the conditions specified in Bagged storage conditions and Out-of-bag duration have **not been exceeded**.

It is necessary to bake the SM7450 if any condition specified in Bagged storage conditions or Out-of-bag duration has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in SMT assembly guidelines can be performed using daisy chain components.

Daisy chain PCB routing recommendations are available for download.

This link will be provided in a future revision of this document.

7 Part reliability

7.1 Reliability qualifications summary

Reliability evaluation report for SM7450 14.0 × 12.0 × 0.91 mm PSP1269B device, foundry source SEC-S5.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (total samples from three different wafer lots)	248	Pass DPPM < 1000
HTOL in FIT (l) failure in billion device hours HTOL: JESD22-A108-A (total samples from three different wafer lots)	248	Pass FIT < 100
Mean time to failure (MTTF) t = 1/l in million hours (total samples from three different wafer lots)	248	> 20
ESD – human-body model (HBM) rating JS001-2017 (total samples from one wafer lot)	21	Pass ±1 KV
ESD – charged-device model (CDM) rating JS-002-2014 (total samples from one wafer lot)	6	Pass ± 250 V
Latch-up (I-test): EIA/JESD78E Trigger current: ±100 mA; temperature: 95°C (total samples from one wafer lot)	6	Pass Class II, Level A
Latch-up (Vsupply overvoltage): EIA/JESD78E Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 95°C (total samples from one wafer lot)	6	Pass Class II, Level A

Table 7-2 Package reliability results

Tests, standards, and conditions	ASE sample size	SPIL sample size	Results
Moisture resistance test (MRT): J-STD-020C MSL3, reflow at 260 +0/-5°C (total samples from three different assembly lots)	1740	1740	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C	600	600	Pass

Table 7-2 Package reliability results (cont.)

Tests, standards, and conditions	ASE sample size	SPIL sample size	Results
(total samples from three different assembly lots)			
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C (total samples from three different assembly lots)	570	570	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C (total samples from three different assembly lots)	234	240	In progress ECD 4/29
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (total samples from three different assembly lots)	510	510	Pass
Flammability Note: Flammability test – not required UL-STD-94 Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See the note under the Tests, standards, and conditions column.
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (total samples from three different assembly lots at each SAT)	30	30	Pass
Die shear MIL-STD-883E, Method 2019 (total samples from three different assembly lots at each SAT)	30	30	Pass
Solder bump shear (total samples from three different assembly lots at each SAT)	30	30	Pass
Solder ball shear: JESD22-B117 (total samples from three different assembly lots at each SAT)	30	30	Pass
Internal/external visual (total samples from three different assembly lots at each SAT)	30	30	Pass

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	September 2021	Initial release
AB	December 2021	■ *SM7450 functional block diagram*: Updated the block diagram ■ *Pin description – general pins*: Updated pins AF44 and AG43 ■ *Part marking*: Added this section ■ *Device ordering information*: Added this section ■ *Daisy chain devices*: Added this section ■ *Device moisture sensitivity level*: Added this section ■ *Thermal characteristics*: Added this section
AC	April 2022	■ Device description: Updated Kryo CPU details ■ Table 1-1 *SM7450 features*: Updated this table ■ Figure 1-1 *SM7450 functional block diagram*: Updated the figure ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Updated GPIO_38, GPIO_59, GPIO_79, and GPIO_161
AD	May 2022	■ Chapter 3 *Electrical specifications*: Added this chapter ■ Table 4-4 *Device identification details*: Added CS sample ■ Chapter 5 C*arrier, storage, and handling information*: Added this chapter ■ Chapter 6 *PCB mounting guidelines*: Added this chapter ■ Chapter 7 *Part reliability*: Added this chapter
AE	September 2022	■ Key features: Updated 64 MP to 84 MP ■ Table 4-4 *Device identification details*: □ Added feature id for ES and CS □ Added CS2 sample

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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