SM7150
Device Specification
80-PG319-1 Rev. H

Qualcomm Technologies, Inc.

Device description

The SM7150 includes the next generation of the Qualcomm® Snapdragon™ 700 series processor and LTE modem.

Key processor and memory characteristics include:

- 8 nm process for lower active power dissipation and faster CPU performance
- 11.10 × 10.50 × 0.99 mm non package-on-package (non-PoP), 0.35 mm pitch
- A customized 64-bit Arm v-8 compliant applications processor (Qualcomm® Kryo™ 470 CPU)
  - Kryo Gold: dual high-performance cores up to 2.208 GHz
  - Kryo Silver: hexa low-power cores 1.804 GHz
- Qualcomm® Adreno™ GPU 618 graphics processing unit (GPU) with 64-bit addressing
- Dedicated Compute DSP for Computer Vision and Video Post Processing. Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (dual HVX 512)
- Dedicated NPU at 600 MHz for Machine Learning
- Low-power island (LPI) – contains DSP shared between Snapdragon sensor core and low-power audio subsystem. The Snapdragon sensor supports always-on use cases.
- Dual-channel non-PoP high-speed memory, LPDDR4X SDRAM designed for 1866 MHz clock (2 × 16 bit)

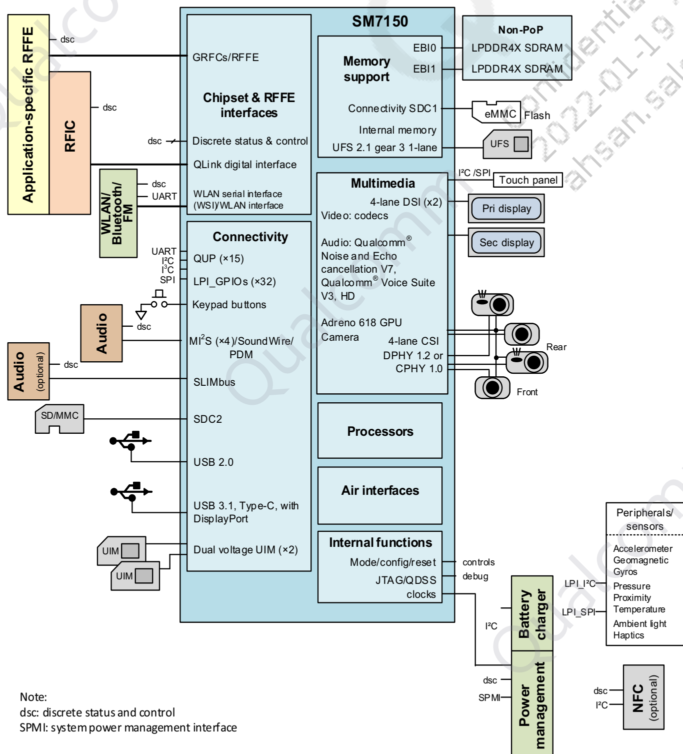
The latest air interface standards are supported, including:

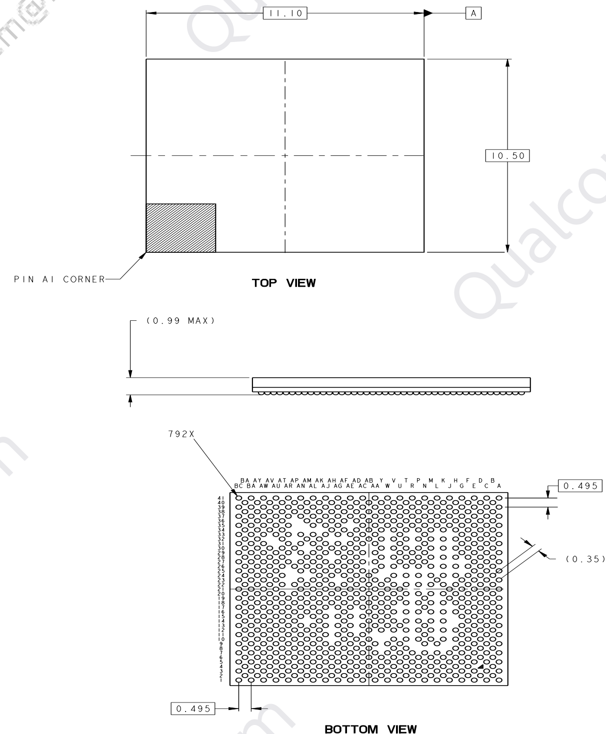
- LTE Cat15 (FDD and TDD)
- DC-HSPA+
- TD-SCDMA
- WCDMA
- CDMA up to 1X advanced and 1xEV-DOrA

Key features (see Section 1.2 for details)

- Always-on subsystem with RPMh for hardware-based resource and power management
- Qualcomm® Universal Bandwidth Compression (UBWC) 2.0, 2x, and 3.0 compression with camera, display, and DSP
- More RF operating bands and advanced techniques with SDR660:
  - Sixth-generation LTE multimode modem Rel. 13
  - Up to 800 Mbps LTE peak throughput for downlink and 150 Mbps for uplink
  - 3DL/1UL and 2DL/2UL LTE (60 MHz CA across RF bands)
  - 256 QAM DL
  - Support for 4 × 4 MIMO with LAA
- Display support: QHD+, 10-bit DP, 10 hardware layers, improved HDR10 and wide color Gamut, Qualcomm® Low-Power Picture Enhancement display feature, and Qualcomm® TruPalette™ display feature, VESA DSC 1.1
- Two 4-lane DSIs D-PHY 1.2 at 2.5 Gbps per lane or C-PHY 1.0 at 17 Gbps (2.5 G symbols per trio per second)
- Dual 14-bit image signal processing (ISP) + 1 Lite ISP: 20 + 20 + 2 MP to support 32 MP/30 fps.
- Three 4-lane and one 2-lane CSIs (4/4/4/2) D-PHY 1.2 at 2.5 Gbps per lane or C-PHY 1.0 at 17 Gbps (5.71 Gbps/trio on 3 trios per port)
- Support for UFS 2.1 gear 3 (one-lane), eMMC 5.1, and SD 3.0
  - UFS + eMMC memory concurrent usage support for storage expansion
- Support for USB 3.1 Type-C with DisplayPort 1.4 and USB 2.0
- WCN3998: WLAN 2 × 2 802.11a/b/g/n/ac (802.11ax Ready), MU-MIMO with DBS support, Bluetooth 5.1 and FM
- WCN3990: WLAN 2 × 2 802.11a/b/g/n/ac MU-MIMO with DBS support, Bluetooth 5.0 and FM
- WCN3980: WLAN 1 × 1 802.11a/b/g/n/ac and Bluetooth 5.0 and FM

SM7150 high-level block diagram and PSP792 drawing





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1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

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1.1 Functional block diagram

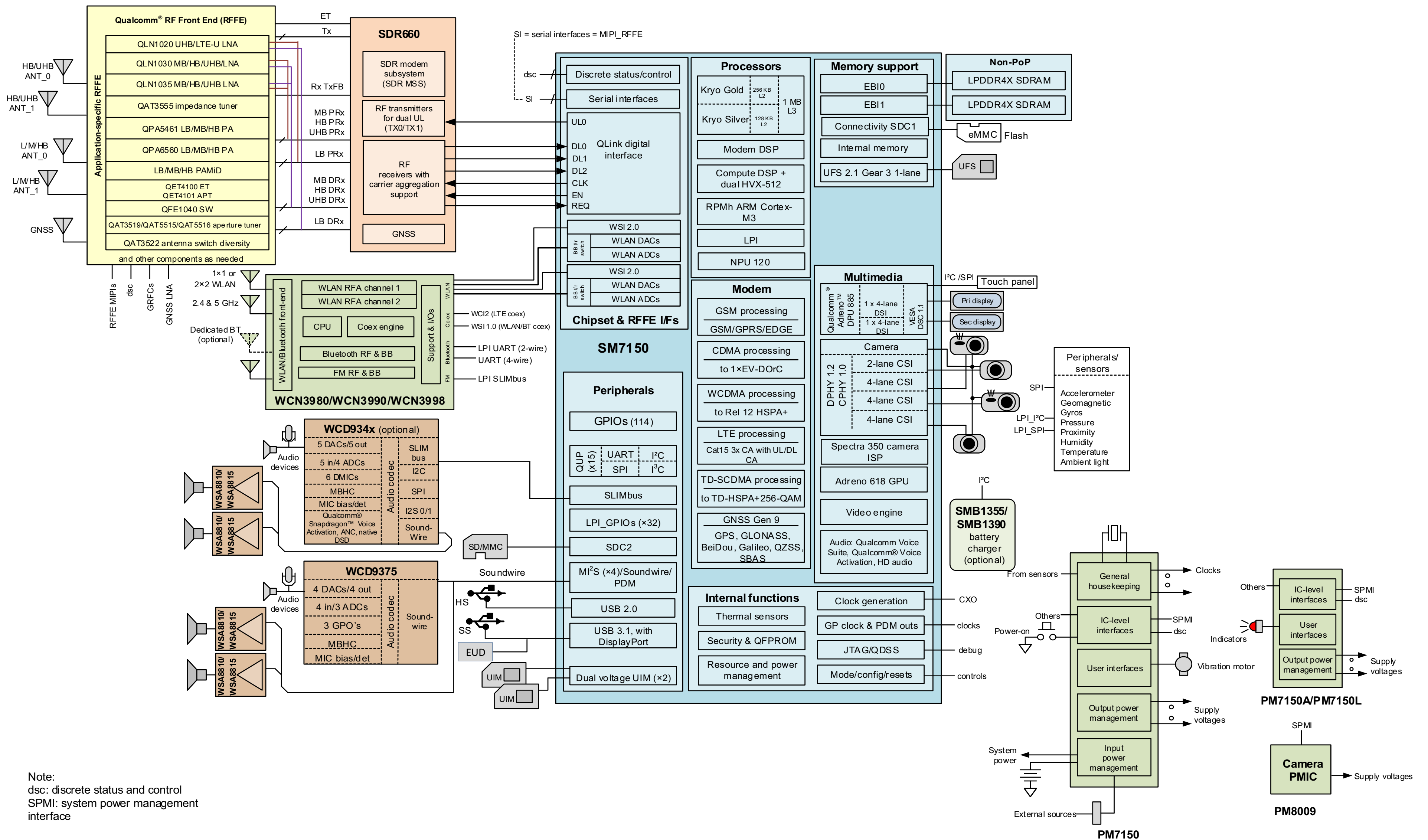

Figure 1-1 SM7150 functional block diagram and example application

1.2 SM7150 features

NOTE: Some of the hardware features integrated within the SM7150 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM7150 features.

Table 1-1 SM7150 features

Feature	SM7150 capability
Processors	
Applications	64-bit applications processor (Kryo 470) with 1 MB L3 cache ■ Dual high-performance Kryo cores 2.208 GHz – Gold cluster with 256 KB L2 cache per core ■ Hexa low-power Kryo cores 1.804 GHz – Silver cluster with 128 KB L2 cache per core
Digital signal processing	Compute DSP with Hexagon Vector eXtensions (dual-HVX512)
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Low-power island	Low-power island with Hexagon DSP consists of Snapdragon sensor core and low-power audio subsystem
Memory support	
System memory via EBI	Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM designed for a 1866 MHz clock (2 × 16 bit) 512 KB system cache
Other internal memory	256 KB IMEM 512 KB GMEM for graphics
External memory	
Via	■ UFS 2.1 gear 3 (one-lane), eMMC 5.1, and SD 3.0 ■ Simultaneous access to UFS + eMMC memory for storage expansion
RF support	
RF operating bands	Defined by the RF transceiver SDR device
Air interfaces	See Table 1-2 for variant support.
GSM	Yes
CDMA	Yes
WCDMA	Yes
TD-SCDMA	Yes
LTE	Yes (Cat15 3 × 20 CA at 800 Mbps DL and 150 Mbps UL capability)
WLAN/Bluetooth	Yes (with WCN3998/WCN3990/WCN3980)
Advanced techniques	Up to 3DLCA, up to 2ULCA, 4 × 4 MIMO using single TRx, LTE-U, and LAA
Antenna sharing	Antenna shared between Wi-Fi and WAN

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Table 1-1 SM7150 features (cont.)

Feature	SM7150 capability
GNSS – Integrated Qualcomm® Location Suite engine	Gen 9; GPS, GLONASS, BeiDou, Galileo, QZSS, and SBAS
Multimedia	
Display support	
MIPI-DSI	Two 4-lane; DSI D-PHY 1.2 or C-PHY 1.0; VESA DSC 1.1
DisplayPort	DisplayPort 1.4+ data concurrency over USB
Miracast	Yes; v2.0 (4k at 30 fps)
Example combinations	■ QHD+ + 4K30 DisplayPort 10-bit or 4K30 Miracast ■ ADv4, 10-layer, HDR10 ■ VESA DSC 1.1
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, and OLED panels
Camera interfaces	2x ISP 14 bit + 1x Lite ISP: 20 + 20 + 2 MP, and 32 MP 30 fps Supports high frame rate slow-motion capture: High speed video capture up to 960fps using 4x frame up-conversion (FRC) HEIF still picture playback and capture
MIPI-CSI	MIPI combination D-PHY 1.2/C-PHY 1.0 configurable in either 4/4/4/2 ■ D-PHY: 2.5 Gbps/lane ■ C-PHY: ~17 Gbps (5.71 Gbps/trio on 3 trios per port)
Performance	■ Real-time sensor input resolution: 20 + 20 + 2 MP ■ 32 MP 30 ZSL with a dual ISP
ImMotion	Create cinemagraphs (still picture with minor and repetitive motion)
Mobile display processor	Adreno DPU 885
Video applications performance	
Encode	4K30 8-bit: H.264, VP8 4K30 10-bit: H.265
Decode	4K30 8-bit: VP8 4K30 8-bit: H.264 4K30 10-bit: H.265, VP9
Concurrency	4K30 playback + 1080p30 encode
HFR capture	720p 240 or 1080p 120
HDR playback	HLG, HDR10, HDR10+ with H.265 main 10, HLG, PQ with VP9 profile 2
HDR capture	HLG and HDR10 with H.265 main 10
Graphics	■ Adreno 618, 3D graphics accelerator with 64-bit addressing ■ OpenGL ES 3.2, Vulkan, DX12.2 ■ OpenCL 2.0, DirectCompute

Table 1-1 SM7150 features (cont.)

Feature	SM7150 capability
Audio Option 1: WCD9375 codec + WSA8810/WSA8815 speaker amplifier Option 2: WCD9340 codec + WSA8810/WSA8815 speaker amplifier Option 3: WCD9341 codec + WSA8810/WSA8815 speaker amplifier	
Low-power audio	Low power; 7.1 surround sound
Voice codec support	EVRC, EVRC-B, and EVRC-WB G.711 and G.729A/AB GSM-FR, GSM-EFR, and GSM-HR AMR-NB, AMR-WB, AMR-eAMR, and AMR-BeAMR
Audio codec support	MP3; AAC; HE AAC v1, v2; WMA 9/Pro; Dolby AC-3, eAC-3, DTS-HD, FLAC, APE, ALAC, and AIFF
Enhanced audio	■ Surround sound: Dolby Digital, Dolby Atmos, and DTS-HD ■ Qualcomm® Audio Post-processing ■ Qualcomm Noise and Echo Cancellation v7 and Qualcomm Voice Suite v3 ■ WSA8810/WSA8815 speaker protection
Connectivity	
Qualcomm universal peripheral (QUP) ports	15 QUP ports, multiplexed serial interface functions (9 ports on GPIO and 6 ports on LPI GPIO)
UART	UART interface; eight on GPIO and two on LPI for sensors
I2C	I2C interface; nine on GPIO and two on LPI for touch, sensors, and NFC, dedicated controller for each port
I3C	I3C interface; three on GPIO and two on LPI
SPI	SPI interfaces; six on GPIO and two on LPI for cameras, sensors, and so on; dedicated controller for each port
CCI I2C	Three dedicated I2C interfaces for camera
UIM	Two – dual voltages (1.8 V and 2.95 V)
USB	USB 3.1, which can support Type-C with DisplayPort
Secure digital interfaces	■ 8-bit port SDC1 and 4-bit port SDC2; eMMC5.1 and SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card; UFS
Audio interfaces	
SLIMbus	Two port SLIMbus interface
MI2S	Four ports
SWR	SoundWire interface to WSA8810/WSA8815
Wireless connectivity	WCN3990/WCN3998 2 × 2 802.11ac RF WCN3980 1 × 1 802.11ac RF
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
Configurable GPIOs	
Number of GPIO ports	114
Input configurations	Pull-up, pull-down, keeper, or no pull

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Table 1-1 SM7150 features (cont.)

Feature	SM7150 capability
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security General hardware security features Crypto engines TrustZone services DRM support in hardware	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment, hardware supported KeyStore Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), inline crypto engine (FIPS-compliant) Secure file system, fast trusted storage PlayReady SL2000/SL3000, Widevine level 1, ISDB-T, and CPZ for GPU and DSP
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, QDSS, embedded USB debug (EUD), and ETM
Others	Thermal sensors, modes and resets, and peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
SDR RF transceivers QLink digital interface	■ Three downlink lanes and one uplink lane ■ Improved layout, routing, package, and signal integrity
Power management	PM7150 ■ Integrated switching charger with Qualcomm® Quick Charge™ technology 4.0 support ■ Five switching regulators and 19 LDOs PM7150A/PM7150L ■ Eight switching regulators and 11 LDOs PM8009 ■ Dedicated camera PMIC ■ Two switching regulators and 7 LDOs
Wireless connectivity WLAN baseband data Bluetooth	I/Q differential pair interface UART interface
Fabrication technology and package	
Digital die	8 nm process for lower active power dissipation
Non-PoP – small, thermally efficient package	PSP792: 11.10 × 10.5 × 0.99 mm; 0.35 mm pitch

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1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
LTE	
Category	15
Carrier aggregation	FDD and TDD; up to 60 MHz CA is not symmetric uplink and downlink; it is 60 MHz down and 40 MHz up.
CA direction	Uplink and downlink
Other LTE support	■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ Four-way Rx diversity ■ 4 × 4 MIMO using single TRx, LTE-U, and LAA
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1xSLTE and 1xSRLTE ■ hVoLTE and hSRLTE
Multi-SIM	
3G	3G + GSM DSDS
4G	4G + GSM DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite with global navigation satellite system (GNSS) support	
Gen 9	GPS, GLONASS, BeiDou, Galileo, QZSS, and SBAS

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN3980	802.11ac, 1 × 1 MIMO
With WCN3990	802.11ac, 2 × 2 MIMO

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Table 1-4 Wireless connectivity summary by standard (cont.)

Standard	Feature descriptions
With WCN3998	802.11ac, 2 × 2 MIMO (802.11ax Ready)
Bluetooth	
With WCN3980	Bluetooth 5.0
With WCN3990	Bluetooth 5.0
With WCN3998	Bluetooth 5.1
FM	
With WCN3980	Rx, RDS, RBDS
With WCN3990	Rx, RDS, RBDS
With WCN3998	Rx, RDS, RBDS

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2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
P2	Pad group 2 (SDC2); 1.8 V or 2.95 V
P3	Pad group 3 (most peripherals); 1.8 V
P5	Pad group 5 (UIM1); 1.8 V or 2.95 V
P6	Pad group 6 (UIM2); 1.8 V or 2.95 V
P7	Pad group 7 (eMMC); tied to VDD_P7 pins (1.8 V only)
P10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
P11	Pad group 11 (CXO); 1.8 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SM7150 is available in the PSP792. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

The text within Figure 2-1 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.
- Download the *SM7150 Pin Assignment and GPIO Configuration Spreadsheet* (80-PG319-1A) – this Microsoft Excel spreadsheet lists all SM7150 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PG319-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PG319-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

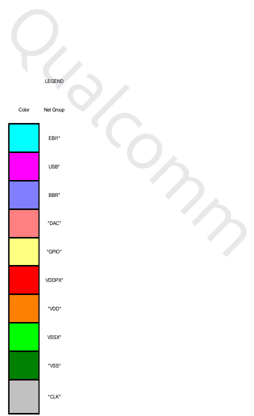

Figure 2-1 SM7150 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AR35	CXO		P11	AI	Core crystal oscillator (digital 19.2 MHz system clock)
AF6	CSI0_NC_CLK_P	DNC	CSI	AI	CSI 0, differential clock – positive
AE5	CSI0_A0_CLK_M	CSI0_TLN0_A	CSI	AI, AO	CSI 0, differential clock – negative
AE7	CSI0_B0_LN0_P	CSI0_TLN0_B	CSI	AI	CSI 0, differential lane 0 – positive
AD6	CSI0_C0_LN0_M	CSI0_TLN0_C	CSI	AI, AO	CSI 0, differential lane 0 – negative
AC5	CSI0_A1_LN1_P	CSI0_TLN1_A	CSI	AI, AO	CSI 0, differential lane 1 – positive
AB4	CSI0_B1_LN1_M	CSI0_TLN1_B	CSI	AI, AO	CSI 0, differential lane 1 – negative
AB6	CSI0_C1_LN2_P	CSI0_TLN1_C	CSI	AI, AO	CSI 0, differential lane 2 – positive
AA5	CSI0_A2_LN2_M	CSI0_TLN2_A	CSI	AI, AO	CSI 0, differential lane 2 – negative
AA7	CSI0_B2_LN3_P	CSI0_TLN2_B	CSI	AI, AO	CSI 0, differential lane 3 – positive
Y6	CSI0_C2_LN3_M	CSI0_TLN2_C	CSI	AI, AO	CSI 0, differential lane 3 – negative
AN5	CSI1_C2_LN3_M	CSI1_TLN2_C	CSI	AI, AO	CSI 1, differential lane 3 – negative
AM4	CSI1_B2_LN3_P	CSI1_TLN0_A	CSI	AI, AO	CSI 1, differential lane 3 – positive
AM6	CSI1_A2_LN2_M	CSI1_TLN2_A	CSI	AI, AO	CSI 1, differential lane 2 – negative
AL5	CSI1_C1_LN2_P	CSI1_TLN1_C	CSI	AI, AO	CSI 1, differential lane 2 – positive
AL7	CSI1_B1_LN1_M	CSI1_TLN1_B	CSI	AI, AO	CSI 1, differential lane 1 – negative
AK6	CSI1_A1_LN1_P	CSI1_TLN1_A	CSI	AI, AO	CSI 1, differential lane 1 – positive
AJ5	CSI1_C0_LN0_M	CSI1_TLN0_C	CSI	AI, AO	CSI 1, differential lane 0 – negative
AH4	CSI1_B0_LN0_P	CSI1_TLN2_A	CSI	AI, AO	CSI 1, differential lane 0 – positive
AH6	CSI1_A0_CLK_M	CSI1_TLN0_A	CSI	AI	CSI 1, differential clock – negative
AG5	CSI1_NC_CLK_P	CSI1_TLN2_C	CSI	AI	CSI 1, differential clock – negative
AK4	CSI2_B1_LN1_M	CSI2_TLN1_B	CSI	AI, AO	CSI 2, differential lane 1– negative
AL1	CSI2_B2_LN3_P	CSI2_TLN2_B	CSI	AI, AO	CSI 2, differential lane 3 – positive
AJ3	CSI2_A1_LN1_P	CSI2_TLN1_A	CSI	AI, AO	CSI 2, differential lane 1 – positive
AF2	CSI2_NC_CLK_P	DNC	CSI	AI	CSI 2, differential clock – positive
AG3	CSI2_A0_CLK_M	CSI2_TLN0_A	CSI	AI	CSI 2, differential clock – negative
AG1	CSI2_B0_LN0_P	CSI2_TLN0_B	CSI	AI, AO	CSI 2, differential lane 0 – positive
AH2	CSI2_C0_LN0_M	CSI2_TLN0_C	CSI	AI, AO	CSI 2, differential lane 0 – negative
AK2	CSI2_C1_LN2_P	CSI2_TLN1_C	CSI	AI, AO	CSI 2, differential lane 2 – positive
AL3	CSI2_A2_LN2_M	CSI2_TLN2_A	CSI	AI, AO	CSI 2, differential lane 2 – negative
AM2	CSI2_C2_LN3_M	CSI2_TLN2_C	CSI	AI, AO	CSI 2, differential lane 3 – negative
AB2	CSI3_B1_LN1_M	DNC	CSI	AI, AO	CSI 3, differential lane 1 – negative
AC3	CSI3_C0_LN0_M	DNC	CSI	AI, AO	CSI 3, differential lane 0 – negative
AC1	CSI3_A1_LN1_P	DNC	CSI	AI, AO	CSI 3, differential lane 1 – positive
AD2	CSI3_B0_LN0_P	DNC	CSI	AI, AO	CSI 3, differential lane 0 – positive
AE3	CSI3_NC_CLK_P	DNC	CSI	AI	CSI 3, differential clock – positive

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Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AD4	CSI3_A0_CLK_M	DNC	CSI	AI	CSI 3, differential clock – negative
C41	DDR_RESET_N		EBI	DO	LPDDR4X reset (shared by EBIs)
AH40	DP_AUX_M		–	AI, AO	DisplayPort auxiliary channel – negative
AG41	DP_AUX_P		–	AI, AO	DisplayPort auxiliary channel – positive
AD36	DSI0_A0_LN0_P		DSI	AO	DSI A0 lane 0 pair plus
AB36	DSI0_A1_LN1_M		DSI	AO	DSI A1 lane 1 pair minus
Y36	DSI0_A2_LN2_P		DSI	AO	DSI A2 lane 1 pair plus
AC37	DSI0_B0_LN0_M		DSI	AO	DSI B0 lane 0 pair plus
AA37	DSI0_B1_CLK_P		DSI	AO	DSI B1 clock plus
W37	DSI0_B2_LN2_M		DSI	AO	DSI B2 lane 2 pair minus
AC35	DSI0_C0_LN1_P		DSI	AO	DSI C0 lane 1 pair plus
Y38	DSI0_C1_CLK_M		DSI	AO	DSI C1 clock minus
W35	DSI0_C2_LN3_P		DSI	AO	DSI C2 lane 3 pair plus
V36	DSI0_NC_LN3_M		DSI	AO	DSI NC lane 3 minus
AG39	DSI1_A0_LN0_P		DSI	AO	DSI A0 lane 0 pair plus
AE39	DSI1_A1_LN1_M		DSI	AO	DSI A1 lane 1 pair minus
AC39	DSI1_A2_LN2_P		DSI	AO	DSI A2 lane 2 pair plus
AF40	DSI1_B0_LN0_M		DSI	AO	DSI B0 lane 0 pair minus
AD40	DSI1_B1_CLK_P		DSI	AO	DSI B1 clock plus
AB40	DSI1_B2_LN2_M		DSI	AO	DSI B2 lane 2 pair minus
AF38	DSI1_C0_LN1_P		DSI	AO	DSI C0 lane 1 pair plus
AC41	DSI1_C1_CLK_M		DSI	AO	DSI C1 clock minus
AB38	DSI1_C2_LN3_P		DSI	AO	DSI C2 lane 3 pair plus
AA39	DSI1_NC_LN3_M		DSI	AO	DSI NC lane 3 pair minus
C1	EBI_CAL		–	AI	EBI0 LPDDR4X calibration resistor
D14	EBI0_CA_0		EBI	DO	EBI0 LPDDR4X command/address bit 0
F12	EBI0_CA_1		EBI	DO	EBI0 LPDDR4X command/address bit 1
E7	EBI0_CA_2		EBI	DO	EBI0 LPDDR4X command/address bit 2
D10	EBI0_CA_3		EBI	DO	EBI0 LPDDR4X command/address bit 3
E11	EBI0_CA_4		EBI	DO	EBI0 LPDDR4X command/address bit 4
D6	EBI0_CA_5		EBI	DO	EBI0 LPDDR4X command/address bit 5
E15	EBI0_CK_C		EBI	DO	EBI0 LPDDR4X differential clock - negative
F16	EBI0_CK_T		EBI	DO	EBI0 LPDDR4X differential clock - positive
F8	EBI0_CKE_0		EBI	DO	EBI0 LPDDR4X clock enable 0
E13	EBI0_CKE_1		EBI	DO	EBI0 LPDDR4X clock enable 1
F10	EBI0_CS_0		EBI	DO	EBI0 LPDDR4X chip select 0
D12	EBI0_CS_1		EBI	DO	EBI0 LPDDR4X chip select 1
B8	EBI0_DM_0		EBI	DO	EBI0 LPDDR4X data mask for byte 0
B14	EBI0_DM_1		EBI	DO	EBI0 LPDDR4X data mask for byte 1
B2	EBI0_DQ_0		EBI	B	EBI0 LPDDR4X data bit 0

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Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
A3	EBI0_DQ_1		EBI	B	EBI0 LPDDR4X data bit 1
A5	EBI0_DQ_2		EBI	B	EBI0 LPDDR4X data bit 2
A7	EBI0_DQ_3		EBI	B	EBI0 LPDDR4X data bit 3
B4	EBI0_DQ_4		EBI	B	EBI0 LPDDR4X data bit 4
B6	EBI0_DQ_5		EBI	B	EBI0 LPDDR4X data bit 5
A9	EBI0_DQ_6		EBI	B	EBI0 LPDDR4X data bit 6
B10	EBI0_DQ_7		EBI	B	EBI0 LPDDR4X data bit 7
A17	EBI0_DQ_8		EBI	B	EBI0 LPDDR4X data bit 8
A19	EBI0_DQ_9		EBI	B	EBI0 LPDDR4X data bit 9
B18	EBI0_DQ_10		EBI	B	EBI0 LPDDR4X data bit 10
B16	EBI0_DQ_11		EBI	B	EBI0 LPDDR4X data bit 11
A15	EBI0_DQ_12		EBI	B	EBI0 LPDDR4X data bit 12
B12	EBI0_DQ_13		EBI	B	EBI0 LPDDR4X data bit 13
A13	EBI0_DQ_14		EBI	B	EBI0 LPDDR4X data bit 14
A11	EBI0_DQ_15		EBI	B	EBI0 LPDDR4X data bit 15
E9	EBI0_DQS_C_0		EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 – negative
D16	EBI0_DQS_C_1		EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 – negative
D8	EBI0_DQS_T_0		EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 – positive
E17	EBI0_DQS_T_1		EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 – positive
D30	EBI1_CA_0		EBI	DO	EBI1 LPDDR4X command/address bit 0
F32	EBI1_CA_1		EBI	DO	EBI1 LPDDR4X command/address bit 1
E37	EBI1_CA_2		EBI	DO	EBI1 LPDDR4X command/address bit 2
D34	EBI1_CA_3		EBI	DO	EBI1 LPDDR4X command/address bit 3
E33	EBI1_CA_4		EBI	DO	EBI1 LPDDR4X command/address bit 4
D38	EBI1_CA_5		EBI	DO	EBI1 LPDDR4X command/address bit 5
E29	EBI1_CK_C		EBI	DO	EBI1 LPDDR4X differential clock – negative
F28	EBI1_CK_T		EBI	DO	EBI1 LPDDR4X differential clock – positive
F36	EBI1_CKE_0		EBI	DO	EBI1 LPDDR4X clock enable 0
E31	EBI1_CKE_1		EBI	DO	EBI1 LPDDR4X clock enable 1
F34	EBI1_CS_0		EBI	DO	EBI1 LPDDR4X chip select 0
D32	EBI1_CS_1		EBI	DO	EBI1 LPDDR4X chip select 1
B40	EBI1_DQ_0		EBI	B	EBI1 LPDDR4X data bit 0
A39	EBI1_DQ_1		EBI	B	EBI1 LPDDR4X data bit 1
A37	EBI1_DQ_2		EBI	B	EBI1 LPDDR4X data bit 2
A35	EBI1_DQ_3		EBI	B	EBI1 LPDDR4X data bit 3
B38	EBI1_DQ_4		EBI	B	EBI1 LPDDR4X data bit 4
B36	EBI1_DQ_5		EBI	B	EBI1 LPDDR4X data bit 5
A33	EBI1_DQ_6		EBI	B	EBI1 LPDDR4X data bit 6
B32	EBI1_DQ_7		EBI	B	EBI1 LPDDR4X data bit 7
A25	EBI1_DQ_8		EBI	B	EBI1 LPDDR4X data bit 8

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Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
A23	EBI1_DQ_9		EBI	B	EBI1 LPDDR4X data bit 9
B24	EBI1_DQ_10		EBI	B	EBI1 LPDDR4X data bit 10
B26	EBI1_DQ_11		EBI	B	EBI1 LPDDR4X data bit 11
A27	EBI1_DQ_12			B	EBI1 LPDDR4X data bit 12
B30	EBI1_DQ_13		EBI	B	EBI1 LPDDR4X data bit 13
A29	EBI1_DQ_14		EBI	B	EBI1 LPDDR4X data bit 14
A31	EBI1_DQ_15		EBI	B	EBI1 LPDDR4X data bit 15
B34	EBI1_DMI_0		EBI	B	EBI1 LPDDR4X data mask for byte 0
B28	EBI1_DMI_1		EBI	B	EBI1 LPDDR4X data mask for byte 1
E35	EBI1_DQS_C_0		EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 – negative
D28	EBI1_DQS_C_1		EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 – negative
D36	EBI1_DQS_T_0		EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 – positive
E27	EBI1_DQS_T_1		EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 – positive
R35	FORCE_USB_ BOOT_POLARITY_ SEL		P3	PD: nppukp	FORCE_USB_BOOT polarity selection, left unconnected for active high FORCE_USB_BOOT, connect to 1.8 V for active low FORCE_USB_BOOT.
AM36	MODE_0		P3	DIS-PD:nppukp	Mode control bit 0 – unconnected for native mode
AL37	MODE_1		P3	DIS-PD:nppukp	Mode control bit 1 – unconnected for native mode
AY24	PMIC_SPMI_CLK		–	AO	Slave and PBUS interface for PMICs – clock
BA25	PMIC_SPMI_DATA		–	B	Slave and PBUS interface for PMICs – data
BA27	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
BA33	QLINK_CLK_M		–	AO	QLink clock – negative
AY32	QLINK_CLK_P		–	AO	QLink clock – positive
BB32	QLINK_DL0_M		–	AI	QLink downlink lane 0 – negative
BA31	QLINK_DL0_P		–	AI	QLink downlink lane 0 – positive
BC31	QLINK_DL1_M		–	AI	QLink downlink lane 1 – negative
BB30	QLINK_DL1_P		–	AI	QLink downlink lane 1 – positive
BB28	QLINK_DL2_M		–	AI	QLink downlink lane 2 – negative
BA29	QLINK_DL2_P		–	AI	QLink downlink lane 2 – positive
BB34	QLINK_UL0_M		–	AO	QLink uplink lane 1 – negative
BC35	QLINK_UL0_P		–	AO	QLink uplink lane 1 – positive
AU41	QREFS_CXO_REXT		–	AI, AO	External resistor for on-die clocking
AV40	REFGEN_REXT0		–	AI	East-side high-speed interface – external resistor
W1	REFGEN_REXT1		–	AI	West-side high-speed interface – external resistor
AY26	RESIN_N		P3	DI	Reset input
B22	RESOUT_N		P3	DO	Reset output
V6	RF_XO_CLK		P3	DI	WLAN reference clock
A21	SDC1_CLK		P7	B-NP: pdpukp	Secure digital controller 1 clock

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Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
B20	SDC1_CMD		P7	B-PD: nppukp	Secure digital controller 1 command
D26	SDC1_DATA_0		P7	B-PD: nppukp	Secure digital controller 1 data bit 0
D20	SDC1_DATA_1		P7	B-PD: nppukp	Secure digital controller 1 data bit 1
D24	SDC1_DATA_2		P7	B-PD: nppukp	Secure digital controller 1 data bit 2
F26	SDC1_DATA_3		P7	B-PD: nppukp	Secure digital controller 1 data bit 3
D22	SDC1_DATA_4		P7	B-PD: nppukp	Secure digital controller 1 data bit 4
E23	SDC1_DATA_5		P7	B-PD: nppukp	Secure digital controller 1 data bit 5
D18	SDC1_DATA_6		P7	B-PD: nppukp	Secure digital controller 1 data bit 6
F18	SDC1_DATA_7		P7	B-PD: nppukp	Secure digital controller 1 data bit 7
C21	SDC1_RCLK		P7	DI-PD: pdpukp	Secure digital controller 1 return clock
BA3	SDC2_CLK		P2	BH-NP: dpukp	Secure digital controller 2 clock
AY2	SDC2_CMD		P2	BH-PD: nppukp	Secure digital controller 2 command
BA1	SDC2_DATA_0		P2	BH-NP: nppukp	Secure digital controller 2 data bit 0
BB2	SDC2_DATA_1		P2	BH-PD: nppukp	Secure digital controller 2 data bit 1
AW3	SDC2_DATA_2		P2	BH-NP: nppukp	Secure digital controller 2 data bit 2
AY4	SDC2_DATA_3		P2	BH-PD: nppukp	Secure digital controller 2 data bit 3
BB26	SLEEP_CLK		P3	DI	Sleep clock
J39	SRST_N		P3	DI-PU	JTAG reset for debug
G39	TCK		P3	DI-PU	JTAG clock input
F40	TDI		P3	DI-PU:nppdkp	JTAG data input
G41	TDO		P3	DO-Z	JTAG data output
H40	TMS		P3	DI-PU:nppdkp	JTAG mode select input
H38	TRST_N		P3	DI-PD:nppukp	JTAG reset
E19	UFS_RESET_N		P10	DO-Z-PD: nppukp	UFS reset
E25	UFS_L0_RXM		P10	AI	UFS receive lane 0 – negative
F24	UFS_L0_RXP		P10	AI	UFS receive lane 0 – positive
F20	UFS_L0_TXM		P10	AO	UFS transmit lane 0 – negative
E21	UFS_L0_TXP		P10	AO	UFS transmit lane 0 – positive

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Table 2-2 Pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
G23	UFS_REFCLK		P10	DO-Z-PD: nppukp	UFS reference clock
AJ37	USB_HS_DM		–	AI, AO	USB high-speed data – negative
AK36	USB_HS_DP		–	AI, AO	USB high-speed data – positive
AP40	USB_SS_RX0_M		–	AI	USB super-speed receive 0 – negative
AR39	USB_SS_RX0_P		–	AI	USB super-speed receive 0 – positive
AK38	USB_SS_RX1_M		–	AI	USB super-speed receive 1 – negative
AJ39	USB_SS_RX1_P		–	AI	USB super-speed receive 1 – positive
AN39	USB_SS_TX0_M		–	AI	USB super-speed transmit 0 – negative
AP38	USB_SS_TX0_P		–	AI	USB super-speed transmit 0 – positive
AL39	USB_SS_TX1_M		–	AI	USB super-speed transmit 1 – negative
AK40	USB_SS_TX1_P		–	AI	USB super-speed transmit 1 – positive
R5	WCSS_CXM_CLK		P3	DO	WLAN coexistence module command clock (WSI 1.0)
P6	WCSS_CXM_DATA		P3	B	WLAN coexistence module command data (WSI 1.0)
U5	WCSS0_BBD_CLK		P3	DO	WLAN chain 1 baseband command clock (WSI 2.0)
U7	WCSS0_BBD_DATA		P3	B	WLAN chain 1 baseband command data (WSI 2.0)
R7	WCSS1_BBD_CLK		P3	DO	WLAN chain 2 baseband command clock (WSI 2.0)
T6	WCSS1_BBD_DATA		P3	B	WLAN chain 2 baseband command data (WSI 2.0)
L3	WLAN_PWR_EN		P3	DO	WLAN power enable
J7	WLAN0_ADC_I_M		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase negative
H6	WLAN0_ADC_I_P		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase positive
K6	WLAN0_ADC_Q_M		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature negative
J5	WLAN0_ADC_Q_P		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature positive
L1	WLAN1_DAC_REXT		–	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
F2	WLAN1_ADC_I_M		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase negative
G3	WLAN1_ADC_I_P		–	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase positive
H2	WLAN1_ADC_Q_M		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature negative
G1	WLAN1_ADC_Q_P		–	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature positive
K2	WLAN0_DAC_REXT		–	AI, AO	WLAN chain 2 digital-to-analog converter external resistor

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

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NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM7150 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the *SM7150 Pin Assignment and GPIO Configuration Spreadsheet* (80-PG319-1A). Make this document a favorite to be notified of any changes.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PG319-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AY36	GPIO_113	Y	 RFFE1_CLK QUP1_L3[4]	P3	B-PD:nppukp DO DI DO	Configurable I/O RF front-end 1 interface clock QUP 1 SE4, lane 3: UART_RX QUP 1 SE4, lane 3: SPI_CS0
BA37	GPIO_112	–	 RFFE1_DATA QUP1_L2[4] BOOT_CONFIG[10]	P3	B-PD:nppukp DO DO B DI	Configurable I/O RF front-end 1 interface data QUP 1 SE4, lane 2: UART_TX QUP 1 SE4, lane 2: SPI_SCLK Boot configuration control bit 10
BB38	GPIO_111	–	 RFFE2_CLK GRFC33 QUP1_L1[4]	P3	B-PD:nppukp DO DO DO B DI	Configurable I/O RF front-end 2 interface clock Generic RF controller bit 33 QUP 1 SE4, lane 1: UART_RFR QUP 1 SE4, lane 1: I2C_SCL QUP 1 SE4, lane 1: SPI_MOSI

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BC39	GPIO_110	Y	 RFFE2_DATA GRFC34 QUP1_L0[4] BOOT_CONFIG[11]	P3	B-PD:nppukp DO DO DI B DI DI	Configurable I/O RF front-end 2 interface data Generic RF controller bit 34 QUP 1 SE4, lane 0: UART_CTS QUP 1 SE4, lane 0: I2C_SDA QUP 1 SE4, lane 0: SPI_MISO Boot configuration control bit 11
R3	GPIO_109	Y	 MSS_LTE_COXM_RXD GPS_TX_AGGRESSOR_A BOOT_CONFIG[14]	P3	B-PD:nppukp DI DI DI	Configurable I/O UART Rx for LTE coex Tx level may degrade GNSS receiver (A) Boot configuration control bit 14
P2	GPIO_108	–	 MSS_LTE_COXM_TXD BOOT_CONFIG[3]	P3	B-PD:nppukp DO DI	Configurable I/O UART Tx for LTE coex Boot configuration control bit 3
AW35	GPIO_107	–	 GRFC5 GPS_TX_AGGRESSOR_D	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 5 Tx level may degrade GNSS receiver (A)
AY38	GPIO_106	–	 RFFE5_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 3 interface clock
AW37	GPIO_105	–	 RFFE5_DATA BOOT_CONFIG[12]	P3	B-PD:nppukp DO DI	Configurable I/O RF front-end 5 interface data Boot configuration control bit 12
AT38	GPIO_104	Y	 USB_PHY_PS QDSS_GPIO_TRACECTL_ LOCA	P3	B-PD:nppukp DI DO	Configurable I/O USB PHY port select QDSS trace data A
BA41	GPIO_103	–	 RFFE4_DATA QUP1_L2[5] BOOT_CONFIG[9]	P3	B-PD:nppukp DO DO DO DI	Configurable I/O RF front-end 4 interface data QUP 1 SE5, lane 2: UART_TX QUP 1 SE5, lane 2: SPI_SCLK Boot configuration control bit 9
BB40	GPIO_102	–	 RFFE3_CLK GRFC32 QUP1_L1[5]	P3	B-PD:nppukp DO DO DO B DO	Configurable I/O RF front-end 6 interface clock Generic RF controller bit 32 QUP 1 SE5, lane 1: UART_RFR QUP 1 SE5, lane 1: I2C_SCL QUP 1 SE5, lane 1: SPI_MOSI
BA39	GPIO_101	Y	 RFFE3_DATA GRFC35 QUP1_L0[5] BOOT_CONFIG[8]	P3	B-PD:nppukp DO DO DI B DI DI	Configurable I/O RF front-end 3 interface data Generic RF controller bit 35 QUP 1 SE5, lane 0: UART_CTS QUP 1 SE5, lane 0: I2C_SDA QUP 1 SE5, lane 0: SPI_MISO Boot configuration control bit 8
AR37	GPIO_100	–	 GRFC1 BOOT_CONFIG(13)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 1 Boot configuration control bit 13
BB36	GPIO_99	–	 GRFC0 PA_INDICATOR_1_OR_2 BOOT_CONFIG(5)	P3	B-PD:nppukp DO DO DI	Configurable I/O Generic RF controller bit 0 PA transmit indicator Boot configuration control bit 5
BA35	GPIO_98	Y	 GRFC2 BOOT_CONFIG(4)	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 2 Boot configuration control bit 4
AY34	GPIO_97	–	 QLINK_ENABLE	P3	B-PD:nppukp DO	Configurable I/O QLink enable
AW33	GPIO_96	Y	 QLINK_REQUEST	P3	B-PD:nppukp DI	Configurable I/O QLink request

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AT36	GPIO_95	Y	 GRFC3 BOOT_CONFIG[6]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 3 Boot configuration control bit 6
T4	GPIO_94	Y	–	P3	B-PD:nppukp	Configurable I/O
N35	GPIO_93	Y	 QDSS_GPIO_TRACEDATA_LOCA	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data A
AY40	GPIO_92	Y	 RFFE4_CLK GRFC36 QUP1_L3(5)	P3	B-PD:nppukp DO DO DI DO	Configurable I/O RF front-end 4 interface clock Generic RF controller bit 36 QUP 1 SE5, lane 3: UART_RX QUP 1 SE5, lane 3: SPI_CS0
L35	GPIO_91	Y	 QDSS_GPIO_TRACEDATA_LOCA[5]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 5 A
J35	GPIO_90	Y	 QDSS_GPIO_TRACEDATA_LOCA[4]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 4 A
M36	GPIO_89	Y	 QDSS_GPIO_TRACEDATA_LOCA[3]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 3 A
L37	GPIO_88	Y	 QDSS_GPIO_TRACEDATA_LOCA[2]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 2 A
K36	GPIO_87	Y	 QDSS_GPIO_TRACEDATA_LOCA[1]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 1 A
K38	GPIO_86	Y	 QDSS_GPIO_TRACEDATA_LOCA[0]	P3	B-PD:nppukp DO	Configurable I/O QDSS trace data bit 0 A
AV36	GPIO_85	Y	 UIM_BATT_ALARM EDP_HOT_PLUG_DETECT BOOT_CONFIG[15]	P3	B-PD:nppukp DI DI DI	Configurable I/O UIM battery alarm Display port hot plug detection Boot configuration control bit 15
AU39	GPIO_84	Y	 GRFC9 GPS_TX_AGGRESSOR_B	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 9 Tx level may degrade GNSS receiver (B)
AT40	GPIO_83	–	 GRFC8 GPS_TX_AGGRESSOR_C	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 8 Tx level may degrade GNSS receiver (C)
BB8	GPIO_82	Y	 UIM1_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM1 presence detection
BC7	GPIO_81	–	 UIM1_RESET	P5	B-PD:nppukp DO	Configurable I/O UIM1 reset (dual voltage)
BA7	GPIO_80	–	 UIM1_CLK	P5	B-PD:nppukp DO	Configurable I/O UIM1 clock (dual voltage)
BB6	GPIO_79	–	 UIM1_DATA	P5	B-PD:nppukp B	Configurable I/O UIM1 data (dual voltage)
AY6	GPIO_78	Y	 UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 presence detection
BA5	GPIO_77	–	 UIM2_RESET	P6	B-PD:nppukp DO	Configurable I/O UIM2 reset (dual voltage)
BB4	GPIO_76	–	 UIM2_CLK	P6	B-PD:nppukp DO	Configurable I/O UIM2 clock (dual voltage)

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BC3	GPIO_75	–	UIM2_DATA	P6	B-PD:nppukp B	Configurable I/O UIM2 data (dual voltage)
AU37	GPIO_74	Y	GRFC4 BOOT_CONFIG[0]	P3	B-PD:nppukp DO DI	Configurable I/O Generic RF controller bit 4 Boot configuration control bit 0
AG35	GPIO_73	Y		P3	B-PD:nppukp	Configurable I/O
AF36	GPIO_72	–	BOOT_CONFIG[1]	P3	B-PD:nppukp DI	Configurable I/O Boot configuration control bit 1
AW39	GPIO_71	–	RFFE6_DATA MDP_VSYNC_S_B BOOT_CONFIG[7]	P3	B-PD:nppukp B DI DI	Configurable I/O RF front-end 6 interface data MDP vertical sync – secondary B Boot configuration control bit 7
AV38	GPIO_70	Y	RFFE6_CLK GRFC37 MDP_VSYNC_P_B	P3	B-PD:nppukp DO DO DI	Configurable I/O RF front-end 6 interface clock Generic RF controller bit 37 MDP vertical sync – primary B
W41	GPIO_69	Y		P3	B-PD:nppukp	Configurable I/O
Y40	GPIO_68	Y	GP_PDM_A[0]	P3	B-PD:nppukp DO	Configurable I/O General-purpose PDM output 0
W39	GPIO_67	Y		P3	B-PU:nppukp	Configurable I/O
V38	GPIO_66	Y		P3	B-PD:nppukp	Configurable I/O
V40	GPIO_65	Y	QUP1_L6[0]	P3	B-PD:nppukp DO	Configurable I/O QUP 1, lane 6: SPI_CS3
U39	GPIO_64	Y	QUP1_L5[0]	P3	B-PD:nppukp	Configurable I/O QUP 1, lane 5: SPI_CS2
T38	GPIO_63	–	QUP1_L4[0] MDP_VSYNC0_OUT MDP_VSYNC1_OUT MDP_VSYNC2_OUT MDP_VSYNC3_OUT QDSS_CTI_TRIG1_OUT_B[31]	P3	B-PD:nppukp DO DO DO DO DO DO	Configurable I/O QUP 1, lane 4: SPI_CS1 MDP vertical sync 0 MDP vertical sync 1 MDP vertical sync 2 MDP vertical sync 3 QDSS trigger output 1 B
T40	GPIO_62	Y	QUP1_L3[0]	P3	B-PD:nppukp DI DO	Configurable I/O QUP 1 SE0, lane 3: UART_RX QUP 1 SE0, lane 3: SPI_CS0
R39	GPIO_61	–	QUP1_L2[0]	P3	B-PD:nppukp DO DO	Configurable I/O QUP 1 SE0, lane 2: UART_TX QUP 1 SE0, lane 2: SPI_SCLK
R41	GPIO_60	–	QUP1_L1[0]	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 1 SE0, lane 1: UART_RFR QUP 1 SE0, lane 1: I2C_SCL QUP 1 SE0, lane 1: SPI_MOSI
P40	GPIO_59	Y	QUP1_L0[0]	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 1 SE0, lane 0: UART_CTS QUP 1 SE0, lane 0: I2C_SDA QUP 1 SE0, lane 0: SPI_MISO
AY8	GPIO_58	Y	QUA_MI2S_MCLK QUP0_L4[0]	P3	B-PD:nppukp DO DO	Configurable I/O MI2S 2 master clock QUP 0 SE0, lane 4: SPI_CS1

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AY10	GPIO_57	Y	 SEC_MI2S_MCLK QUP0_L5[0] GP_PDM_A[2] QDSS_GPIO_TRACEDATA_LOCA[11]	P3	B-PD:nppukp DO DO DO DO	Configurable I/O MI2S master clock QUP 0 SE0, lane 5: SPI_CS2 General-purpose PDM output 2 A Global general-purpose clock 1 A
AY12	GPIO_56	Y	 TER_MI2S_DATA1 QUP0_L3[4] GCC_GP1_CLK_B QDSS_GPIO_TRACEDATA_LOCA[13]	P3	B-PD:nppukp B DI DO DO DO	Configurable I/O Tertiary MI2S data 1 QUP 0 SE4, lane 3: UART_RX QUP 0 SE4, lane 3: SPI_CS0 Global general-purpose clock 1 B QDSS trace data bit 13 A
AW11	GPIO_55	Y	 TER_MI2S_DATA0 QUP0_L2[4] QDSS_GPIO_TRACEDATA_LOCA[10]	P3	B-PD:nppukp B DO B DO	Configurable I/O Tertiary MI2S data 0 QUP 0 SE4, lane 2: UART_TX QUP 0 SE4, lane 2: SPI_SCLK QDSS trace data bit 10 A
AV12	GPIO_54	–	 TER_MI2S_WS QUP0_L1[4] QDSS_GPIO_TRACEDATA_LOCA[9]	P3	B-PD:nppukp B DO B DO DO	Configurable I/O Tertiary MI2S word strobe QUP 0 SE4, lane 1: UART_RFR QUP 0 SE4, lane 1: I2C_SCL QUP 0 SE4, lane 1: SPI_MOSI QDSS trace data bit 9 A
AW13	GPIO_53	Y	 TER_MI2S_SCK QUP0_L0[4] QDSS_GPIO_TRACEDATA_LOCA[8]	P3	B-PD:nppukp B DI B DI DO	Configurable I/O Tertiary MI2S clock QUP 0 SE4, lane 0: UART_CTS QUP 0 SE4, lane 0: I2C_SDA QUP 0 SE4, lane 0: SPI_MISO QDSS trace data bit 8 A
BB12	GPIO_52	Y	 PRI_MI2S_DATA0 QUP0_L3[0]	P3	B-PD:nppukp B DI DO	Configurable I/O Primary MI2S data 0 QUP 0 SE0, lane 3: UART_RX QUP 0 SE0, lane 3: SPI_CS0
BA11	GPIO_51	–	 PRI_MI2S_DATA1 QUP0_L2[0]	P3	B-PD:nppukp B DO DO	Configurable I/O Primary MI2S data 1 QUP 0 SE0, lane 2: UART_TX QUP 0 SE0, lane 2: SPI_SCLK
BC11	GPIO_50	Y	 PRI_MI2S_WS QUP0_L1[0] GP_PDM_A[1] SWR_DATA	P3	B-PD:nppukp B DO B DO DO B	Configurable I/O Primary MI2S word strobe QUP 0 SE0, lane 1: UART_RFR QUP 0 SE0, lane 1: I2C_SCL QUP 0 SE0, lane 1: SPI_MOSI General-purpose PDM 1 A output SoundWire data
BB10	GPIO_49	Y	 PRI_MI2S_SCK QUP0_L0[0] SWR_CLK	P3	B-PD:nppukp B DI B DI DO	Configurable I/O Primary MI2S clock QUP 0 SE0, lane 0: UART_CTS QUP 0 SE0, lane 0: I2C_SDA QUP 0 SE0, lane 0: SPI_MISO SoundWire clock
BA9	GPIO_48	Y	 GCC_GP1_CLK_A FORCED_USB_BOOT	P3	B-PD:nppukp DO DI	Configurable I/O Global general-purpose clock 1 A Forced USB boot
AH36	GPIO_47	Y	 QUP1_L1(3)	P3	B-PD:nppukp B	Configurable I/O QUP 1 SE3, lane 1: I2C_SCL

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AG37	GPIO_46	–	 QUP1_L0(3)	P3	B-PD:nppukp B	Configurable I/O QUP 1 SE3, lane 0: I2C_SDA
L41	GPIO_45	Y	 QUP1_L3(2) QDSS_CTI_TRIG0_IN_A	P3	B-PD:nppukp DI DO	Configurable I/O QUP 1 SE2, lane 3: UART_RX QDSS trigger input 0 A
K40	GPIO_44	–	 QUP1_L2(2) QDSS_CTI_TRIG0_OUT_A	P3	B-PD:nppukp DO DO	Configurable I/O QUP 1 SE2, lane 2: UART_TX QDSS trigger output 0 A
M40	GPIO_43	Y	 QUP1_L1(2)	P3	B-PD:nppukp B	Configurable I/O QUP 1 SE2, lane 1: I2C_SCL
L39	GPIO_42	Y	 QUP1_L0(2)	P3	B-PD:nppukp B	Configurable I/O QUP 1 SE2, lane 0: I2C_SDA
P4	GPIO_41	Y	 QUP0_L3(3)	P3	B-PD:nppukp DI DI	Configurable I/O QUP 0 SE3, lane 3: UART_RX QUP 0 SE3, lane 3: SPI_CS0
N3	GPIO_40	–	 QUP0_L2(3)	P3	B-PU:nppukp DO B	Configurable I/O QUP 0 SE3, lane 2: UART_TX QUP 0 SE3, lane 2: SPI_SCLK
M2	GPIO_39	Y	 QUP0_L1[3]	P3	B-PD:nppukp DO B DO	Configurable I/O QUP 0 SE3, lane 1: UART_RFR QUP 0 SE3, lane 1: I2C_SCL QUP 0 SE3, lane 1: SPI_MOSI
M4	GPIO_38	Y	 QUP0_L0[3]	P3	B-PD:nppukp DI B DI	Configurable I/O QUP 0 SE3, lane 0: UART_CTS QUP 0 SE3, lane 0: I2C_SDA QUP 0 SE3, lane 0: SPI_MISO
V2	GPIO_37	Y	 QUP0_L5[1] GP_PDM_B[0]	P3	PD:nppukp DO	Configurable I/O QUP 0 SE1, lane 5: SPI_CS2 General-purpose PDM output 0 B
V4	GPIO_36	Y	 QDSS_GPIO_TRACEDATA_LOCA[14]	P3	PD:nppukp DO	Configurable I/O QDSS trace data bit 14 A
U3	GPIO_35	–	 QUP0_L1[2] QDSS_GPIO_TRACEDATA_LOCA[7]	P3	B-PD:nppukp B DO	Configurable I/O QUP 0 SE2, lane 1: I2C_SCL QDSS trace data bit 7 A
T2	GPIO_34	Y	 QUP0_L0[2] QDSS_GPIO_TRACEDATA_LOCA[6]	P3	B-PD:nppukp B DO	Configurable I/O QUP 0 SE2, lane 0: I2C_SDA QDSS trace data bit 6 A
U35	GPIO_33	Y	 SD_WRITE_PROTECT	P3	PD:nppukp DO	Configurable I/O SD card write protect
M38	GPIO_32	Y	 QDSS_CTI_TRIG1_IN_B	P3	PD:nppukp	Configurable I/O QDSS trigger input 1 B
AV34	GPIO_31	Y	 QDSS_GPIO_TRACEDATA_LOCA[12]	P3	PD:nppukp DO	Configurable I/O QDSS trace data bit 12 A

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AW7	GPIO_30	Y	 QDSS_GPIO_TRACECTL_LOCB	P3	B-PD:nppukp DO	Configurable I/O QDSS trace control B
N39	GPIO_29	–	 QDSS_GPIO_TRACEDATA_LOCB[15] BOOT_CONFIG[2]	P3	B-PD:nppukp DO DI	Configurable I/O QDSS trace data bit 15 B Boot configuration control bit 2
AV4	GPIO_28	–	 CCI_I2C_SCL2 QDSS_GPIO_TRACEDATA_LOCB[14]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 2 clock QDSS trace data bit 14 B
AV2	GPIO_27	–	 CCI_I2C_SDA2 QDSS_GPIO_TRACEDATA_LOCB[13]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 2 serial data QDSS trace data bit 13 B
AV6	GPIO_26	Y	 CCI_ASYNC_IN0 QDSS_GPIO_TRACEDATA_LOCB[12]	P3	B-PD:nppukp DI DO	Configurable I/O Camera control interface async 0 QDSS trace data bit 12 B
AW5	GPIO_25	–	 CCI_TIMER4 CCI_ASYNC_IN2 QDSS_TRACEDATA_11B	P3	B-PD:nppukp DO DI DO	Configurable I/O Camera control interface timer 4 Camera control interface async 2 QDSS trace data bit 11 B
AU5	GPIO_24	Y	 CCI_TIMER3 CCI_ASYNC_IN1 QDSS_GPIO_TRACEDATA_LOCB[10]	P3	B-PD:nppukp DO DI DO	Configurable I/O Camera control interface timer 3 Camera control interface async 1 QDSS trace data bit 10 B
AT6	GPIO_23	–	 CCI_TIMER2 QDSS_GPIO_TRACEDATA_LOCB[9]	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 2 QDSS trace data bit 9 B
AR5	GPIO_22	Y	 CCI_TIMER1 GCC_GP3_CLK_B QDSS_GPIO_TRACECLK_LOCB	P3	B-PD:nppukp DO DO DO	Configurable I/O Camera control interface timer 1 Global general-purpose clock 3 B QDSS trace clock B
AP6	GPIO_21	–	 CCI_TIMER0 GCC_GP2_CLK_B QDSS_GPIO_TRACEDATA_LOCB[8]	P3	B-PD:nppukp DO DO DO	Configurable I/O Camera control interface timer 0 Global general-purpose clock 2 B QDSS trace data bit 8 B
AU3	GPIO_20	–	 CCI_I2C_SCL1 QDSS_GPIO_TRACEDATA_LOCB[7]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 1 clock QDSS trace data bit 7 B
AT4	GPIO_19	–	 CCI_I2C_SDA1 QDSS_GPIO_TRACEDATA_LOCB[6]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 1 serial data QDSS trace data bit 6 B
AT2	GPIO_18	–	 CCI_I2C_SCL0 QDSS_GPIO_TRACEDATA_LOCB[5]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 0 clock QDSS trace data bit 5 B
AR1	GPIO_17	–	 CCI_I2C0_SDA0 QDSS_GPIO_TRACEDATA_LOCB[4]	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I^{2}C 0 serial data QDSS trace data bit 4 B

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AP4	GPIO_16	–	 CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB[3]	P3	B-PD:nppukp DO DI	Configurable I/O Camera master clock 3 QDSS trace data bit 3 B
AN3	GPIO_15	–	 CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB[2]	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 2 QDSS trace data bit 2 B
AR3	GPIO_14	–	 CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB[1]	P3	B-PD:nppukp DO DI	Configurable I/O Camera master clock 1 QDSS trace data bit 1 B
AP2	GPIO_13	–	 CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB[0]	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 0 QDSS trace data bit 0 B
R1	GPIO_12	–	 MDP_VSYNC_E QUP0_L4[1]	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – external QUP 0 SE1, lane 4: SPI_CS1
U37	GPIO_11	Y	 MDP_VSYNC_S_A	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – secondary
T36	GPIO_10	Y	 MDP_VSYNC_P_A	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – primary
N37	GPIO_9	Y	 QUP1_L3(1)	P3	B-PD:nppukp DI	Configurable I/O QUP 1 SE1, lane 3: UART_RX
R37	GPIO_8	–	 QUP1_L2(1) GP_PDM_B[1]	P3	B-PD:nppukp DO DO	Configurable I/O QUP 1 SE1, lane 2: UART_TX General-purpose PDM output 1 B
P36	GPIO_7	–	 QUP1_L1(1)	P3	B-PD:nppukp B B	Configurable I/O QUP 1 SE1, lane 1: I2C_SCL QUP 1 SE1, lane 1: I3C_SCL
P38	GPIO_6	Y	 QUP1_L0(1)	P3	B-PD:nppukp B B	Configurable I/O QUP 1 SE1, lane 0: I2C_SDA QUP 1 SE1, lane 0: I3C_SDA
J37	GPIO_5	Y	 QDSS_CTI_TRIG0_IN_B	P3	B-PD:nppukp DI	Configurable I/O QDSS trigger input 0 B
H36	GPIO_4	Y	 QDSS_CTI_TRIG0_OUT_A	P3	B-PD:nppukp DO	Configurable I/O QDSS trigger output 0 A
AA3	GPIO_3	Y	 QUP0_L3(0)	P3	B-PD:nppukp DI DO	Configurable I/O QUP 0 SE1, lane 3: UART_RX QUP 0 SE1, lane 3: SPI_CS0
Y4	GPIO_2	–	 QUP0_L2(1)	P3	B-PD:nppukp DO DO	Configurable I/O QUP 0 SE1, lane 2: UART_TX QUP 0 SE1, lane 2: SPI_SCLK
Y2	GPIO_1	–	 QUP0_L1(1)	P3	B-PD:nppukp DO B DO B	Configurable I/O QUP 0 SE1, lane 1: UART_RFR QUP 0 SE1, lane 1: I2C_SCL QUP 0 SE1, lane 1: SPI_MOSI QUP 0 SE1, lane 1: I3C_SCL

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
W3	GPIO_0	Y	QUP0_L0(1)	P3	B-PD:nppukp DI B DI B	Configurable I/O QUP 0 SE1, lane 0: UART_CTS QUP 0 SE1, lane 0: I2C_SDA QUP 0 SE1, lane 0: SPI_MISO QUP 0 SE1, lane 0: I3C_SDA
LPI pins						
AV14	LPI_GPIO_31	–	LPI_QCA_SB_CLK	P3	B-PD:nppukp DO	Bluetooth/FM SLIMbus clock
AW15	LPI_GPIO_30	–	LPI_QCA_SB_DATA	P3	B-PD:nppukp B	Bluetooth/FM SLIMbus data
AV16	LPI_GPIO_29	Y	LPI_PRIM_MCLK_B LPI_DMIC2_DATA	P3	B-PD:nppukp DO DI	LPI primary master clock B LPI DMIC 2 data
AW17	LPI_GPIO_28	Y	LPI_QUA_MI2S_DATA3 LPI_DMIC2_CLK GP_PDM_B_2 QDSS_CTI_TRIG1_IN_A	P3	B-PD:nppukp B DO DO DI	LPI quaternary MI2S data channel 3 LPI DMIC 2 clock General-purpose PDM 2 B output QDSS trigger input 1 A
AY18	LPI_GPIO_27	Y	LPI_QUA_MI2S_DATA2 LPI_DMIC1_DATA QDSS_CTI_TRIG1_OUT_A BOOT_CONFIG(5)	P3	B-PD:nppukp B DI DO DI	LPI quaternary MI2S data channel 2 LPI DMIC 1 data QDSS trigger output 1 A Boot configuration control bit 5
AW19	LPI_GPIO_26	Y	LPI_QUA_MI2S_DATA1 LPI_DMIC1_CLK	P3	B-PD:nppukp B DO	LPI quaternary MI2S data channel 0 LPI DMIC 1 clock
AV18	LPI_GPIO_25	Y	LPI_QUA_MI2S_DATA0	P3	B-PD:nppukp B	LPI quaternary MI2S data channel 0
AU19	LPI_GPIO_24	Y	LPI_QUA_MI2S_WS LPI_CDC_PDM_RX1_DRE GCC_GP3_CLK_A	P3	B-PD:nppukp B DO DO	LPI quaternary MI2S word select Audio codec PDM receive 1 (DRE) Global general-purpose clock 3 A
BA13	LPI_GPIO_23	Y	LPI_QUA_MI2S_SCK GCC_GP2_CLK_A GCC_GP_CLK_2A LPI_SWR_RX_DATA2 LPI_SWR_TX_DATA3	P3	B-PD:nppukp B DO DO DI DO	LPI quaternary MI2S bit clock Global general-purpose clock A Global general-purpose clock 2 A SoundWire Rx data 2 SoundWire Tx data 3
BB14	LPI_GPIO_22	–	LPI_AUD_SLIMBUS_DATA2 LPI_SWR_RX_DATA1 LPI_PRIM_MCLK_A	P3	B-PD:nppukp B DI DO	Audio SLIMbus data channel 2 SoundWire receive data 1 Audio master clock A
AY14	LPI_GPIO_21	–	LPI_AUD_SLIMBUS_DATA1 LPI_SWR_RX_CLK	P3	B-PD:nppukp B DO	LPI audio SLIMbus data channel 1 SoundWire receive clock
BA15	LPI_GPIO_20	–	LPI_AUD_SLIMBUS_DATA0 LPI_SWR_TX_DATA2	P3	B-PD:nppukp B DO	LPI audio SLIMbus data channel 0 SoundWire transmit data 2
BB16	LPI_GPIO_19	Y	LPI_SWR_TX_DATA1 LPI_AUDIO_REF_CLK	P3	B-PD:nppukp DO DO	SoundWire transmit data channel 1 Audio reference clock

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BC15	LPI_GPIO_18	–		P3	B-PD:nppukp	
			LPI_AUD_SLIMBUS_CLK		DO	LPI audio SLIMbus clock
			LPI_SWR_TX_CLK		DO	SoundWire transmit clock
BB18	LPI_GPIO_17	–		P3	B-PD:nppukp	
			LPI_QUP_L1(3)		DO	LPI QUP 3, lane 1: UART_RFR
					B	LPI QUP 3, lane 1: I2C_SCL
					DO	LPI QUP 3, lane 1: SPI_MOSI
			LPI_QUP_L1(4)		DO	LPI QUP 4, lane 1: UART_RFR
					B	LPI QUP 4, lane 1: I2C_SCL
					DO	LPI QUP 4, lane 1: SPI_MOSI
			LPI_QUP_L3(5)		DI	LPI QUP 5, lane 3: UART_RX
					DO	LPI QUP 5, lane 3: SPI_CS0
BC19	LPI_GPIO_16	–		P3	B-PD:nppukp	
			LPI_QUP_L0(3)		DI	LPI QUP 3, lane 0: UART_CTS
					B	LPI QUP 3, lane 0: I2C_SDA
					DI	LPI QUP 3, lane 0: SPI_MISO
			LPI_QUP_L0(4)		DI	LPI QUP 4, lane 0: UART_CTS
					B	LPI QUP 4, lane 0: I2C_SDA
					DI	LPI QUP 4, lane 0: SPI_MISO
			LPI_QUP_L2(5)		DO	LPI QUP 5, lane 2: UART_TX
					DO	LPI QUP 5, lane 2: SPI_SCLK
AY16	LPI_GPIO_15	–		P3	B-PD:nppukp	
			LPI_QUP_L3(4)		DI	LPI QUP 4, lane 3: UART_RX
					DO	LPI QUP 4, lane 3: SPI_CS0
			LPI_QUP_L1(5)		DO	LPI QUP 5, lane 1: UART_RFR
					B	LPI QUP 5, lane 1: I2C_SCL
					DO	LPI QUP 5, lane 1: SPI_MOSI
BA17	LPI_GPIO_14	–		P3	B-PD:nppukp	
			LPI_QUP_L2(4)		DO	LPI QUP 4, lane 2: UART_TX
					DO	LPI QUP 4, lane 2: SPI_SCLK
			LPI_QUP_L0(5)		DI	LPI QUP 5, lane 0: UART_CTS
					B	LPI QUP 5, lane 0: I2C_SDA
					DI	LPI QUP 5, lane 0: SPI_MISO
BA19	LPI_GPIO_13	–		P3	B-PD:nppukp	
			LPI_QUP_L3(3)		DI	LPI QUP 3, lane 3: UART_RX
					DO	LPI QUP 3, lane 3: SPI_CS0
			LPI_QUP_L4(5)		DO	LPI QUP 5, lane 4: SPI_CS1
BB20	LPI_GPIO_12	–		P3	B-PD:nppukp	
			LPI_QUP_L2(3)		DO	LPI QUP 3, lane 2: UART_TX
					DO	LPI QUP 3, lane 2: SPI_SCLK
BA21	LPI_GPIO_11	–		P3	B-PD:nppukp	
			LPI_I2S1_DATA1		B	LPI I^{2}S 1 serial data channel 1
			LPI_QUP_L3(2)		DI	LPI QUP 2, lane 3: UART_RX
					DO	LPI QUP 2, lane 3: SPI_CS0
AY22	LPI_GPIO_10	–		P3	B-PD:nppukp	
			LPI_I2S1_DATA0		B	LPI I^{2}S 1 serial data channel 0
			LPI_QUP_L2(2)		DO	LPI QUP 2, lane 2: UART_TX
					DO	LPI QUP 2, lane 2: SPI_SCLK
			LPI_QUP_L6(4)		DO	LPI QUP 4, lane 6: SPI_CS3
			LPI_QUP_L6(5)		DO	LPI QUP 5, lane 6: SPI_CS3

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1] Voltage	Pad characteristics [1] Type	Functional description
BC23	LPI_GPIO_9	–		P3	B-PD:nppukp	
			LPI_I2S1_WS		B	LPI I^{2}S 1 word select
			LPI_QUP_L6(1)		DO	LPI QUP 1, lane 6: SPI_CS3
			LPI_QUP_L1(2)		DO	LPI QUP 2, lane 1: UART_RFR
					B	LPI QUP 2, lane 1: I2C_SCL
					DO	LPI QUP 2, lane 1: SPI_MOSI
BB22	LPI_GPIO_8	–		P3	B-PD:nppukp	
			LPI_I2S1_SCK		B	LPI I^{2}S 1 bit clock
			LPI_QUP_L4(0)		DO	LPI QUP 0, lane 4: SPI_CS1
			LPI_QUP_L0(2)		DI	LPI QUP 2, lane 0: UART_CTS
					B	LPI QUP 2, lane 0: I2C_SDA
					DI	LPI QUP 2, lane 0: SPI_MISO
BB24	LPI_GPIO_7	–		P3	B-PD:nppukp	
			LPI_QUP_L5(1)		DO	LPI QUP 1, lane 5: SPI_CS2
			LPI_QUP_L5(2)		DO	LPI QUP 2, lane 5: SPI_CS2
			LPI_QUP_L5(3)		DO	LPI QUP 3, lane 5: SPI_CS2
			LPI_QUP_L1(4)B		DO	LPI QUP 4, lane 1: UART_RFR
					B	LPI QUP 4, lane 1: I2C_SCL
					DO	LPI QUP 4, lane 1: SPI_MOSI
BA23	LPI_GPIO_6	–		P3	B-PD:nppukp	
			LPI_QUP_L2(0)		DO	LPI QUP 0, lane 2: UART_TX
					DO	LPI QUP 0, lane 2: SPI_SCLK
			LPI_QUP_L4(1)		DO	LPI QUP 1, lane 4: SPI_CS1
			LPI_QUP_L4(2)		DO	LPI QUP 2, lane 4: SPI_CS1
			LPI_QUP_L0(4)B		DI	LPI QUP 4, lane 0: UART_CTS
					B	LPI QUP 4, lane 0: I2C_SDA
					DI	LPI QUP 4, lane 0: SPI_MISO
			LPI_QUP_L4(5)B		DO	LPI QUP 5, lane 4: SPI_CS1
AW23	LPI_GPIO_5	–		P3	B-PD:nppukp	
			LPI_QUP_L3(0)		DI	LPI QUP 0, lane 3: UART_RX
					DO	LPI QUP 0, lane 3: SPI_CS0
			LPI_QUP_L3(1)		DI	LPI QUP 1, lane 3: UART_RX
					DO	LPI QUP 1, lane 3: SPI_CS0
			LPI_QUP_L6(2)		DO	LPI QUP 2, lane 6: SPI_CS3
AV22	LPI_GPIO_4	–		P3	B-PD:nppukp	
			LPI_QUP_L2(1)		DO	LPI QUP 1 lane 2: UART_TX
					DO	LPI QUP 1 lane 2: SPI_SCLK
			LPI_QUP_L6(3)		DO	LPI QUP 3, lane 6: SPI_CS3
			LPI_QUP_L4(3)		DO	LPI QUP 3, lane 4: SPI_CS1
AW21	LPI_GPIO_3	–		P3	B-PD:nppukp	
			LPI_QUP_L1(1)		DO	LPI QUP 1, lane 1: UART_RFR
					B	LPI QUP 1, lane 1: I2C_SCL
					DO	LPI QUP 1, lane 1: SPI_MOSI
					B	LPI QUP 1, lane 1: I3C_SCL
AU21	LPI_GPIO_2	–		P3	B-PD:nppukp	
			LPI_QUP_L0(1)		DI	LPI QUP 1, lane 0: UART_CTS
					B	LPI QUP 1, lane 0: I2C_SDA
					DI	LPI QUP 1, lane 0: SPI_MISO
					B	LPI QUP 1, lane 0: I3C_SDA

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Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1] Voltage	Pad characteristics [1] Type	Functional description
AY20	LPI_GPIO_1	–	LPI_QUP_L1(0)	P3	B-PD:nppukp DO B DO B	LPI QUP 0, lane 1: UART_RFR LPI QUP 0, lane 1: I2C_SCL LPI QUP 0, lane 1: SPI_MOSI LPI QUP 0, lane 1: I3C_SCL
AV20	LPI_GPIO_0	–	SYNC_OUT LPI_QUP_L0(0)	P3	B-PD:nppukp DI B DI B	32 kHz clock output for synchronization LPI QUP 0, lane 0: UART_CTS LPI QUP 0, lane 0: I2C_SDA LPI QUP 0, lane 0: SPI_MISO LPI QUP 0, lane 0: I3C_SDA

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad #	Pad name	Functional description
AE11, AE13, AE15, AE17, AF12, AF14, AF16, AJ9, AJ11, AJ13, AJ15, AJ17, AK12, AK14, AK16	VDD_APC0	Power for the Kryo Silver application processor
AM10, AM12, AN9, AN11, AN13, AN15, AN17, AP12, AP14, AP16, AT10, AT12, AT14, AT16, AU9, AU11, AU13, AU15, AU17	VDD_APC1	Power for the Kryo Gold application processor
AA13, AA15, AA17, AA19, AA21, AB14, AB16, AB18, AB20, AB22, AB24, AC21, AD20, AD22, AE21, AE25, AE27, AE29, AE31, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AG19, AG21, AG25, AG27, AG29, AG31, AH18, AH22, AH24, AK18, AK24, AM16, AM18, AM20, AN19, AN21, AR19, V12, W13, W15, W17, W19, W21, Y14, Y16, Y18, Y20, Y22	VDDMX	Power for an on-chip memory
AA25, AA27, AA29, AA31, AC25, AC27, AC29, AC31, M24, M26, N13, N17, P14, P16, P18, P20, P22, P24, P26, T14, T16, T18, T20, T22, T24, T26, U19, U21, V24, V26, Y26	VDDCX	Power for the digital core circuits
M28, M30, M32, M34, N29, N31, N33, P28, T28, U29, U31, U33, V28, V30, V32, V34	VDD_GFX	Power for the graphics
AJ25, AK26, AK28, AK30, AK32, AL27, AL29, AL31, AL33, AM32, AN27, AN29, AN31, AN33, AP30	VDD_MODEM	Power for the modem circuits
AJ19	VDDA_APC_CS_1P8	Power for the APC current sense circuits
AD34	VDDA_USB_SS_DP_1P2	
AJ35	VDDA_USB_SS_DP_CORE	
AJ23	VDD_LPI_MX	Power for the LPI core memory
AA9	VDD_QFPROM	Power for programming the QFPROM
AH34	VDD_USB_HS_CORE	Power for the USB HS core circuits
AJ21, AK22, AM22, AP22	VDD_SSC_CX	
G17	VDDA_CC_EBI01	Power for the EBI clock circuits
H18	VDDIO_CK_EBI0	Power for the EBI0 I/O clock circuits
H22	VDDIO_CK_EBI1	Power for the EBI1 I/O clock circuits
H10, H12, H16, K10, K12, K14, K16	VDDA_EBI	Power for the EBI circuits
L23	VDDA_HV_EBI	P
H20, J19, J21, K18, K20, K22	VDDIO_EBI	Power for the EBI I/O circuits
H26	VDDA_PLL_HV_CC_EBI01	Power for the EBI PLL circuits

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Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AD10	VDDA_CSI0_0P9	Power for the CSI0 0.9 V circuits
AB8	VDDA_CSI3_1P2	Power for the CSI3 1.2 V circuits
AD8	VDDA_CSI2_1P2	Power for the CSI2 1.2 V circuits
AE9	VDDA_CSI3_0P9	Power for the CSI3 0.9 V circuits
AF8	VDDA_CSI2_0P9	Power for the CSI2 0.9 V circuits
AC9	VDDA_CSI0_1P2	Power for the CSI0 1.2 V circuits
AG7	VDDA_CSI1_0P9	Power for the CSI1 0.9 V circuits
AC7	VDDA_CSI1_1P2	Power for the CSI1 1.2 V circuits
AA35	VDDA_DSI0_0P9	Power for the DSI0 0.9 V circuits
AB34	VDDA_DSI0_1P2	Power for the DSI0 1.2 V circuits
AB32	VDDA_DSI1_0P9	Power for the DSI1 0.9 V circuits
AC33	VDDA_DSI1_1P2	Power for the DSI1 1.2 V circuits
Y34	VDDA_DSI0_PLL_0P9	Power for the DSI0 0.9 V circuits
AA33	VDDA_DSI1_PLL_0P9	Power for the DSI1 0.9 V circuits
AT32	VDDA_QLINK_LV	Power for the low voltage QLink clock circuits
AT30	VDDA_QLINK_LV_CK	Power for the low voltage QLink clock circuits
F38	VDDA_QREFS_0P9	Reference voltage for the QREFS 0.9 V circuits
AU29	VDDA_QREFS_1P25	Reference voltage for the QREFS 1.25 V circuits
AT26	VDDA_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits
AE33	VDDA_USB_HS_1P8	Power for the USB HS 1.8 V circuits
AF34	VDDA_USB_HS_3P1	Power for the USB HS 3.1 V circuits
H24	VDDA_UFS_1P2	Power for the UFS 1.2 V circuits
H28	VDDA_UFS_CORE	Power for the UFS core circuits
L7	VDDA_WCSS_ADCDAC_0	Power for the WCSS ADC and DAC 0
N7	VDDA_WCSS_ADCDAC_1	Power for the WCSS ADC and DAC 1
N9	VDDA_WCSS_PLL	Power for the WCSS PLL circuits
L9, M10	VDD_WCSS_CX	Power for the WCSS circuits
AT28	VDDP0	Power for the pad group 0
G21	VDDP1	Power for the pad group 1 – EBI pads
AJ7	VDDP2	Power for the pad group 2 – SDC2 pads
AR7, AT8, AT24, AT34, AU35, H34, K34, U9, V10	VDDP3	Power for the pad group 3 – most I/O pads
AV8	VDDP5	Power for the pad group 5 – UIM1 pads
AW9	VDDP6	Power for the pad group 6 – UIM2 pads
H30	VDDP7	Power for the pad group 7 – eMMC pads
K24	VDDP10	Power for the pad group 10 – UFS pad
AL35	VDDP11	Power for the pad group 11 – CXO pad
AH8	VDDPX_VBIAS_SDC	
AU7	VDDPX_VBIAS_UIM	

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Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AE37, AM38, AM40, AN37, AT18, AT20, AU23, AU25, AU27, AV24, AV26, AV28, AV30, AW27, AW29, AW31, AY28, AY30, BC27, H32, N19, W5, W7	DNC	Do not connect; connected internally, do not connect externally
A1, A41, AA1, AA23, AA41, AB10, AB12, AC11, AC13, AC15, AC17, AC19, AC23, AD18, AD24, AD26, AD28, AD30, AD32, AD38, AE1, AE19, AE23, AE41, AF10, AF4, AG9, AG11, AG13, AG15, AG17, AG33, AH20, AH26, AH30, AH38, AJ1, AJ27, AJ29, AJ31, AJ33, AJ41, AK8, AK10, AK20, AL9, AL11, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL41, AM8, AM26, AM28, AN1, AN7, AN23, AN25, AN41, AP8, AP10, AP18, AP20, AP26, AR9, AR11, AR13, AR15, AR17, AR27, AR29, AR31, AR33, AR41, AT22, AU1, AU33, AV10, AW1, AW25, AW41, BC1, BC5, BC9, BC13, BC17, BC21, BC25, BC29, BC33, BC37, BC41, C3, C5, C7, C9, C11, C13, C15, C17, C19, C23, C25, C27, C29, C31, C33, C35, C37, C39, D2, D40, E1, E3, E5, E39, E41, F4, F6, F14, F22, F30, G5, G7, G9, G11, G13, G15, G19, G29, G31, G33, G35, G37, H4, H8, J1, J3, J41, K4, K26, K28, K30, K32, L5, M6, M12, M14, M16, M18, M20, M22, N1, N5, N11, N27, N41, P10, P12, P30, P32, P34, R27, R29, T8, T10, T12, T30, T32, T34, U1, U13, U27, U41, V8, V14, V16, V18, V20, V22, W9, W23, Y12, Y28, Y30, Y32	GND	Ground

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3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	-0.3	1.13	V
VDD_APC1	Kryo Gold application processor	-0.3	1.25	V
VDD_GFX	Graphics processor	-0.3	1.22	V
VDDA_QREFS_0P9 VDDA_DSIx_0P9 VDDA_DSIx_PLL_0P9 VDDA_QLINK_LV_CK VDDA_QLINK_LV VDDA_UFS_CORE VDDA_CSIx_0P9 VDDA_PLL_HV_CC_EBI01 VDD_USB_HS_CORE VDDA_USB_SS_DP_CORE	QILnk reference 0.9 circuits DSI core 0.9 V circuits DSI PLL 0.9 V circuits QLink clock circuits QLink core circuits UFS core circuits CSI core 0.9 V circuits EBI PLL circuit supply USB digital core circuits – HS USB SS DP core circuits	-0.3	0.99	V
VDD_SSC_CX	LPI core	-0.3	1.13	V
VDD_LPI_MX	LPI core memory	-0.3	1.04	V
VDDCX	Digital core circuits	-0.3	1.13	V
VDDMX VDDA_EBI VDDA_CC_EBI01 VDDA_WCSS_PLL	On-chip memory EBI PHY circuits DDR PLL circuit WCSS PLL circuits	-0.3	1.08	V
VDD_MODEM	Modem circuits	-0.3	1.13	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_QFPROM VDDP11 VDDA_USB_HS_1P8 VDDA_APC_CS_1P8 VDDA_QREFS_1P8	Programming the QFPROM; otherwise, ground Digital pad circuits – CXO USB HS1 1.8 V circuits APC current sense circuits Reference voltage for QREFS	-0.3	2.07	V
VDDP1	Digital pad circuits – EBI	-0.3	1.30	V
VDDP2	Digital pad circuits – SDC2 Low voltage High voltage	-0.3	3.33	V
VDDP3 VDDP7	Digital pad circuits – most I/Os Digital pad circuits – eMMC	-0.3	2.09	V
VDDP5	Digital pad circuits – UIM1 dual-voltage Low voltage High voltage	-0.3	3.33	V
VDDP6	Digital pad circuits – UIM2 dual-voltage Low voltage High voltage	-0.3	3.33	V
VDDP10 VDDA_HV_EB VDDA_CSIx_1P2 VDDA_DSIx_1P2 VDDA_USB_SS_DP_1P2 VDDA_UFS_1P2	Digital pad circuits – UFS clock EBI PHY high-voltage circuits MIPI CSI 1.2 V circuits MIPI DSI 1.2 V circuits USB SS and DP 1.2 V circuit supply UFS 1.2 V circuits	-0.3	1.36	V
VDDA_WCSS_ADCDAC_x	WCSS ADC and DAC	-0.3	1.53	V
VDDA_WCSS_CS	WCSS core circuits	-0.3	0.89	V
VDDIO_EBI VDDIO_CK_EBI0 VDDIO_CK_EBI1	EBI I/O circuits EBI0 Clock circuit EBI1 Clock circuit	-0.3	0.69	V
VDDA_USB_HS_3P1	USB HS 3.1 V circuits	-0.3	3.52	V
T_S	Storage temperature [1] [2]	-55	150	°C

1. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
2. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-3). The SM7150 meets all performance specifications listed in Section 3.3 through Section 3.11, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor			
	Turbo	0.69	1.03	V
	Nominal-L1	0.66	0.95	V
	Nominal	0.62	0.89	V
	SVS-L1	0.57	0.85	V
	SVS	0.55	0.79	V
	Low-SVS	0.55	0.72	V
VDD_APC1	Kryo Gold application processor			
	Turbo-L1	0.73	1.11	V
	Turbo	0.69	1.03	V
	Nominal-L1	0.66	0.95	V
	Nominal	0.62	0.89	V
	SVS-L1	0.57	0.85	V
	SVS	0.55	0.79	V
	Low-SVS	0.55	0.72	V
VDD_SSC_CX	LPI core			
	Turbo	0.67	1.03	V
	Nominal	0.61	0.89	V
	SVS	0.51	0.79	V
	Low-SVS	0.49	0.72	V
VDD_LPI_MX	LPI memory			
	Turbo	0.74	095	V
	Nominal	0.74	0.95	V
	SVS	0.74	0.86	V
	Low-SVS	0.74	0.86	V
VDD_MODEM	Modem circuits			
	Turbo	0.67	1.03	V
	Nominal_L1	0.635	0.95	V
	Nominal	0.605	0.89	V
	SVS_L1	0.56	0.85	V
	SVS	0.51	0.79	V
	Low_SVS	0.49	0.72	V

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Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_GFX	Graphics			
	Turbo_L1	0.71	1.11	V
	Turbo	0.67	1.03	V
	Nominal_L1	0.64	0.95	V
	Nominal	0.61	0.89	V
	SVS_L1	0.56	0.85	V
	SVS	0.51	0.79	V
	Low_SVS	0.49	0.72	V
VDDCX	Digital core circuits			
	Turbo	0.67	1.03	V
	Nominal	0.61	0.89	V
	SVS-L1	0.56	0.85	V
	SVS	0.51	0.79	V
	Low-SVS	0.49	0.72	V
VDDMX	Memory circuits and analog PLL circuits			
	Turbo-L1	0.74	0.90	V
	Turbo	0.74	0.98	V
	Nominal-L1	0.74	0.98	V
	Nominal	0.74	0.95	V
	SVS-L1	0.74	0.86	V
	SVS	0.74	0.86	V
	Low-SVS	0.74	0.86	V
VDDA_EBI	EBI PHY circuits			
VDDA_CC_EBI01	DDR PLL circuits			
VDDA_WCSS_PLL	Turbo	0.74	0.98	V
	Nominal-L1	0.74	0.95	V
	Nominal	0.74	0.95	V
	SVS-L1	0.74	0.86	V
	SVS	0.74	0.86	V
	Low-SVS	0.74	0.86	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

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Table 3-3 Operating conditions

Parameter [1]		Min[3]	Typ [2]	Max [3]	Unit
Power supply voltages					
VDDA_QREFS_0P9 VDDA_DSIx_0P9 VDDA_DSIx_PLL_0P9 VDDA_QLINK_LV_CK VDDA_QLINK_LV VDDA_UFS_CORE VDDA_CSIx_0P9 VDDA_PLL_HV_CC_EBI01 VDD_USB_HS_CORE VDDA_USB_SS_DP_CORE	QLink reference 0.9 circuits DSI core 0.9 V circuits DSI PLL 0.9 V circuits QLink clock circuits QLink core circuits UFS core circuits CSI core 0.9 V circuits EBI PLL circuit supply USB digital core circuits – HS USB SS DP core circuits	0.85	0.88	0.90	V
VDD_QFPROM [4] VDDP11 VDDA_USB_HS_1P8 VDDA_APC_CS_1P8 VDDA_QREFS_1P8	Programming the QFPROM; otherwise, ground Digital pad circuits – CXO USB HS1 1.8 V circuits APC current sense circuits Reference voltage for QREFS	1.70	1.8	1.88	V
VDDP1 LPDDR4X VDD2	Digital pad circuits – EBI LPDDR4X VDD2 supply	1.02	1.128	1.18	V
VDDP2	Digital pad circuits – SDC2 Low voltage High voltage	 1.73 2.84	 1.8 2.96	 1.89 3.03	 V V
VDDP3 VDDP7	Digital pad circuits – most I/Os Digital pad circuits – eMMC	1.71	1.8	1.9	V
VDDP5	Digital pad circuits – UIM1 dual-voltage Low voltage High voltage	 1.73 2.80	 1.808 2.96	 1.89 3.03	 V V
VDDP6	Digital pad circuits – UIM2 dual-voltage Low voltage High voltage	 1.73 2.80	 1.808 2.96	 1.89 3.03	 V V
VDDP10 VDDA_HV_EB VDDA_CSIx_1P2 VDDA_DSIx_1P2 VDDA_USB_SS_DP_1P2 VDDA_UFS_1P2	Digital pad circuits – UFS clock EBI PHY high-voltage circuits MIPI CSI 1.2 V circuits MIPI DSI 1.2 V circuits USB SS and DP 1.2 V circuit supply UFS 1.2 V circuits	1.13	1.2	1.24	V
VDDA_WCSS_ADCDAC_x	WCSS ADC and DAC	1.23	1.304	1.39	V
VDDIO_EBI VDDIO_CK_EBI0 VDDIO_CK_EBI1	EBI I/O circuits EBI0 Clock circuit EBI1 Clock circuit	0.585	0.60	0.63	V
VDDA_USB_HS_3P1	USB HS1 3.1 V circuits	2.96	3.088	3.2	V

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Table 3-3 Operating conditions (cont.)

Parameter [1]		Min[3]	Typ [2]	Max [3]	Unit
Thermal conditions					
T_j or T_C	Device operating temperature (junction)	–	–	95	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. Minimum and maximum values refer to the voltage at SM7150 BGA.
4. The VDD_QFPROM_PRG pin should be connected to a 1.8 V power supply only during programming.

3.2.1 Core and memory voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE and VDD_MEM retention mode. This technique reduces the leakage of the digital logic and memory by reducing VDD to the minimum required to maintain the register and memory state. The V (MIN) for state retention is found through characterization.

Table 3-4 Core voltage in retention mode [1, 2]

VDDCX	Bit 63 (MSB)	Bit 62	Bit 61 (LSB)
0.4 V	1	0	0
0.44V	0	1	1
0.48V	0	1	0
0.52 V	0	0	1
0.56 V	1	1	1

1. The VDDCX voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x00780134.

Table 3-5 Memory voltage in retention mode [1, 2]

VDDMX	Bit 19 (MSB)	Bit 18	Bit 17 (LSB)
0.488 V	1	0	0
0.54 V	0	1	1
0.592 V	0	1	0
0.644 V	0	0	1

1. The VDDMX voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x00780148.

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3.3 Power distribution network (PDN)

Table 3-6 lists the impedance specifications for the core PDN rails.

Table 3-6 SM7150 PDN specifications

Power domain	Specification				Pad numbers of positive ports	Pad numbers of negative ports
	Maximum DC resistance (mΩ)	Parameters for max impedance (z_{spec}) calculation (1-200 MHz) [1]		Port number		
		R_{mid_freq} (mΩ)	L (pH)			
VDD_APC0	5	22	130	1	AE11, AE13, AE15, AE17, AF12, AF14, AF16, AJ11, AJ13, AJ15, AJ17, AJ9, AK12, AK14, AK16	AC11, AC13, AC15, AC17, AD18, AF10, AG11, AG13, AG15, AG17, AG9, AK10, AK8, AL11, AL13, AL15, AL17, AL9
VDD_APC1	2	14	80	1	AM10, AM12, AN11, AN13, AN15, AN17, AN9, AP12, AP14, AP16, AT10, AT12, AT14, AT16, AU11, AU13, AU15, AU17, AU9	AK10, AK8, AL11, AL13, AL15, AL17, AL9, AM8, AN7, AP10, AP18, AP8, AR11, AR13, AR15, AR17, AR9, AV10
VDD_MODEM	7	29	170	1	AJ25, AK26, AK28, AK30, AK32, AL27, AL29, AL31, AL33, AM32, AN27, AN29, AN31, AN33, AP30	AH26, AH30, AJ27, AJ29, AJ31, AJ33, AL23, AL25, AM26, AM28, AN23, AN25, AP26, AR27, AR29, AR31, AR33
VDD_GFX	3	20	120	1	M28, M30, M32, M34, N29, N31, N33, P28, T28, U29, U31, U33, V28, V30, V32, V34	K26, K28, K30, K32, N27, P30, P32, P34, R27, R29, T30, T32, T34, U27, Y28, Y30, Y32
VDDCX (Lumped)	3	20	100	1	AA25, AA27, AA29, AA31, AC25, AC27, AC29, AC31, Y26, M24, M26, N13, N17, P14, P16, P18, P20, P22, P24, P26, T14, T16, T18, T20, T22, T24, T26, U19, U21, V24, V26	AA23, AC23, AD24, AD26, AD28, AD30, AD32, Y28, Y30, Y32, K26, M12, M14, M16, M18, M20, M22, N11, N27, P12, R27, T12, U13, U27, V14, V16, V18, V20, V22, W23

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Table 3-6 SM7150 PDN specifications (cont.)

Power domain	Specification				Pad numbers of positive ports	Pad numbers of negative ports
	Maximum DC resistance (mΩ)	Parameters for max impedance (z_{spec}) calculation (1-200 MHz) [1]		Port number		
		R_{mid_freq} (mΩ)	L (pH)			
VDDMX (Lumped)	5	24	130	1	AM16, AM18, AN19, AR19, AA13, AA15, AA17, AA19, AA21, AB14, AB16, AB18, AB20, AB22, AB24, AC21, AD20, AD22, AE21, AE25, AE27, AE29, AE31, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AG19, AG21, AG25, AG27, AG29, AG31, AH18, AH22, AH24, AK24, W13, W15, W17, W19, W21, Y14, Y16, Y18, Y20, Y22	AL15, AL17, AP18, AR17, AA23, AB12, AC13, AC15, AC17, AC19, AC23, AD18, AD24, AD26, AD28, AD30, AD32, AE19, AE23, AG17, AG33, AH20, AH26, AH30, AJ27, AJ29, AJ31, AL23, AL25, V14, V16, V18, V20, V22, W23, Y12
VDD_WCSS_CX	55	100	600	1	L9, M10	M12, N11, P12
VDD_SSC_CX	70	83	500	1	AK22, AM22, AP22, AJ21	AH20, AH26, AL21, AL23, AN23
VDD_LPI_MX	100	170	1000	1	AJ23	AH26, AL21
VDDCX (Distributed)	5	25	150	1	AA25, AA27, AA29, AA31, AC25, AC27, AC29, AC31, Y26	AA23, AC23, AD24, AD26, AD28, AD30, AD32, Y28, Y30, Y32
	5	20	110	2	M24, M26, N13, N17, P14, P16, P18, P20, P22, P24, P26, T14, T16, T18, T20, T22, T24, T26, U19, U21, V24, V26	K26, M12, M14, M16, M18, M20, M22, N11, N27, P12, R27, T12, U13, U27, V14, V16, V18, V20, V22, W23
VDDMX (Distributed)	10	50	320	1	AM16, AM18, AN19, AR19	AL15, AL17, AP18, AR17
	5	24	140	2	AA13, AA15, AA17, AA19, AA21, AB14, AB16, AB18, AB20, AB22, AB24, AC21, AD20, AD22, AE21, AE25, AE27, AE29, AE31, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AG19, AG21, AG25, AG27, AG29, AG31, AH18, AH22, AH24, AK24, W13, W15, W17, W19, W21, Y14, Y16, Y18, Y20, Y22	AA23, AB12, AC13, AC15, AC17, AC19, AC23, AD18, AD24, AD26, AD28, AD30, AD32, AE19, AE23, AG17, AG33, AH20, AH26, AH30, AJ27, AJ29, AJ31, AL23, AL25, V14, V16, V18, V20, V22, W23, Y12

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1. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using R_{mid_freq} and inductance (L) values from the Table 3-7. Z_{spec} is the maximum impedance allowed from 1 MHz to 200 MHz.

   It is calculated as

$$Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$$

Table 3-7 PDN specifications – LPDDR4X

Power domain	Specification			Port number	Pad numbers of positive ports	Pad numbers of negative ports
	Maximum DC resistance	Parameters for max impedance (z_{spec}) calculation [1]				
		R_{mid_freq} (mΩ)	Inductance L (pH)			
VDDA_EBI	30	75	1000	1	K16, K14, K12, K10, H16, H12, H10	M16, M14, M12, H8, G9, G11, F14, G13, G15
VDDIO_EBI	10	30	600	1	K22, K18, K20, J21, J19, H20	M22, M20, M18, F22, G19

1. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using R_{mid_freq} and inductance (L) values from the Table 3-7. Z_{spec} is the maximum impedance allowed from 1 MHz to 200 MHz.

   It is calculated as

$$Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$$

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Table 3-8 PDN specifications – SerDes rails

Power rail	Power domain	Maximum DC resistance (mΩ)	Parameters for max impedance (z_{spec}) calculation [1]		Port number	Pad number of positive ports	Pad number of negative ports
			R_{mid_freq} (mΩ)	Inductance L (pH)			
VREG_L3C	VDDA_UFS_1P2	857	235	1500	1	H24	K26
	VDDA_USB_SS_DP_1P2	500	196	1250	2	AD34	AD32
	VDDA_DSI0_1P2	1200	157	1000	3	AB34	AD32
	VDDA_DSI1_1P2	1200	157	1000	4	AC33	AD32
	VDDA_CSI0_1P2	2400	235	1500	5	AC9	AB10, AC11
	VDDA_CSI1_1P2	2400	235	1500	6	AC7	AB10, AC11
	VDDA_CSI2_1P2	2400	235	1500	7	AD8	AB10, AC11
	VDDA_CSI3_1P2	2400	235	1500	8	AB8	AB10, AC11
VREG_L4A	VDDA_QLINK_LV	729	235	1500	1	AT32	AR33, AU33
	VDDA_QLINK_LV_CK	625	117	750	2	AT30	AR29, AR31
	VDDA_UFS_CORE	438	176	1125	3	H28	G29
	VDDA_USB_SS_DP_CORE	159	138	880	4	AJ35	AJ33
	VDD_USB_HS_CORE	1250	235	1500	5	AH34	AG33, AJ33
	VDDA_DSI0_0P9	350	169	1080	6	AA35	Y32
	VDDA_DSI1_0P9	350	169	1080	7	AB32	Y32
	VDDA_CSI0_0P9	521	235	1500	8	AD10	AC11
	VDDA_CSI1_0P9	521	235	1500	9	AG7	AG9
	VDDA_CSI2_0P9	521	235	1500	10	AF8	AG9, AF10
	VDDA_CSI3_0P9	521	235	1500	11	AE9	AG9, AF10
VREG_L11A	VDDA_USB_HS_1P8	600	157	1000	1	AE33	AD32
VREG_L17A	VDDA_USB_HS_3P1	4393	235	1500	1	AF34	AG33
VREF_MSM	VDDPX_VBIAS_SDC	-	117	750	1	AH8	AG9
	VDDPX_VBIAS_UIM	-	117	750	2	AU7	AR9, AV10

1. The PDN AC impedance specification (mask) is obtained by plotting Z_{spec} using R_{mid_freq} and Inductance (L) values from the Table 3-8. Z_{spec} is the maximum impedance allowed from 1 MHz to 200 MHz.

It is calculated as

$$Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$$

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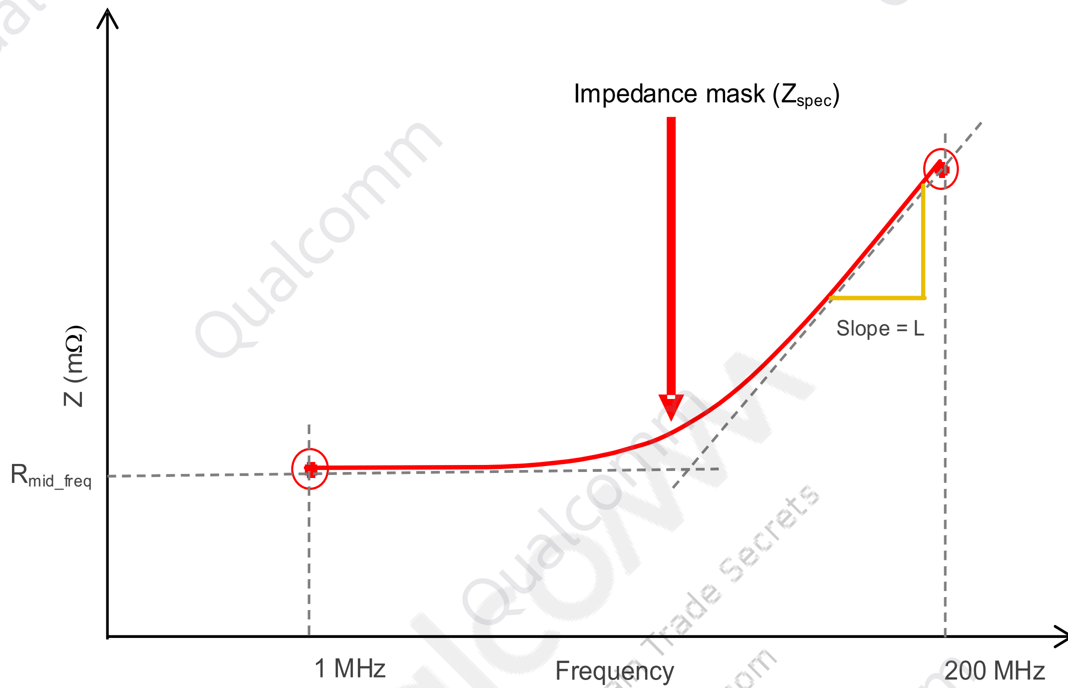

Figure 3-1 PDN impedance mask

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3.4 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire SM7150 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. See the appropriate PMIC device specification, such as the *PM6150A/PM6150L and PM7150A/PM7150L Device Specification* (80-PG281-1) or the *PM6150/PM7150 Power Management IC Device Specification* (80-PH856-1) for details.

A high-level summary of the required default power-on sequence is:

1. VDDMX (on-chip memory), VDDA_EBI (EBI PHY circuits), VDDA_CC_EBI01, and VDDA_WCSS_PLL (WCSS PLL circuits)
2. VDD_LPI_MX (LPI memory)
3. VDDCX (digital core circuits)
4. VDD_SSC_CX (LPI core)
5. VDDP3 (GEN 1.8 V IO), VDD1 (LPDDR4X VDD1 supply)
6. VDD_WCSS_CX (WCSS core supply)
7. VDDPX_VBIAS_SDC, VDDPX_VBIAS_UIM, and VDDA_QREFS_1P25
8. VDDP1 and VDD2 (LPDDR4X VDD2 supply)
9. VDDIO_EBI (EBI IO supply), VDDIO_CK_EBI0, VDDIO_CK_EBI1 (EBI clock supply), VDDQ (LPDDR4X VDDQ supply)
10. VCCQ2 (UFS/eMMC VCCQ supply)
11. VDDP10 (UFS), VDDA_CSIx_1P2 (MIPI CSI 1.2 V), VDDA_DSIx_1P2 (MIPI DSI 1.2 V), VDDA_UFS_1P2 (UFS clock), VDDA_USB_SS_DP_1P2 (USB SS 1.2 V), VDDA_HV_EBI (EBI PHY)
12. VDDA_QREFS_0P9 (QLink reference), VDDA_DSIx_0P9 (DSI core), VDDA_DSIx_PLL_0P9 (DSI PLL), VDDA_QLINK_LV_CK (QLink clock), VDDA_QLINK_LV (QLink core), VDDA_UFS_CORE (UFS core), VDDA_CSIx_0P9 (CSI core), VDDA_PLL_HV_CC_EBI01 (EBI PLL), VDD_USB_HS_CORE (USB digital core), VDDA_USB_SS_DP_CORE (USB SS DP core)
13. VDD_QFPROM (QFPROM), VDDP11 (Digital IO), VDDA_USB_HS_1P8 (USB HS1), VDDA_APC_CS_1P8 (APC current sense), VDDA_QREFS_1P8 (QREFS)
14. VDDA_USB_HS_3P1 (USB HS)
15. VDDP2 (SDC2)
16. VDD_MODEM
17. VDD_APC0

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Comments regarding this sequence include:

- The core voltage (VDDCX) needs to power up before the pad circuits (VDD_PX), so that the internal circuits can take control of the I/Os and pads. If pad voltages power up first, the output drivers might be stuck in unknown states and might cause large leakage currents until VDDCX powers on.
- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDDCX reaches 90% of its value, the VDDP3 supply can start ramping up.

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the document *SM7150 Linux Android Current Consumption Data* (80-PG319-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-9 Dhrystone and rock bottom maximum power

SDM version	Octa core – 2X Gold at 2.2 GHz for SM7150 or 2.3 GHz for SM7150-AC and 6X Silver at 1.8 GHz, Dhrystone (W) at +95°C (Tj) [1, 2, 3]	Rock bottom (mW) at 30°C (Tj) [4]
SM7150	5	8.5
SM7150-AC	5.4	8.5

1. This Kryo Gold dual core Dhrystone specification applies to SM7150 CS devices that run at 2.2 GHz for SM7150 or 2.3 GHz for SM7150-AC and for six Silver core at 1.8 GHz.
2. Dhrystone power should be measured on the VDD_APC1 rail, right before PDN capacitors (with a small serial sampling resistor inserted, if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 μs), and the average window should be > 1 ms (or > 1250 samples).
4. Rock bottom (VDDCX and VDDMX) power should be measured at VDDCX and VDDMX rails when VDDCX and VDDMX are at retention voltage. See AIR1 in Table 3-1 Test definitions in the *SM7150 Linux Android Current Consumption Data* (80-PG319-7) document for the test setup.

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SDM device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^{2}C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-10 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDP3	VDDP3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDP3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDP3	VDDP3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDP3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	1.0	μA
I_{IL}	Input low leakage current [1]	-1.0	–	μA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	μA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	μA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	1.0	μA
I_{OZL}	Low-level, tri-state leakage current [1]	-1.0	–	μA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	μA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	μA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	μA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	μA (kΩ)
V_{OH}	High-level output voltage, CMOS	VDDP3 - 0.45	VDDP3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
2. Pin voltage = VDDP3 maximum. For keeper pins, pin voltage = VDDP3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDDP3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDP3 maximum.

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Table 3-11 SDC2 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDP2	–	VDDP2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDP2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	μA
I_{IL}	Input low leakage current	-10	–	–	μA
I_{OZH}	High-level, tri-state leakage current	–	–	10	μA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDDP2	–	VDDP2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDP2	V

Table 3-12 SDC2 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.65 × VDDP2	–	VDDP2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.35 × VDDP2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	μA
I_{IL}	Input low leakage current	-5	–	–	μA
I_{OZH}	High-level, tri-state leakage current	–	–	5	μA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

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Table 3-13 SDC1 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.65 × VDDP7	–	VDDP7 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.35 × VDDP7	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	2	μA
I_{IL}	Input low leakage current	-2	–	–	μA
I_{OZH}	High-level, tri-state leakage current	–	–	2	μA
I_{OZL}	Low-level, tri-state leakage current	-2	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	VDDP7 - 0.45	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 UICC 3 V mode DC specifications (VDDP5 and VDDP6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPx	–	VDDPx + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPx	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{OZH}	High-level, tri-state leakage current	–	–	10	μA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPx	–	VDDPx	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. VHYS is not a required specification for UICC.
3. UICC specifies VOH = 0.8 × VDDPx (RST) and 0.7 × VDDPx (CLK, I/O). The worse-case VOH is used in this table.
4. UICC specifies VOL = 0.2 × VDDPx (RST, CLK) and 0.4 V (I/O). The worse-case VOL is used in this table.

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NOTE: UICC supply range for class B is 2.7 V to 3.3 V.

Table 3-15 UICC 1.8 V mode DC specifications (VDDP5 and VDDP6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPx	–	VDDPx + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPx	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{OZH}	High-level, tri-state leakage current	–	–	5	μA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	μA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPx	–	VDDPx	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. VHYS is not a required specification for UICC.
3. UICC specifies VOH = 0.8 × VDDPx (RST) and 0.7 × VDDPx (CLK, I/O). The worse-case VOH is used in this table.
4. UICC specifies VOL = 0.2 × VDDPx (RST, CLK) and 0.3 V (I/O). The worse-case VOL is used in this table.

NOTE: UICC supply range for class C is 1.62 V to 1.98 V.

Table 3-16 Digital I/O characteristics for VDDP10 nominal (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDDP10	V
V_{OH}	Output high-level voltage	0.75 × VDDP10	VDDP10	V
$R_{PULL-UP}$	Pull-up resistance	100	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	100	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	5	μA
I_{OZL}	Low-level, tri-state leakage current	-5	–	μA

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-2), with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

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$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

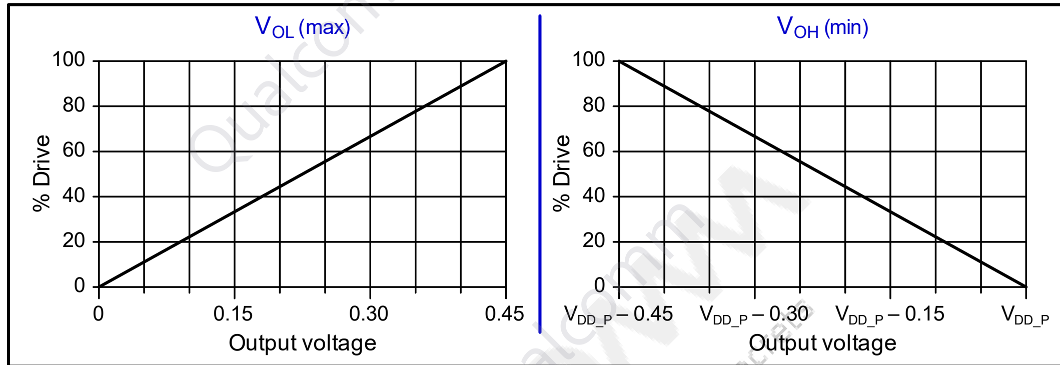

Figure 3-2 IV curve for V_{OL} and V_{OH} (valid for all V_{DDPx})

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE: All SM7150 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

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3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-3.

Waveform	Description
	Don't care or bus is driven
	Signal is changing from low to high
	Signal is changing from high to low
	Bus is changing from invalid to valid
Keeper	Bus is changing from valid to keeper
	Bus is changing from Hi-Z to valid
	Denotes multiple clock periods

Figure 3-3 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SM7150 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-4.

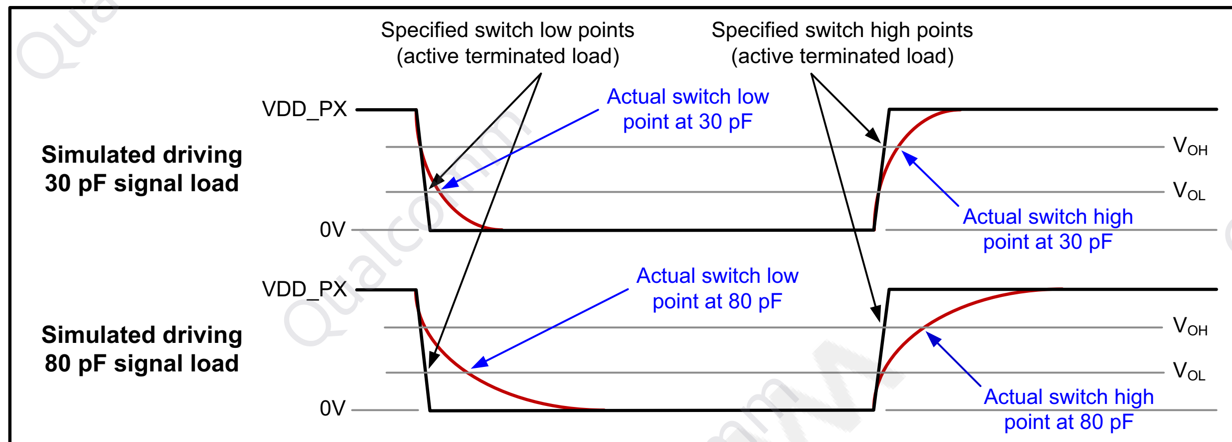

Figure 3-4 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SDM device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SM7150 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated V_{DDPX} supply (Figure 3-5). The input switch point for pure input-only pads is designed to be $V_{DDPX}/2$ (or 50% of V_{DDPX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX} for V_{IL} and 65% of V_{DDPX} for V_{IH}.

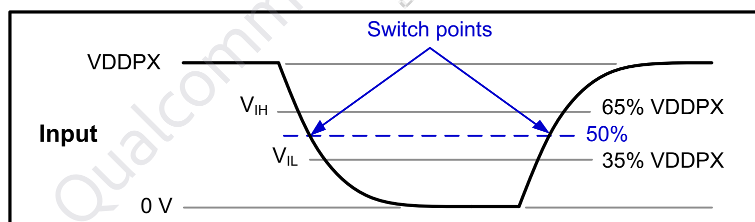

Figure 3-5 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-6) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- $V_{OH} \sim V_{DDPX}$ - 50 mV or more
- $V_{OL} \sim$ 50 mV or less

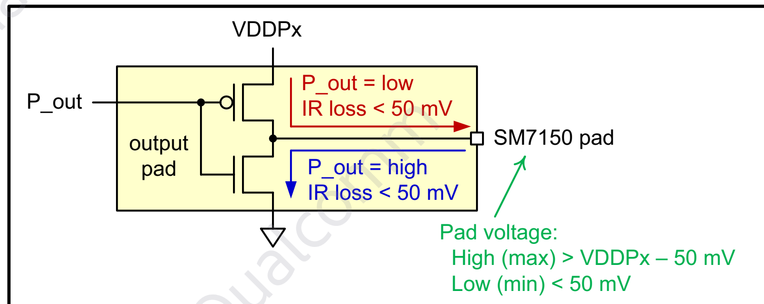

Figure 3-6 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both the input and output behaviors were described above.

3.7 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.7.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4x SDRAM memory that is attached to the SM7150 chipset.

3.7.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.9.1 for secure digital interface details.

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SM7150 device supports four MIPI_CSIs:

- CSI0 is 4-lane CSI
- CSI1 is 4-lane CSI
- CSI2 is 4-lane CSI
- CSI3 is 2-lane CSI

Table 3-17 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.0	None

3.8.2 Display support

The SM7150 device supports up to two DPHY displays.

Table 3-18 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

3.8.3 Audio support

The SM7150 provides the system's digital audio functions that supplement one of the two analog audio codec implementations:

- A dedicated audio codec, such as the WCD9340/WCD9341, uses the industry standard SLIMbus interface.
- A dedicated audio codec, such as the WCD9375, uses the industry standard SoundWire interface.

Other audio-related interface options include:

- SLIMbus – Section 3.9.6
- I^2S – Section 3.9.7
- Digital microphone – Section 3.9.8

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- SoundWire – Section 3.9.9

See the *WCD9340/WCD9341 Audio Codec Device Specification* (80-P4986-1) for performance characteristics.

See the *Qualcomm AQSTIC WCD9375 Device Specification* (80-PG245-1) for performance characteristics.

3.9 Connectivity

The connectivity functions supported by the SM7150 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Universal integrated circuit card (UICC) interface
- DisplayPort support over USB Type-C
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power interchip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Dedicated I^2C interfaces for camera (CCI I^2C)
- Through proper configuration of QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

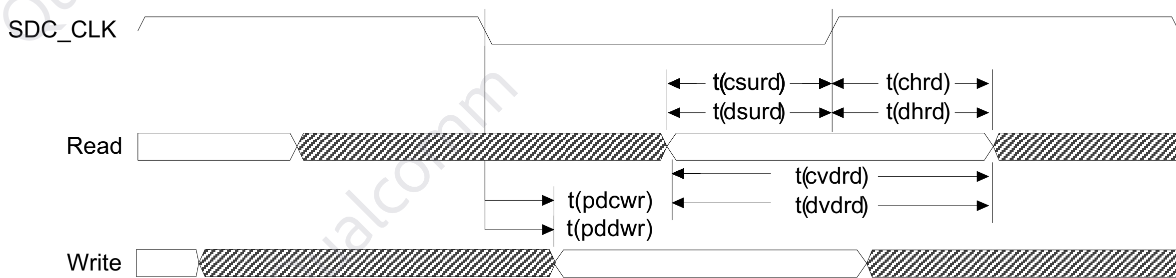
NOTE: In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 Secured digital interfaces

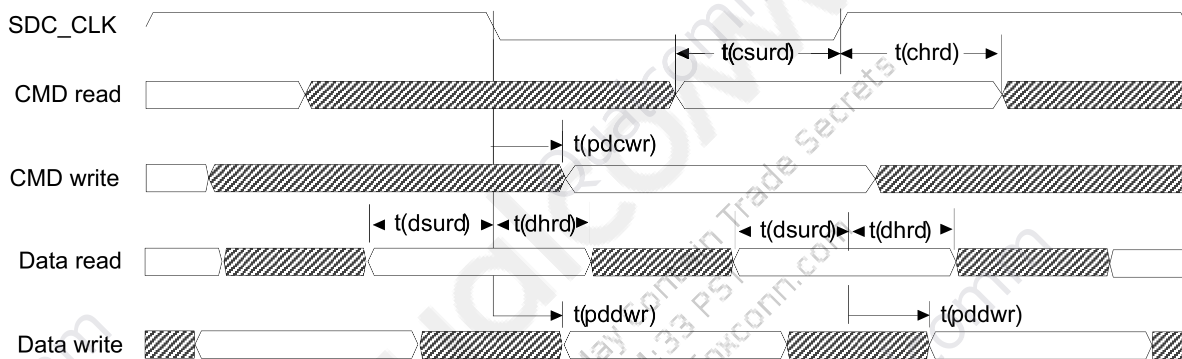
Table 3-19 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

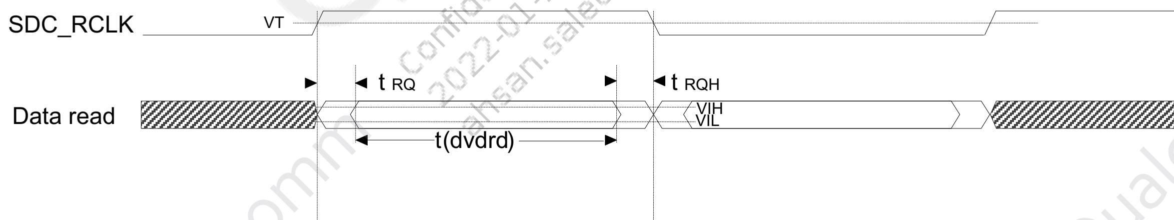
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

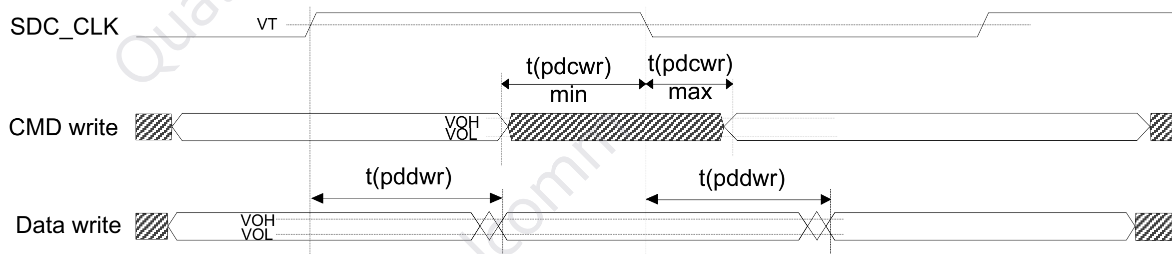


Figure 3-7 Secured digital interface timing

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3.9.2 USB interfaces

Table 3-20 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.9.3 DisplayPort

Table 3-21 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.9.4 UFS interface

Table 3-22 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 2.1	None

3.9.5 UIM interface

Table 3-23 Supported UIM standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.6 SLIMbus interface

Table 3-24 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.9.7 I²S interfaces

There are two I²S interface types supported by the SM7150:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI2S) interface for microphone and speaker functions

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The following information applies to both interface types.

Table 3-25 applies to MI2S.

Table 3-25 Supported I^{2}S standards and exceptions

Applicable standards	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	None

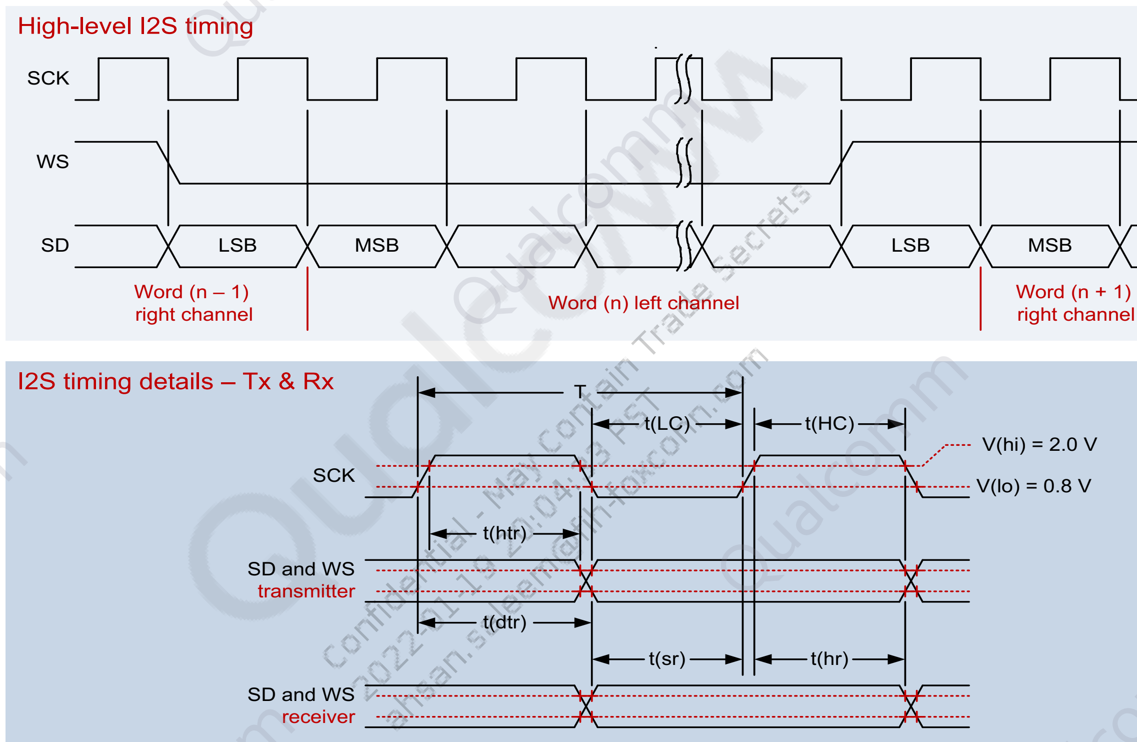

Figure 3-8 I^{2}S timing diagram

Table 3-26 I^{2}S interface timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency[1]		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 · T	–	0.55 · T	ns
t(LC)	Clock low	–	0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						

Table 3-26 I²S interface timing (cont.)

Parameter		Comments	Min	Typ	Max	Unit
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 · T	–	0.55 · T	ns
t(LC)	Clock low	–	0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
t(htr)	SD and WS output hold time	–	–	–	–	ns

1. Load capacitance is between 10 and 40 pF.

3.9.8 Digital microphone PDM interface

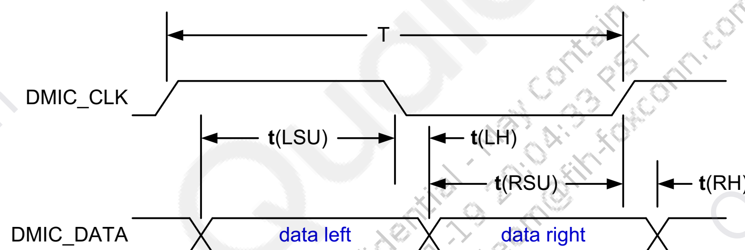

Figure 3-9 Digital microphone PDM interface timing

Table 3-27 Digital microphone timing

Parameter		Min	Typ	Max	Units
T	DMIC clock period	163	–	1666	ns
t(LSU)	Data left setup time to clock falling edge	5	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	5	–	–	ns
t(RH)	Data right hold time to clock falling edge	0	–	–	ns

3.9.9 SoundWire

SM7150 SoundWire PHY timing parameters, as specified in Table 3-28, are compliant to clock and data specifications, as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04. See Figure 3-10 and Figure 3-11.

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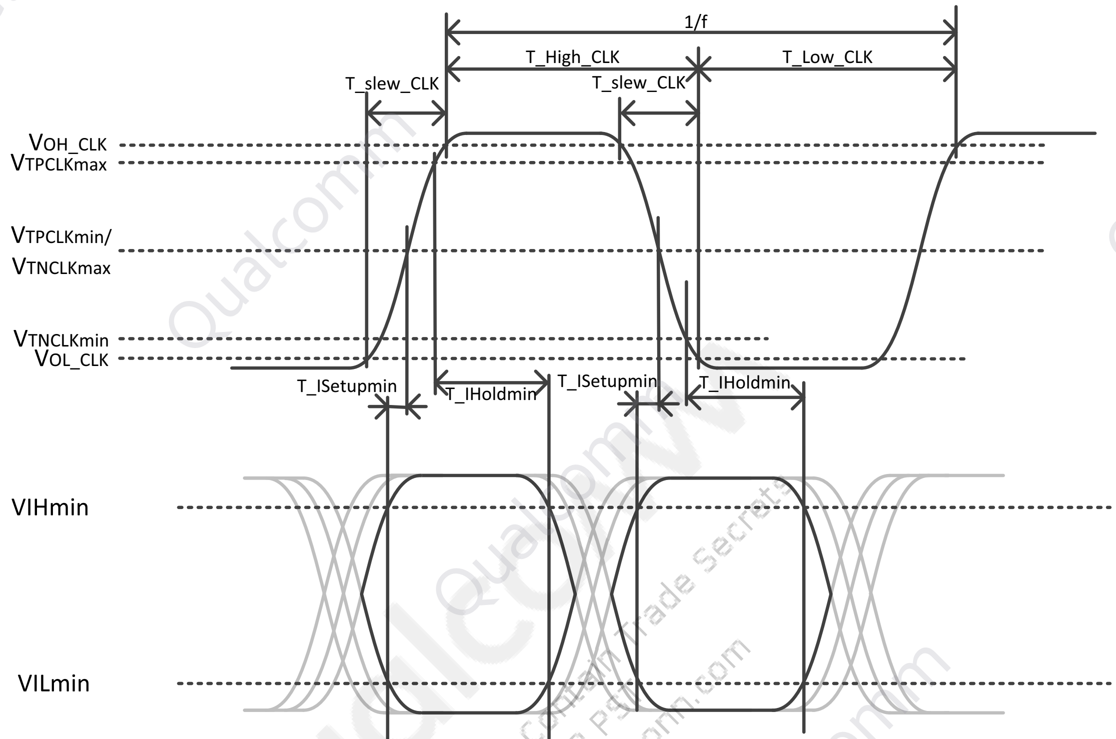

Figure 3-10 PHY timing – clock output/input and data input

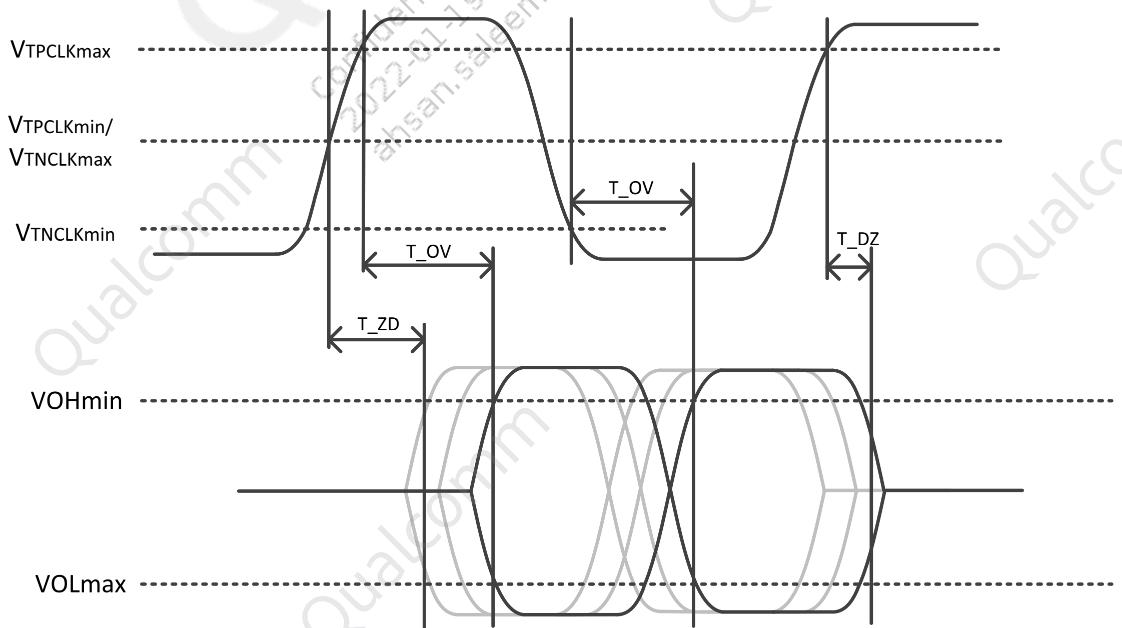

Figure 3-11 PHY timing – clock output and data output

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Table 3-28 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Units
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	V
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	V
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	%
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	4	–	ns
t_IHold_min_Data_1V8	Input hold time	–	4	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.9.10 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.9.11) and GPIOs configured as discrete digital inputs (Section 3.5) or through SPI bus (Section 3.9.13) through LPI GPIO.

3.9.11 I^{2}C interface

Table 3-29 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions
I^{2}C Specification, version 3.0	HS mode, slave mode, and 10-bit addressing are not supported.

3.9.12 I3C interface

Table 3-30 Supported I3C standards and exceptions

Applicable standard	Feature exceptions
I3C Specification, version 1.0	TBD

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3.9.13 Serial peripheral interface

The SM7150 supports SPI as a master only. Any one of the 13 QUP ports can be configured as an SPI master.

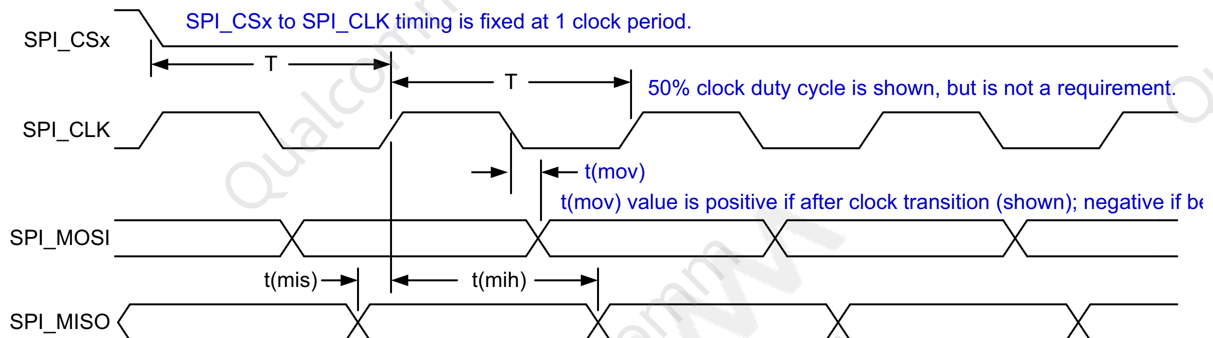

Figure 3-12 SPI master timing diagram

Table 3-31 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	9	–	–	ns
t(cl)	Clock low	9	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns
t(ov) [2]	Chip CS to CLK	-5	–	5	ns

1. The minimum clock period includes 1% jitter of maximum frequency.
2. For extra SPI chip select function supported on GPIO_12, GPIO_37, GPIO_57,GPIO_58, GPIO_63, GPIO_64, and GPIO_65, the min and max values are +/- 6 ns.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

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3.10.1.1 19.2 MHz CXO input

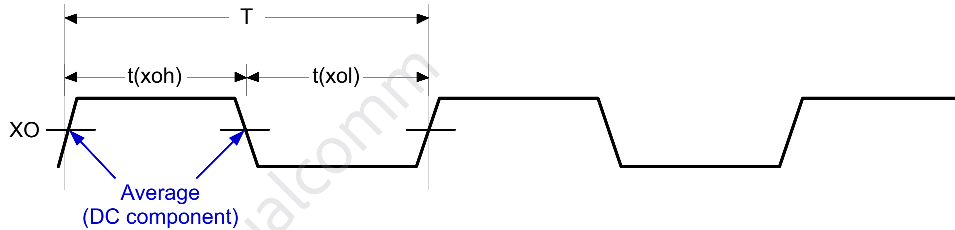

Figure 3-13 XO timing parameters

Table 3-32 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.10.1.2 Sleep clock

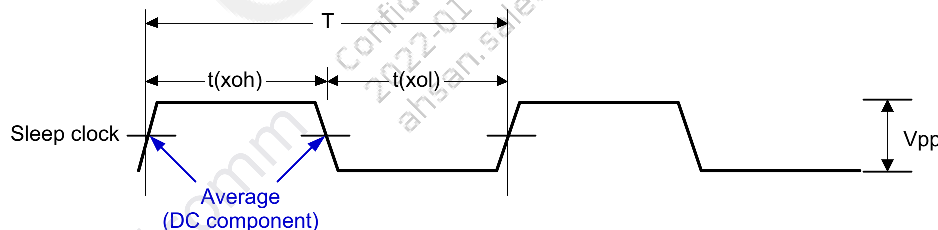

Figure 3-14 Sleep-clock timing parameters

Table 3-33 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

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3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.5.

3.10.3 JTAG

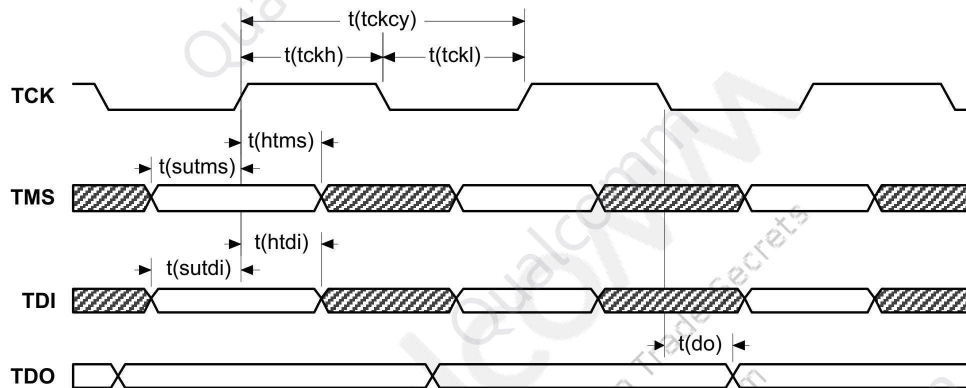

Figure 3-15 JTAG interface timing diagram

Table 3-34 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.11 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-3. The digital I/Os must meet the logic-level requirements specified in Section 3.5. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.11.1 RF front end (RFFE)

Table 3-35 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None

Table 3-36 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

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4 Mechanical information

4.1 Device physical dimensions

The SM7150 device is available in the PSP792, a 11.10 × 10.50 × 0.99 mm non-PoP package. The package includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download the *Package Outline Drawing, PSP792, 11.10 × 10.50 × 0.99 mm, M530, S243* (NT90-PJ243-1) from the Qualcomm CreatePoint website.
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PJ243-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

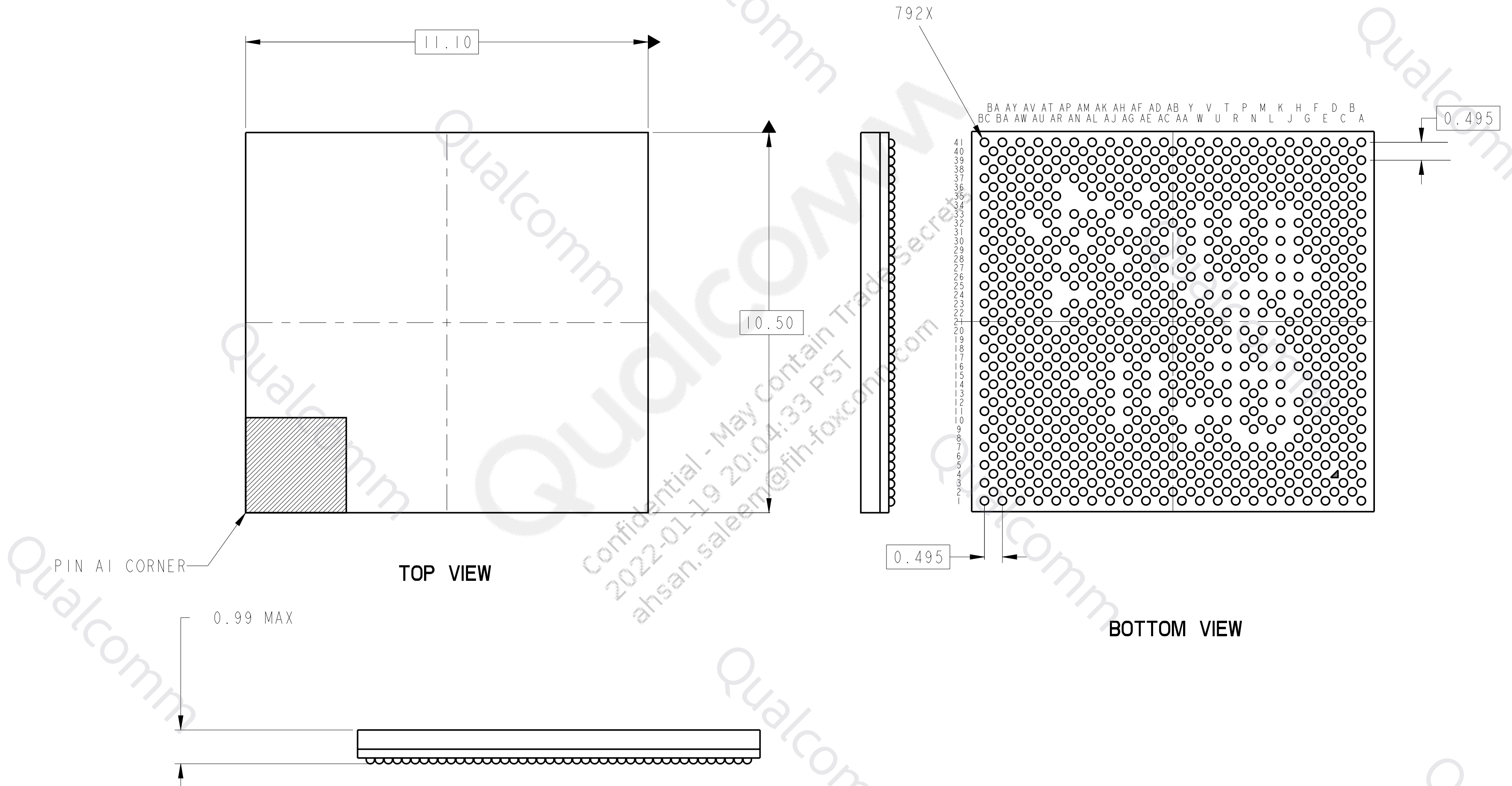

Figure 4-1 Simplified PSP792 (11.10 × 10.50 × 0.99 mm) outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 SM7150 part marking

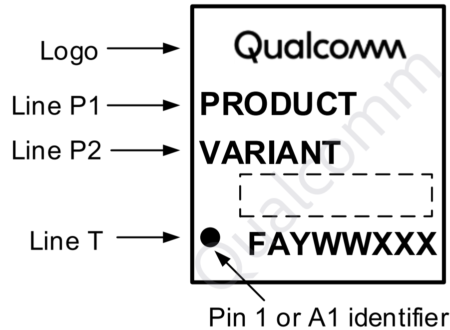

Figure 4-2 Device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
Logo	QUALCOMM	Qualcomm name or logo
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ SM7150
P2	VARIANT	Device variant information ■ See Table 4-4 for assigned values.
	Blank or variable	Additional content as necessary
T	FAYWWXXX	F = supply source code ■ F = J (Samsung) A = assembly site code ■ A = E (ASE, Taiwan) ■ A = K (SPIL, Taiwan) ■ A = H (JCET STATS ChipPAC, Korea) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE: For complete marking definitions of all SM7150 variants and revisions, see the *SM7150 Device Revision Guide* (80-PG319-4).

The 28-bit QFPROM PTE register is summarized in Table 4-2.

Table 4-2 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants see Table 4-4.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the JTAG ID see Table 4-4.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-7150	-0	-PSP	792			-MT	-00	-0	-AA

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-7150-0-PSP792-MT-00-0-AA

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [1]	FEATURE_ID (see Table 4-2) [2]	Hardware revision number (JTAG_ID - see Table 4-2)	Hardware version	S value [3]	Comments
SM7150	ES/CS	100-AB	0x1	0x0 00E6 0E1	v1.0	0	SM7150, PSP792, QHD+, Gold CPU 2.208 GHz, Silver CPU 1.804 GHz, 4 × 4 MIMO with LAA, NPU at 600 MHz, GPU at 700 MHz, 3xCA, CDMA, GSM, LTE, TD-SCDMA, DC-HSPA+, WCDMA, 20 MP YWW ≥ 905 [4]
	ES/CS	100-AA	0x2	0x0 00E6 0E1	v1.0	0	SM7150, PSP792, FHD+, Gold CPU 2.208 GHz, Silver CPU 1.804 GHz, 4 × 4 MIMO with LAA, NPU at 600 MHz, GPU at 610 MHz, 3xCA, CDMA, GSM, LTE, TD-SCDMA, DC-HSPA+, WCDMA, 20 MP YWW ≥ 905 [4] YWW 904 [5]
	CS	100-AC	0x9	0x0 00E6 0E1	v1.0	0	SM7150, PSP792, QHD+, Gold CPU 2.3 GHz, Silver CPU 1.8 GHz, 4 × 4 MIMO with LAA, NPU at 700 MHz, GPU at 800 MHz, 3x CA, CDMA, GSM, LTE, TD-SCDMA, DC-HSPA+, WCDMA, 20 MP YWW ≥ 015 [6]

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
2. FEATURE_ID combined with hardware revision number defines unique product variants.
3. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-5.
4. Date code of YWW ≥ 905 are CS devices.
5. Lot numbers 000JK9049JL.0K001 and 000JK9049MC.0K001 with date code 904 is also CS devices.
6. Date code of YWW ≥ 015 are CS devices.

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Table 4-5 Source configuration code

S value	Die	F value = J	F value = TBD	F value = TBD	F value = TBD
0	Digital	Samsung			
Other columns and rows will be added in future revisions of this document, if needed.					

4.3.2 Daisy chain devices

For daisy chain part information, contact the Qualcomm sales team for support.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Note: The appropriate MSL rating is shaded in the table.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SM7150 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM7150 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

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4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SM7150 Package Thermal Model Icepak* (HS11-PG319-5HW) and the *SM7150 Package Thermal Model FloTHERM* (HS11-PG319-6HW) from the CreatPoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PG319-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PG319-6HW

After successfully logging on, the document is downloaded.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

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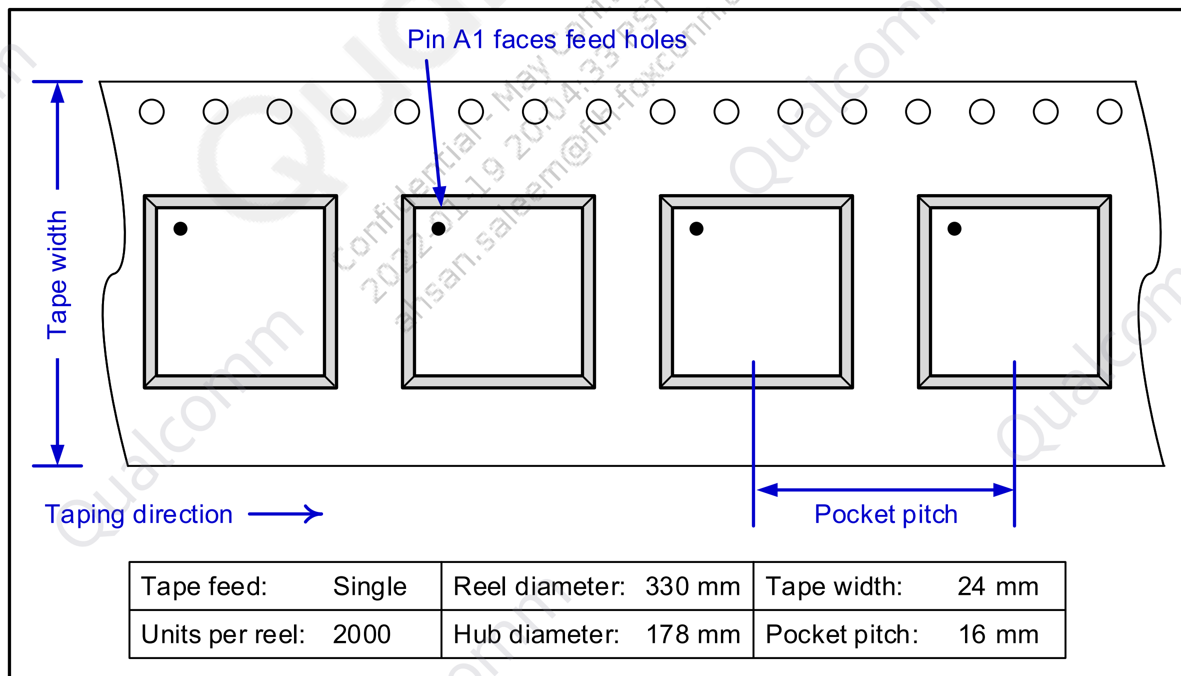
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM7150 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions



Tape feed: Single	Reel diameter: 330 mm	Tape width: 24 mm
Units per reel: 2000	Hub diameter: 178 mm	Pocket pitch: 16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

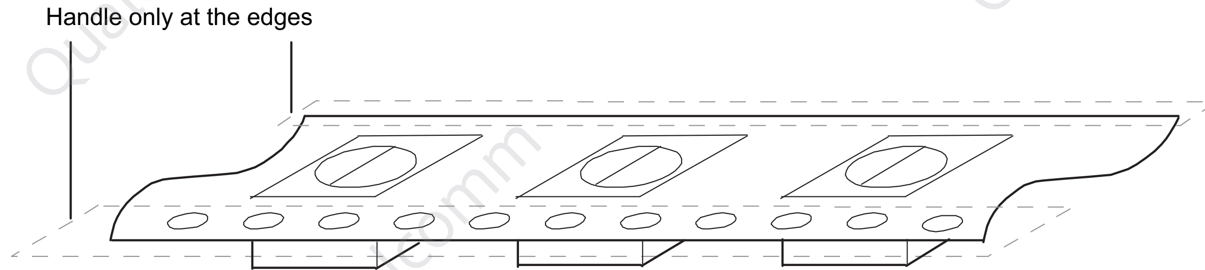


Figure 5-2 Tape handling

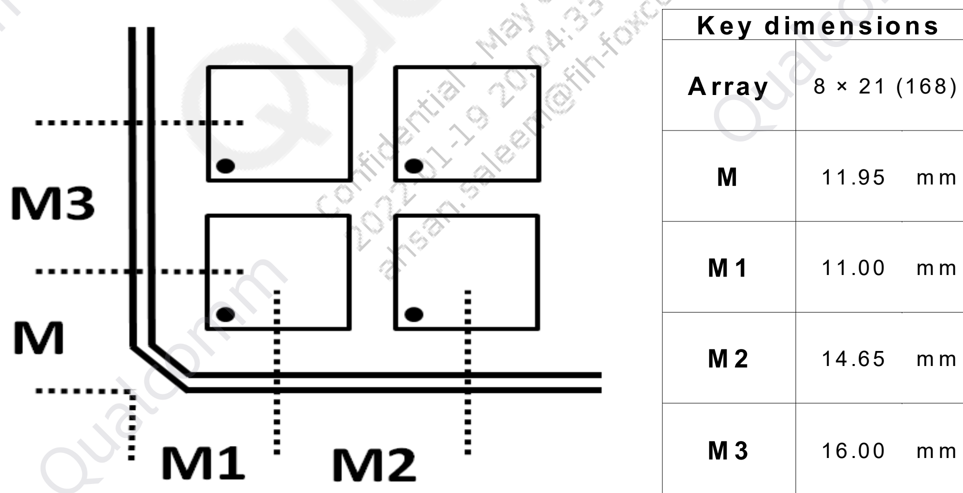
5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

Each tray of the SM7150 contains up to 168 devices. Production orders of the SM7150 that are shipped in matrix tray carriers will be in [10 + 1] tray stacks of [1680] units. The stacking configuration and quantity for sample orders will vary.

See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	8 × 21 (168)
M	11.95 mm
M1	11.00 mm
M2	14.65 mm
M3	16.00 mm

Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Storage

5.2.1 Bagged storage conditions

SM7150 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

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5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM7150 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SM7150 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

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6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy chain components

This information will be provided in a future revision of this document.

7 Part reliability

7.1 Reliability evaluation summary

Reliability evaluation report for SM7150 PSP792 device.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	288	Pass DPPM < 1000
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	288	Pass FIT < 100
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	288	> 10
ESD – Human body model (HBM) rating JS001-2017 (Total samples from one wafer lot)	3	Pass ±1 kV
ESD – Charged device model (CDM) rating JS-002-2014 (Total samples from one wafer lot)	3	Pass ±250 V
Latch-up (I-test): EIA/JESD78E Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	6	Pass class II, Level A
Latch-up (Vsupply overvoltage): EIA/JESD78E Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C (Total samples from one wafer lot)	6	Pass class II, Level A

Table 7-2 Package reliability results

Tests, standards, and conditions	SCK Sample size	ASE Sample size	SPIL Sample size	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C (Total samples from three different assembly lots)	750	750	750	Pass MSL3
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 CPH **Preconditioning:** JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	258	258	258	Pass 1000 hrs
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration *or* 110°C/85% RH and 264-hour duration Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	240	240	240	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration *or* 110°C/85% RH and 264-hour duration Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	231	231	231	Pass [1]
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (Total samples from three different assembly lots)	258	258	258	Pass 1000 hrs
Flammability Note: Flammability test – not required UL-STD-94 Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	-	See note in test column.

Table 7-2 Package reliability results (cont.)

Tests, standards, and conditions	SCK Sample size	ASE Sample size	SPIL Sample size	Results
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	30	30	30	Pass [1]
Die shear MIL-STD-883E, method 2019 (Total samples from three different assembly lots at each SAT)	30	30	30	Pass [1]
Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	30	30	30	Pass [1]
Internal/external visual (Total samples from three different assembly lots at each SAT)	30	30	30	Pass [1]

1. Data is leveraged from other previously qualified PSP packages that are similar to this configuration.

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	SM7150
Package type	PSP
Package body size	11.10 × 10.50 × 0.99 mm
Ball count	792
Ball composition	SAC125/Ni
Fab process	8 nm
Fab sites	Samsung
Assembly sites	■ ASE, Taiwan ■ SPIL, Taiwan ■ JCET STATS ChipPAC, Korea
Solder ball pitch	0.35 mm

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8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	August 2018	Initial release
B	September 2018	■ Table 1-1 *SM7150 features*: Corrected mobile display processor specification ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Updated wakeup pin functions for LPI_GPIO_19, LPI_GPIO_23, LPI_GPIO_24, LPI_GPIO_25, LPI_GPIO_26, LPI_GPIO_27, LPI_GPIO_28, and LPI_GPIO_29
C	October 2018	■ Global: Corrected package dimension ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Updated GPIO_35 ■ Section 4.1 *Device physical dimensions*: Updated package outline document number
D	December 7, 2018	■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Corrected the functional description of the following GPIO_3, GPIO_6, GPIO_7, GPIO_8, GPIO_9, GPIO_34, GPIO_35, GPIO_40, GPIO_42, GPIO_43, GPIO_44, GPIO_45, GPIO_46, GPIO_53, GPIO_60, GPIO_63, GPIO_112, and GPIO_113 pins ■ Added the following sections: □ Section 4.2 *SM7150 part marking* □ Section 4.3 *Device ordering information* □ Section 4.4 *Device moisture sensitivity level*
E	December 12, 2018	■ Updated the following tables: □ Table 3-1 *SM7150 PDN specifications* □ Table 3-2 *PDN specifications – LPDDR4X* □ Table 3-3 *PDN specifications – SerDes rails*
F	February 2019	■ Global: Updated Kryo Gold to 2.208 GHz and Kryo Silver to 1.804 GHz ■ Section 3 *Electrical specifications*: Added sections for CS related information ■ Section 4.5 *Thermal characteristics*: Updated this section ■ Section 5 *Carrier, handling, and storage information*: Added this chapter ■ Section 6 *PCB mounting guidelines*: Added this chapter ■ Section 7.1 *Reliability evaluation summary*: Added this section ■ Section 7.2 *Qualification sample description*: Updated this section ■ Table 4-3 *Device identification code*: Updated this table ■ Table 4-4 *Device identification details*: Updated this table for CS device variant

Revision	Date	Description
G	March 2019	■ Global: Updated Kryo processor to 470 ■ Table 2-4 Pin descriptions – DNC, ground, and power-supply pins: Updated pad name for pad AJ19 ■ Table 3-6 SM7150 PDN specifications: Removed pin AN21 from VDD_SSC_CX power domain ■ Table 4-4 Device identification details: Added date code for CS variants ■ Table 7-2 Package reliability results: Updated Temperature cycle and High-temperature storage life results
H	August 2020	■ Table 3-3 *Operating conditions*: Updated the maximum value for T_j or T_C ■ Table 3-9 *Dhrystone and rock bottom maximum power*: Added the Dhrystone value for an AC SKU ■ Table 4-4 *Device identification details*: Added an AC SKU for a CS sample

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