Device description

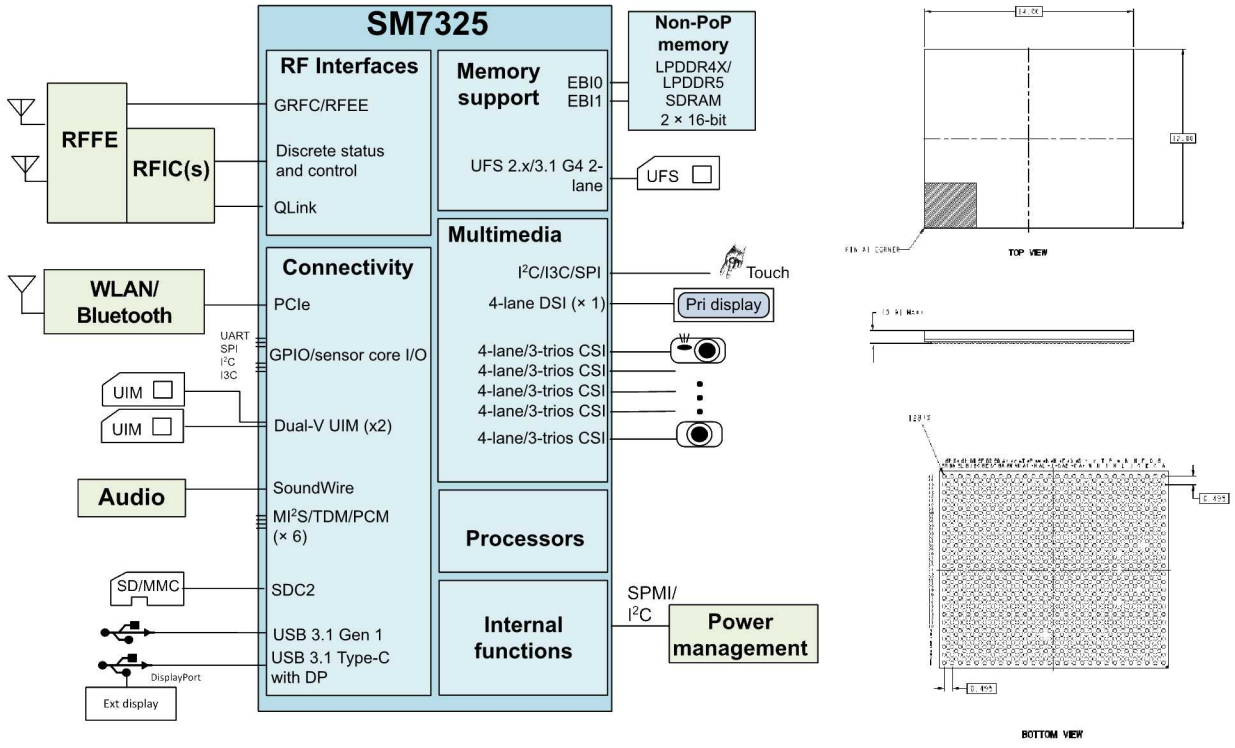
The SM7325 device is the new generation Qualcomm® Snapdragon high-tier 5G SoC with an integrated modem. It is designed with the 6 nm process, for superior performance and power efficiency. SM7325 includes the following key components:

- Qualcomm® Kryo™ CPU 6xx built on Arm v8 Cortex technology
  - Kryo Gold: Four high-performance Kryo core upto 2.4 GHz
  - Kryo Silver: Four low-power Kryo cores upto 1.8 GHz
- Qualcomm® Adreno™ GPU 6xx for better graphics performance and power efficiency
- Compute Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (HVX) and Hexagon Tensor Accelerator
- Qualcomm Spectra™ ISP 5xx image-processing engine for the ultimate photography and videography experiences
- Adreno 633 VPU for high-quality, ultra HD video encode and decode
- Adreno DPU 1075 for on-device and external ultra HD display support
- Low-power island (LPI): contains DSP and embedded AI accelerator shared between the Snapdragon sensor core and low-power audio subsystem, supporting always-on use cases like sensors and keyword detection.
- Memory: dual-channel non-package-on-package (non-PoP) high-speed LPDDR5/LPDDR4X SDRAM
  - LPDDR5 SDRAM designed for 3200 MHz clock (2 × 16 bit)
  - LPDDR4X SDRAM designed for 2133 MHz clock (2 × 16 bit)

Key features

- Always-on subsystem with RPMh for hardware-based resource and power management.
- Qualcomm® Universal Bandwidth Compression (UBWC) with camera, display, GPU, video, and compute DSP
- More RF operating bands and advanced techniques with SDR735, QTM525, and SMR526:
  - 3GPP Rel. 15 5G NR
  - mmW and sub-6 GHz 5G NR
  - UL 256 QAM and DL 256 QAM support for sub-6 GHz
  - EN-DC mode support
  - 64 QAM uplink/downlink in mmW TDD
  - Rel.15 LTE multimode modem
  - UL 256 QAM and DL 256 QAM support for LTE
  - DC-HSPA+, CDMA, WCDMA, and GSM
- Display support: FHD+, 10 bit DisplayPort, eight hardware layers, improved HDR10+, and wide color Gamut, Qualcomm® Low-Power Picture Enhancement display feature, and Qualcomm® True Palette Display feature, VESA DSC 1.2
- One 4-lane DSI DSC1.2, D-PHY 1.2, or C-PHY 1.0
- Triple 14-bit image signal processing (ISP) + two lite ISP 22 + 22 + 22 MP, 64 MP/30 fps
- Five 4-lane CSIs (4/4/4/4/4) D-PHY 1.2 or C-PHY 1.2
- Support for UFS 3.1 Gear 4 (two-lane), eMMC 5.1, SD 3.0
- Support for USB 3.1 Type-C with DisplayPort 1.4 and USB 2.0
- WLAN 2 × 2 802.11a/b/g/n/ac/ax MU-MIMO, Bluetooth 5.2, and FM

SM7325 high-level block diagram and PSP1287 outline drawing



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1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

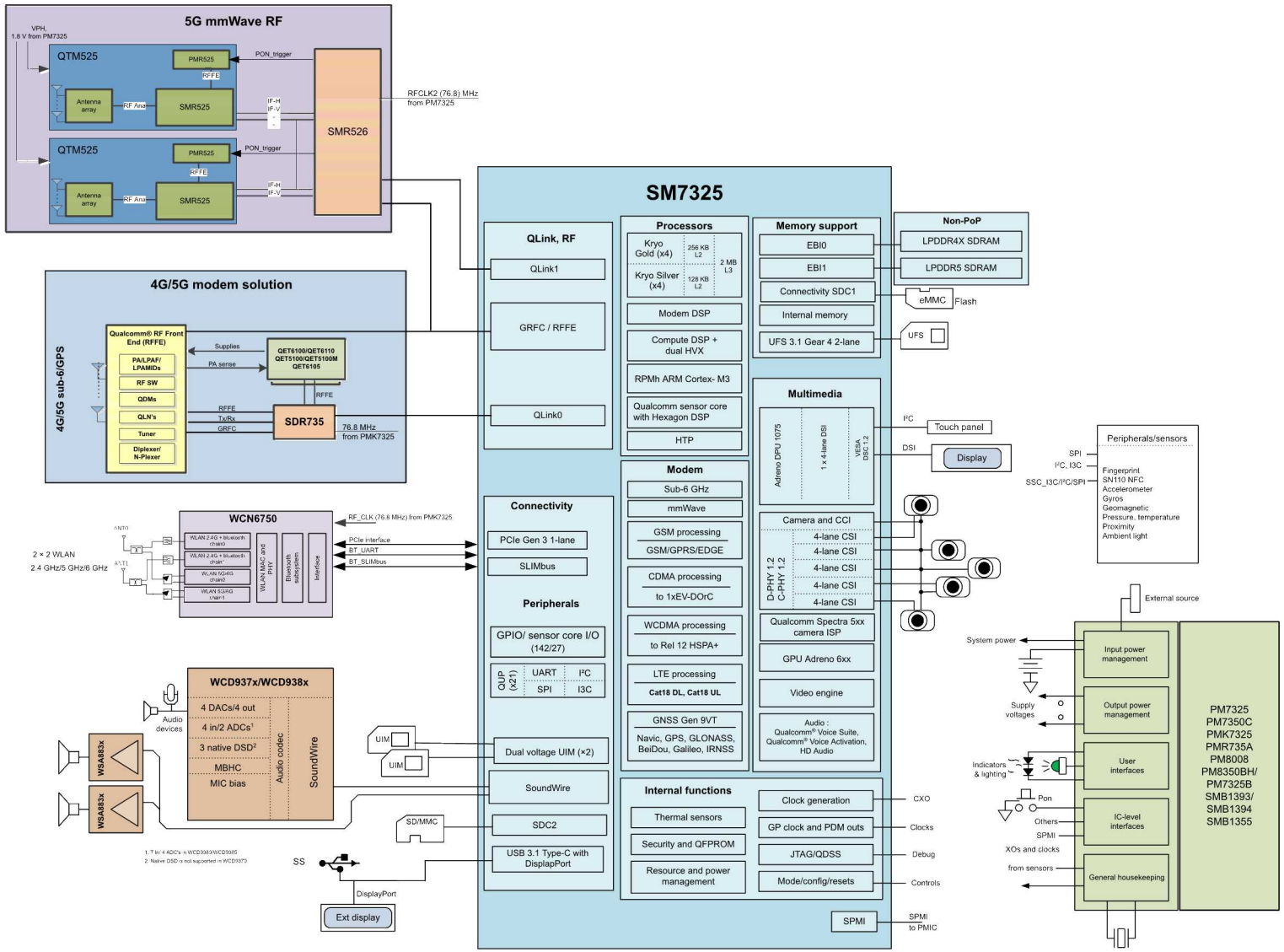


Figure 1-1 Functional block diagram

1.2 SM7325 features

NOTE Some of the hardware features integrated within the SM7325 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM7325 features.

Table 1-1 SM7325 features

Feature	SM7325 capability
Processors	
Applications	Kryo 6xx CPU built on Arm v8 Cortex technology ■ Kryo Gold: Four high-performance Kryo core upto 2.4 GHz ■ Kryo Silver: Four low-power Kryo cores upto 1.8 GHz
Digital signal processing and artificial intelligence	Compute Hexagon DSP with dual HVX and Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Low power island (LPI)	LPI with Hexagon DSP consists of Snapdragon sensor core and lowpower audio subsystem
Modem	2G/3G/4G/5G – mmWave and sub-6 GHz bands (Rel. 15) 3.7 Gbps DL, 2.5 Gbps UL, 400 MHz mmW, 120 MHz sub-6
Location	Gen 9 VT v4
Memory support	
System memory via non-PoP and EBI	■ Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM designed for a 2133 MHz (2 × 16-bit) clock ■ LPDDR5 3200 MHz (2 × 16-bit) clock
External memory Via UFS Via SDC Other internal memory	 UFS 3.1, two-lane HS gear 4 SD v3.0 4 bit for SD card and eMMC 5.1 172 KB IMEM 512 KB GMEM for graphics
RF support	
RF operating bands	Defined by the RF transceiver SDR device
Air interfaces 5G NR LTE CDMA, WCDMA, and GSM WLAN/Bluetooth Antenna sharing GNSS – Integrated Qualcomm® Location Suite engine	 Yes Yes, Rel.15 LTE multimode modem Yes Yes with WCN6750 Antenna shared between Wi-Fi and WAN Gen 9VT; GPS, GLONASS, NavIC, BeiDou, Galileo, QZSS, and SBAS

Table 1-1 SM7325 features (cont.)

Feature	SM7325 capability
Multimedia	
Display support	Adreno DPU 1075: ■ Maximum resolution for internal panel: FHD+ 144 Hz QCLTM, HDR10+, WCG, improved inline rot, rounded corner, SPR, Demura, CWB-ROI ■ One 4-lane; DSI D-PHY 1.2 or C-PHY 1.2; VESA DSC 1.2 ■ 4K60 display support over DisplayPort (USB3 + DisplayPort concurrency)
Camera support	Qualcomm Spectra 5xx: 36 + 22 MP at 30 fps/3x22 MP 30 fps ZSL Qualcomm Spectra 5xx ISP supports connectivity to multiple cameras due to five C-PHY/D-PHY interfaces. ■ Real-time sensor input resolution: 22 + 22 + 22 ■ Three IFE + two IFE lite, up to eight sensors, five concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 configuration ■ 5x D-PHY v1.2 /C-PHY v1.2
Adreno video processing unit (VPU)	Adreno VPU 633 – fifth-generation UHD video processing unit ■ Video decode: Up to 4K30 for H.264/H.265/VP9 ■ Video encode: Up to 4K30 for H.264/H.265 ■ Video concurrency: 1080p60 decode and 1080p60 encode/ 4K30 decode + 1080p30 encode ■ HDR playback: Support for HDR10 and HDR10+ ■ HFR capture: 720p at 480 fps or 1080p at 240 fps
Adreno graphic processing unit (GPU)	Adreno GPU 6xx OpenGL ES 3.2, Vulkan 1.x OpenCL 2.0, DX FL12
Audio (Low power audio subsystem)	LPI, improved voice UI concurrencies, ML hardware accelerator; V66M, LPI shared with Sensor SS ■ eNPU/AI accelerator: Embedded AI accelerator for LPI and low power use cases ■ Hardware adaptive filter enabled voice UI always by offloading echo cancellation processing ■ Hardware resampler ■ DSP offload for audio playback, including USB digital audio and Bluetooth audio
Codec	WCD9370/WCD9375/WCD9380/WCD9385 high fidelity audio codec
Speaker amplifier	WSA8830/WSA8835 class-H, low noise smart amplifier
Audio interfaces	■ SLIMbus for WCN6750 ■ SoundWire interface (two Tx and two Rx data for codec) ■ SoundWire MIC support ■ Dedicated SoundWire interface for smart speaker amplifier ■ Three DMIC ports in LPI ■ Five MI^{2}S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application ■ One MI^{2}S supports four data lanes for up to eight channels Tx/Rx application
Connectivity	
Qualcomm universal peripheral (QUP) ports	21: Multiplexed serial interface functions
USB	One USB 3.1 port: Gen 1, 5 Gbps (DisplayPort + data), support Type-C with DisplayPort v1.4
PCIe	PCIe Gen 3 1-lane

Table 1-1 SM7325 features (cont.)

Feature	SM7325 capability
Secure digital interfaces	■ Two ports (SDC1 and SDC2); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card; UFS
Touchscreen support	Capacitive panels via ext IC (I^2C, I3C, SPI, and interrupts)
Configurable GPIOs	
Number of GPIO ports	169
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
Crypto	AES-GCM, hardware ECC and RSA (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP certifiable
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure Boot with Sec tools 2.0; easy to use tool set
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted
TrustZone	Qualcomm® Trusted Execution Environment (TEE) v5.3
DRM	Widevine V16 L1, HDCP v2.3
QTEE services	ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
Boot sequence	1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) rest of subsystems Emergency boot over USB 3.1
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Chipset interface features	
QLink	Two QLink0/1 ports for sub-6 and mmWave applications
Power management	2-line SPMI; plus other lines, as needed, via GPIOs, I^2C PM7325, PM7350C, PMK7325, PMR735A, PM8008, PM8350BH/PM7325B, SMB1393/SMB1394, SMB1355
Wireless connectivity	
WLAN	PCIe interface
Bluetooth	SLIMbus/UART interface
Fabrication technology and package	
Digital die	6 nm process
Non-PoP – small, thermally efficient package	14.0 × 12.0 × 0.91 mm

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
3GPP 5G Rel.15	▪ Sub-6 GHz, 5G NR - FDD < 3 GHz, TDD frequencies n77, n78, and n79 ▪ Standalone mode (SA) and non-standalone mode (NSA) support ▪ 256 QAM for uplink and downlink ▪ DL 4 × 4 MIMO and UL 2 × 2 UL MIMO support for sub-6 ▪ EN-DC mode support ▪ NR CA support
	▪ mmW – n257, n258, n260, and n261 ▪ TDD only ▪ 64 QAM for uplink (UL)/downlink (DL)
3GPP LTE Rel.15	▪ Cat18 download and upload ▪ TM9 (FDD up to four Tx, TDD up to eight Tx) ▪ Four-way Rx diversity ▪ 4 × 4 MIMO using single LTE TRx, LTE-U, and LAA ▪ UL: 256 QAM; DL: 256 QAM for LTE
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	▪ 1x SLTE and 1x SRLTE ▪ hVoLTE and hSRLTE ▪ VoNR support
Multi-SIM	
MSIM	5G/4G/3G/2G (SIM1) + 4G/3G/2G (SIM2)
5G + 5G	5G (SIM1) + 5G (SIM2) DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/5G - Wi-Fi selection

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite with global navigation satellite system (GNSS) support	
Gen 9VT	GPS, GLONASS, NavIC, BeiDou, Galileo, QZSS, and SBAS

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN6750	802.11ax, 2 × 2 MIMO (Wi-Fi 6E)
Bluetooth	
With WCN6750	Bluetooth 5.2 compliant

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX0	Power for pad group 0
PX1	Power for pad group 1
PX2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX3	Pad group 3 (most peripherals); 1.8 V
PX5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX7	Pad group 7 (eMMC); tied to VDD_PX7 pins (1.8 V only)
PX10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_A_CSI_X_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_A_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The SM7325 is available in the PSP1287. See Mechanical information for package details. A high-level view of the pin assignments is shown in the following figure. The text within the figure is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM7325 Pin Assignment and GPIO Configuration Spreadsheet* (80-19448-1A). This Microsoft Excel spreadsheet lists all SM7325 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the pin assignment spreadsheet (80-19448-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-19448-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

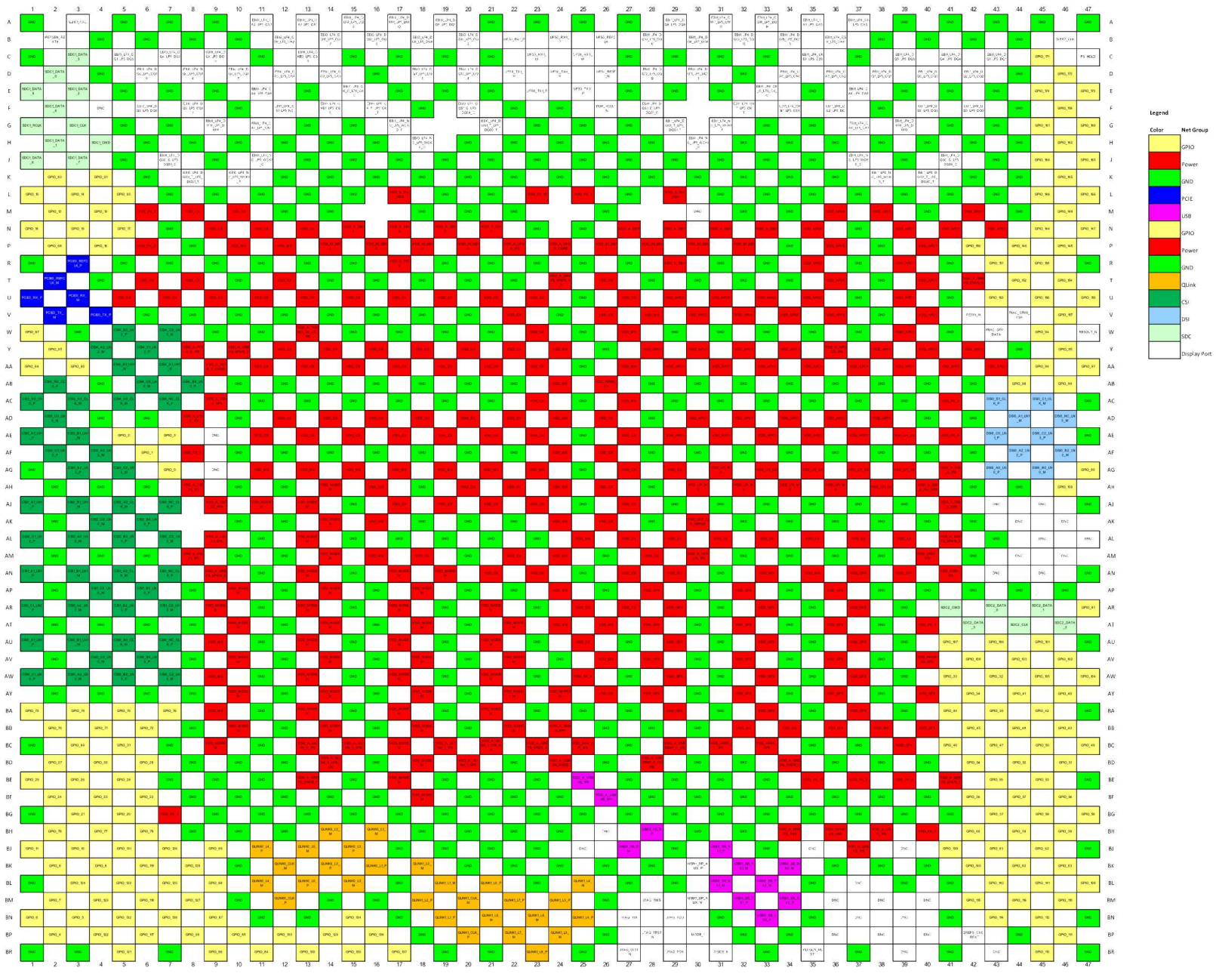


Figure 2-1 SM7325 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AU5	CSI0_A0_CLK_M	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
AU1	CSI0_A1_LN1_P	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
AW3	CSI0_A2_LN2_M	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
AV6	CSI0_B0_LN0_P	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY), trio lane 0 – B
AU3	CSI0_B1_LN1_M	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
AW5	CSI0_B2_LN3_P	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
AV4	CSI0_C0_LN0_M	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
AW1	CSI0_C1_LN2_P	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
AW7	CSI0_C2_LN3_M	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
AU7	CSI0_NC_CLK_P	CSI	AI AI, AO	MIPI CSI 0 (D-PHY), differential clock – positive MIPI CSI 0 (C-PHY), no connect
AN5	CSI1_A0_CLK_M	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A
AN1	CSI1_A1_LN1_P	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A
AR3	CSI1_A2_LN2_M	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A
AP6	CSI1_B0_LN0_P	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 – positive MIPI CSI 1 (C-PHY), trio lane 0 – B
AN3	CSI1_B1_LN1_M	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B
AR5	CSI1_B2_LN3_P	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B
AP4	CSI1_C0_LN0_M	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AR1	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C
AR7	CSI1_C2_LN3_M	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C
AN7	CSI1_NC_CLK_P	CSI	AI AI, AO	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
AJ5	CSI2_A0_CLK_M	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential clock – negative MIPI CSI 2 (C-PHY), trio lane 0 – A
AJ1	CSI2_A1_LN1_P	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 – positive MIPI CSI 2 (C-PHY), trio lane 1 – A
AL3	CSI2_A2_LN2_M	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – negative MIPI CSI 2 (C-PHY), trio lane 2 – A
AK6	CSI2_B0_LN0_P	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
AJ3	CSI2_B1_LN1_M	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 – negative MIPI CSI 2 (C-PHY), trio lane 1 – B
AL5	CSI2_B2_LN3_P	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – positive MIPI CSI 2 (C-PHY), trio lane 2 – B
AK4	CSI2_C0_LN0_M	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 – negative MIPI CSI 2 (C-PHY), trio lane 0 – C
AL1	CSI2_C1_LN2_P	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 – positive MIPI CSI 2 (C-PHY), trio lane 1 – C
AL7	CSI2_C2_LN3_M	CSI	AI AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 – negative MIPI CSI 2 (C-PHY), trio lane 2 – C
AJ7	CSI2_NC_CLK_P	CSI	AI AI, AO	MIPI CSI 2 (C-PHY), no connect MIPI CSI 2 (D-PHY), differential clock – positive
AC3	CSI3_A0_CLK_M	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A
AE1	CSI3_A1_LN1_P	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A
AF4	CSI3_A2_LN2_M	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A
AC1	CSI3_B0_LN0_P	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B
AE3	CSI3_B1_LN1_M	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B
AG3	CSI3_B2_LN3_P	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AD2	CSI3_C0_LN0_M	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C
AF2	CSI3_C1_LN2_P	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C
AG5	CSI3_C2_LN3_M	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C
AB2	CSI3_NC_CLK_P	CSI	AI AI, AO	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect
AC5	CSI4_A0_CLK_M	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential clock – negative MIPI CSI 4 (C-PHY), trio lane 0 – A
AA7	CSI4_A1_LN1_P	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 – positive MIPI CSI 4 (C-PHY), trio lane 1 – A
Y4	CSI4_A2_LN2_M	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 – negative MIPI CSI 4 (C-PHY), trio lane 2 – A
AB8	CSI4_B0_LN0_P	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 – positive MIPI CSI 4 (C-PHY), trio lane 0 – B
AA5	CSI4_B1_LN1_M	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 – negative MIPI CSI 4 (C-PHY), trio lane 1 – B
W5	CSI4_B2_LN3_P	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 – positive MIPI CSI 4 (C-PHY), trio lane 2 – B
AB6	CSI4_C0_LN0_M	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 – negative MIPI CSI 4 (C-PHY), trio lane 0 – C
Y6	CSI4_C1_LN2_P	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 – positive MIPI CSI 4 (C-PHY), trio lane 1 – C
W7	CSI4_C2_LN3_M	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 – negative MIPI CSI 4 (C-PHY), trio lane 2 – C
AC7	CSI4_NC_CLK_P	CSI	AI AI, AO	MIPI CSI 4 (D-PHY), differential clock – positive MIPI CSI 4 (C-PHY), no connect
BR43	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
F26	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
BM30	USB0_DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – negative
BK30	USB0_DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – positive
AG43	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 – positive MIPI DSI 0 (C-PHY), trio lane 0 – A
AD44	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 – negative MIPI DSI 0 (C-PHY), trio lane 1 – A
AF44	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 – positive MIPI DSI 0 (C-PHY), trio lane 2 – A

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AG45	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 – negative MIPI DSI 0 (C-PHY), trio lane 0 – B
AC43	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock – positive MIPI DSI 0 (C-PHY), trio lane 1 – B
AF46	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 – negative MIPI DSI 0 (C-PHY), trio lane 2 – B
AE43	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 – positive MIPI DSI 0 (C-PHY), trio lane 0– C
AC45	DSI0_C1_CLK_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock – negative MIPI DSI 0 (C-PHY), trio lane 1 – C
AE45	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 – positive MIPI DSI 0 (C-PHY), trio lane 2 – C
AD46	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 – negative MIPI DSI 0 (C-PHY), no connect
A3	EBI01_CAL	EBI	AI	EBI 0/1 LPDDRx calibration resistor
D14	EBI0_LP4_CA0_LP5_CA0	EBI	DO	EBI0 LPDDR4X command/address bit 0 EBI0 LPDDR5 command/address bit 0
A13	EBI0_LP4_CA1_LP5_CA1	EBI	DO	EBI0 LPDDR4X command/address bit 1 EBI0 LPDDR5 command/address bit 1
B12	EBI0_LP4_CS0_LP5_CA2	EBI	DO	EBI0 LPDDR4X chip select 0 EBI0 LPDDR5 command/address bit 2
A11	EBI0_LP4_CA2_LP5_CA3	EBI	DO	EBI0 LPDDR4X command/address bit 2 EBI0 LPDDR5 command/address bit 3
D12	EBI0_LP4_CA3_LP5_CA4	EBI	DO	EBI0 LPDDR4X command/address bit 3 EBI0 LPDDR5 command/address bit 4
E11	EBI0_LP4_CA4_LP5_CA5	EBI	DO	EBI0 LPDDR4X command/address bit 4 EBI0 LPDDR5 command/address bit 5
G11	EBI0_LP4_CA5_LP5_CA6	EBI	DO	EBI0 LPDDR4X command/address bit 5 EBI0 LPDDR5 command/address bit 6
F14	EBI0_LP4_CKE1_LP5_CS0	EBI	DO	EBI0 LPDDR4X clock enable 1 EBI0 LPDDR5 chip select 0
C13	EBI0_LP4_CKE0_LP5_CS1	EBI	DO	EBI0 LPDDR4X clock enable 0 EBI0 LPDDR5 chip select 1
F12	EBI0_LP4_CS1_LP5_NC	EBI	DO	EBI0 LPDDR4 chip select 1
E15	EBI0_LP4_CK_C_LP5_CK_C	EBI	DO	EBI0 LPDDR4X differential clock – negative EBI0 LPDDR5 differential clock – negative
F16	EBI0_LP4_CK_T_LP5_CK_T	EBI	DO	EBI0 LPDDR4X differential clock – positive EBI0 LPDDR5 differential clock – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
A17	EBI0_LP4_DMI1_LP5_DMI0	EBI	DO	EBI0 LPDDR4X data mask inversion 1 EBI0 LPDDR5 data mask inversion 0
G9	EBI0_LP4_DMI0_LP5_DMI1	EBI	DO	EBI0 LPDDR4X data mask inversion 0 EBI0 LPDDR5 data mask inversion 1
F20	EBI0_LP4_DQS1_C_LP5_DQS0_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 negative EBI0 LPDDR5 differential data strobe for byte 0 negative
J7	EBI0_LP4_DQS0_C_LP5_DQS1_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 negative EBI0 LPDDR5 differential data strobe for byte 1 negative
G21	EBI0_LP4_DQS1_T_LP5_DQS0_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 positive EBI0 LPDDR5 differential data strobe for byte 0 positive
K8	EBI0_LP4_DQS0_T_LP5_DQS1_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 positive EBI0 LPDDR5 differential data strobe for byte 1 positive
B18	EBI0_LP4_DQ8_LP5_DQ0	EBI	B	EBI0 LPDDR4X data bit 8 EBI0 LPDDR5 data bit 0
A19	EBI0_LP4_DQ9_LP5_DQ1	EBI	B	EBI0 LPDDR4X data bit 9 EBI0 LPDDR5 data bit 1
B20	EBI0_LP4_DQ10_LP5_DQ2	EBI	B	EBI0 LPDDR4X data bit 10 EBI0 LPDDR5 data bit 2
D18	EBI0_LP4_DQ11_LP5_DQ3	EBI	B	EBI0 LPDDR4X data bit 11 EBI0 LPDDR5 data bit 3
D20	EBI0_LP4_DQ12_LP5_DQ4	EBI	B	EBI0 LPDDR4X data bit 12 EBI0 LPDDR5 data bit 4
B16	EBI0_LP4_DQ13_LP5_DQ5	EBI	B	EBI0 LPDDR4X data bit 13 EBI0 LPDDR5 data bit 5
A15	EBI0_LP4_DQ14_LP5_DQ6	EBI	B	EBI0 LPDDR4X data bit 14 EBI0 LPDDR5 data bit 6
B14	EBI0_LP4_DQ15_LP5_DQ7	EBI	B	EBI0 LPDDR4X data bit 15 EBI0 LPDDR5 data bit 7
F6	EBI0_LP4_DQ0_LP5_DQ8	EBI	B	EBI0 LPDDR4X data bit 0 EBI0 LPDDR5 data bit 8
C5	EBI0_LP4_DQ1_LP5_DQ9	EBI	B	EBI0 LPDDR4X data bit 1 EBI0 LPDDR5 data bit 9
D6	EBI0_LP4_DQ2_LP5_DQ10	EBI	B	EBI0 LPDDR4X data bit 2 EBI0 LPDDR5 data bit 10

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
F8	EBI0_LP4_DQ3_LP5_DQ11	EBI	B	EBI0 LPDDR4X data bit 3 EBI0 LPDDR5 data bit 11
C7	EBI0_LP4_DQ4_LP5_DQ12	EBI	B	EBI0 LPDDR4X data bit 4 EBI0 LPDDR5 data bit 12
C9	EBI0_LP4_DQ5_LP5_DQ13	EBI	B	EBI0 LPDDR4X data bit 5 EBI0 LPDDR5 data bit 13
D8	EBI0_LP4_DQ6_LP5_DQ14	EBI	B	EBI0 LPDDR4X data bit 6 EBI0 LPDDR5 data bit 14
D10	EBI0_LP4_DQ7_LP5_DQ15	EBI	B	EBI0 LPDDR4X data bit 7 EBI0 LPDDR5 data bit 15
H18	EBI0_LP4_NC_LP5_WCK0_C	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 negative
J11	EBI0_LP4_NC_LP5_WCK1_C	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 negative
G17	EBI0_LP4_NC_LP5_WCK0_T	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 positive
K10	EBI0_LP4_NC_LP5_WCK1_T	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 positive
E37	EBI1_LP4_CA5_LP5_CA0	EBI	DO	EBI1 LPDDR4X command/address bit 5 EBI1 LPDDR5 command/address bit 0
G37	EBI1_LP4_CA4_LP5_CA1	EBI	DO	EBI1 LPDDR4X command/address bit 4 EBI1 LPDDR5 command/address bit 1
D36	EBI1_LP4_CA3_LP5_CA2	EBI	DO	EBI1 LPDDR4X command/address bit 3 EBI1 LPDDR5 command/address bit 2
A37	EBI1_LP4_CS1_LP5_CA3	EBI	DO	EBI1 LPDDR4X chip select 1 EBI1 LPDDR5 command/address bit 3
B36	EBI1_LP4_CS0_LP5_CA4	EBI	DO	EBI1 LPDDR4X chip select 0 EBI1 LPDDR5 command/address bit 4
A35	EBI1_LP4_CA1_LP5_CA5	EBI	DO	EBI1 LPDDR4X command/address bit 1 EBI1 LPDDR5 command/address bit 5
D34	EBI1_LP4_CA0_LP5_CA6	EBI	DO	EBI1 LPDDR4X command/address bit 0 EBI1 LPDDR5 command/address bit 6
C35	EBI1_LP4_CKE0_LP5_CS0	EBI	DO	EBI1 LPDDR4X clock enable 0 EBI1 LPDDR5 chip select 0
F34	EBI1_LP4_CKE1_LP5_CS1	EBI	DO	EBI1 LPDDR4X clock enable 1 EBI1 LPDDR5 chip select 1
F36	EBI1_LP4_CA2_LP5_NC	EBI	DO	EBI1 LPDDR4X command/address bit 2
E33	EBI1_LP4_CK_C_LP5_CK_C	EBI	DO	EBI1 LPDDR4X differential clock – negative EBI1 LPDDR5 differential clock – negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
F32	EBI1_LP4_CK_T_LP5_CK_T	EBI	DO	EBI1 LPDDR4X differential clock – positive EBI1 LPDDR5 differential clock – positive
G39	EBI1_LP4_DMI0_LP5_DMI0	EBI	DO	EBI1 LPDDR4X data mask 0 EBI1 LPDDR5 data mask 0
A31	EBI1_LP4_DMI1_LP5_DMI1	EBI	DO	EBI1 LPDDR4X data mask 1 EBI1 LPDDR5 data mask 1
J41	EBI1_LP4_DQS0_C_LP5_DQS0_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 negative EBI1 LPDDR5 differential data strobe for byte 0 negative
F28	EBI1_LP4_DQS1_C_LP5_DQS1_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 negative EBI1 LPDDR5 differential data strobe for byte 1 negative
K40	EBI1_LP4_DQS0_T_LP5_DQS0_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 positive EBI1 LPDDR5 differential data strobe for byte 0 positive
G29	EBI1_LP4_DQS1_T_LP5_DQS1_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 positive EBI1 LPDDR5 differential data strobe for byte 1 positive
F42	EBI1_LP4_DQ0_LP5_DQ0	EBI	B	EBI1 LPDDR4X data bit 0 EBI1 LPDDR5 data bit 0
C43	EBI1_LP4_DQ1_LP5_DQ1	EBI	B	EBI1 LPDDR4X data bit 1 EBI1 LPDDR5 data bit 1
D42	EBI1_LP4_DQ2_LP5_DQ2	EBI	B	EBI1 LPDDR4X data bit 2 EBI1 LPDDR5 data bit 2
F40	EBI1_LP4_DQ3_LP5_DQ3	EBI	B	EBI1 LPDDR4X data bit 3 EBI1 LPDDR5 data bit 3
C41	EBI1_LP4_DQ4_LP5_DQ4	EBI	B	EBI1 LPDDR4X data bit 4 EBI1 LPDDR5 data bit 4
C39	EBI1_LP4_DQ5_LP5_DQ5	EBI	B	EBI1 LPDDR4X data bit 5 EBI1 LPDDR5 data bit 5
D40	EBI1_LP4_DQ6_LP5_DQ6	EBI	B	EBI1 LPDDR4X data bit 6 EBI1 LPDDR5 data bit 6
D38	EBI1_LP4_DQ7_LP5_DQ7	EBI	B	EBI1 LPDDR4X data bit 7 EBI1 LPDDR5 data bit 7
B30	EBI1_LP4_DQ8_LP5_DQ8	EBI	B	EBI1 LPDDR4X data bit 8 EBI1 LPDDR5 data bit 8
A29	EBI1_LP4_DQ9_LP5_DQ9	EBI	B	EBI1 LPDDR4X data bit 9 EBI1 LPDDR5 data bit 9

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B28	EBI1_LP4_DQ10_LP5_DQ10	EBI	B	EBI1 LPDDR4X data bit 10 EBI1 LPDDR5 data bit 10
D30	EBI1_LP4_DQ11_LP5_DQ11	EBI	B	EBI1 LPDDR4X data bit 11 EBI1 LPDDR5 data bit 11
D28	EBI1_LP4_DQ12_LP5_DQ12	EBI	B	EBI1 LPDDR4X data bit 12 EBI1 LPDDR5 data bit 12
B32	EBI1_LP4_DQ13_LP5_DQ13	EBI	B	EBI1 LPDDR4X data bit 13 EBI1 LPDDR5 data bit 13
A33	EBI1_LP4_DQ14_LP5_DQ14	EBI	B	EBI1 LPDDR4X data bit 14 EBI1 LPDDR5 data bit 14
B34	EBI1_LP4_DQ15_LP5_DQ15	EBI	B	EBI1 LPDDR4X data bit 15 EBI1 LPDDR5 data bit 15
J37	EBI1_LP4_NC_LP5_WCK0_C	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 negative
H30	EBI1_LP4_NC_LP5_WCK1_C	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 negative
K38	EBI1_LP4_NC_LP5_WCK0_T	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 positive
G31	EBI1_LP4_NC_LP5_WCK1_T	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 positive
BR31	MODE_0	PX_3	DI	Mode control bit 0 – unconnected for native mode
BP30	MODE_1	PX_3	DI	Mode control bit 1 – unconnected for native mode
T2	PCIE0_REFCLK_M	–	AI, AO	PCIe 0 Gen 3 reference clock – negative
R3	PCIE0_REFCLK_P	–	AI, AO	PCIe 0 Gen 3 reference clock – positive
U3	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – negative
U1	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – positive
V2	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – negative
V4	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – positive
V44	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
W43	PMIC_SPMI_DATA	PX_0	BH-PD:nppukp	Slave and PBUS interface for PMICs – data
C47	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
BK12	QLINK0_CLK_M	–	AI, AO	QLink0 clock – negative
BM12	QLINK0_CLK_P	–	AI, AO	QLink0 clock – positive
BH14	QLINK0_L2_M	–	AI, AO	QLink0 lane 2 – negative
BK14	QLINK0_L2_P	–	AI, AO	QLink0 lane 2 – positive
BL11	QLINK0_L4_M	–	AI, AO	QLink0 lane 4 – negative
BJ11	QLINK0_L4_P	–	AI, AO	QLink0 lane 4 – positive
BL15	QLINK0_L3_M	–	AI, AO	QLink0 lane 3 – negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
BJ15	QLINK0_L3_P	–	AI, AO	QLink0 lane 3 – positive
BJ13	QLINK0_L0_M	–	AI, AO	QLink0 lane 0 – negative
BL13	QLINK0_L0_P	–	AI, AO	QLink0 lane 0 – positive
BH16	QLINK0_L1_M	–	AI, AO	QLink0 lane 1 – negative
BK16	QLINK0_L1_P	–	AI, AO	QLink0 lane 1 – positive
BM20	QLINK1_CLK_M	–	AI, AO	QLink1 clock – negative
BP20	QLINK1_CLK_P	–	AI, AO	QLink1 clock – positive
BP22	QLINK1_L7_M	–	AI, AO	QLink0 lane 7 – negative
BM22	QLINK1_L7_P	–	AI, AO	QLink0 lane 7 – positive
BL19	QLINK1_L1_M	–	AI, AO	QLink1 lane 1 – negative
BN19	QLINK1_L1_P	–	AI, AO	QLink1 lane 1 – positive
BK18	QLINK1_L2_M	–	AI, AO	QLink1 lane 2 – negative
BM18	QLINK1_L2_P	–	AI, AO	QLink1 lane 2 – positive
BN23	QLINK1_L8_M	–	AI, AO	QLink1 lane 8 – negative
BR23	QLINK1_L8_P	–	AI, AO	QLink1 lane 8 – positive
BN21	QLINK1_L0_M	–	AI, AO	QLink1 lane 0 – negative
BL21	QLINK1_L0_P	–	AI, AO	QLink1 lane 0 – positive
BP24	QLINK1_L3_M	–	AI, AO	QLink1 lane 3 – negative
BM24	QLINK1_L3_P	–	AI, AO	QLink1 lane 3 – positive
BL25	QLINK1_L4_M	–	AI, AO	QLink1 lane 4 – negative
BN25	QLINK1_L4_P	–	AI, AO	QLink1 lane 4 – positive
BP42	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-die clocking
B2	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
BR35	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
V42	RESIN_N	PX_0	DI	Reset input
W47	RESOUT_N	PX_3	DO	Reset output
G3	SDC1_CLK	PX_7	DO-NP:pdpukp	Secure digital controller 1 clock
H4	SDC1_CMD	PX_7	B-NP:pdpukp	Secure digital controller 1 command
D2	SDC1_DATA0	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 0
H2	SDC1_DATA1	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 1
E3	SDC1_DATA2	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 2

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
C3	SDC1_DATA3	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 3
F2	SDC1_DATA4	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 4
E1	SDC1_DATA5	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 5
J1	SDC1_DATA6	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 6
J3	SDC1_DATA7	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 7
G1	SDC1_RCLK	PX_7	DI-PD:pdpukp	Secure digital controller 1 return clock
AT44	SDC2_CLK	PX_2	DO-NP:pdpukp	Secure digital controller 2 clock
AR41	SDC2_CMD	PX_2	BH-NP:pdpukp	Secure digital controller 2 command
AR43	SDC2_DATA0	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 0
AR45	SDC2_DATA1	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 1
AT46	SDC2_DATA2	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 2
AT42	SDC2_DATA3	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 3
B46	SLEEP_CLK	PX_3	DI	Sleep clock
BR27	JTAG_SRST_N	PX_3	DI-PU:nppdkp	JTAG reset for debug
BR29	JTAG_TCK	PX_3	DI-PU:nppdkp	JTAG clock input
BN27	JTAG_TDI	PX_3	DI-PU:nppdkp	JTAG data input
BN29	JTAG_TDO	PX_3	DO-Z	JTAG data output
BM28	JTAG_TMS	PX_3	DI-PU:nppdkp	JTAG mode select input

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
BP28	JTAG_TRST_N	PX_3	DI-PU:nppdkp	JTAG reset
C25	UFS_RX0_M	–	AI	UFS lane 0 receiver – negative
B24	UFS_RX0_P	–	AI	UFS lane 0 receiver – positive
D24	UFS_TX0_M	–	AO	UFS lane 0 transmit – negative
E25	UFS_TX0_P	–	AO	UFS lane 0 transmit – positive
C23	UFS_RX1_M	–	AI	UFS lane 1 receiver – negative
B22	UFS_RX1_P	–	AI	UFS lane 1 receiver – positive
D22	UFS_TX1_M	–	AO	UFS lane 1 transmit – negative
E23	UFS_TX1_P	–	AO	UFS lane 1 transmit – positive
B26	UFS0_REFCLK	PX_10	DO-Z:PD:nppukp	UFS reference clock
D26	UFS0_RESET_N	PX_10	DO-Z:PD:nppukp	UFS reset
BJ27	USB0_HS_DM	–	AI, AO	USB 2.0 high-speed data – negative
BH28	USB0_HS_DP	–	AI, AO	USB 2.0 high-speed data – positive
BK34	USB0_SS_RX0_M	–	AI	USB 3.0 Type-C PHY receiver 0 – negative
BM34	USB0_SS_RX0_P	–	AI	USB 3.0 Type-C PHY receiver 0 – positive
BL31	USB0_SS_RX1_M	–	AI	USB 3.0 Type-C PHY receiver 1 – negative
BJ31	USB0_SS_RX1_P	–	AI	USB 3.0 Type-C PHY receiver 1 – positive
BL33	USB0_SS_TX0_M	–	AO	USB 3.0 Type-C PHY transmit 0 – negative
BN33	USB0_SS_TX0_P	–	AO	USB 3.0 Type-C PHY transmit 0 – positive
BK32	USB0_SS_TX1_M	–	AO	USB 3.0 Type-C PHY transmit 1 – negative
BM32	USB0_SS_TX1_P	–	AO	USB 3.0 Type-C PHY transmit 1 – positive

[a] See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See the following table for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down

- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM7325 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the *SM7325 Pin Assignment and GPIO Configuration Spreadsheet* (80-19448-1A) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-19448-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AG7	GPIO_0		PX_3	PD:nppuk	Configurable I/O	Y
		UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP 0 SE0, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO	
		I3C_SDA		B	QUP 0 SE0, lane 0: I3C_SDA	
AF6	GPIO_1		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP 0 SE0, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 0 SE0, lane 1: I3C_SCL	
AE5	GPIO_2		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP 0 SE0, lane 2: UART_TX	
		SPI_SCLK		DO	QUP 0 SE0, lane 2: SPI_SCLK	
		SPI_CS_1		DO	QUP 0 SE7, lane 4: SPI_CS_1	
		QDSS_GPIO_TRACEDATA_LOCA(0)		DO	QDSS trace data bit 0 A	
AE7	GPIO_3		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE0, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE0, lane 3: SPI_CS_0	
		SPI_CS_2		DO	QUP0 SE7, lane 5: SPI_CS_2	
		QDSS_GPIO_TRACEDATA_LOCA(1)		DO	QDSS trace data bit 1 A	
BP2	GPIO_4		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE1, lane 0 UART_CTS	
		I2C_SDA		B	QUP0 SE1, lane 0 I2C_SDA	
		SPI_MISO		DI	QUP0 SE1, lane 0 SPI_MISO	
		I3C_SDA		B	QUP 0 SE1, lane 0: I3C_SDA	
BN3	GPIO_5		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_RFR		DO	QUP0 SE1, lane 1:UART_RFR	
		I2C_SCL		DO	QUP0 SE1, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE1, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 0 SE1, lane 1: I3C_SCL	
BN1	GPIO_6		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE1, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE1, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP0 SE7, lane 6: SPI_CS_3	
BM2	GPIO_7		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE1, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE1, lane 3: SPI_CS_0	
BK4	GPIO_8		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE2, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE2, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE2, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA(2)		DO	QDSS trace data bit 2 A	
BK2	GPIO_9		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE2, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE2, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE2, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA(3)		DO	QDSS trace data bit 3 A	
BJ3	GPIO_10		PX_3	PD:nppukp	Configurable I/O	N
		GNSS_L1_ELNA_EN		DO	eLNA enable for L1	
		UART_TX		DO	QUP0 SE2, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE2, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA(4)		DO	QDSS trace data bit 4 A	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BJ1	GPIO_11		PX_3	PD:nppukp	Configurable I/O	Y
		GNSS_L2_L5_ELNA_EN		DO	eLNA enable for L2_L5	
		UART_RX		DI	QUP0 SE2, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE2, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA(5)		DO	QDSS trace data bit 5 A	
M2	GPIO_12		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE3, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE3, lane 0: I2C_SDA	
		QDSS_GPIO_TRACECTL_LOCA		DO	QDSS trace control A	
M4	GPIO_13		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE3, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE3, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE3, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACECLK_LOCA		DO	QDSS trace clock A	
L3	GPIO_14		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE3, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE3, lane 2: SPI_SCLK	
		BOOT_CONFIG(12)		DI	Boot configuration control bit 12	
L1	GPIO_15		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE3, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE3, lane 3: SPI_CS_0	
		QDSS_CTI_TRIG0_OUT_MIRA		DO	QDSS trigger output 0 A	
		BOOT_CONFIG(9)		DI	Boot configuration control bit 9	
P4	GPIO_16		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE4, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE4, lane 0: I2C_SDA	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		SPI_MISO		DI	QUP0 SE4, lane 0: SPI_MISO	
		QDSS_CTI_TRIG1_OUT_MIRA		DO	QDSS trigger output 1 A	
N5	GPIO_17		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE4, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE4, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE4, lane 1: SPI_MOSI	
N1	GPIO_18		PX_3	PD:nppukp	Configurable I/O	Y
		UART_TX		DO	QUP0 SE4, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE4, lane 2: SPI_SCLK	
		QDSS_CTI_TRIG1_IN_MIRA		DI	QDSS trigger input 1 A	
N3	GPIO_19		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE4, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE4, lane 3: SPI_CS_0	
BG5	GPIO_20		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE5, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE5, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE5, lane 0: SPI_MISO	
		CCI_TIMER0		DO	Camera control interface timer	
		QDSS_GPIO_TRACEDATA_LOCA(6)		DO	QDSS trace data 6	
BG3	GPIO_21		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP0 SE5, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE5, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP 0 SE5, lane 1: SPI_MOSI	
		CCI_TIMER1		DO	Camera control interface timer 1	
		QDSS_GPIO_TRACEDATA_LOCA(7)		DO	QDSS trace data 7	
BF6	GPIO_22		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_TX		DO	QUP0 SE5, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE5, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA(8)		DO	QDSS trace data 8	
BF4	GPIO_23		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE5, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE5, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA(9)		DO	QDSS trace data 9	
BF2	GPIO_24		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE6, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE6, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE6, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA(10)		DO	QDSS trace data bit 10 A	
BE1	GPIO_25		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP0 SE6, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE6, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE6, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA(11)		DO	QDSS trace data bit 11 A	
BE3	GPIO_26		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE6, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE6, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA(12)		DO	QDSS trace data bit 12 A	
BD2	GPIO_27		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE6, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA(13)		DO	QDSS trace data 13	
BE5	GPIO_28		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_CTS		DI	QUP0 SE7, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE7, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE7, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA(14)		DO	QDSS trace data 14	
BD6	GPIO_29		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE7, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE7, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE7, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA(15)		DO	QDSS trace data bit 15 A	
BD4	GPIO_30		PX_3	PU:nppdkp	Configurable I/O	N
		UART_TX		DO	QUP0 SE7, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE7, lane 2: SPI_SCLK	
BC5	GPIO_31		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE7, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE7, lane 3: SPI_CS_0	
AW43	GPIO_32		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE0, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE0, lane 0: SPI_MISO	
		QUP_SPMI_DATA		B		
AW41	GPIO_33		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE0, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE0, lane 1: SPI_MOSI	
		QUP_SPMI_CLK		DO		
AY42	GPIO_34		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_TX		DO	QUP1 SE0, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE0, lane 2: SPI_SCLK	
BA43	GPIO_35		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE0, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE0, lane 3: SPI_CS_0	
BF42	GPIO_36		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE1, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE1, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE1, lane 0: SPI_MISO	
		I3C_SDA		B	QUP 1SE1, lane 0: I3C_SDA	
BG43	GPIO_37		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE1, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE1, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE1, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 1SE1, lane 1: I3C_SCL	
BH46	GPIO_38		PX_3	PU:nppdkp	Configurable I/O	N
		UART_TX		DO	QUP1 SE1, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE1, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP1 SE4, lane 6: SPI_CS_3	
BH44	GPIO_39		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE1, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE1, lane 3: SPI_CS_0	
AY46	GPIO_40		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE2, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE2, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE2, lane 0: SPI_MISO	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AY44	GPIO_41		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE2, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE2, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE2, lane 1: SPI_MOSI	
BA45	GPIO_42		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE2, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE2, lane 2: SPI_SCLK	
BB46	GPIO_43		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE2, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE2, lane 3: SPI_CS_0	
BA41	GPIO_44		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE3, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE3, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE3, lane 0: SPI_MISO	
BB42	GPIO_45		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE3, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE3, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE3, lane 1: SPI_MOSI	
BC41	GPIO_46		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE3, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE3, lane 2: SPI_SCLK	
BC43	GPIO_47		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE3, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE3, lane 3: SPI_CS_0	
		DP_HOT_PLUG_DETECT		DI	DisplayPort hot plug detect	
BB44	GPIO_48		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_CTS		DI	QUP1 SE4, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE4, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE4, lane 0: SPI_MISO	
BC47	GPIO_49		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE4, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE4, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE4, lane 1: SPI_MOSI	
BC45	GPIO_50		PX_3	PD-nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE4, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE4, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP1 SE6, lane 6: SPI_CS_3	
BD46	GPIO_51		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE4, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE4, lane 3: SPI_CS_0	
BD44	GPIO_52		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE5, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE5, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE5, lane 0: SPI_MISO	
BE45	GPIO_53		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE5, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE5, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE5, lane 1: SPI_MOSI	
BD42	GPIO_54		PX_3	PD:nppukp	Configurable I/O	Y
		UART_TX		DO	QUP1 SE5, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE5, lane 2: SPI_SCLK	
		SPI_CS_2		DO	QUP1 SE4, lane 5: SPI_CS_2	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BE43	GPIO_55		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE5, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE5, lane 3: SPI_CS_0	
		SPI_CS_1		DO	QUP1 SE4, lane 4: SPI_CS_1	
BF46	GPIO_56		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE6, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE6, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE6, lane 0: SPI_MISO	
BF44	GPIO_57		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE6, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE6, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE6, lane 1: SPI_MOSI	
BG47	GPIO_58		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE6, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE6, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACECTL_LOCB		DO	QDSS trace control B	
BG45	GPIO_59		PX_3	PU:nppdkp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE6, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACECLK_LOCB		DO	QDSS trace clock B	
BH42	GPIO_60		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE7, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE7, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE7, lane 0: SPI_MISO	
BJ43	GPIO_61		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE7, lane 1: UART_RFR	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		I2C_SCL		DO	QUP1 SE7, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE7, lane 1: SPI_MOSI	
		SD_WRITE_PROTECT		DO	Secure digital card write protection	
BJ45	GPIO_62		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE7, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE7, lane 2: SPI_SCLK	
		SPI_CS_1		DO	QUP1 SE6, lane 4: SPI_CS_1	
BK46	GPIO_63		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE6, lane 3: SPI_CS_0	
		SPI_CS_2		DO	QUP1 SE6, lane 5: SPI_CS_2	
		BOOT_CONFIG(11)		DI	Boot configuration control bit 11	
AA1	GPIO_64		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK0		DO	Camera master clock 0	
Y2	GPIO_65		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK1		DO	Camera master clock 1	
AA3	GPIO_66		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK2		DO	Camera master clock 2	
W1	GPIO_67		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK3		DO	Camera master clock 3	
P2	GPIO_68		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK4		DO	Camera master clock 4	
BC3	GPIO_69		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0		B	Dedicated camera control interface I²C serial data	
BB2	GPIO_70		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		CCI_I2C_SCL0		DO	Dedicated camera control interface I²C clock	
BB4	GPIO_71		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1		B	Dedicated camera control interface I²C 1 serial data	
BB6	GPIO_72		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SCL1		DO	Dedicated camera control interface I²C 1 clock	
BA1	GPIO_73		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2		B	Dedicated camera control interface I²C 2 serial data	
BA3	GPIO_74		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2		DO	Dedicated camera control interface I²C 2 clock	
BA5	GPIO_75		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SDA3		B	Dedicated camera control interface I²C 3 serial data	
BA7	GPIO_76		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL3		DO	Dedicated camera control interface I²C 3 clock	
		GCC_GP1_CLK_MIRB		DO	Global general purpose clock 1 B	
BH4	GPIO_77		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER2		DO	Camera control interface timer 2	
		GCC_GP2_CLK_MIRB		DO	General purpose clock 2 B	
BH2	GPIO_78		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3		DO	Camera control interface timer 3	
		CCI_ASYNC_IN1		DI	Camera control interface async 1	
		GCC_GP3_CLK_MIRB		DO	General purpose clock 3 B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BH6	GPIO_79		PX_3	PU:nppdkp	Configurable I/O	Y
		CCI_TIMER4		DO	Camera control interface timer 4	
		CCI_ASYNC_IN2		DI	Camera control interface async 2	
		PCIE1_CLKREQN		DI	PCIe1 clock request signal	
		MDP_VSYNC_E		DI	MDP vertical sync – external	
AG47	GPIO_80		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA		DI	MDP vertical sync – primary	
		MDP_VSYNC0_OUT		DO	MDP vertical sync 0 output	
		MDP_VSYNC1_OUT		DO	MDP vertical sync 1 output	
		MDP_VSYNC4_OUT		DO	MDP vertical sync 4 output	
AR47	GPIO_81		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA		DI	MDP vertical sync – secondary	
		MDP_VSYNC2_OUT		DO	MDP vertical sync 2 output	
		MDP_VSYNC3_OUT		DO	MDP vertical sync 3 output	
		MDP_VSYNC5_OUT		DO	MDP vertical sync 5 output	
BK44	GPIO_82		PX_3	PD:nppukp	Configurable I/O	Y
		FORCED_USB_BOOT		DI	Forced USB boot	
K2	GPIO_83		PX_3	PD:nppukp	Configurable I/O	Y
		BOOT_CONFIG[8]		DI	Boot configuration control bit 8	
BR11	GPIO_84		PX_3	PD:nppukp	Configurable I/O	N
		USB2PHY_AC_EN0		DO	USB AC coupling 0 control	
BP10	GPIO_85		PX_3	PD:nppukp	Configurable I/O	N
		USB2PHY_AC_EN1		DO	USB AC coupling 1 control	
BR9	GPIO_86	–	PX_3	PD:nppukp	Configurable I/O	Y
BN9	GPIO_87	–	PX_3	PD:nppukp	Configurable I/O	N
BL9	GPIO_88		PX_3	PU:nppdkp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		PCIE0_CLKREQN		DI	PCIe clock request	
BJ9	GPIO_89	–	PX_3	PD:nppukp	Configurable I/O	Y
BP8	GPIO_90	–	PX_3	PD:nppukp	Configurable I/O	Y
K4	GPIO_91	–	PX_3	PD:nppukp	Configurable I/O	Y
L5	GPIO_93		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK5		DO	Camera master clock 5	
		CCI_ASYNC_IN0		DI	Camera control interface async	
		BOOT_CONFIG[13]		DI	Boot configuration control bit 13	
W45	GPIO_94		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_CLK		B	Low-power audio SLIMbus clock	
Y46	GPIO_95		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA0		B	Low-power audio SLIMbus data 0	
AA45	GPIO_96		PX_3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_MCLK		DO	Primary MI²S master clock	
AA47	GPIO_97		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_SCK		DO	MI²S 0 clock	
AB44	GPIO_98		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_DATA0		B	MI²S 0 serial data channel 0	
AB46	GPIO_99		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_DATA1		B	MI²S 0 serial data channel 1	
AH46	GPIO_100		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_WS		B	MI²S 0 serial data word select	
AU45	GPIO_101		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_SCK		B	MI²S 2 clock	
		QDSS_GPIO_TRACEDATA_LOCB[0]		DO	QDSS trace data bit 0 B	
AV46	GPIO_102		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		MI2S2_DATA0		B	MI²S 2 serial data channel 0	
		GP_PDM_MIRA[0]		DO	General purpose PDM output 0 A	
		QDSS_GPIO_TRACEDATA_LOCB[1]		DO	QDSS trace data bit 1 B	
AV44	GPIO_103		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_WS		B	MI²S 2 serial data word select	
		GP_PDM_MIRA[1]		DO	General purpose PDM output 1 A	
		QDSS_GPIO_TRACEDATA_LOCB[2]		DO	QDSS trace data bit 2 B	
AW47	GPIO_104		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_DATA1		B	MI²S 2 serial data channel 1	
		GP_PDM_MIRA[2]		DO	General purpose PDM output 2 A	
		QDSS_GPIO_TRACEDATA_LOCB[3]		DO	QDSS trace data bit 3	
AW45	GPIO_105		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_MCLK		DO	Secondary MI²S master clock	
		MI2S1_DATA1		B	MI²S 1 serial data channel 1	
		AUDIO_REF_CLK		DI	Audio reference clock	
		GCC_GP1_CLK_MIRA		A	General purpose clock 1 A	
		QDSS_GPIO_TRACEDATA_LOCB[4]		DO	QDSS trace data bit 4 B	
AU43	GPIO_106		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_SCK		B	MI²S 1 clock	
		GCC_GP2_CLK_MIRA		DO	General purpose clock 2 A	
		QDSS_GPIO_TRACEDATA_LOCB[5]		DO	QDSS trace data bit 5 B	
AU41	GPIO_107		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_DATA0		B	MI²S 1 serial data channel 0	
		GCC_GP3_CLK_MIRA		DO	General purpose clock 3 A	
		QDSS_GPIO_TRACEDATA_LOCB[6]		DO	QDSS trace data bit 6 B	
AV42	GPIO_108		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		MI2S1_WS		B	MI²S 1 serial word select	
		QDSS_GPIO_TRACEDATA_LOCB[7]		DO	QDSS trace data bit 7 B	
BL47	GPIO_109		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_DATA		B	UIM1 data (dual voltage)	
BM46	GPIO_110		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_CLK		DO	UIM1 clock (dual voltage)	
BP46	GPIO_111		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_RESET		DO	UIM1 reset (dual voltage)	
BN45	GPIO_112		PX_3	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT		DI	UIM1 presence detection	
BR45	GPIO_113		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_DATA		B	UIM0 data (dual voltage)	
BN43	GPIO_114		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_CLK		DO	UIM0 clock (dual voltage)	
BM42	GPIO_115		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_RESET		DO	UIM0_RESET	
BM44	GPIO_116		PX_3	PD:nppukp	Configurable I/O	Y
		UIM0_PRESENT		DI	UIM0 presence detection	
BP6	GPIO_117		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE0_CLK		DO	RF front end interface clock	
		GRFC0		DO	Generic RF controller bit 0	
BM6	GPIO_118		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA		B	RF front end 0 interface data	
		GRFC1		DO	Generic RF controller bit 1	
		BOOT_CONFIG[0]		DI	Boot configuration control bit 0	
BK6	GPIO_119		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		RFFE1_CLK		DO	RF front end 1 interface clock	
		GRFC2		DO	Generic RF controller bit 2	
BL5	GPIO_120		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_DATA		B	RF front end 1 interface data	
		GRFC3		DO	Generic RF controller bit 3	
		BOOT_CONFIG[1]		DI	Boot configuration control bit 1	
BR5	GPIO_121		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE2_CLK		DO	RF front end 2 interface clock	
		GRFC4		DO	Generic RF controller bit 4	
BP4	GPIO_122		PX_3	PD:nppukp	Configurable I/O	N
		RFFE2_DATA		B	RF front end 1 interface data	
		GRFC5		DO	Generic RF controller bit 3	
		BOOT_CONFIG[2]		DI	Boot configuration control bit 2	
BM4	GPIO_123		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE3_CLK		DO	RF front end 3 interface clock	
		GRFC6		DO	Generic RF controller bit 6	
BL3	GPIO_124		PX_3	PD:nppukp	Configurable I/O	N
		RFFE3_DATA		B	RF front end 3 interface data	
		GRFC7		DO	Generic RF controller bit 7	
		BOOT_CONFIG[3]		DI	Boot configuration control bit 3	
BL7	GPIO_125		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE4_CLK		DO	RF front end 4interface clock	
		GRFC8		DO	Generic RF controller bit 8	
BJ7	GPIO_126		PX_3	PD:nppukp	Configurable I/O	N
		RFFE4_DATA		B	RF front end 4 interface data	
		GRFC9		DO	Generic RF controller bit 9	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		BOOT_CONFIG[4]		DI	Boot configuration control bit 4	
BM8	GPIO_127		PX_3	PD:nppukp	Configurable I/O	Y
		WLAN_COEX_UART1_RX		DI	Interface between WCN and SM7325	
		GRFC10		DO	Generic RF controller bit 10	
BK8	GPIO_128		PX_3	PD:nppukp	Configurable I/O	Y
		WLAN_COEX_UART1_TX		DO	Interface between WCN and SM7325	
		GRFC11		DO	Generic RF controller bit 11	
		BOOT_CONFIG[10]		DI	Boot configuration control bit 10	
BP14	GPIO_129		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_0		B	Generic input/output 0 for GNSS	
BR13	GPIO_130		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_1		B	Generic input/output 1 for GNSS	
		BOOT_CONFIG[7]		DI	Boot configuration control bit 7	
BJ5	GPIO_131		PX_3	PD:nppukp	Configurable I/O	Y
		GRFC12		DO	Generic RF controller bit 12	
		PA_INDICATOR_1_OR_2		DO	PA transmit indicator	
		NAV_GPIO_2		B	Generic input/output 2 for GNSS	
		BOOT_CONFIG[5]		DI	Boot configuration control bit 5	
BN5	GPIO_132		PX_3	PD:nppukp	Configurable I/O	N
		GRFC0_MIRA		DO	Generic RF controller bit 0 A	
		BOOT_CONFIG[6]		DI	Boot configuration control bit 6	
BP12	GPIO_133		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK0_REQUEST		DI	QLink0 request	
BN15	GPIO_134		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_ENABLE		DO	QLink0 enable	
BR15	GPIO_135		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		QLINK0_WMSS_RESET_N		DO	QLINK0 SDR modem subsystem reset output	
		BOOT_CONFIG[14]		DI	Boot configuration control bit 14	
BP16	GPIO_136		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK1_REQUEST		DI	QLink1 request	
BR17	GPIO_137		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_ENABLE		DO	QLink1 enable	
BN7	GPIO_138		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_WMSS_RESET_N		DO	QLINK1 SDR modem subsystem reset output	
		BOOT_CONFIG[15]		DI	Boot configuration control bit 15	
BJ41	GPIO_139		PX_3	PD:nppukp	Configurable I/O	N
		FORCED_USB_BOOT_POLARITY_ SEL		DI	Forced USB boot parity select	
BK42	GPIO_140		PX_3	PD:nppukp	Configurable I/O	Y
		USB_PHY_PS		DI	USB PHY port select	
BL45	GPIO_141	_	PX_3	PD:nppukp	Configurable I/O	Y
BL43	GPIO_142	_	PX_3	PD:nppukp	Configurable I/O	Y
N45	GPIO_144		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_0 [b]		B	LPI GPIO 0	
		SWR_TX_CLK		DO	SoundWire transmit clock	
		LPI_QUA_MI2S_SCK		B	LPI quaternary MI²S clock 0	
P46	GPIO_145		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_1		B	LPI GPIO 1	
		SWR_TX_DATA0		DO	SoundWire transmit data 0	
		LPI_QUA_MI2S_WS		B	LPI quaternary MI²S word select	
P44	GPIO_146		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_GPIO_2		B	LPI GPIO 2	
		SWR_TX_DATA1		DO	SoundWire transmit data 1	
		LPI_QUA_MI2S_DATA0		B	LPI quaternary MI²S data 0	
N47	GPIO_147		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_3		B	LPI GPIO 3	
		SWR_RX_CLK		DI	SoundWire receive clock	
		LPI_QUA_MI2S_DATA1		B	LPI quaternary MI²S data 1	
L45	GPIO_148		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_4		B	LPI GPIO 4	
		SWR_RX_DATA0		DI	SoundWire receive data 0	
		LPI_QUA_MI2S_DATA2		B	LPI quaternary MI²S data 2	
M46	GPIO_149		PX_3	PD:nppuk	Configurable I/O	N
		LPI_GPIO_5		B	LPI GPIO 5	
		SWR_RX_DATA1		DI	SoundWire receive data 1	
		EXT_MCLK1_C		DO	External master clock 1 C	
		LPI_QUA_MI2S_DATA3		B	LPI quaternary MI²S data 3	
P42	GPIO_150		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data bit 8 A	
		LPI_GPIO_6		B	LPI GPIO 6	
		LPI_DMIC1_CLK		DO	LPI DMIC 1 Clock	
		LPI_I2S1_CLK		B	LPI I2S 1 clock	
R43	GPIO_151		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data bit 9 A	
		LPI_GPIO_7		B	LPI GPIO 7	
		LPI_DMIC1_DATA		DI	LPI DMIC 1 Data	
		LPI_I2S1_WS		B	LPI I2S 1 word select	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
T44	GPIO_152		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCA[10]		DO	QDSS trace data bit 10 A	
		LPI_GPIO_8		B	LPI GPIO 8	
		LPI_DMIC2_CLK		DO	LPI DMIC 2 clock	
		LPI_I2S1_DATA0		B	LPI I2S 1 Data 0	
U43	GPIO_153		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[11]		DO	QDSS trace data bit 11 A	
		LPI_GPIO_9		B	LPI GPIO 9	
		LPI_DMIC2_DATA		DI	LPI DMIC 2 data	
		LPI_I2S1_DATA1		B	LPI I2S 1 Data 1	
		EXT_MCLK1_B		DO	External master clock 1 B	
T46	GPIO_154		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_10		B	LPI GPIO 10	
		LPI_I2S2_CLK		B	LPI MI²S 2 clock	
		WSA_SWR_CLK		DO	SoundWire clock for WSA	
U47	GPIO_155		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_11		B	LPI GPIO 11	
		LPI_I2S2_WS		B	LPI I2S 2 Word select	
		WSA_SWR_DATA		B	SoundWire data for WSA	
U45	GPIO_156		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG0_IN_MIRB		DI	QDSS trigger input 0 B	
		LPI_GPIO_12		B	LPI GPIO 12	
		LPI_DMIC3_CLK		DO	LPI DMIC 3 clock	
		LPI_I2S2_DATA0		B	LPI I2S 2 Data 0	
V46	GPIO_157		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG1_IN_MIRB		DI	QDSS trigger input 1 B	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_GPIO_13		B	LPI GPIO 13	
		LPI_DMIC3_DATA		DO	LPI DMIC 3 data	
		LPI_I2S2_DATA1		B	LPI I2S 2 data 1	
		EXT_MCLK1_A		DO	External master clock 1 A	
R45	GPIO_158		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_14		B	LPI GPIO 14	
		SWR_TX_DATA2		DO	SoundWire transmit data 2	
F46	GPIO_159		PX_3	PD:nppuk	Configurable I/O	N
		LPI_GPIO_15 [c]		B	LPI GPIO 15	
		LPI_I2C_SDA		B	LPI_QUP0 SE0, lane 0: I2C_SDA	
		LPI_I3C_SDA		B	LPI_QUP0 SE0, lane 0: I3C_SDA	
		SYNC_OUT_GPIO_0		DO	Sync out GPIO_0	
G47	GPIO_160		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_16		B	LPI GPIO 16	
		LPI_I2C_SCL		DO	LPI_QUP0 SE0, lane 1: I2C_SCL	
		LPI_I3C_SCL		DO	LPI_QUP0 SE0, lane 1: I3C_SCL	
		SYNC_OUT_GPIO_1		DO	Sync out GPIO_1	
G45	GPIO_161		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_17		B	LPI GPIO 17	
		LPI_I2C_SDA		B	LPI_QUP0 SE1, lane 0: I2C_SDA	
		LPI_I3C_SDA		B	LPI_QUP0 SE1, lane 0: I3C_SDA	
		SPI_CS_1		DO	LPI_QUP0 SE2, lane 4: SPI_CS_1	
		SYNC_OUT_GPIO_2		DO	Sync out GPIO_2	
H46	GPIO_162		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_18		B	LPI GPIO 18	
		LPI_I2C_SCL		DO	LPI_QUP0 SE1, lane 1: I2C_SCL	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_I3C_SCL		DO	LPI_QUP0 SE1, lane 1: I3C_SCL	
		SYNC_OUT_GPIO_3		DO	Sync out GPIO_3	
J47	GPIO_163		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_19		B	LPI GPIO 19	
		LPI_UART_CTS		DI	LPI_QUP0 SE2, lane 0: UART_CTS	
		LPI_I2C_SDA		B	LPI_QUP0 SE2, lane 0: I2C_SDA	
		LPI_SPI_MISO		DI	LPI_QUP0 SE2, lane 0: SPI_MISO	
		SYNC_OUT_GPIO_4		DO	Sync out GPIO_4	
J45	GPIO_164		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_20		B	LPI GPIO 20	
		LPI_UART_RFR		DO	LPI_QUP0 SE2, lane 1: UART_RFR	
		LPI_I2C_SCL		DO	LPI_QUP0 SE2, lane 1: I2C_SCL	
		LPI_SPI_MOSI		DO	LPI_QUP0 SE2, lane 1: SPI_MOSI	
		SYNC_OUT_GPIO_5		DO	Sync out GPIO_5	
K46	GPIO_165		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_CTI_TRIG0_OUT_MIRB		DO	QDSS trigger output 0 B	
		LPI_GPIO_21		B	LPI GPIO 21	
		LPI_UART_TX		DO	LPI_QUP0 SE2, lane 2: UART_TX	
		LPI_SPI_SCLK		DO	LPI_QUP0 SE2, lane 2: SPI_SCLK	
		SYNC_OUT_GPIO_6		DO	Sync out GPIO_6	
L47	GPIO_166		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG1_OUT_MIRB		DO	QDSS trigger output 1 B	
		LPI_GPIO_22		B	LPI GPIO 22	
		LPI_UART_RX		DI	LPI_QUP0 SE2, lane 3: UART_RX	
		LPI_SPI_CS_0		DO	LPI_QUP0 SE2, lane 3: SPI_CS_0	
		SYNC_OUT_GPIO_7		DO	Sync out GPIO_7	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
C45	GPIO_171		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCB[12]		DO	QDSS trace data bit 12 B	
		LPI_GPIO_23		B	LPI GPIO 23	
		LPI_I2C_SDA		B	LPI_QUP0 SE5, lane 0: I2C_SDA	
		LPI_UART_TX		DO	LPI_QUP0 SE5, lane 2: UART_TX	
		SYNC_OUT_GPIO_12		DO	Sync out GPIO_12	
D46	GPIO_172		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[13]		DO	QDSS trace data bit 13 B	
		LPI_GPIO_24		B	LPI GPIO 24	
		LPI_I2C_SCL		DO	LPI_QUP0 SE5, lane 1: I2C_SCL	
		LPI_UART_RX		DI	LPI_QUP0 SE5, lane 3: UART_RX	
		SYNC_OUT_GPIO_13		DO	Sync out GPIO_13	
E47	GPIO_173		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCB[14]		DO	QDSS trace data bit 14 B	
		LPI_GPIO_25		B	LPI GPIO 25	
		LPI_UART_TX		DO	LPI_QUP0 SE6, lane 2: UART_TX	
		SYNC_OUT_GPIO_14		DO	Sync out GPIO_14	
E45	GPIO_174		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[15]		DO	QDSS trace data bit 15 B	
		LPI_GPIO_26		B	LPI GPIO 26	
		LPI_UART_RX		DI	LPI_QUP0 SE6, lane 3: UART_RX	
		SYNC_OUT_GPIO_15		DO	Sync out GPIO_15	

[a] See Table 2-1 for parameter and acronym definitions.
[b] LPI_GPIO_144 to LPI_GPIO_158 supports LPASS application (15 LPI GPIOs)
[c] LPI_GPIO_159 to LPI_GPIO_174 supports SSC application (12 LPI GPIOs)

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad number	Pad name	Functional description
AG9, AE9, M30, BJ39, F4, BJ35, AN45, AN43, AM46, AM44,AL47, AL45, AK46, AK44, AJ45, AJ43, BJ25, BH26, BP36, BM36,BM40, BP40, BN37, BL37, BN39, BR39, BM38, BP38	DNC	Do not connect; connected internally, do not connect externally.
A1, A5, A7, A9, A21, A23, A25, A27, A39, A41, A43, A45, A47,AA25, AB4, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB28, AB30, AB32, AB34, AB36, AB38, AB40, AB42, AC11, AC13, AC15, AC17, AC19, AC21, AC25, AC29, AC31, AC33, AC35, AC37, AC39, AC47, AD4, AD6, AD10, AD28, AD40, AD42, AE25, AE47, AF10, AF12, AF14, AF16, AF18, AF20,AF22, AF28, AF30, AF32, AF34, AF36, AF38, AF40, AF42, AG1, AG25, AH2, AH4, AH6, AH10, AH12, AH18, AH28, AH42, AH44, AJ15, AJ25, AJ29, AJ31, AJ33, AJ35, AJ37, AJ39, AJ47, AK2, AK10, AK12, AK18, AK20, AK22, AK28, AK32, AK34, AK36, AK38, AK40, AK42, AL11, AL15, AL17, AL19, AL21, AL23, AL43, AM2, AM4, AM6, AM10, AM12, AM20, AM26, AM32, AM34, AM36, AM38, AM42, AN11, AN15, AN25, AN31, AN47, AP2, AP8, AP12, AP16, AP20, AP22, AP26, AP30, AP34, AP38, AP40, AP42, AP44, AP46, AR11, AR15, AR19, AR23, AR31, AR35, AR39, AT2, AT4, AT6, AT8, AT12, AT16, AT20, AT30, AT34, AT38, AU11, AU15, AU19, AU23, AU27, AU31, AU35, AU39, AU47, AV2, AV8, AV12, AV16, AV20, AV24, AV30, AV34, AV38, AW11, AW15, AW19, AW23, AW27, AW31, AW35, AW39, AY2, AY4, AY6, AY8, AY12, AY16, AY20, AY30, AY34, AY38, B4, B6, B8, B10, B38, B40, B42, B44, BA11, BA15, BA19, BA23, BA25, BA27, BA31, BA35, BA39, BA47, BB8, BB12, BB16, BB20, BB26, BB28, BB30, BC1, BC7, BC11, BC27, BC35, BC37, BD8, BD10, BD12, BD16, BD22, BD26, BD30, BD32, BD36, BD38, BD40, BE7, BE9, BE11, BE15, BE19, BE21, BE23, BE27, BE29, BE31, BE33, BE47, BF8, BF10, BF12, BF14, BF16, BF20, BF22, BF24, BF28, BF30, BF32, BF34, BF36, BF38, BF40, BG1, BG9, BG11, BG13, BG15, BG17, BG19, BG21, BG23, BG25, BG27, BG29, BG31, BG33, BG35, BG37, BG39, BG41, BH8, BH10, BH12, BH18, BH20, BH22, BH24, BH30, BH32, BJ17, BJ19, BJ21, BJ23, BJ29, BJ33, BJ47, BK10, BK20, BK22, BK24, BK26, BK28, BK36, BK38, BK40, BL1, BL17, BL23, BL27, BL29, BL35, BL39, BL41, BM10, BM14, BM16, BM26, BN11, BN13, BN17, BN31, BN35, BN41, BN47, BP18, BP26, BP32, BP34, BP44, BR1, BR3, BR7, BR19, BR21, BR25, BR33, BR37, BR41, BR47, C1, C11, C15, C17, C19, C21, C27, C29, C31, C33, C37, D4, D16, D32, D44, E5, E7, E9, E13, E17, E19, E21, E27, E29, E31, E35, E39, E41, E43, F10, F18, F22, F24, F38, F44, G5, G7, G13, G15, G23,	GND	Ground

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
G25, G27, G33, G35, G41, G43, H6, H8, H10, H12, H14, H16, H20, H22, H24, H26, H28, H32, H34, H36, H38, H40, H42, H44, J5, J9, J13, J15, J17, J19, J21, J23, J25, J27, J29, J31, J33, J35, J39, J43, K6, K12, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K34, K36, K42, K44, L7, L9, L11, L13, L15, L19, L21, L27, L31, L33, L35, L37, L39, L41, L43, M12, M14, M18, M20, M22, M26, M32, M34, M40, M44, N7, N23, N25, N37, P8, P34, P38, R1, R5, R7, R9, R11, R13, R15, R19, R21, R23, R25, R27, R31, R33, R37, R41, R47, T4, T10, T14, T16, T18, T20, T22, T28, T30, T32, T34, T38, U25, U37, U41, V6, V8, V10, V12, V14, V16, V18, V20, V24, V38, W3, W9, W11,W15, W17, W19, W21, W25, W29, W31, W33, W35, W37, W41,Y26, Y44		
Y36	VDD_A_APC_CS_1P8	Power for application processor current sensor; 1.8 V circuits
AL9	VDD_A_CSI_01_0P9	Power for CSI 0, 1: 0.9 V circuits
AM8	VDD_A_CSI_01_1P2	Power for CSI 0, 1: 1.2 V circuits
AJ9	VDD_A_CSI_23_0P9	Power for CSI 2, 3: 0.9 V circuits
AH8	VDD_A_CSI_23_1P2	Power for CSI 2, 3: 1.2 V circuits
AC9	VDD_A_CSI_4_0P9	Power for CSI 4: 0.9 V circuits
AD8	VDD_A_CSI_4_1P2	Power for CSI 4: 1.2 V circuits
BH38	VDD_A_CXO_1P8	Power for 1.8 V clock circuits
N15, N17, N19, N21	VDD_A_EBI0	Power for EBI PHY circuits
N27, N29, N31, N33	VDD_A_EBI1	Power for EBI PHY circuits
AM30	VDD_A_GFX_CS_1P8	Power for graphics current sensor circuits
L17	VDD_A_PLL_EBI0	Power for EBI0 PLL circuits
L29	VDD_A_PLL_EBI1	Power for EBI1 PLL circuits
W13	VDD_A_TURING_Q6_CS_1P8	Power for Q6 current sensor1.8 V circuits
W23, Y14, Y16, V26, V22, Y18, Y20, Y22, Y12, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AC23, AD12, AD14, AD16, AD18, AD20, AD22, AD26, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE27, AF26, AG27, AG29, AH20, AH22, AH26, AJ17, AJ19, AJ21, AJ23, AJ27, AK26, AL27, AL29, AL31, AL33, AL35, AL37, AL39, AM18, AM22, AM28, AN21, AN23, AN27, AR25, AR27, AU25, AY26, M8, M10, N9, N11, N13, T6, T8, T12, T26, U5, U7, U9, U11, U13, U15, U17, U19, U21, U23, U27	VDD_CX	Power for digital core circuits
R17	VDD_D_EBI0	Power for EBI0 digital circuits
R29	VDD_D_EBI1	Power for EBI1 digital circuits
P14, P16, P18, P20	VDD_IO_EBI0	Power for EBI0 I/O circuits
P26, P28, P30, P32	VDD_IO_EBI1	Power for EBI1 I/O circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
AA27, AB24, AC27, AD24, AF24, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AH16, AH24, AK16, AK24, AL25, AM16, AM24, AN29, AN33, AN35, AP24, AT24, AT26, AU9, AV26, AW9, BA9, BB32, BB34, BB36, BB38, P10, P12, V28, Y24, W27	VDD_MX	Power for on-chip memory
AE41	VDD_PX0	Power for pad group 0 – control signals
L25	VDD_PX1	Power for pad group 1
L23	VDD_PX10	Power for pad group 10 – UFS
BE35	VDD_PX11	Power for pad group 11 – CXO pad
AT40	VDD_PX2	Power for pad group 2 – SDC2 pads
AC41, AF8, AW25, BG7, BH40, P6	VDD_PX3	Power for pad group 3 – most I/O pads
BE37	VDD_PX5	Power for pad group 5 – UIM1 pads
BE39	VDD_PX6	Power for pad group 6 – UIM2 pads
M6	VDD_PX7	Power for pad group 7
AV40	VDDPX_VBIAS_SDC	Reference voltage for SDC
BH36	VDDPX_VBIAS_UIM	Reference voltage for UIM
M36, N35, P36, R35, T36, U29, U31, U33, U35, V30, V32, V34, V36	VDD_APC0	Power for the Kryo Silver application processor
Y40, Y32, Y34, Y38, Y30, Y28, Y42, W39, V40, U39, AA29, AA31, AA33, AA35, AA37, AA39, AA41, AA43, AD30, AD32, AD34, AD36, AD38, AE29, AE31, AE33, AE35, AE37, M38, M42, N39, N41, N43, P40, R39, T40	VDD_APC1	Power for the Kryo Gold application processor
AJ41	VDD_A_DSI_0_0P9	Power for the DSI0 0.9 V circuits
AG41	VDD_A_DSI_0_1P2	Power for the DSI0 1.2 V circuits
AH40	VDD_A_DSI_0_PLL_0P9	Power for the DSI0 0.9 V PLL circuits
AM40	VDD_VREF_0P9	Power for VREF 0.9 V circuits
AN41	VDD_VREF_1P2	Power for VREF 1.2 V circuits
BB24	VDD_A_GNSS_0P9	Power for 0.9 V GNSS circuits
Y8	VDD_A_PCIE_0_1P2	Power for the PCIe0 PLL
AA9	VDD_A_PCIE_0_CORE	Power for PCIe0 core circuits
BC31	VDD_VREF_1P2	Power for VREF 1.2 V circuits
BC33	VDD_VREF_0P9	Power for VREF 0.9 V circuits
BC15	VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits
BD14	VDD_A_QLINK_0_0P9_CK	Power for the QLink0 0.9 V clock circuits
BC13	VDD_A_QLINK_0_1P2_CK	Power for the QLink0 1.2 V clock circuits
BD20	VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits
BC21	VDD_A_QLINK_1_0P9_CK	Power for the QLink1 0.9 V clock circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
BC19	VDD_A_QLINK_1_1P2	Power for the QLink1 1.2 V clock circuits
AL41, AN9, BD34, BE41, BC23, BE13, T42, T24, Y10	VDD_A_QREFS_0P875	Reference voltage for the QREFS 0.875 V circuits
BH34	VDD_A_QREFS_1P25	Reference voltage for the QREFS 1.25 V circuits
BJ37	VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits
P22	VDD_A_UFS_0_1P2	Power for the UFS 1.2 V circuits
P24	VDD_A_UFS_0_CORE	Power for the UFS core circuits
BE25	VDD_A_USBHS_1P8	Power for the USB high speed1.8 V circuits
BF26	VDD_A_USBHS_3P1	Power for the USB high speed3.1 V circuits
BD24	VDD_A_USBHS_CORE	Power for the USB HS core
BC29	VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort 1.2 V circuits
BD28	VDD_A_USBSSDP_0_CORE	Power for the USB SS and DisplayPort core circuits
AN37, AN39, AP28, AP32, AP36, AR29, AR33, AR37, AT28, AT32, AT36, AU29, AU33, AU37, AV28, AV32, AV36, AW29, AW33, AW37, AY28, AY32, AY36, AY40, BA29, BA33, BA37, BB40, BC39	VDD_GFX	Power for graphics
AK30	VDD_GFX_CX_ISENSE	Power for the GFX current sensor circuits
AE39, AG33, AG35, AG37, AG39, AH38	VDD_LPI_CX	Power for LPI digital core circuits
AG31, AH30, AH32, AH34, AH36	VDD_LPI_MX	Power for low-power island memory circuits
AH14, AJ11, AJ13, AK14, AL13, AM14, AN13, AN17, AN19, AP10, AP14, AP18, AR9, AR13, AR17, AR21, AT10, AT14, AT18, AT22, AU13, AU17, AU21, AV10, AV14, AV18, AV22, AW13, AW17, AW21, AY10, AY14, AY18, AY22, BA13, BA17, BA21, BB10, BB14, BB18, BB22, BC9, BC17, BD18, BE17, BF18	VDD_MODEM	Power for modem circuits
BC25	VDD_LPI_NAV_MX	Power for LPI on chip memory – NAV
AY24	VDD_QFPROM	Power for programming the QFPROM
AB26	VDD_WPSS_CX	Power for WLAN digital core circuits

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings shown in the following table reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	TBD	TBD	V
VDD_APC1	Kryo Gold application processor	TBD	TBD	V
VDD_MODEM	Modem circuits	TBD	TBD	V
VDD_GFX	Graphics processor	TBD	TBD	V
VDD_PX1	Pad Group 1 - DDR Pads	TBD	TBD	V
VDD_PX2	Pad Group 2 - SDC2 Pads	TBD	TBD	V
VDD_PX5	Pad Group 5 - UIM1 Pads	TBD	TBD	V
VDD_PX6	Pad Group 6 - UIM2 Pads	TBD	TBD	V
VDD_PX10	Pad Groups 10-UFS pads	TBD	TBD	V
VDD_PX11	Pad Groups 11-CXO pads	TBD	TBD	V
VDD_MX	On-Chip memory	TBD	TBD	V
VDD_LPI_CX	LPI Core	TBD	TBD	V
VDD_A_USBSSDP_0_CORE	USB SS 0.9 V circuit	TBD	TBD	V
VDD_IO_EBIx	EBI I/O circuit	TBD	TBD	V
VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuit	TBD	TBD	V
VDD_A_USBHS_3P1	USB HS 3.1 V circuit	TBD	TBD	V
VDD_A_CXO_1P8	1.8 V for clock circuits	TBD	TBD	V
VDDPX_VBIAS_SDC VDDPX_VBIAS_UIM	Bias voltage for SDC& UIM circuits	TBD	TBD	V
VDD_PX0	Pad Group 3-Control signal Pads	TBD	TBD	V
VDD_PX3	Pad Group 3-IO Pads			
VDD_PX7	Pad Group 7- SDC1 pads			
VDD_CX VDD_WPSS_CX VDD_D_EBIx	Digital Core Circuits WPSS Circuit EBI Digital Circuits	TBD	TBD	V
VDD_A_PCIE_0_1P2 VDD_VREF_1P2 VDD_A_CSI_x_1P2 VDD_A_UFS_0_1P2	PCIe Circuit PCIe Circuit QLink1 Circuit CSI 1.2 V Circuits UFS 1.2V Circuits	TBD	TBD	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_USBSSDP_0_1P2	USB SS 1.2 V Circuits			
VDD_A_QLINK_0_1P2_CK	QLINK 0 clock circuit			
VDD_A_QLINK_1_1P2	QLINK 1 clock circuit			
VDD_A_DSI_0_1P2	DSI 1.2 V circuit			
VDD_A_PCIE_0_CORE	PCIe Circuit	TBD	TBD	V
VDD_VREF_0P9	PCIe Reference voltage			
VDD_A_CSI_x_0P9	CSIX 0.9V Circuits			
VDD_A_QLINK_x_0P9	QLINK 0.9V Circuits			
VDD_A_QLINK_x_0P9_CK	QLINK Clock circuits			
VDD_A_UFS_0_CORE	UFS 0.9V Circuits			
VDD_A_USBHS_CORE	USB HS 0.9V Circuits			
VDD_A_GNSS_0P9	GNSS Circuits			
VDD_A_DSI_0_0P9	DSI 0.9V Circuits			
VDD_A_DSI_0_PLL_0P9	DSI PLL 0.9V Circuits			
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V circuit			
VDD_A_EBIx	EBI Phy voltage circuits	TBD	TBD	V
VDD_A_PLL_EBIx	EBI PLL Circuit			
VDD_A_USBHS_1P8	USB HS 1.8V Circuits	TBD	TBD	V
VDD_QFPROM	Programming the QFPROM			
VDD_A_GFX_CS_1P8	GFX 1.8V circuits			
VDD_A_TURNING_Q6_CS_1P8	Power for Q6 current sensor 1.8 V circuits			
VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits			
VDD_A_APC_CS_1P8	Power for application processor current sensor; 1.8 V circuits			
VDD_LPI_NAV_MX	LPI on chip memory – NAV	TBD	TBD	V
VDD_LPI_MX	Low-power island memory circuits			
T_s	Storage temperature [a] [b]	TBD	TBD	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~+35°C] and < 90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions. The SM7325 meets all performance specifications listed in the following table, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

NOTE Customers should keep the thermal mitigation algorithm enabled with default limits to ensure that the operating temperature range is kept within the specification.

Table 3-2 Operating conditions

Parameter		Min	Type [a]	Max	Unit
Power supply voltages					
VDD_APC0	Kryo Silver application processor	TBD	TBD	TBD	V
VDD_APC1	Kryo Gold application processor	TBD	TBD	TBD	V
VDD_MODEM	Modem circuits	TBD	TBD	TBD	V
VDD_GFX	Graphics processor	TBD	TBD	TBD	V
VDD_PX1	Pad Group 1 - DDR Pads	TBD	TBD	TBD	V
VDD_PX2	Pad Group 2 - SDC2 Pads	TBD	TBD	TBD	V
VDD_PX5	Pad Group 5 - UIM1 Pads	TBD	TBD	TBD	V
VDD_PX6	Pad Group 6 - UIM2 Pads	TBD	TBD	TBD	V
VDD_PX10	Pad Groups 10-UFS pads	TBD	TBD	TBD	V
VDD_PX11	Pad Groups 11-CXO pads	TBD	TBD	TBD	V
VDD_MX	On-Chip memory	TBD	TBD	TBD	V
VDD_LPI_CX	LPI Core	TBD	TBD	TBD	V
VDD_A_USBSSDP_0_CORE	USB SS 0.9 V circuit	TBD	TBD	TBD	V
VDD_IO_EBIx	EBI I/O circuit	TBD	TBD	TBD	V
VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuit	TBD	TBD	TBD	V
VDD_A_USBHS_3P1	USB HS 3.1 V circuit	TBD	TBD	TBD	V
VDD_A_CXO_1P8	1.8 V for clock circuits	TBD	TBD	TBD	V
VDDPX_VBIAS_SDC VDDPX_VBIAS_UIM	Bias voltage for SDC& UIM circuits	TBD	TBD	TBD	V
VDD_PX0	Pad Group 3-Control signal Pads	TBD	TBD	TBD	V
VDD_PX3	Pad Group 3-IO Pads				
VDD_PX7	Pad Group 7- SDC1 pads				
VDD_CX VDD_WPSS_CX VDD_D_EBIx	Digital Core Circuits WPSS Circuit EBI Digital Circuits	TBD	TBD	TBD	V
VDD_A_PCIE_0_1P2 VDD_VREF_1P2 VDD_A_CSI_x_1P2 VDD_A_UFS_0_1P2 VDD_A_USBSSDP_0_1P2 VDD_A_QLINK_0_1P2_CK VDD_A_QLINK_1_1P2 VDD_A_DSI_0_1P2	PCIe Circuit PCIe Circuit QLink1 Circuit CSI 1.2 V Circuits UFS 1.2V Circuits USB SS 1.2 V Circuits QLINK 0 clock circuit QLINK 1 clock circuit	TBD	TBD	TBD	V
VDD_A_PCIE_0_CORE VDD_VREF_0P9 VDD_A_CSI_x_0P9 VDD_A_QLINK_x_0P9 VDD_A_QLINK_x_0P9_CK	PCIe Circuit PCIe Reference voltage CSIX 0.9V Circuits QLINK 0.9V Circuits QLINK Clock circuits	TBD	TBD	TBD	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Type [a]	Max	Unit
VDD_A_UFS_0_CORE	UFS 0.9V Circuits				
VDD_A_USBHS_CORE	USB HS 0.9V Circuits				
VDD_A_GNSS_0P9	GNSS Circuits				
VDD_A_DSI_0_0P9	DSI 0.9V Circuits				
VDD_A_DSI_0_PLL_0P9	DSI PLL 0.9V Circuits				
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V circuit				
VDD_A_EBIx	EBI Phy voltage circuits	TBD	TBD	TBD	V
VDD_A_PLL_EBIx	EBI PLL Circuit				
VDD_A_USBHS_1P8	USB HS 1.8V Circuits	TBD	TBD	TBD	V
VDD_QFPROM	Programming the QFPROM				
VDD_A_GFX_CS_1P8	GFX 1.8V circuits				
VDD_A_TURNING_Q6_CS_1P8	Power for Q6 current sensor 1.8 V circuits				
VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits				
VDD_A_APC_CS_1P8	Power for application processor current sensor; 1.8 V circuits				
VDD_LPI_NAV_MX	LPI on chip memory – NAV	TBD	TBD	TBD	V
VDD_LPI_MX	Low-power island memory circuits				
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	TBD	$T_{junction}$ = +95	°C

[a] Typical voltages represent the recommended output settings of the companion PMIC device.

3.3 Power delivery network specification

A detailed power delivery network specification is available in the *SM7325 Chipset Power Delivery Network Specification* (80-19448-1P) document.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the *SM7325 Linux Android Current Consumption Data Application Note* (80-19448-7) document.

3.4.2 Dhrystone and rock bottom maximum power

Table 3-3 Dhrystone and rock bottom maximum power

SDM version	Octa core – Gold at 2.4 GHz and Silver at 1.8 GHz , Dhrystone (W) at +95°C (Tj) [a] [b] [c]	Rock bottom (mW) at 30°C (Tj) [d]
SM7325	TBD	TBD

[a] This Kryo Gold dual core Dhrystone specification applies to SM7325 CS devices.
[b] Dhrystone power should be measured on the VDD_APC1 rail, right before PDN capacitors (with a small serial sampling resistor inserted, if necessary).
[c] Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and the average window should be > 1 ms (or > 1250 samples).
[d] Rock bottom (VDDCX and VDDMX) power should be measured at VDDCX and VDDMX rails when VDDCX and VDDMX are at retention voltage.

3.5 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage.

- Some are dedicated for interconnections between the SDM device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-4 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	TBD	TBD	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	TBD	TBD	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	TBD	TBD	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	TBD	TBD	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	TBD	TBD	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	TBD	TBD	mV
I_{IH}	Input high leakage current [a]	TBD	TBD	µA
I_{IL}	Input low leakage current	TBD	TBD	µA
I_{IHPD}	Input high leakage current with pull-down	TBD	TBD	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	TBD	TBD	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current	TBD	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	TBD	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	TBD	TBD	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	TBD	TBD	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [b]	TBD	TBD	µA (kΩ)

Table 3-4 DC specification of 1.8 V GPIOs and WCSS WSI I/Os (cont.)

Parameter	Description	Min	Max	Unit
I_{OZLKP}	Low-level, tri-state leakage current with keeper [c]	TBD	TBD	µA (kΩ)
V_{OH}	High-level output voltage, CMOS	TBD	TBD	V
V_{OL}	Low-level output voltage, CMOS	TBD	TBD	V

[a] I_{IH}, I_{IL}, I_{OZH}, and I_{OZL} values are based on nominal PVT (TT/25°C).
[b] Pin voltage = VDD_PX3 maximum. For keeper pins, pin voltage = VDD_PX3 maximum - 0.45 V.
[c] Pin voltage = GND and supply = VDD_PX3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_PX3 maximum.

Table 3-5 SDC2 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	TBD	–	TBD	V
V_{IL}	Low-level input voltage	TBD	–	TBD	V
V_{HYS}	Schmitt hysteresis voltage	TBD	–	TBD	mV
I_{IH}	Input high leakage current	TBD	–	TBD	µA
I_{IL}	Input low leakage current	TBD	–	TBD	µA
I_{OZH}	High-level, tri-state leakage current	TBD	–	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	–	TBD	µA
$R_{PULL-UP}$	Pull-up resistance	TBD	–	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	–	TBD	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	TBD	–	TBD	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	TBD	–	TBD	kΩ
V_{OH}	High-level output voltage	TBD	–	TBD	V
V_{OL}	Low-level output voltage	TBD	–	TBD	V

Table 3-6 SDC2 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	TBD	–	TBD	V
V_{IL}	Low-level input voltage	TBD	–	TBD	V
V_{HYS}	Schmitt hysteresis voltage	TBD	–	TBD	mV
I_{IH}	Input high leakage current	TBD	–	TBD	µA
I_{IL}	Input low leakage current	TBD	–	TBD	µA
I_{OZH}	High-level, tri-state leakage current	TBD	–	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	–	TBD	µA
$R_{PULL-UP}$	Pull-up resistance	TBD	–	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	–	TBD	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	TBD	–	TBD	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	TBD	–	TBD	kΩ
V_{OH}	High-level output voltage	TBD	–	TBD	V
V_{OL}	Low-level output voltage	TBD	–	TBD	V

Table 3-7 SDC1 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	TBD	–	TBD	V
V_{IL}	Low-level input voltage	TBD	–	TBD	V
V_{HYS}	Schmitt hysteresis voltage	TBD	–	TBD	mV
I_{IH}	Input high leakage current	TBD	–	TBD	µA
I_{IL}	Input low leakage current	TBD	–	TBD	µA
I_{OZH}	High-level, tri-state leakage current	TBD	–	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	–	TBD	µA
$R_{PULL-UP}$	Pull-up resistance	TBD	–	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	–	TBD	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	TBD	–	TBD	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	TBD	–	TBD	kΩ
V_{OH}	High-level output voltage	TBD	–	TBD	V
V_{OL}	Low-level output voltage	TBD	–	TBD	V

Table 3-8 UICC 3 V mode DC specifications (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage [a]	TBD	–	TBD	V
V_{IL}	Low-level input voltage	TBD	–	TBD	V
V_{HYS}	Schmitt hysteresis voltage [b]	TBD	–	TBD	mV
I_{OZH}	High-level, tri-state leakage current	TBD	–	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	–	TBD	µA
$R_{PULL-UP}$	Pull-up resistance	TBD	–	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	–	TBD	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	TBD	–	TBD	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	TBD	–	TBD	kΩ
V_{OH}	High-level output voltage [c]	TBD	–	TBD	V
V_{OL}	Low-level output voltage [d]	TBD	–	TBD	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal.
[b] V_{HYS} is not a required specification for UICC.
[c] UICC specifies V_{OH} = 0.8 × VDDPx (RST) and 0.7 × VDDPx (CLK, I/O). The worse-case V_{OH} is used in this table.
[d] UICC specifies V_{OL} = 0.2 × VDDPx (RST, CLK) and 0.4 V (I/O). The worse-case V_{OL} is used in this table.

NOTE UICC supply range for class B is 2.7 V to 3.3 V.

Table 3-9 UICC 1.8 V mode DC specifications (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage [a]	TBD	–	TBD	V
V_{IL}	Low-level input voltage	TBD	–	TBD	V
V_{HYS}	Schmitt hysteresis voltage [b]	TBD	–	TBD	mV
I_{OZH}	High-level, tri-state leakage current	TBD	–	TBD	µA

Table 3-9 UICC 1.8 V mode DC specifications (VDD_PX5 and VDD_PX6) (cont.)

Parameter	Description	Min	Typ	Max	Unit
I_{OZL}	Low-level, tri-state leakage current	TBD	–	TBD	µA
$R_{PULL-UP}$	Pull-up resistance	TBD	–	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	–	TBD	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	TBD	–	TBD	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	TBD	–	TBD	kΩ
V_{OH}	High-level output voltage [c]	TBD	–	TBD	V
V_{OL}	Low-level output voltage [d]	TBD	–	TBD	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal.
[b] V_{HYS} is not a required specification for UICC.
[c] UICC specifies V_{OH} = 0.8 × VDDPx (RST) and 0.7 × VDDPx (CLK, I/O). The worse-case V_{OH} is used in this table.
[d] UICC specifies V_{OL} = 0.2 × VDDPx (RST, CLK) and 0.3 V (I/O). The worse-case V_{OL} is used in this table.

NOTE UICC supply range for class C is 1.62 V to 1.98 V.

Table 3-10 Digital I/O characteristics for VDD_PX10 nominal (UFS)

Parameter	Description	Min	Max	Unit
V_{OL}	Output low-level voltage	TBD	TBD	V
V_{OH}	Output high-level voltage	TBD	TBD	V
$R_{PULL-UP}$	Pull-up resistance	TBD	TBD	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	TBD	TBD	kΩ
I_{OZH}	High-level, tri-state leakage current	TBD	TBD	µA
I_{OZL}	Low-level, tri-state leakage current	TBD	TBD	µA

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM7325 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Rise and fall time specifications.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the following figure.

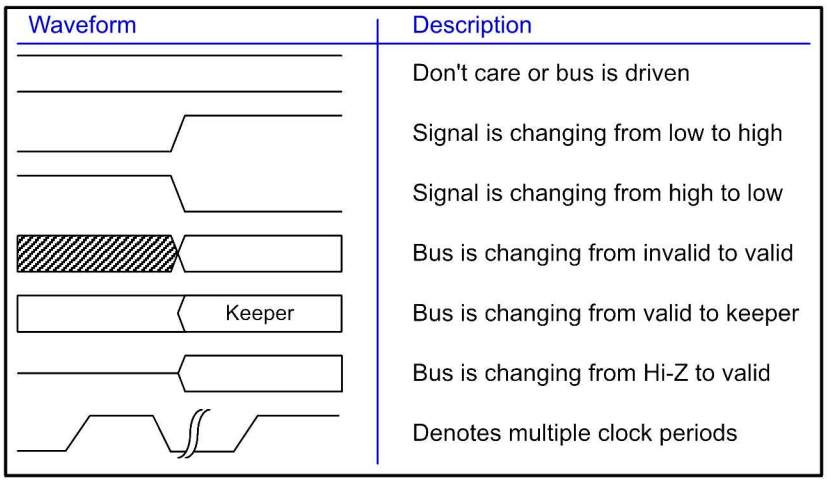


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates *don't care*.

3.6.2 Rise and fall time specifications

The testers that characterize SM7325 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the following figure.

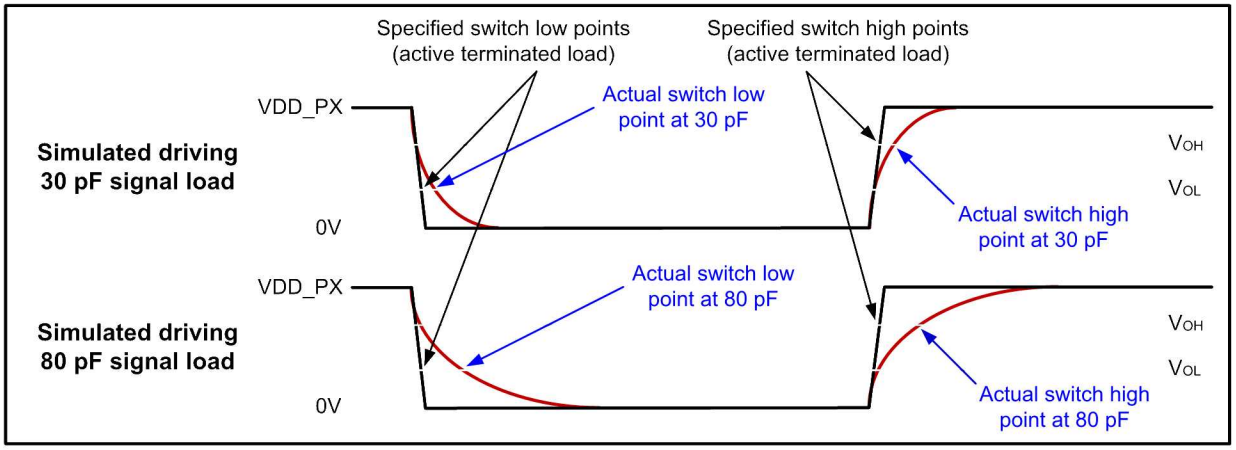


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM7325 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SM7325 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated $V_{DD\_PXDD\_PX}/2$ (or 50% of V supply. The input switch point for pure input-only pads is designed to be V_{DD_PX} supply. The). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

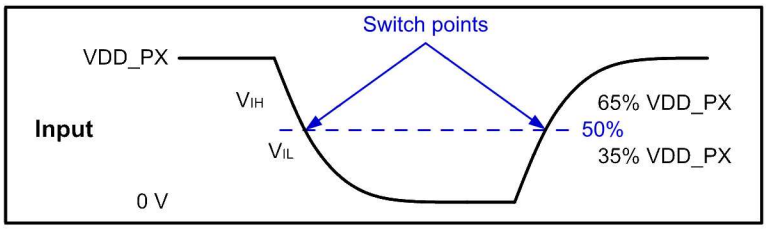


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented VOH (min) and VOL(max) levels over worst-case process/voltage/temperature. Because the pad output structures are essentially CMOS drivers that possibly have a small amount of

IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX} - 50 mV or more
- V_{OL} ~ 50 mV or less

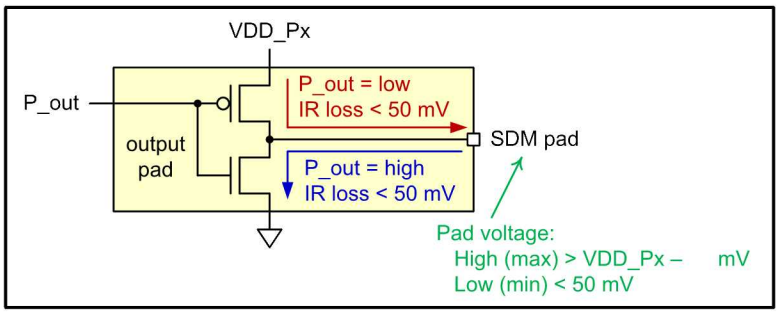


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) provides approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) provides approximately 1.25 mA or more at ½ × [V_{DDPX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

3.7 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.7.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4X/LPDDR5 SDRAM memory that is attached to the SM7325 chipset.

3.7.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Secured digital interfaces for details.

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SM7325 device supports four 4-lane MIPI_CSIs: CSI0, CSI1, CSI2, and CSI3.

Table 3-11 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.0	None

3.8.2 Audio support

- A dedicated audio codec, such as the WCD9370/WCD9375/WCD9380/WCD9385, uses the industry standard SoundWire interface.

Other audio-related interface options include:

- Digital microphone: Digital microphone PDM interface
- SWR: SoundWire (SWR) interface
- SLIMbus: SLIMbus interface
- I^2S: I^2S interfaces
- I^2C/I3C: I^2C/I3C interface
- SPI: Serial peripheral interface

See the *Qualcomm AQSTIC WCD9370 Device Specification* (80-PG244-1), *Qualcomm AQSTIC WCD9375 Device Specification* (80-PG245-1), and *Qualcomm AQSTIC WCD9380/WCD9385 Device Specification* (80-PL335-1) for performance characteristics.

3.8.3 Display support

The SM7325 device supports up to one D-PHY display.

Table 3-12 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

3.8.4 DMB support

The SM7350 supports an external DMB solution using the following interface options:

- SPI: Serial peripheral interface
- SD: Secured digital interfaces

3.9 Connectivity

The connectivity functions supported by the SM7325 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Universal integrated circuit card (UICC) interface
- DisplayPort support over USB Type-C
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power interchip media bus (SLIMbus) interface for Bluetooth, FM
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Dedicated I^2C interfaces for camera (CCI I^2C)
- Through proper configuration of QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

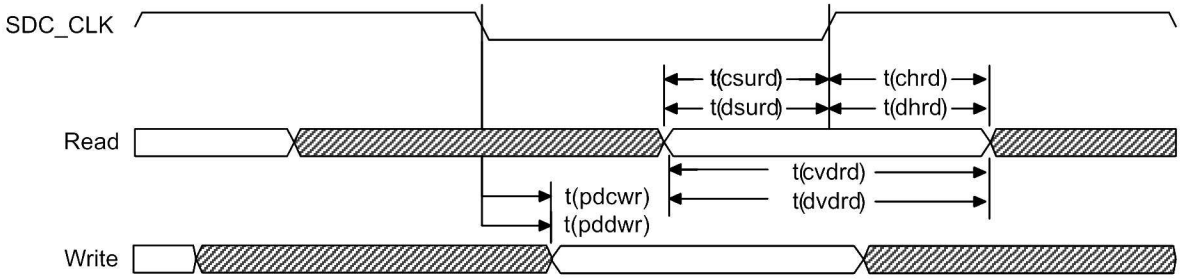
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 Secured digital interfaces

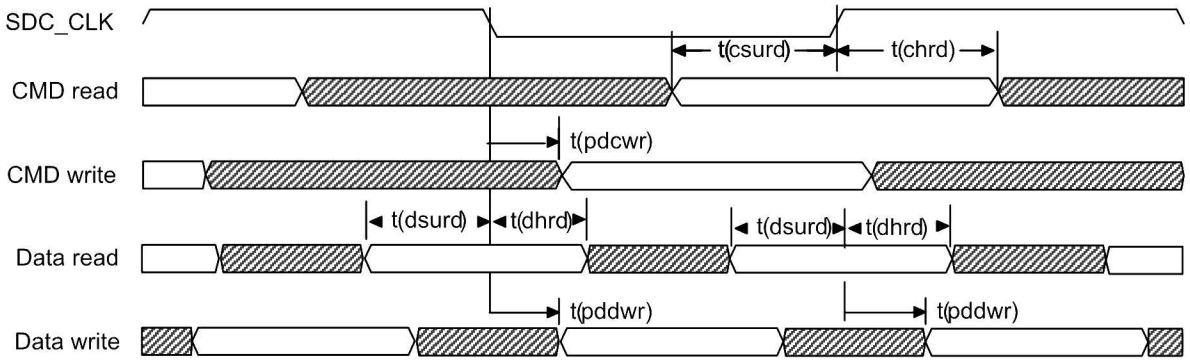
Table 3-13 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

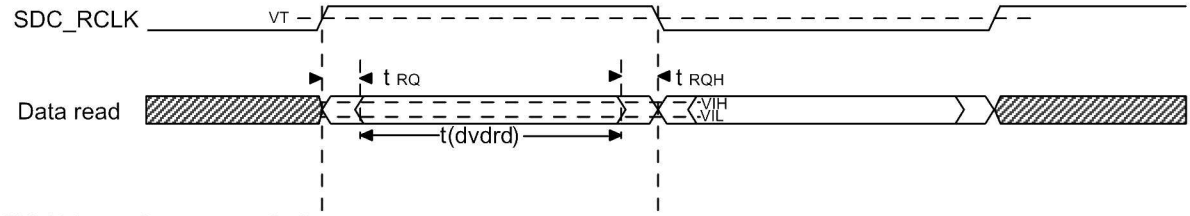
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

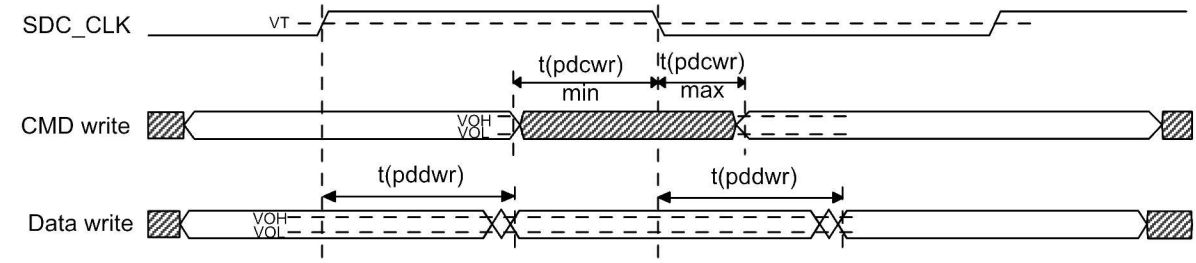


Figure 3-5 Secured digital interface timing

3.9.2 USB interfaces

Table 3-14 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 1
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.9.3 DisplayPort

Table 3-15 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.9.4 PCIe interface

Table 3-16 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link upconfigure capability

3.9.5 UFS interface

Table 3-17 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None
Universal Flash Storage (UFS), Version 2.1	None

3.9.6 Digital microphone PDM interface

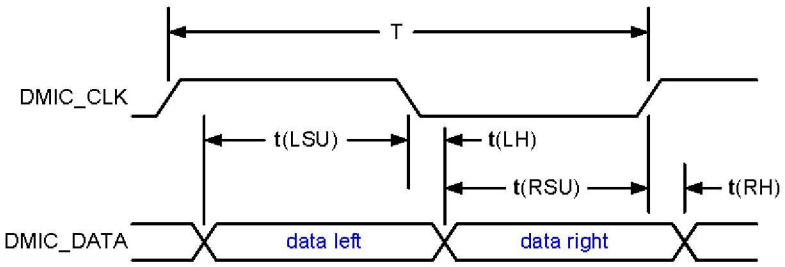


Figure 3-6 Digital microphone PDM interface timing

Table 3-18 Digital microphone timing

Parameter		Min	Typ	Max	Unit
T	DMIC clock period	–	–	–	ns
t(LSU)	Data left setup time to clock falling edge	–	–	–	ns
t(LH)	Data left hold time to clock falling edge	–	–	–	ns
t(RSU)	Data right setup time to clock rising edge	–	–	–	ns
t(RH)	Data right hold time to clock falling edge	–	–	–	ns

3.9.7 SoundWire (SWR) interface

SM7325 SoundWire PHY timing parameters, as specified in the following table, are compliant to clock and data specifications, as specified in the *MIPI Alliance Specification for SoundWire Version 0.8, Revision 04*.

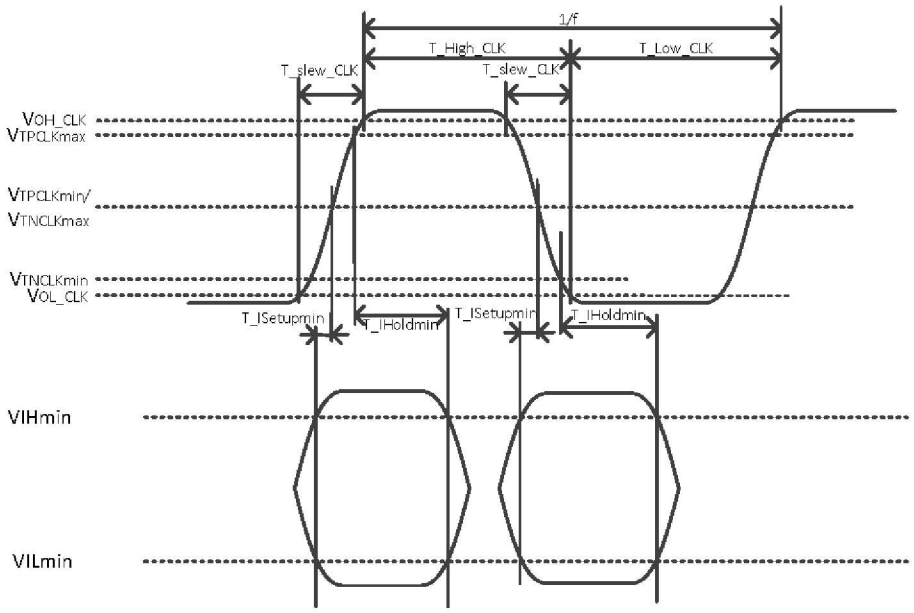


Figure 3-7 PHY timing – clock output/input and data input

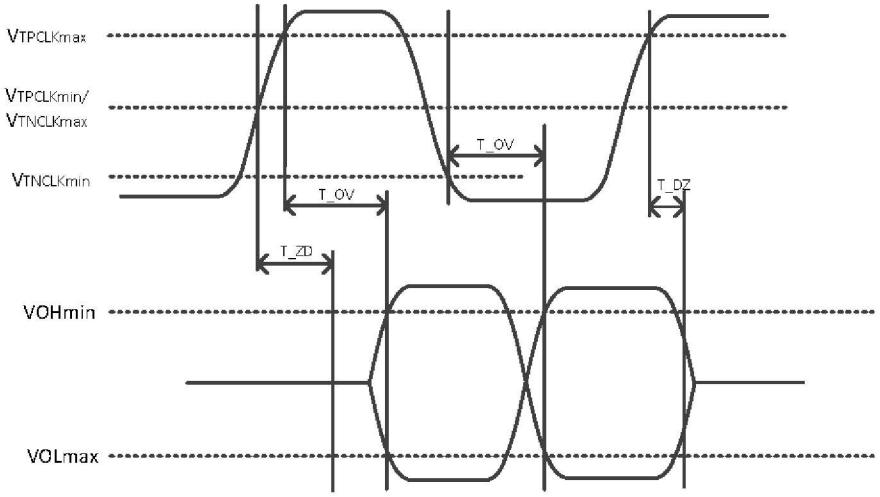


Figure 3-8 PHY timing – clock output and data output

Table 3-19 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Unit
f_Clock_small_1V8	Frequency of clock signal in small systems	TBD	TBD	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	TBD	TBD	ns
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	TBD	TBD	ns
t_DZ_Data_1V8	Time to disable data output signal after positive ornegative edge on clock input signal	TBD	TBD	ns
t_ZD_Data_1V8	Time to enable data output signal after positive ornegative edge on clock input signal	TBD	TBD	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	TBD	TBD	%
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	TBD	TBD	ns
t_ISetup_min_Data_1V8	Input setup time	TBD	TBD	ns
t_IHold_min_Data_1V8	Input hold time	TBD	TBD	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	TBD	TBD	ns

3.9.8 SLIMbus interface

Table 3-20 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.9.9 I²S interfaces

The following information applies:

Table 3-21 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

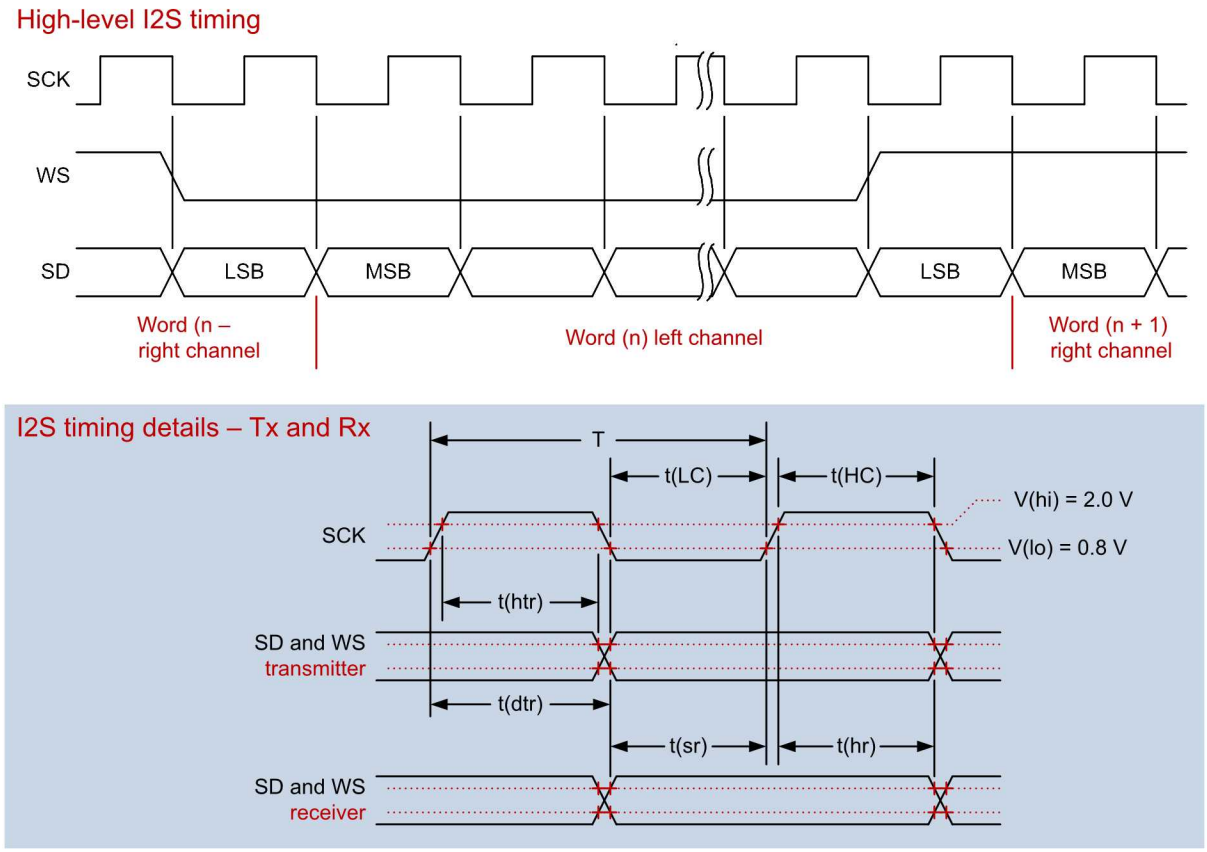


Figure 3-9 I²S timing diagram

Table 3-22 I²S interface timing – MI²S interface 0 and 1, LPI_MI2S interface

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency [a]		TBD	TBD	TBD	TBD	MHz
T	Clock period	TBD	TBD	TBD	TBD	ns
t(HC)	Clock high	TBD	TBD	TBD	TBD	ns
t(LC)	Clock low	TBD	TBD	TBD	TBD	ns
t(sr)	SD and WS input setup time	TBD	TBD	TBD	TBD	ns
t(hr)	SD and WS input hold time	TBD	TBD	TBD	TBD	ns

Table 3-22 I²S interface timing – MI²S interface 0 and 1, LPI_MI2S interface (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(dtr)	SD and WS output delay	TBD	TBD	TBD	TBD	ns
t(htr)	SD and WS output hold time	TBD	TBD	TBD	TBD	ns
Using external SCK						
Frequency		TBD	TBD	TBD	TBD	MHz
T	Clock period	TBD	TBD	TBD	TBD	ns
t(HC)	Clock high	TBD	TBD	TBD	TBD	ns
t(LC)	Clock low	TBD	TBD	TBD	TBD	ns
t(sr)	SD and WS input setup time	TBD	TBD	TBD	TBD	ns
t(hr)	SD and WS input hold time	TBD	TBD	TBD	TBD	ns
t(dtr)	SD and WS output delay	TBD	TBD	TBD	TBD	ns
t(htr)	SD and WS output hold time	TBD	TBD	TBD	TBD	ns

[a] Load capacitance is between 10 and 40 pF.

Table 3-23 I²S interface timing – MI²S interface 2

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency [a]		TBD	TBD	TBD	TBD	MHz
T	Clock period	TBD	TBD	TBD	TBD	ns
t(HC)	Clock high	TBD	TBD	TBD	TBD	ns
t(LC)	Clock low	TBD	TBD	TBD	TBD	ns
t(sr)	SD and WS input setup time	TBD	TBD	TBD	TBD	ns
t(hr)	SD and WS input hold time	TBD	TBD	TBD	TBD	ns
t(dtr)	SD and WS output delay	TBD	TBD	TBD	TBD	ns
t(htr)	SD and WS output hold time	TBD	TBD	TBD	TBD	ns
Using external SCK						
Frequency		TBD	TBD	TBD	TBD	MHz
T	Clock period	TBD	TBD	TBD	TBD	ns
t(HC)	Clock high	TBD	TBD	TBD	TBD	ns
t(LC)	Clock low	TBD	TBD	TBD	TBD	ns
t(sr)	SD and WS input setup time	TBD	TBD	TBD	TBD	ns
t(hr)	SD and WS input hold time	TBD	TBD	TBD	TBD	ns
t(dtr)	SD and WS output delay	TBD	TBD	TBD	TBD	ns
t(htr)	SD and WS output hold time	TBD	TBD	TBD	TBD	ns

[a] Load capacitance is between 10 and 40 pF.

3.9.10 Touchscreen connections

Touchscreen panels are supported using I²C buses (I²C/I3C interface) and GPIOs configured as discrete digital inputs (Digital-logic characteristics). Additional specifications are not required.

3.9.11 I²C/I3C interface

Table 3-24 Supported I²C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C Specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.9.12 Serial peripheral interface

The SM7325 supports SPI as a master only.

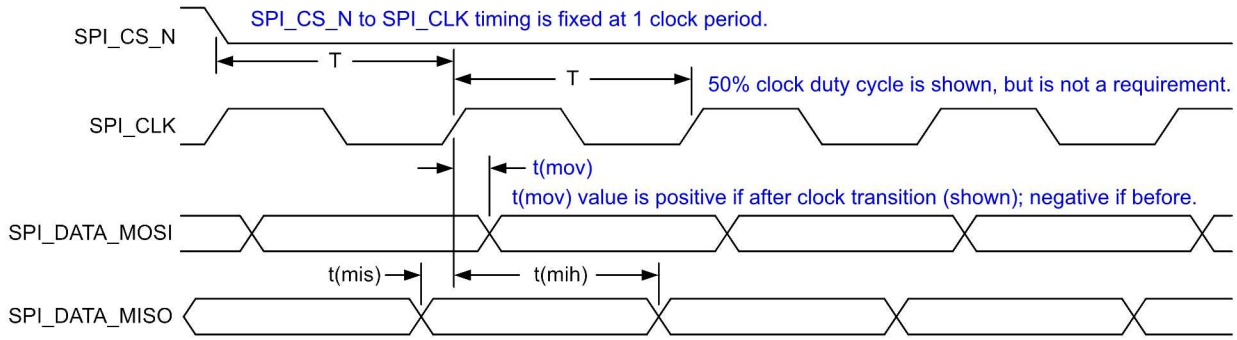


Figure 3-10 SPI master timing diagram

Table 3-25 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clockperiod) [a]	50 MHz maximum	TBD	TBD	TBD	ns
t(ch)	Clock high	TBD	TBD	TBD	ns
t(cl)	Clock low	TBD	TBD	TBD	ns
t(mov)	Master output valid	TBD	TBD	TBD	ns
t(mis)	Master input setup	TBD	TBD	TBD	ns
t(mih)	Master input hold	TBD	TBD	TBD	ns
t(ov)	Chip CS to CLK	TBD	TBD	TBD	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

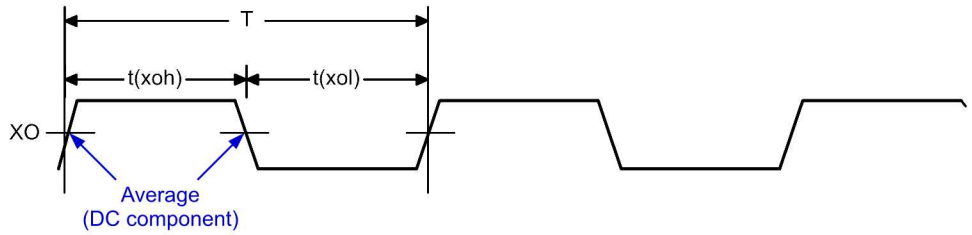


Figure 3-11 XO timing parameters

Table 3-26 XO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	TBD	TBD	TBD	ns
t(xol)	XO logic low	–	TBD	TBD	TBD	ns
T	XO clock period	–	TBD	TBD	TBD	ns
1/T	Frequency	19.2 MHz must be used	TBD	TBD	TBD	MHz

[a] See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.10.1.2 Sleep clock

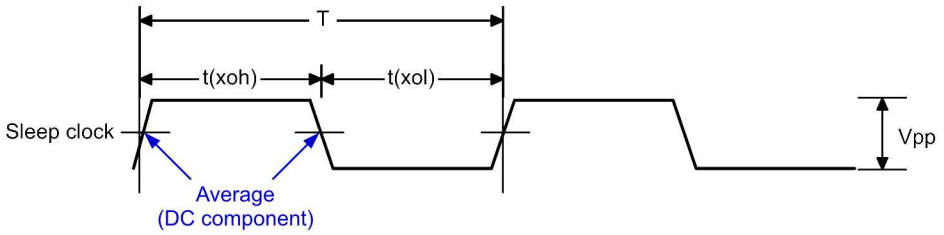


Figure 3-12 Sleep-clock timing parameters

Table 3-27 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F= 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Digital-logic characteristics.

3.10.3 JTAG

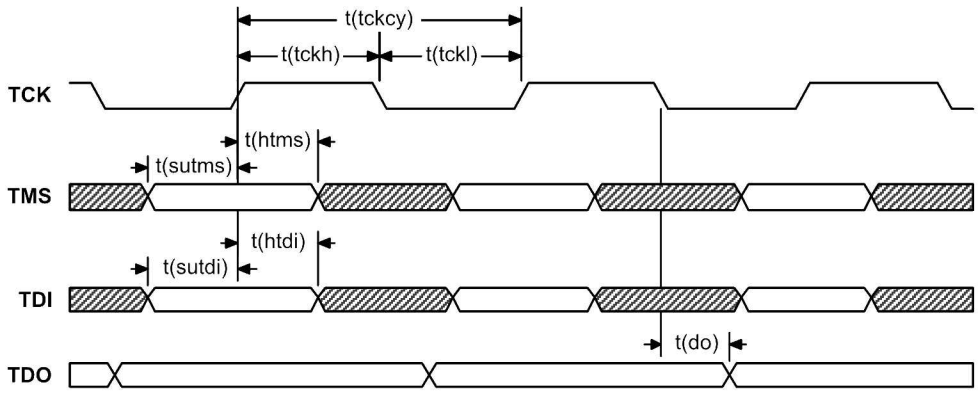


Figure 3-13 JTAG interface timing diagram

Table 3-28 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	TBD	TBD	TBD	ns
t(tckh)	TCK pulse width high	TBD	TBD	TBD	ns
t(tckl)	TCK pulse width low	TBD	TBD	TBD	ns
t(sutms)	TMS inputsetup time	TBD	TBD	TBD	ns
t(htms)	TMS input hold time	TBD	TBD	TBD	ns
t(sutdi)	TDI inputsetup time	TBD	TBD	TBD	ns
t(htdi)	TDI input hold time	TBD	TBD	TBD	ns
t(do)	TDO data output delay	TBD	TBD	TBD	ns

3.10.4 SWD

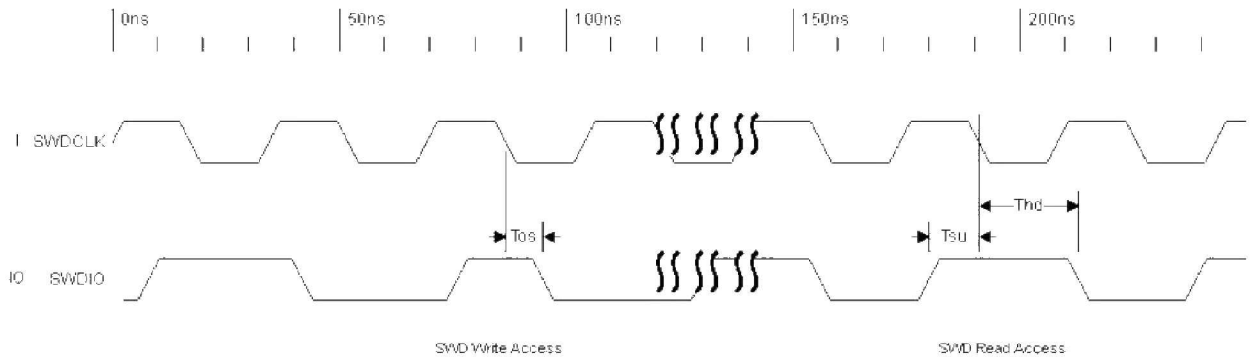


Figure 3-14 SWD write and read AC timing diagram

Table 3-29 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	TBD	TBD	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	TBD	TBD	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	TBD	TBD	ns

NOTE SWDCLK runs at 20 MHz or lower.

3.11 RF and power management interfaces

3.11.1 RF front end (RFFE)

Table 3-30 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None

3.11.2 System power management interface (SPMI)

Table 3-31 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM7325 device is available in the PSP1287 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The PSP1287 has a 14 mm by 12 mm body, with a maximum height of 0.91 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in the following figure.

NOTE Click the following link to download the *Package Outline Drawing PSP1287, 14.0 × 12.0 × 0.91 mm, M530, S164* (NT90-18083-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-18083-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

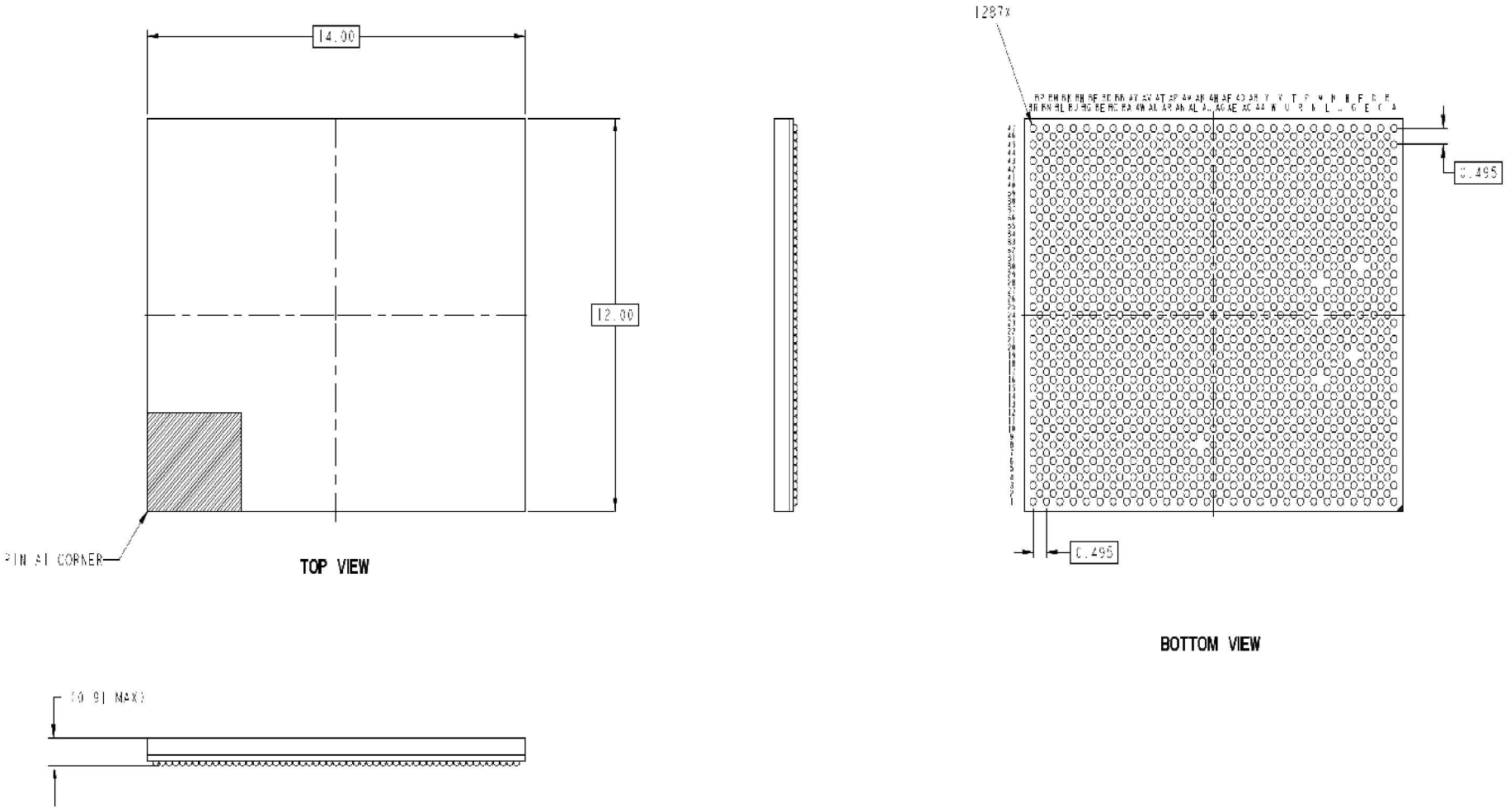


Figure 4-1 PSP1287 outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

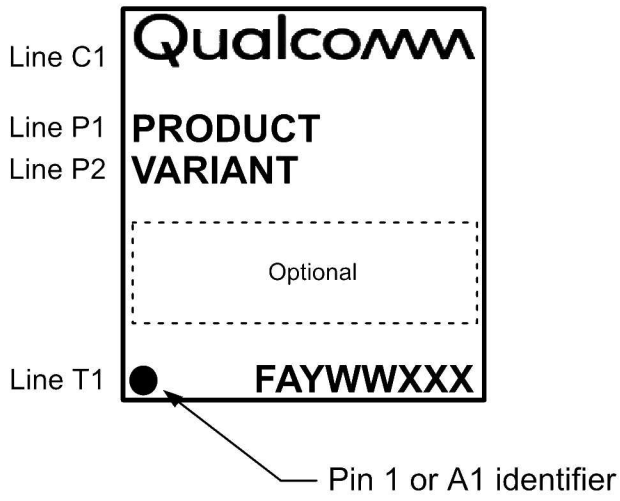


Figure 4-2 SM7325 device marking (top view, not to scale)

Table 4-1 SM7325 device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ SM7325
P2	VARIANT	Device variant information ▪ See Table 4-4 for the assigned values.
	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ▪ F = F (TSMC) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = H (JCET STATS ChipPAC, Korea) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Pin 1 or pin A1 indicator

NOTE For complete marking definitions of all SM7325 variants and revisions, see the *SM7325 Device Revision Guide* (80-19448-4)

Table 4-2 QFPROM_CORR_PTE_ROW0_LS

Bit location	Name	Description
[bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and thisdocument. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code as shown in the following table:

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	SM-7325	-1	-PSP	1287			-TR	-00	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example: SM-7325-1-PSP1287-TR-00-0-AB

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in the following table:

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	Hardware revision number (JTAG_ID - see Table 4-2)	FEATURE_ID (see Table 4-2) [b]	Hardware version	Source configuration code (S) [c]	Comments	Sample date
SM7325	ES	100-AB	0x0 0192 0E1	0x3	v1.0	0	CPU 4X 2.4 GHz,4X 1.8 GHz; 16 GB LPDDR4; GPU 550 M; ELITEG; SEC-CAM-DSP; C/G/W/T/L-DLL 12- ULL 2/5G sub-6, 120 M mmW, SHDR	2/11/2021

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
[b] The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-5.

Table 4-5 Source configuration code

S value	Die	F value = F
0	Digital	TSMC
Other columns and rows will be added in future revisions of this document, if needed.		

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in the following table:

NOTE The appropriate MSL rating is shaded in the table.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM7325 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM7325 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SM7325 Package Thermal Model Icepak* (HS11-19448-5HW) and the *SM7325 Package Thermal Model FloTHERM* (HS11-19448-6HW) from the CreatPoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-19448-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-19448-6HW

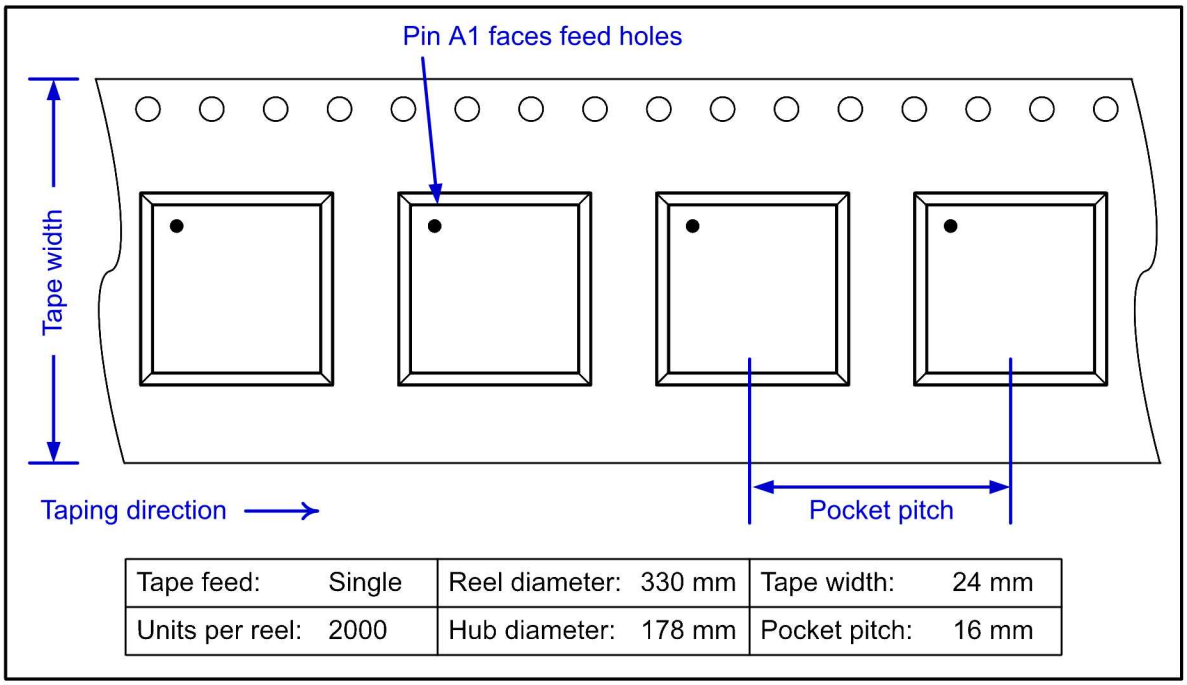
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM7325 tape carrier is shown in the following figure, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in the following figure.

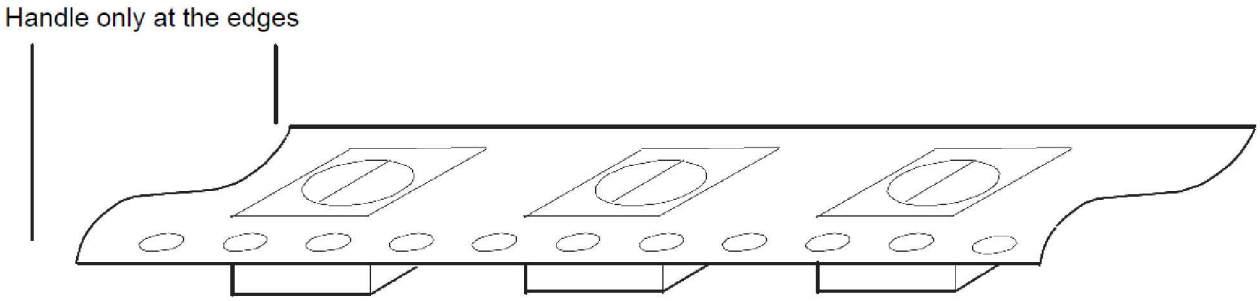


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

SM7325 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM7325 if the conditions specified in and have **not been exceeded**.

It is necessary to bake the SM7325 if any condition specified in or has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in SMT assembly guidelines can be performed using daisy chain components.

Daisy chain PCB routing recommendations are available for download.

This link will be provided in a future revision of this document.

7 Part reliability

This information will be provided in a future revision of this document.

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	November 2020	Initial release
AB	January 2021	■ Global: Updated the CreatePoint link for pin assignment spreadsheet ■ Figure 2-1 *SM7325 pin assignments*: Updated the pin map ■ Table 2-2 *Pin descriptions – general-purpose input/output ports*: ▫ Updated the functional description of GPIO_76, GPIO_77, GPIO_78, GPIO_144, and GPIO_161 ▫ Updated BL15 and BJ15 pad name and functional description ■ Table 2-4 *Pin descriptions – DNC, ground, and power-supply pins*: ▫ Added W29, AF32, BD38, BB8, L11, and AJ37 in the ground pins ▫ Added V30 in the VDD_APC0 power-supply pins ▫ Added AE33 in the VDD_APC1 power-supply pins ▫ Added BC39 in the VDD_GFX power-supply pins ▫ Added BC9 in the VDD_MODEM power-supply pins ▫ Added AV26 in the VDD_MX power-supply pins ▫ Added M10 in the VDD_CX power-supply pins ▫ Added AG39 in the VDD_LPI_CX power-supply pins
AC	March 2021	■ Global: ▫ Updated the Kryo Gold and Kryo Silver application frequency ▫ Updated the LPDDR5 SDRAM frequency to 3200 MHz ■ Table 1-1 *SM7325 features*: Updated the modem capability ■ Table 1-2 *Key modem features*: Corrected the 5G (SIM2) description ■ Table 2-1 *I/O description (pad type) parameters*: Updated the voltage for pad group 11 ■ Figure 2-1 *SM7325 pin assignments*: Updated the QLink1_L3_M/P pin ■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: ▫ Added GNSS configurable function in GPIO_10, GPIO_11 ▫ Updated the wake-up function for GPIO_159, GPIO_161, and GPIO_163 ■ Electrical specifications: Added the following sections: ▫ Absolute maximum ratings through RF and power management interfaces ■ Mechanical information Added the following sections: ▫ Part marking ▫ Device ordering information ▫ Device moisture sensitivity level ▫ Thermal characteristics ■ Carrier, storage, and handling information: Added information ■ PCB mounting guidelines: Added information

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.