Device description

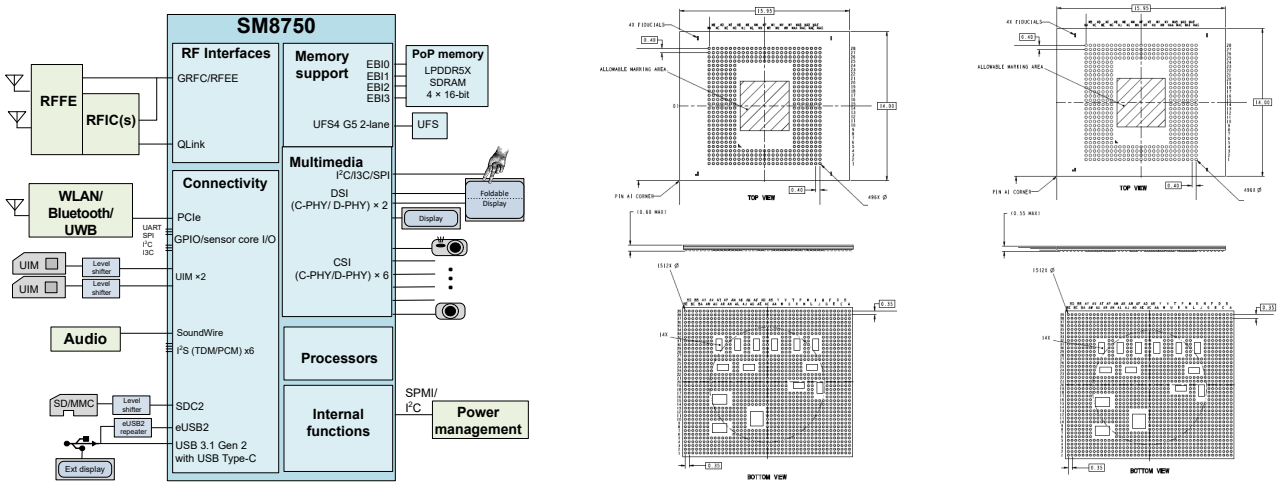
The SM8750/SM8750P device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with a 3 nm process, for superior performance and power efficiency. SM8750/SM8750P includes the following key components:

- Qualcomm® Oryon™ CPU
- Qualcomm® Adreno™ GPU 8-series for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ Image Signal Processor (ISP) 8-series for the ultimate photography and videography experiences
- Adreno VPU 8-series for high-quality, ultra HD video encode and decode
- Adreno DPU 8-series for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 bands (Rel 17 integrated modem)

Key features

- Low-Power AI (LPAI) subsystem with dedicated DSP and AI accelerator (eNPU) supporting always-on audio, always sensing camera (ASC), sensors, and contextual data streams that is, Qualcomm Sensing Hub (QSH).
- Qualcomm Aqstic™ Audio Technologies WCD9395 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Secure Processing Unit for advanced secure use cases
- Qualcomm® Hexagon™ Tensor Processor (HTP) with Hexagon Vector eXtensions (HVX) and Hexagon Matrix eXtensions (HMX)
- Qualcomm® FastConnect™ 7900 system with WCN788x, 802.11be, 2x2 MIMO, Bluetooth 5.4, and ultra wideband (UWB)
- Quad-channel package-on-package (PoP) high-speed LPDDR5X SDRAM
- 15.95 × 14.0 × 0.60 mm MPSP1512 PoP
- 15.95 × 14.0 × 0.55 mm MPSP1512 PoP

SM8750/SM8750P high-level block diagram and MPSP1512 outline drawing



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Figures

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

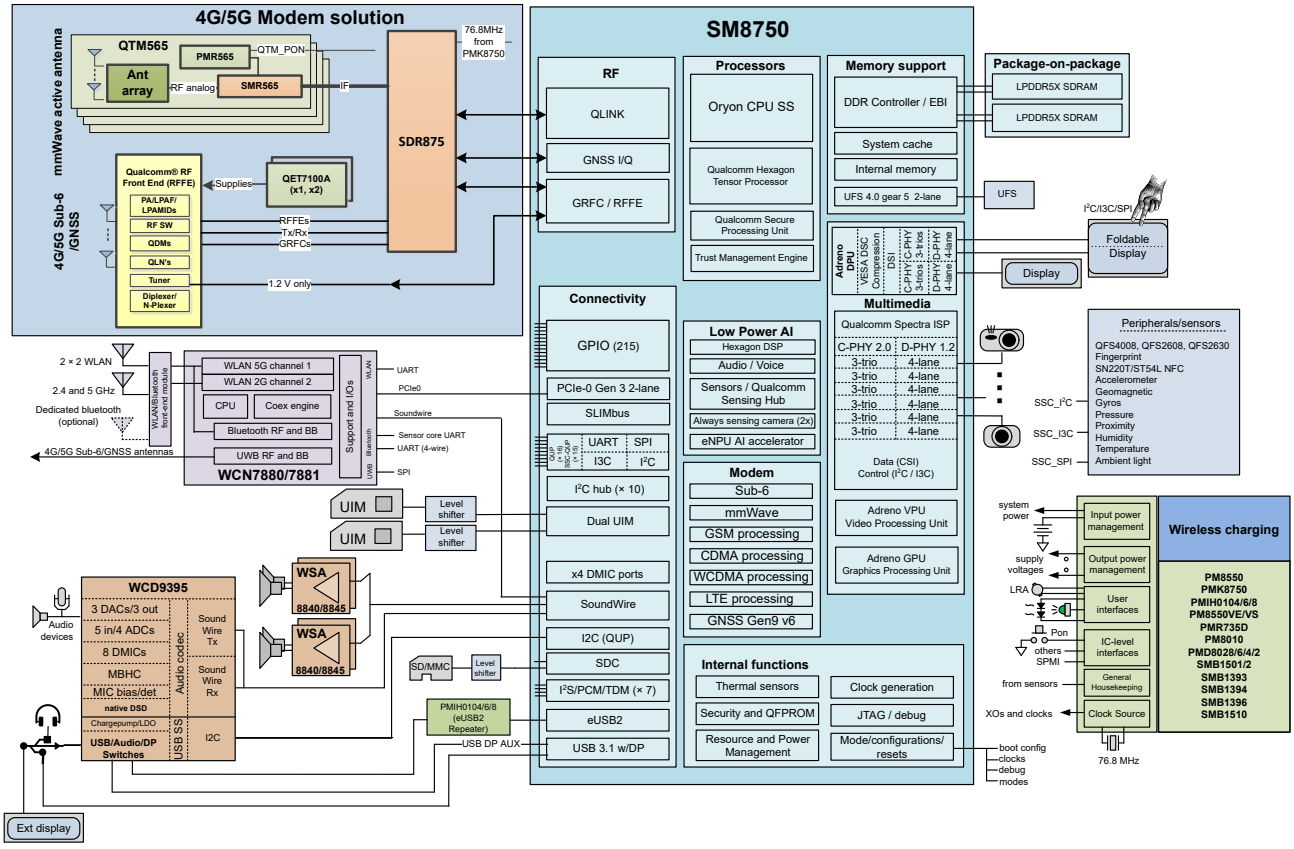

Figure 1-1 SM8750 + SDR875 (sub-6/mmW solution) functional block diagram and example application

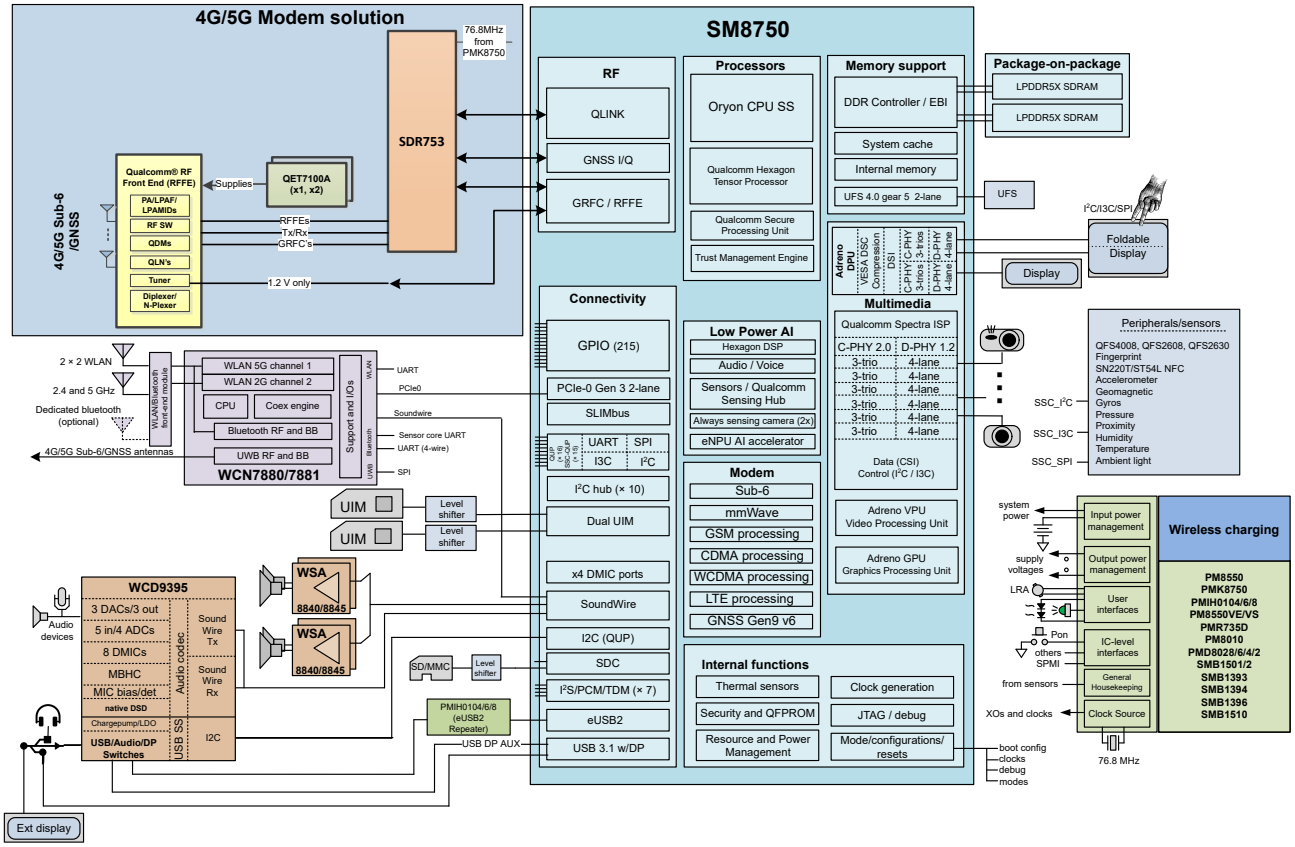

Figure 1-2 SM8750 + SDR753 (sub-6 solution) functional block diagram and example application

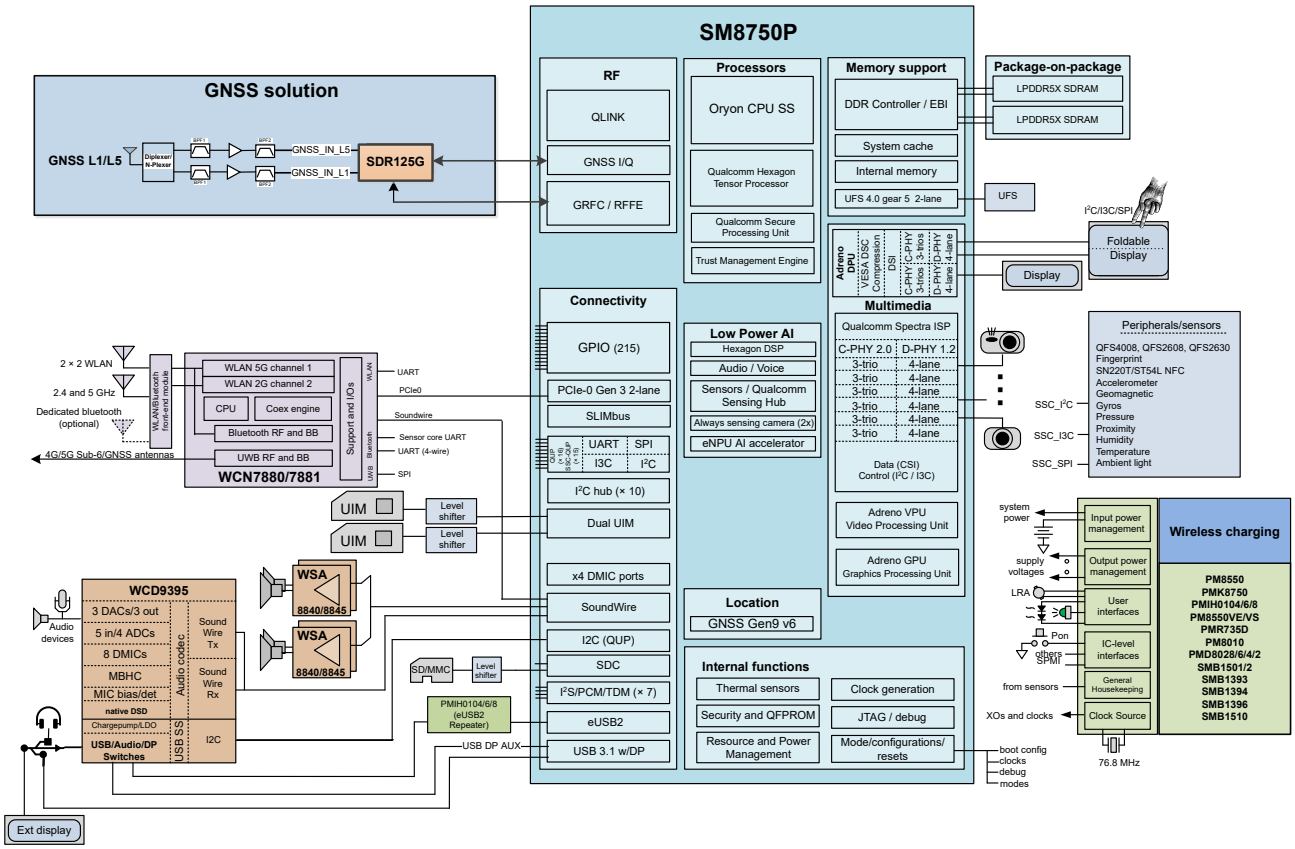

Figure 1-3 SM8750P functional block diagram and example application

1.2 SM8750/SM8750P features

NOTE Some of the hardware features integrated within the SM8750/SM8750P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8750/SM8750P features.

Table 1-1 SM8750/SM8750P features

Feature	SM8750/SM8750P capability
Processors	
Applications	Oryon CPU subsystem
Digital signal processing and artificial intelligence	■ Hexagon Tensor Processor □ V79 AI-optimized tensor processor □ 8x scalar threads with enhanced micro architecture □ 6x HVX vector tightly couple coprocessors optimized for pixel processing □ 1x HMX matrix tightly couple coprocessor optimized for deep neural network processing, MAC arithmetic formats include INT8, A16W8, A8W4, and FP16 □ Large VTCM □ BW compression □ Improved power efficiency and concurrency ■ AI use cases □ Generative AI □ Noise reduction □ Super resolution □ AI ISP □ HDR □ Image enhancement □ Segmentation □ Depth estimation □ Classification/detection ■ For imaging, video, audio, and data-based NN use cases. ■ The hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the hexagon software algorithmic functions. ■ The audio/sensors hexagon DSP is dedicated to the low-power AI subsystem with support for always-on, low-power use cases. It incorporates a dedicated AI processor for offloading neural network use cases to improve the performance and minimize power consumption. ■ All hexagon DSP is cache-based processors with full access to DDR memory for large memory requirements.
Always-on system	■ Always-on subsystem with always-on processor ■ Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Modem and location	
Modem	3G/4G/5G – mmWave and sub-6 bands (Rel 17) only for SM8750
Location	■ Gen9 v6 ■ LocTech 24 SW ■ GPS L1/L5/L2C, GLO G1, BDS B1I/B1C/B2A/B2B, GAL E1/E5A/E5B, QZSS L1/L5/L2C, NavIC L1/L5 ■ An analog GNSS interface to the transceiver IC
Memory support	

Table 1-1 SM8750/SM8750P features (cont.)

Feature	SM8750/SM8750P capability
System memory via EBI on PoP	Four-channel PoP high-speed memory – LPDDR5X SDRAM (4 × 16-bit) designed for a TBD MHz with system cache
Storage Via UFS Via SDC	UFS 4.0 gear 5 Rate B, 1x 2-lane ICE with 4500 MB/s read and 4000 MB/s write SD v3.0 4 bit for SD card
Multimedia	
Display	Adreno 8-series DPU ■ Internal panel resolution up to 3840 × 2560 at 144 Hz. Higher resolutions and refresh rates can also be supported. ■ Supports dual MIPI-DSI ports, with support for split-link for fold use case. ■ External panel support: DisplayPort v1.4 with MST (up to 8K60) ■ Compression support: 8x DSC v1.2 ■ Processing: HDR10/10+, HDR Vivid, Dolby Vision HDR, Wide color gamut, Scaling, SPR, Demura, FP16 blending ■ Power-saving: Local tone mapping, QSync, variable refresh rate
Camera	New upgrade Spectra ISP with flexible architecture to support connectivity to multiple cameras and advanced RAW domain image processing plug in and out. Furthermore, up to 5 cameras may operate concurrently due to the Qualcomm Spectra's 3 TFEs and 2 IFE-lites. ■ Hardware interface ▫ Triple 48 MP ISPs ▫ Six combo-PHYs with 4 lanes for D-PHY and 3 trios for C-PHY each – D-PHY v1.2: 2.5 Gbps/lane – C-PHY v2.0: 13.68 Gbps/trio ▫ Connect up to 12x/18x cameras, 5x concurrent ■ Throughput ▫ 3 × 48 MP at 30 fps ZSL without in-ISP binning ▫ 320 MP non-ZSL snapshot capture ▫ 3 × 12 MP at 240 fps fast shutter sensor support - PHY and RAW dump ■ Key improvements ▫ Provision of RAW and RGB tap-out/tap-in ▫ Unified HDR dataflow ▫ Enhanced HDR alignment ▫ Enhanced temporal denoise ▫ 3A enhancement with AI segmentation ▫ Improved cognitive ISP feature with AI brain
EVA	■ A depth processor for iTOF ■ Reprojection and grid inversion engine (RGE) ■ Dense motion map (SGM based OF, 1080p at 60 fps) ■ Depth from stereo (SGM-based DFS, 720p at 60 fps), concurrent with DMM ■ Warping, scaling, rotation engine ■ fTexture, pyramid generation, Harris corner detector, Shi-Tomasi detector, FREAK descriptors, global motion estimation using feature points
Adreno video processing unit (VPU)	■ Adreno 8-series VPU ■ UHD 8K video processing unit ■ Video decode up to 4K at 240 fps/8K at 60 fps and video encode up to 4K at 120 fps/8K at 30 fps

Table 1-1 SM8750/SM8750P features (cont.)

Feature	SM8750/SM8750P capability
	■ Concurrent decode up to 4K at 60 fps and encode up to 4K at 60 fps for wireless display ■ Max 24 concurrent stream support ■ Native decode support for H.264, H.265, VP9, and AV1 formats ■ Native encode support for H.264 and H.265 formats ■ Slice-based encoder support for low-latency performance ■ Max 8192 × 4320/Min 96 × 96 resolution of frame support ■ Loss frame compression (UBWC) support
Adreno graphic processing unit (GPU)	■ Adreno 8-series GPU ■ OpenGL ES 3.2, Vulkan 1.3 OpenCL 3.0 full profile Adreno NN direct ■ Ray tracing pipelines ■ GMEM improvements for compute and graphics
Low-power AI subsystem	Merged low-power island, for always-on audio/voice, sensors, sensing hub, and always sensing camera ■ Hexagon V79 2 × cluster – 4 Thread DSP ■ 11.75 MB of LPI memory ▫ 4 MB TCM (DSP and LPAI) ▫ 7.75 MB of LPI LLC ■ Dual eNPU5 AI processor to accelerate neural networking use cases ■ Qualcomm Sensing Hub – ultrasound stream added; AI Activity Recognition 2.0 using eNPU5
Sensors hardware	■ Data acquisition engine (DAE) - buffer to enable batching of sensor data without waking up the DSP ■ Context change detector (CCD) 6.0 ▫ Hardware blocks to detect potential changes in context that are validated in software ▫ Wakes up DSP once context changes are detected
Sensors interfaces and supported sensors	■ Fifteen dedicated buses ▫ 4 I3C/I^2C, 3 SPI, 3 I^2C, 2 UART ▫ 2 I3C/I^2C, 1 I^2C for ASC ■ 7 × I3C IBI for DAE and DSP ■ Sensors supported in QTI POR: ▫ 2 × Accelerometer/Gyroscope ▫ Magnetometer ▫ Ambient Light/Proximity ▫ Pressure ▫ Humidity/Temperature ▫ SAR ▫ Hall ▫ Always sensing camera ▫ Plus others per customer inputs with I3C, I^2C, UART, SPI interface could be supported
Qualcomm Sensing Hub (QSH) supported technologies	■ QSH enables multiple data streams providing enhanced contextual data from: ▫ Sensors ▫ Always sensing camera ▫ Audio ▫ WWAN ▫ Location/Geofencing

Table 1-1 SM8750/SM8750P features (cont.)

Feature	SM8750/SM8750P capability
	▫ BLE ▫ Wi-Fi
Audio and voice hardware	■ Hardware linear echo cancellation accelerator ■ DSP-offload for audio playback (analog, Bluetooth audio, USB digital audio)
Audio interfaces	SoundWire ■ One for WCN788x ■ Two (Tx with 3 data lanes and Rx with 2 data lanes) for WCD9395 and PMIC haptics ■ Two to support up to 4 WSA884x smart speaker amplifiers DMICs ■ 4 DMIC ports support up to 8 DMICs ■ Up to 4 DMICs for low-power voice activation I^2S ■ 6 I^2S with 2x data lanes to support full duplex stereo, or up to 4 channel Tx/Rx application ■ 1 I^2S supports 4 data lanes for up to 8 channels Tx/Rx application TDM/PCM: Up to 32 channels at 48 kHz per individual interface (Qualcomm Technologies, Inc. (QTI) I^2S supports both TDM and PCM modes.)
Audio and voice algorithms	Voice UI ■ Snapdragon Voice Activation keyword detection ■ Echo cancellation and noise suppression (ECNS) Voice call ■ AI-based noise suppression ■ Far-end noise suppression Audio record ■ Ambient noise suppression ■ HDR record
Codec	Integrated within the WCD9395 high fidelity audio codec
Speaker amplifier	Integrated within the WSA8840/WSA8845/WSA8845H class-H, low noise smart amplifier
Connectivity	
I/Os	Dual voltage (1.2 V/1.8 V) support. For details, see Pin definitions.
Qualcomm universal peripheral (QUP) ports	Qualcomm universal peripheral (QUP) v3 support. 16 QUP serial engines + 15 SSC-QUP serial engines ■ UART ■ I^2C ■ I3C ■ SPI 10 I^2C hubs
USB	One USB 3.1 ports: Gen 2 10 Gbps (DisplayPort + data), support Type-C with DisplayPort v1.4, embedded USB (eUSB2.0)
UIM	Two 1.8 V/3 V SIM card using external level shifter
PCIe	2-lane Gen 3
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4) ■ SDC2: 1.2 V only; SD 3.0

Table 1-1 SM8750/SM8750P features (cont.)

Feature	SM8750/SM8750P capability
	■ 1.8 V/3 V SD card operation using external level shifter ■ SDC4: dual-voltage, SDIO 3.0
Touchscreen support	Capacitive panels via ext IC (I^2C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display QFS4008, QFS2608, QFS2630
Configurable GPIOs	
Number of GPIOs	215 – GPIO_0 to GPIO_214
Security technologies	
Crypto	AES-GCM, HW ECC, RSA, SHA2, SHA3, SHAKE 128/256, SM2/SM3/SM4, ICE crypto engine v5 (CE5), FIPS 140-3 certified, PRNG compliant to NIST 800-90B
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sandboxing
Secure boot, debug and related tools	Secure boot/debug security with Sectools 2.0; easy to use tool set
Key management	Hardware key manager
User data encryption	File-based encryption (FBE)
Memory protection	DRAM memory protection for execution environments (TEEs and VMs)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.x)
Hypervisor	Qualcomm® Type-1 hypervisor enables multiple trusted VMs (TVMs), Google AVF support
DSP security	DSP secure domain
HLOS kernel security	Qualcomm® runtime kernel security (QRKS)
Cellular connection security	Qualcomm® cellular connection security
QTEE and TVM services	DRM Widevine V18 L1, HDCP v2.3, Qualcomm® content protection, IP protection framework, camera security framework, trusted UI framework, trusted location, trusted time, QC WES device attestation service, QC WES secure provisioning service, QC WES third-party feature licensing service
SPU	EAL5+ common criteria certified secure processing unit (SPU) for high assurance use cases like Android Strongbox and ieUICC (iSIM)
Internal functions	
Boot	See *SM8750 Boot and CoreBSP Architecture Overview* (80-TBD-11) for the details of boot sequence. Emergency boot over USB 3.1
PLLs and clocks	■ 76.8 MHz X'tal ■ Multiple clock regimes; watchdog and sleep timers ■ Input: 38.4 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD)
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	SPMI; also I^2C as needed

Table 1-1 SM8750/SM8750P features (cont.)

Feature	SM8750/SM8750P capability
Wireless connectivity	
WLAN	PCIe interface
Bluetooth	SoundWire/UART interface
UWB	SPI/UCI interface
Fabrication technology, package, and major companion ICs	
Digital die	3 nm process
Package	1512 MPSP
PoP– small, thermally efficient package	15.95 × 14.0 × 0.60 mm 15.95 × 14.0 × 0.55 mm
WLAN/ Bluetooth/UWB	WCN7881, WCN7880
WLAN/Bluetooth	WCN7861, WCN7860
RF	SDR875 (4G/Sub-6/mmW/GNSS), SDR753 (4G/Sub-6/GNSS) QTM565 (mmW)
PMIC	PM8550, PMK8750, PMIH0104/6/8, PM8550VE/VS, PMD8028/6/4/2, PM8010 × 2, PMR735D
Audio	WCD9395, WSA8840/WSA8845/WSA8845H

2 Pin definitions

The SM8750/SM8750P is the lower device within a PoP system, as shown and explained in the figure below.

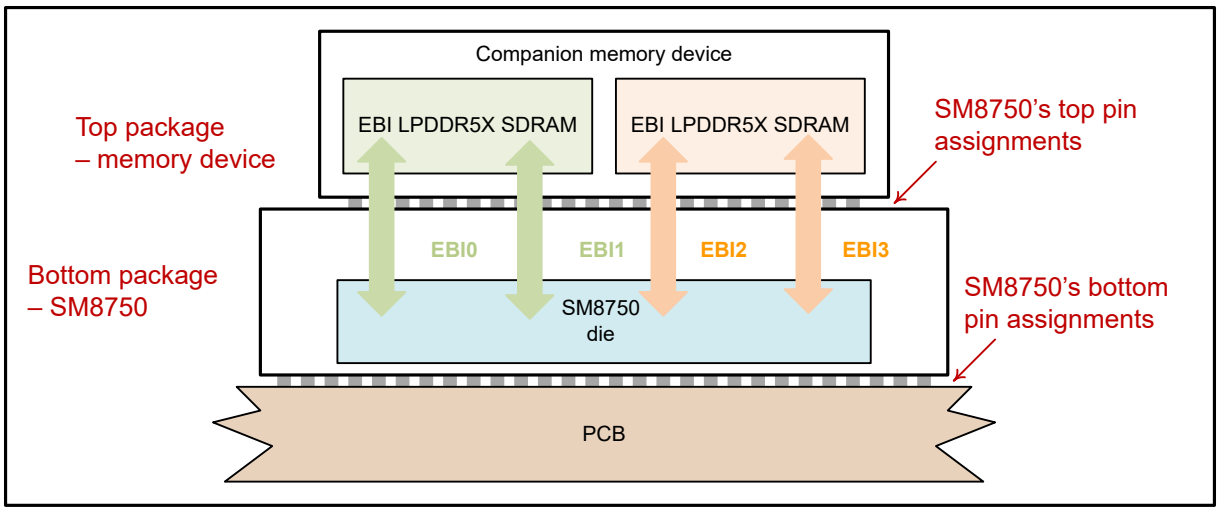

Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8750 bottom pins (Pin assignments: MSM bottom)
- SM8750 top pins (Pin assignments: MSM top)

2.1 I/O parameter definitions

Table 2-1 I/O description (pin type) parameters

Symbol	Description
Pin attribute	
AI	Analog input (does not include pin circuitry)
AO	Analog output (does not include pin circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pin pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pin voltage groupings for baseband circuits	
PX0	Pin group 0 (SPMI0, SPMI1, RESIN_N); 1.2 V
PX11	Pin group 11 (CXO); 1.2 V
PX13	Pin group 13 (SP_ARI_POWER_ALARM); 1.85 V
PX14	Pin group 14 (UFS0_RESET_N , SDC2, JTAG, UIM0, PS_HOLD, SLEEP_CLK, MODE, Modem, Audio SWR); 1.2 V
PX701	Pad group 701 (I/O pad); 1.8 V/1.2 V
PX702	Pad group 702 (I/O pad); 1.8 V/1.2 V
PX703	Pad group 703 (I/O pad); 1.8 V/1.2 V
PX704	Pad group 704 (I/O pad); 1.8 V/1.2 V
PX705	Pad group 705 (I/O pad); 1.8 V/1.2 V
PX706	Pad group 706 (I/O pad); 1.8 V/1.2 V
PX708	Pad group 708 (I/O pad); 1.8 V/1.2 V
PX709	Pad group 709 (I/O pad); 1.8 V/1.2 V
PX710	Pad group 710 (I/O pad); 1.8 V/1.2 V
PX711	Pad group 711 (I/O pad); 1.8 V/1.2 V
PX712	Pad group 712 (I/O pad); 1.8 V/1.2 V

Table 2-1 I/O description (pin type) parameters (cont.)

Symbol	Description
PX713	Pad group 713 (I/O pad); 1.8 V/1.2 V
PX714	Pad group 714 (I/O pad); 1.8 V/1.2 V
PX715	Pad group 715 (I/O pad); 1.8 V/1.2 V
PX716	Pad group 716 (I/O pad); 1.8 V/1.2 V
PX717	Pad group 717 (I/O pad); 1.8 V/1.2 V
PX718	Pad group 718 (I/O pad); 1.8 V/1.2 V
PX719	Pad group 719 (I/O pad); 1.8 V/1.2 V
PX720	Pad group 720 (I/O pad); 1.8 V/1.2 V
PX721	Pad group 721 (I/O pad); 1.8 V/1.2 V
PX722	Pad group 722 (I/O pad); 1.8 V/1.2 V

NOTE For detailed SM8750 pad group assignment, see the *SM8750/SM8750P Digital Baseband Design Guidelines/Training Slides* (80-64994-5).

2.2 Pin assignments: MSM bottom

2.2.1 Pin map: MSM bottom

The SM8750/SM8750P is available in the MPSP1512 package. Its bottom surface is equivalent to an MPSP1512 that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Mechanical information for package details and Pin assignments: MSM top for information about the top pin assignments.

A high-level view of the pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM8750/SM8750P Pin Assignment and GPIO Configuration Spreadsheet* (80-64994-1A). This Microsoft Excel spreadsheet lists all SM8750/SM8750P pin numbers (in alphanumeric order), pin names, pin voltages, pin types, and functional descriptions.

NOTE Click the following link to download the *SM8750/SM8750P Pin Assignment and GPIO Configuration Spreadsheet* (80-64994-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-64994-1A

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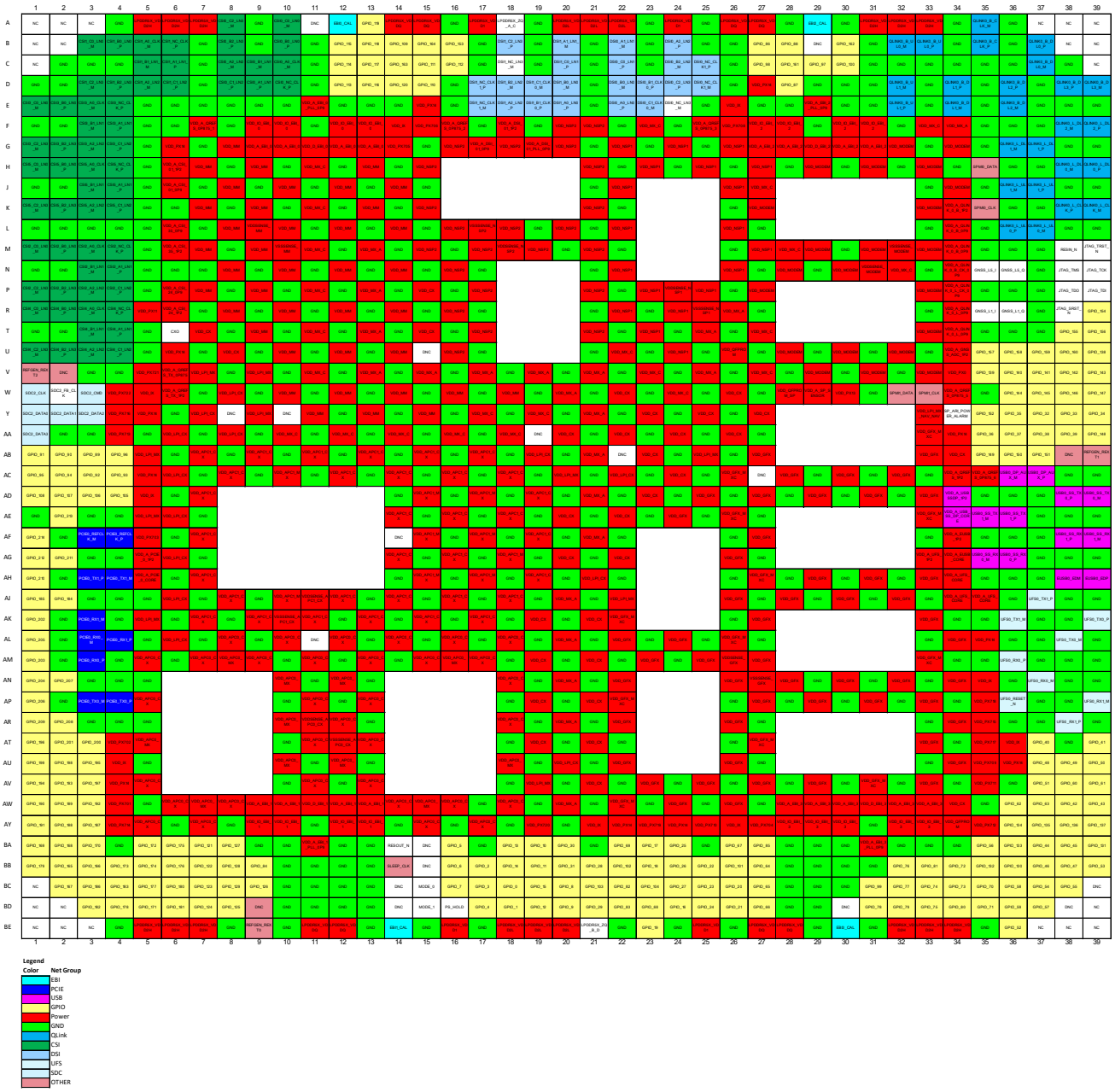

Figure 2-2 SM8750 bottom pin assignments (top view)

2.2.2 Pin descriptions: MSM bottom

The bottom pins are described in Table 2-2 through Table 2-6.

Table 2-2 MSM bottom pin descriptions – general pins

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
C10	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential clock - minus MIPI CSI0 (C-PHY), trio lane 0 – A
D9	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 1 - plus MIPI CSI0 (C-PHY), trio lane 1 – A
C8	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 2 - minus MIPI CSI0 (C-PHY), trio lane 2 – A
B10	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 0 - plus MIPI CSI0 (C-PHY), trio lane 0 – B
C9	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 1 - minus MIPI CSI0 (C-PHY), trio lane 1 – B
B8	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 3 - plus MIPI CSI0 (C-PHY), trio lane 2 – B
A10	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 0 - minus MIPI CSI0 (C-PHY), trio lane 0 – C
D8	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 2 - plus MIPI CSI0 (C-PHY), trio lane 1 – C
A8	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 3 - minus MIPI CSI0 (C-PHY), trio lane 2 – C
D10	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential clock - plus MIPI CSI0 (C-PHY), no connect
B5	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential clock - minus MIPI CSI1 (C-PHY), trio lane 0 – A
C6	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 1 - plus MIPI CSI1 (C-PHY), trio lane 1 – A

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
D5	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 2 - minus MIPI CSI1 (C-PHY), trio lane 2 – A
B4	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 0 - plus MIPI CSI1 (C-PHY), trio lane 0 – B
C5	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 1 - minus MIPI CSI1 (C-PHY), trio lane 1 – B
D4	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 3 - plus MIPI CSI1 (C-PHY), trio lane 2 – B
B3	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 0 - minus MIPI CSI1 (C-PHY), trio lane 0 – C
D6	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 2 - plus MIPI CSI1 (C-PHY), trio lane 1 – C
D3	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 3 - minus MIPI CSI1 (C-PHY), trio lane 2 – C
B6	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential clock - plus MIPI CSI1 (C-PHY), no connect
M3	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential clock - minus MIPI CSI2 (C-PHY), trio lane 0 – A
N4	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 1 - plus MIPI CSI2 (C-PHY), trio lane 1 – A
P3	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 2 - minus MIPI CSI2 (C-PHY), trio lane 2 – A
M2	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 0 - plus MIPI CSI2 (C-PHY), trio lane 0 – B
N3	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 1 - minus MIPI CSI2 (C-PHY), trio lane 1 – B
P2	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 3 - plus MIPI CSI2 (C-PHY), trio lane 2 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M1	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 0 - minus MIPI CSI2 (C-PHY), trio lane 0 – C
P4	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 2 - plus MIPI CSI2 (C-PHY), trio lane 1 – C
P1	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 3 - minus MIPI CSI2 (C-PHY), trio lane 2 – C
M4	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential clock - plus MIPI CSI2 (C-PHY), no connect
E3	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential clock - minus MIPI CSI3 (C-PHY), trio lane 0 – A
F4	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 1 - plus MIPI CSI3 (C-PHY), trio lane 1 – A
G3	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 2 - minus MIPI CSI3 (C-PHY), trio lane 2 – A
E2	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 0 - plus MIPI CSI3 (C-PHY), trio lane 0 – B
F3	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 1 - minus MIPI CSI3 (C-PHY), trio lane 1 – B
G2	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 3 - plus MIPI CSI3 (C-PHY), trio lane 2 – B
E1	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 0 - minus MIPI CSI3 (C-PHY), trio lane 0 – C
G4	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 2 - plus MIPI CSI3 (C-PHY), trio lane 1 – C
G1	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 3 - minus MIPI CSI3 (C-PHY), trio lane 2 – C
E4	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential clock - plus MIPI CSI3 (C-PHY), no connect

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
R3	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential clock - minus MIPI CSI4 (C-PHY), trio lane 0 – A
T4	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 1 - plus MIPI CSI4 (C-PHY), trio lane 1 – A
U3	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 2 - minus MIPI CSI4 (C-PHY), trio lane 2 – A
R2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 0 - plus MIPI CSI4 (C-PHY), trio lane 0 – B
T3	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 1 - minus MIPI CSI4 (C-PHY), trio lane 1 – B
U2	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 3 - plus MIPI CSI4 (C-PHY), trio lane 2 – B
R1	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 0 - minus MIPI CSI4 (C-PHY), trio lane 0 – C
U4	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 2 - plus MIPI CSI4 (C-PHY), trio lane 1 – C
U1	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 3 - minus MIPI CSI4 (C-PHY), trio lane 2 – C
R4	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential clock - plus MIPI CSI4 (C-PHY), no connect
H3	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential clock - minus MIPI CSI5 (C-PHY), trio lane 0 – A
J4	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 1 - plus MIPI CSI5 (C-PHY), trio lane 1 – A
K3	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 2 - minus MIPI CSI5 (C-PHY), trio lane 2 – A
H2	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 0 - plus MIPI CSI5 (C-PHY), trio lane 0 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
J3	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 1 - minus MIPI CSI5 (C-PHY), trio lane 1 – B
K2	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 3 - plus MIPI CSI5 (C-PHY), trio lane 2 – B
H1	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 0 - minus MIPI CSI5 (C-PHY), trio lane 0 – C
K4	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 2 - plus MIPI CSI5 (C-PHY), trio lane 1 – C
K1	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 3 - minus MIPI CSI5 (C-PHY), trio lane 2 – C
H4	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential clock - plus MIPI CSI5 (C-PHY), no connect
T6	CXO	PX11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
E22	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 0 - plus MIPI DSI0 (C-PHY), trio lane 0 – A
B22	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 1 - minus MIPI DSI0 (C-PHY), trio lane 1 – A
B24	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 2 - plus MIPI DSI0 (C-PHY), trio lane 2 – A
D22	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 0 - minus MIPI DSI0 (C-PHY), trio lane 0 – B
D23	DSI0_B1_CLK0_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 0 - plus MIPI DSI0 (C-PHY), trio lane 1 – B
C24	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 2 - minus MIPI DSI0 (C-PHY), trio lane 2 – B
C22	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 1 - plus MIPI DSI0 (C-PHY), trio lane 0 – C

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
E23	DSI0_C1_CLK0_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 0 - minus MIPI DSI0 (C-PHY), trio lane 1 – C
D24	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 3 - plus MIPI DSI0 (C-PHY), trio lane 2 – C
D25	DSI0_NC_CLK1_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 1 - minus MIPI DSI0 (C-PHY), no connect
C25	DSI0_NC_CLK1_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 1 - plus MIPI DSI0 (C-PHY), no connect
E24	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 – minus MIPI DSI 0 (C-PHY), no connect
E20	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 0 - plus MIPI DSI1 (C-PHY), trio lane 0 – A
B20	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 1 - minus MIPI DSI1 (C-PHY), trio lane 1 – A
E18	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 2 - plus MIPI DSI1 (C-PHY), trio lane 2 – A
D20	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 0 - minus MIPI DSI1 (C-PHY), trio lane 0 – B
E19	DSI1_B1_CLK0_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 0 - plus MIPI DSI1 (C-PHY), trio lane 1 – B
D18	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 2 - minus MIPI DSI1 (C-PHY), trio lane 2 – B
C20	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 1 - plus MIPI DSI1 (C-PHY), trio lane 0 – C
D19	DSI1_C1_CLK0_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 0 - minus MIPI DSI1 (C-PHY), trio lane 1 – C
B18	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 3 - plus MIPI DSI1 (C-PHY), trio lane 2 – C

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
E17	DSI1_NC_CLK1_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 1 - minus (no support for DSI1 split clock) MIPI DSI1 (C-PHY), no connect
D17	DSI1_NC_CLK1_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 1 - plus (no support for DSI1 split clock) MIPI DSI1 (C-PHY), no connect
C18	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - minus MIPI DSI 1 (C-PHY), no connect
A12	EBI0_CAL	EBI	AI	EBI0 calibration resistor
BE14	EBI1_CAL	EBI	AI	EBI1 calibration resistor
A29	EBI2_CAL	EBI	AI	EBI2 calibration resistor
BE30	EBI3_CAL	EBI	AI	EBI3 calibration resistor
AH38	EUSB0_EDM	–	AI, AO	EUSB0 port - minus
AH39	EUSB0_EDP	–	AI, AO	EUSB0 port - plus
R35	GNSS_L1_I	–	AI	GNSS L1 - I
R36	GNSS_L1_Q	–	AI	GNSS L1 - Q
N35	GNSS_L5_I	–	AI	GNSS L5 - I
N36	GNSS_L5_Q	–	AI	GNSS L5 - Q
R38	JTAG_SRST_N	PX14	DIS-PU	JTAG reset for debug
N39	JTAG_TCK	PX14	DIS-PU	JTAG clock input
P39	JTAG_TDI	PX14	DIS-PU:nppdkp	JTAG data input
P38	JTAG_TDO	PX14	DO-Z	JTAG data output
N38	JTAG_TMS	PX14	DI-PU:nppdkp	JTAG mode select input
M39	JTAG_TRST_N	PX14	DI-PD:pu	JTAG reset
A18	LPDDR5X_ZQ_A_C	LPDDR5X_VDDQ	AI	ZQ calibration reference (channels A and C)
BE21	LPDDR5X_ZQ_B_D	LPDDR5X_VDDQ	AI	ZQ calibration reference (channels B and D)
BC15	MODE_0	PX14	DI	Mode control bit 0 – unconnected for native mode
BD15	MODE_1	PX14	DI	Mode control bit 1 – unconnected for native mode

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
AF3	PCIE0_REFCLK_M	–	AO	PCIe 0 Gen 3 reference clock - minus
AF4	PCIE0_REFCLK_P	–	AO	PCIe 0 Gen 3 reference clock - plus
AL3	PCIE0_RX0_M	–	AI	PCIe 0 Gen 3 receive 0 - minus
AM3	PCIE0_RX0_P	–	AI	PCIe 0 Gen 3 receive 0 - plus
AK3	PCIE0_RX1_M	–	AI	PCIe 0 Gen 3 receive 1 - minus
AL4	PCIE0_RX1_P	–	AI	PCIe 0 Gen 3 receive 1 - plus
AP3	PCIE0_TX0_M	–	AO	PCIe 0 Gen 3 transmit 0 - minus
AP4	PCIE0_TX0_P	–	AO	PCIe 0 Gen 3 transmit 0 - plus
AH4	PCIE0_TX1_M	–	AO	PCIe 0 Gen 3 transmit 1 - minus
AH3	PCIE0_TX1_P	–	AO	PCIe 0 Gen 3 transmit 1 - plus
BD16	PS_HOLD	PX14	Z	Power-supply hold signal to PMIC
A35	QLINK0_B_CLK_M	–	AO	QLink0 port B clock - minus
B35	QLINK0_B_CLK_P	–	AO	QLink0 port B clock - plus
C37	QLINK0_B_DL0_M	–	AI	QLink0 port B lane D0 - minus
B37	QLINK0_B_DL0_P	–	AI	QLink0 port B lane D0 - plus
E34	QLINK0_B_DL1_M	–	AI	QLink0 port B lane D1 - minus
D34	QLINK0_B_DL1_P	–	AI	QLink0 port B lane D1 - plus
E36	QLINK0_B_DL2_M	–	AI	QLink0 port B lane D2 - minus
D36	QLINK0_B_DL2_P	–	AI	QLink0 port B lane D2 - plus
D39	QLINK0_B_DL3_M	–	AI	QLink0 port B lane D3 - minus
D38	QLINK0_B_DL3_P	–	AI	QLink0 port B lane D3 - plus
B32	QLINK0_B_UL0_M	–	AO	QLink0 port B lane U0 - minus
B33	QLINK0_B_UL0_P	–	AO	QLink0 port B lane U0 - plus
D32	QLINK0_B_UL1_M	–	AO	QLink0 port B lane U1 - minus
E32	QLINK0_B_UL1_P	–	AO	QLink0 port B lane U1 - plus
K39	QLINK0_L_CLK_M	–	AO	QLink0 port L clock - minus
K38	QLINK0_L_CLK_P	–	AO	QLink0 port L clock - plus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
H38	QLINK0_L_DL0_M	–	AI	QLink0 port L lane D0 - minus
H39	QLINK0_L_DL0_P	–	AI	QLink0 port L lane D0 - plus
G36	QLINK0_L_DL1_M	–	AI	QLink0 port L lane D1 - minus
G37	QLINK0_L_DL1_P	–	AI	QLink0 port L lane D1 - plus
F38	QLINK0_L_DL2_M	–	AI	QLink0 port L lane D2 - minus
F39	QLINK0_L_DL2_P	–	AI	QLink0 port L lane D2 - plus
L37	QLINK0_L_UL0_M	–	AO	QLink0 port L lane U0 - minus
L36	QLINK0_L_UL0_P	–	AO	QLink0 port L lane U0 - plus
J36	QLINK0_L_UL1_M	–	AO	QLink0 port L lane U1 - minus
J37	QLINK0_L_UL1_P	–	AO	QLink0 port L lane U1 - plus
BE9	REFGEN_REXT0	–	AI	Reference voltage bias
AB39	REFGEN_REXT1	–	AI	Reference voltage bias
V1	REFGEN_REXT2	–	AI	Reference voltage bias
M38	RESIN_N	PX0	DI	Reset input
BA14	RESOUT_N	PX14	DO	Reset output
W1	SDC2_CLK	PX14	DO	Secure digital controller 2 clock
W3	SDC2_CMD	PX14	B	Secure digital controller 2 command
Y1	SDC2_DATA_0	PX14	B	Secure digital controller 2 data bit 0
Y2	SDC2_DATA_1	PX14	B	Secure digital controller 2 data bit 1
Y3	SDC2_DATA_2	PX14	B	Secure digital controller 2 data bit 2
AA1	SDC2_DATA_3	PX14	B	Secure digital controller 2 data bit 3
W2	SDC2_FB_CLK	PX14	DI	Secure digital controller 2 feedback clock
BB14	SLEEP_CLK	PX14	DI	Sleep clock
K35	SPMI0_CLK	PX0	DO	Slave and PBUS interface for PMICs – clock
H35	SPMI0_DATA	PX0	BS-PD:nppukp	Slave and PBUS interface for PMICs – data
W33	SPMI1_CLK	PX0	DO	Slave and PBUS interface for PMICs – clock
W32	SPMI1_DATA	PX0	BS-PD:nppukp	Slave and PBUS interface for PMICs – data

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Y34	SP_ARI_POWER_ALARM	PX13	DI	Power alarm
AP36	UFS0_RESET_N	PX14	DO	UFS0 reset
AN37	UFS0_RX0_M	–	AI	UFS0 receive 0 - minus
AM36	UFS0_RX0_P	–	AI	UFS0 receive 0 - plus
AP39	UFS0_RX1_M	–	AI	UFS0 receive 1 - minus
AR38	UFS0_RX1_P	–	AI	UFS0 receive 1 - plus
AL38	UFS0_TX0_M	–	AO	UFS0 transmit 0 - minus
AK39	UFS0_TX0_P	–	AO	UFS0 transmit 0 - plus
AK36	UFS0_TX1_M	–	AO	UFS0 transmit 1 - minus
AJ37	UFS0_TX1_P	–	AO	UFS0 transmit 1 - plus
AC36	USB0_DP_AUX_M	–	AI, AO	USB0 DisplayPort aux – minus
AC37	USB0_DP_AUX_P	–	AI, AO	USB0 DisplayPort aux – plus
AG35	USB0_SS_RX0_M	–	AI	USB0 SuperSpeed receive 0 - minus
AG36	USB0_SS_RX0_P	–	AI	USB0 SuperSpeed receive 0 - plus
AF39	USB0_SS_RX1_M	–	AI	USB0 SuperSpeed receive 1 - minus
AF38	USB0_SS_RX1_P	–	AI	USB0 SuperSpeed receive 1 - plus
AD39	USB0_SS_TX0_M	–	AO	USB0 SuperSpeed transmit 0 - minus
AD38	USB0_SS_TX0_P	–	AO	USB0 SuperSpeed transmit 0 - plus
AE35	USB0_SS_TX1_M	–	AO	USB0 SuperSpeed transmit 1 - minus
AE36	USB0_SS_TX1_P	–	AO	USB0 SuperSpeed transmit 1 - plus

[a] See Table 2-1 for parameter and acronym definitions

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function - carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull up or pull down
- External connections
  - Unused inputs
  - Connections to high impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM8750/SM8750P GPIOs (in numeric order), pin numbers, pin voltages, pull states, and available configurations. Click the following link to download the *SM8750/SM8750P Pin Assignment and GPIO Configuration Spreadsheet* (80-64994-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-64994-1A

After successfully logging on, the document is downloaded.

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BC18	GPIO_0		PX720	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L0			QUP 2 SE 0 lane 0	
		IBI_I3C_QUP2_SE0_SDA			QUP2 in-band interrupt I3C SE clock 2	
		SSC_20			eGPIO - SSC I/O 20	
		SSC_20:SSC_QUPV3_SE8_0				
BD18	GPIO_1		PX720	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L1			QUP 2 SE 0 lane 1	
		IBI_I3C_QUP2_SE0_SCL			QUP2 in-band interrupt I3C SE data 2	
		SSC_21			eGPIO - SSC I/O 21	
		SSC_21:SSC_QUPV3_SE8_1				
BB17	GPIO_2		PX720	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L2			QUP 2 SE 0 lane 2	
		SSC_39			eGPIO - SSC I/O 39	
		SSC_39:ASC_CAM0_STANDBY				
BC17	GPIO_3		PX720	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L3			QUP 2 SE 0 lane 3	
		SSC_38			eGPIO - SSC I/O 38	
		SSC_38:ASC_CAM0_RESET				
BD17	GPIO_4		PX720	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L0			QUP 2 SE 1 lane 0	
		IBI_I3C_QUP2_SE1_SDA			QUP2 in-band interrupt I3C SE clock 2	
		SSC_22			eGPIO - SSC I/O 22	
		SSC_22:SSC_QUPV3_SE9_0				
BA16	GPIO_5		PX720	PD:nppukp	Configurable I/O	N
		QUP2_SE1_L1			QUP 2 SE 1 lane 1	
		IBI_I3C_QUP2_SE1_SCL			QUP2 in-band interrupt I3C SE data 2	
		SSC_23			eGPIO - SSC I/O 23	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_23:SSC_QUPV3_SE9_1				
BB16	GPIO_6		PX720	PD:nppukp	Configurable I/O	N
		QUP2_SE1_L2			QUP 2 SE 1 lane 2	
		SSC_41			eGPIO - SSC I/O 41	
		SSC_41:ASC_CAM1_STANDBY				
BC16	GPIO_7		PX720	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L3			QUP 2 SE 1 lane 3	
		SSC_40			eGPIO - SSC I/O 40	
		SSC_40:ASC_CAM1_RESET				
BC20	GPIO_8		PX719	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L0			QUP 2 SE 2 lane 0	
		IBI_I3C_QUP2_SE2_SDA			QUP2 in-band interrupt I3C SE clock 2	
BD20	GPIO_9		PX719	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L1			QUP 2 SE 2 lane 1	
		IBI_I3C_QUP2_SE2_SCL			QUP2 in-band interrupt I3C SE data 2	
BA19	GPIO_10		PX719	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L2			QUP 2 SE 2 lane 2	
		CCI_ASYNC_IN1			Camera control interface async 1	
BB19	GPIO_11		PX719	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L3			QUP 2 SE 2 lane 3	
		CCI_ASYNC_IN2			Camera control interface async 2	
BD19	GPIO_12		PX719	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L0			QUP 2 SE 3 lane 0	
		IBI_I3C_QUP2_SE3_SDA			QUP2 in-band interrupt I3C SE clock 2	
		QUP2_SE2_L6			QUP 2 SE 2 lane 6	
BA18	GPIO_13		PX719	PD:nppukp	Configurable I/O	N
		QUP2_SE3_L1			QUP 2 SE 3 lane 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		IBI_I3C_QUP2_SE3_SCL			QUP2 in-band interrupt I3C SE data 2	
		QUP2_SE2_L4			QUP 2 SE 2 lane 4	
BB18	GPIO_14		PX719	PD:nppukp	Configurable I/O	N
		QUP2_SE3_L2			QUP 2 SE 3 lane 2	
BC19	GPIO_15		PX719	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L3			QUP 2 SE 3 lane 3	
		CCI_ASYNC_IN0			Camera control interface async 0	
		QUP2_SE2_L5			QUP 2 SE 2 lane 5	
BD24	GPIO_16		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE4_L0			QUP 2 SE 4 lane 0	
BA23	GPIO_17		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE4_L1			QUP 2 SE 4 lane 1	
BB23	GPIO_18		PX14	PD:nppukp	Configurable I/O	Y
		WCN_SW_CTRL				
		QUP2_SE4_L2			QUP 2 SE 4 lane 2	
BE23	GPIO_19		PX14	PD:nppukp	Configurable I/O	Y
		WCN_SW_CTRL_WL_CX				
		QUP2_SE4_L3			QUP 2 SE 4 lane 3	
BC26	GPIO_20		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE5_L0			QUP 2 SE 5 lane 0	
BD26	GPIO_21		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE5_L1			QUP 2 SE 5 lane 1	
BB25	GPIO_22		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE5_L2			QUP 2 SE 5 lane 2	
BC25	GPIO_23		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L3			QUP 2 SE 5 lane 3	
		QUP2_SE5_L6			QUP 2 SE 5 lane 6	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BD25	GPIO_24		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L0			QUP 2 SE 6 lane 0	
BA24	GPIO_25		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE6_L1			QUP 2 SE 6 lane 1	
BB24	GPIO_26		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE6_L2			QUP 2 SE 6 lane 2	
BC24	GPIO_27		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L3			QUP 2 SE 6 lane 3	
BB21	GPIO_28		PX710	PD:nppukp	Configurable I/O	Y
		QUP2_SE7_L0			QUP 2 SE 7 lane 0	
		IBI_I3C_QUP2_SE7_SDA			QUP2 in-band interrupt I3C SE clock 2	
BD21	GPIO_29		PX710	PD:nppukp	Configurable I/O	N
		QUP2_SE7_L1			QUP 2 SE 7 lane 1	
		IBI_I3C_QUP2_SE7_SCL			QUP2 in-band interrupt I3C SE data 2	
BA20	GPIO_30		PX710	PD:nppukp	Configurable I/O	N
		QUP2_SE7_L2			QUP 2 SE 7 lane 2	
BB20	GPIO_31		PX710	PD:nppukp	Configurable I/O	Y
		QUP2_SE7_L3			QUP 2 SE 7 lane 3	
Y37	GPIO_32		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L0			QUP 1 SE 0 lane 0	
		IBI_I3C_QUP1_SE0_SDA			QUP1 in-band interrupt I3C SE clock 1	
		SSC_32			eGPIO - SSC I/O 32	
		SSC_32:SSC_QUPV3_SE13_0				
Y38	GPIO_33		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE0_L1			QUP 1 SE 0 lane 1	
		IBI_I3C_QUP1_SE0_SCL			QUP1 in-band interrupt I3C SE data 1	
		SSC_33			eGPIO - SSC I/O 33	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_33:SSC_QUPV3_SE13_1				
Y39	GPIO_34		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE0_L2			QUP 1 SE 0 lane 2	
		SSC_34			eGPIO - SSC I/O 34	
		SSC_34:SSC_QUPV3_SE13_2				
		SSC_34:SSC_GPIO_34_CLK				
Y36	GPIO_35		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L3			QUP 1 SE 0 lane 3	
		SSC_35			eGPIO - SSC I/O 35	
		SSC_35:SSC_QUPV3_SE13_3				
		SSC_35:SSC_GPIO_35_CLK				
AA35	GPIO_36		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L0			QUP 1 SE 1 lane 0	
		UIM1_DATA_MIRB				
		IBI_I3C_QUP1_SE1_SDA			QUP1 in-band interrupt I3C SE clock 1	
		SDC4_DATA_MIRA[0]			Secure digital controller data	
		SSC_36			eGPIO - SSC I/O 36	
		SSC_36:SSC_QUPV3_SE14_0				
AA36	GPIO_37		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE1_L1			QUP 1 SE 1 lane 1	
		UIM1_CLK_MIRB			UIM1 clock	
		IBI_I3C_QUP1_SE1_SCL			QUP1 in-band interrupt I3C SE data 1	
		SDC4_DATA_MIRA[1]			Secure digital controller data	
		SSC_37			eGPIO - SSC I/O 37	
		SSC_37:SSC_QUPV3_SE14_1				
AA37	GPIO_38		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE1_L2			QUP 1 SE 1 lane 2	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SDC4_DATA_MIRA[2]			Secure digital controller data	
AA38	GPIO_39		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L3			QUP 1 SE 1 lane 3	
		UIM1_RESET_MIRB			UIM1 reset	
		SDC4_DATA_MIRA[3]			Secure digital controller data	
AT37	GPIO_40		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L0			QUP 1 SE 2 lane 0	
AT39	GPIO_41		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L1			QUP 1 SE 2 lane 1	
AW38	GPIO_42		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L2			QUP 1 SE 2 lane 2	
AW39	GPIO_43		PX715	PD:nppukp	Configurable I/O	Y
		QUP1_SE2_L3			QUP 1 SE 2 lane 3	
BA37	GPIO_44		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE3_L0			QUP 1 SE 3 lane 0	
BA38	GPIO_45		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE3_L1			QUP 1 SE 3 lane 1	
BB37	GPIO_46		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L2			QUP 1 SE 3 lane 2	
BB38	GPIO_47		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L3			QUP 1 SE 3 lane 3	
		DP_HOT_PLUG_DETECT			DisplayPort hot plug detect	
AU37	GPIO_48		PX718	PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L0			QUP 1 SE 4 lane 0	
		IBI_I3C_QUP1_SE4_SDA			QUP1 in-band interrupt I3C SE clock 1	
		SDC4_CMD_MIRB			Secure digital controller 4 command	
AU38	GPIO_49		PX718	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QUP1_SE4_L1			QUP 1 SE 4 lane 1	
		IBI_I3C_QUP1_SE4_SCL			QUP1 in-band interrupt I3C SE data 1	
		SDC4_DATA_MIRB[0]			Secure digital controller data	
AU39	GPIO_50		PX718	PD:nppukp	Configurable I/O	N
		QUP1_SE4_L2			QUP 1 SE 4 lane 2	
		SDC4_CLK_MIRB			Secure digital controller clock	
AV37	GPIO_51		PX718	PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L3			QUP 1 SE 4 lane 3	
		SDC4_DATA_MIRB[1]			Secure digital controller data	
BE36	GPIO_52		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L0			QUP 1 SE 5 lane 0	
		QSPI_DATA[0]			Quad-SPI data	
BB39	GPIO_53		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L1			QUP 1 SE 5 lane 1	
		QSPI_DATA[1]			Quad-SPI data	
		GP_MN			General-purpose M/N:D counter output	
BC37	GPIO_54		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L2			QUP 1 SE 5 lane 2	
		QSPI_CLK			Quad SPI clock	
		UIM1_DATA_MIRC			UIM1 data	
BC38	GPIO_55		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L3			QUP 1 SE 5 lane 3	
		QSPI_DATA[2]			Quad-SPI data	
		UIM1_CLK_MIRC			UIM1 clock	
BA35	GPIO_56		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L0			QUP 1 SE 6 lane 0	
		QSPI_DATA[3]			Quad-SPI data	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		UIM1_RESET_MIRC			UIM1 reset	
BD37	GPIO_57		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L1			QUP 1 SE 6 lane 1	
		QSPI_CS_N_0			Quad-SPI chip select 0	
BC36	GPIO_58		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE6_L2			QUP 1 SE 6 lane 2	
		QSPI_CS_N_1			Quad-SPI chip select 1	
BD36	GPIO_59		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L3			QUP 1 SE 6 lane 3	
		USB_PHY_PS_MIRA			USB PHY port select	
AV38	GPIO_60		PX718	PD:nppukp	Configurable I/O	N
		QUP1_SE7_L0			QUP 1 SE 7 lane 0	
		SDC4_DATA_MIRB[2]			Secure digital controller data	
AV39	GPIO_61		PX718	PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L1			QUP 1 SE 7 lane 1	
		USB_PHY_PS_MIRB			USB PHY port select	
		SDC4_DATA_MIRB[3]			Secure digital controller data	
AW36	GPIO_62		PX718	PD:nppukp	Configurable I/O	N
		QUP1_SE7_L2			QUP 1 SE 7 lane 2	
AW37	GPIO_63		PX718	PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L3			QUP 1 SE 7 lane 3	
BB27	GPIO_64		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L0			I^2C hub 0 SE 0 lane 0	
BC27	GPIO_65		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L1			I^2C hub 0 SE 0 lane 1	
BD27	GPIO_66		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE1_L0			I^2C hub 0 SE 1 lane 0	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BA26	GPIO_67		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE1_L1			I^2C hub 0 SE 1 lane 1	
BD23	GPIO_68		PX710	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE2_L0			I^2C hub 0 SE 2 lane 0	
BA22	GPIO_69		PX710	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE2_L1			I^2C hub 0 SE 2 lane 1	
BC35	GPIO_70		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L0			I^2C hub 0 SE 3 lane 0	
		UIM1_DATA_MIRD			UIM1 data	
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
BD35	GPIO_71		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L1			I^2C hub 0 SE 3 lane 1	
		UIM1_CLK_MIRD			UIM1 clock	
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
BB34	GPIO_72		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L0			I^2C hub 0 SE 4 lane 0	
		UIM1_RESET_MIRD			UIM1 reset	
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	
BC34	GPIO_73		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L1			I^2C hub 0 SE 4 lane 1	
BC33	GPIO_74		PX14	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE5_L0			I^2C hub 0 SE 5 lane 0	
BD33	GPIO_75		PX14	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE5_L1			I^2C hub 0 SE 5 lane 1	
BB32	GPIO_76		PX14	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE6_L0			I^2C hub 0 SE 6 lane 0	
BC32	GPIO_77		PX14	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		I2CHUB0_SE6_L1			I^{2}C hub 0 SE 6 lane 1	
BD31	GPIO_78		PX712	PD:nppukp	Configurable I/O	Y
BD32	GPIO_79		PX712	PD:nppukp	Configurable I/O	Y
		USB1_HS_AC_EN			USB1 HS AC coupling 0 control	
BD34	GPIO_80		PX711	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE9_L0			I^{2}C hub 0 SE 9 lane 0	
BB33	GPIO_81		PX711	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE9_L1			I^{2}C hub 0 SE 9 lane 1	
BC22	GPIO_82		PX710	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE7_L0			I^{2}C hub 0 SE 7 lane 0	
		FORCED_USB_BOOT			Forced USB boot	
BD22	GPIO_83		PX710	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE7_L1			I^{2}C hub 0 SE 7 lane 1	
BB9	GPIO_84		PX714	PD:nppukp	Configurable I/O	Y
BA27	GPIO_85		PX704	PD:nppukp	Configurable I/O	Y
		SD_WRITE_PROTECT			Secure digital card write protection	
B27	GPIO_86		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA			MDP vertical sync – primary A	
		MDP_VSYNC0_OUT			MDP vertical sync 0 output	
		MDP_VSYNC1_OUT			MDP vertical sync 1 output	
		GCC_GP1_CLK_MIRB			General-purpose clock 1 B	
D28	GPIO_87		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA			MDP vertical sync – secondary A	
		MDP_VSYNC2_OUT			MDP vertical sync 2 output	
		MDP_VSYNC3_OUT			MDP vertical sync 3 output	
		MDP_VSYNC5_OUT			MDP vertical sync 5 output	
		GCC_GP2_CLK_MIRB			General-purpose clock 2 B	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
B28	GPIO_88		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_E			MDP vertical sync – external	
		MDP_ESYNC0_OUT				
		GCC_GP3_CLK_MIRB			General-purpose clock 3 B	
AB3	GPIO_89		PX722	PD:nppukp	Configurable I/O	N
		CAM_MCLK0			Camera 0 MCLK	
AB2	GPIO_90		PX722	PD:nppukp	Configurable I/O	N
		CAM_MCLK1			Camera 1 MCLK	
AB1	GPIO_91		PX721	PD:nppukp	Configurable I/O	N
		CAM_ASC_MCLK2			ASC camera 2 MCLK	
AC3	GPIO_92		PX722	PD:nppukp	Configurable I/O	N
		CAM_MCLK3			Camera 3 MCLK	
AC4	GPIO_93		PX721	PD:nppukp	Configurable I/O	N
		CAM_ASC_MCLK4			ASC camera 4 MCLK	
AC2	GPIO_94		PX722	PD:nppukp	Configurable I/O	N
		CAM_MCLK5			Camera 5 MCLK	
AC1	GPIO_95		PX721	PD:nppukp	Configurable I/O	Y
		CAM_MCLK7			Camera 7 MCLK	
AB4	GPIO_96		PX721	PD:nppukp	Configurable I/O	Y
		CAM_MCLK6			Camera 6 MCLK	
C29	GPIO_97		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRB			MDP vertical sync – secondary B	
C27	GPIO_98		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRB			MDP vertical sync – primary B	
BC31	GPIO_99		PX712	PD:nppukp	Configurable I/O	Y
C30	GPIO_100		PX708	PD:nppukp	Configurable I/O	N
		MDP_ESYNC1_OUT				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BB26	GPIO_101		PX14	PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[6]			Boot configuration bit 6	
BB22	GPIO_102		PX14	PD:nppukp	Configurable I/O	Y
BC21	GPIO_103	PCIE0_CLK_REQ_N	PX14	PU:nppdkp	Configurable I/O	Y
BC23	GPIO_104		PX14	PD:nppukp	Configurable I/O	Y
AD4	GPIO_105		PX716	PD:nppukp	Configurable I/O	N
		SSC_30			eGPIO - SSC I/O 30	
		SSC_30:SSC_QUPV3_SE12_0				
		SSC_30:SSC_GPIO_30_CLK				
AD3	GPIO_106		PX716	PD:nppukp	Configurable I/O	N
		SSC_31			eGPIO - SSC I/O 31	
		SSC_31:SSC_QUPV3_SE12_1				
		SSC_31:SSC_GPIO_31_CLK				
AD2	GPIO_107		PX716	PD:nppukp	Configurable I/O	N
		SSC_42			eGPIO - SSC I/O 42	
		SSC_42:LPI_GPIO0				
AD1	GPIO_108		PX716	PD:nppukp	Configurable I/O	Y
		SSC_43			eGPIO - SSC I/O 43	
		SSC_43:LPI_GPIO1				
B14	GPIO_109		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera control interface timer 0	
D15	GPIO_110		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera control interface timer 1	
C15	GPIO_111		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER4			Camera control interface timer 4	
		CCI_I2C_SDA3			Camera I^2C data 3	
C16	GPIO_112		PX706	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		CCI_I2C_SDA4			Camera I^2C data 4	
D12	GPIO_113		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Camera I2C data 0	
C12	GPIO_114		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Camera I^2C clock 0	
B12	GPIO_115		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Camera I^2C data 1	
D13	GPIO_116		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Camera I^2C clock 1	
C13	GPIO_117		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Camera I^2C data 2	
B13	GPIO_118		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Camera I^2C clock 2	
A13	GPIO_119		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA5			Camera I^2C data 5	
D14	GPIO_120		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL5			Camera I^2C clock 5	
BA7	GPIO_121		PX714	PD:nppukp	Configurable I/O	N
		I2S1_SCK			I^2S 1 clock	
BB7	GPIO_122		PX714	PD:nppukp	Configurable I/O	N
		I2S1_DATA0			I^2S 1 serial data channel 0	
BC7	GPIO_123		PX714	PD:nppukp	Configurable I/O	N
		I2S1_WS			I^2S 1 serial data word select	
BD7	GPIO_124		PX714	PD:nppukp	Configurable I/O	N
		I2S1_DATA1			I^2S 1 serial data channel 1	
		AUDIO_EXT_MCLK1			Audio external MCLK 1	
		AUDIO_REF_CLK			Audio reference clock	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BD8	GPIO_125		PX714	PD:nppukp	Configurable I/O	N
		AUDIO_EXT_MCLK0			Audio external MCLK 0	
BC9	GPIO_126		PX714	PD:nppukp	Configurable I/O	N
		I2S0_SCK			I^2S 0 clock	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
BA8	GPIO_127		PX714	PD:nppukp	Configurable I/O	N
		I2S0_DATA0			I^2S 0 serial data channel 0	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
BB8	GPIO_128		PX714	PD:nppukp	Configurable I/O	N
		I2S0_DATA1			I^2S 0 serial data channel 1	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
BC8	GPIO_129		PX714	PD:nppukp	Configurable I/O	N
		I2S0_WS			I^2S 0 serial data word select	
BB36	GPIO_130		PX14	PD:nppukp	Configurable I/O	N
		UIM0_DATA			UIM0 data	
BA39	GPIO_131		PX14	PD:nppukp	Configurable I/O	N
		UIM0_CLK			UIM0 clock	
BB35	GPIO_132		PX14	PD:nppukp	Configurable I/O	N
		UIM0_RESET			UIM0 reset	
BA36	GPIO_133		PX14	PD:nppukp	Configurable I/O	Y
		UIM0_PRESENT			UIM0 presence detection	
AY36	GPIO_134		PX717	PD:nppukp	Configurable I/O	N
		UIM1_DATA_MIRA				
		QUP1_SE2_L4			QUP 1 SE 2 lane 4	
		GCC_GP1_CLK_MIRA			General-purpose clock 1 A	
AY37	GPIO_135		PX717	PD:nppukp	Configurable I/O	N
		UIM1_CLK_MIRA				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QUP1_SE2_L5			QUP 1 SE 2 lane 5	
		GCC_GP2_CLK_MIRA			General-purpose clock 2 A	
AY38	GPIO_136		PX717	PD:nppukp	Configurable I/O	N
		UIM1_RESET_MIRA				
		QUP1_SE2_L6			QUP 1 SE 2 lane 6	
		GCC_GP3_CLK_MIRA			General-purpose clock 3 A	
AY39	GPIO_137		PX14	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT			UIM1 presence detection	
U39	GPIO_138		PX14	PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front end 0 interface clock	
		GRFC0			Generic RF controller bit 0	
V35	GPIO_139		PX14	PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front end 0 interface data	
		GRFC1			Generic RF controller bit 1	
V36	GPIO_140		PX14	PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front end 1 interface clock	
		GRFC2			Generic RF controller bit 2	
V37	GPIO_141		PX14	PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front end 1 interface data	
		GRFC3			Generic RF controller bit 3	
V38	GPIO_142		PX14	PD:nppukp	Configurable I/O	N
		RFFE2_CLK			RF front end 2 interface clock	
		GRFC4			Generic RF controller bit 4	
V39	GPIO_143		PX14	PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front end 2 interface data	
		GRFC5			Generic RF controller bit 5	
W36	GPIO_144		PX14	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		GRFC6			Generic RF controller bit 6	
		BOOT_CONFIG[1]			Boot configuration bit 1	
W37	GPIO_145		PX14	PD:nppukp	Configurable I/O	N
		GRFC7			Generic RF controller bit 7	
		BOOT_CONFIG[2]			Boot configuration bit 2	
W38	GPIO_146		PX14	PD:nppukp	Configurable I/O	N
		GRFC8			Generic RF controller bit 8	
		BOOT_CONFIG[3]			Boot configuration bit 3	
W39	GPIO_147		PX14	PD:nppukp	Configurable I/O	N
		GRFC9			Generic RF controller bit 9	
		BOOT_CONFIG[4]			Boot configuration bit 4	
AA39	GPIO_148		PX14	PD:nppukp	Configurable I/O	Y
		COEX_UART1_RX			Interface between WCN and MSM 1	
AB35	GPIO_149		PX14	PD:nppukp	Configurable I/O	N
		COEX_UART1_TX			Interface between WCN and MSM 1	
AB36	GPIO_150		PX14	PD:nppukp	Configurable I/O	Y
		GRFC10			Generic RF controller bit 10	
		COEX_UART2_RX			Interface between WCN and MSM 2	
		SDC4_CLK_MIRA			Secure digital controller clock	
AB37	GPIO_151		PX14	PD:nppukp	Configurable I/O	N
		GRFC11			Generic RF controller bit 11	
		COEX_UART2_TX			Interface between WCN and MSM 2	
		SDC4_CMD_MIRA				
Y35	GPIO_152		PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO2			GPS control signal 2	
		GRFC12			Generic RF controller bit 12	
		BOOT_CONFIG[7]			Boot configuration bit 7	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
B16	GPIO_153		PX706	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL4			Camera I2C clock 4	
R39	GPIO_154		PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO0			GPS control signal 0	
		NAV_GPIO3			GPS control signal 3	
T38	GPIO_155		PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO1			GPS control signal 1	
		BOOT_CONFIG[11]			Boot configuration bit 11	
T39	GPIO_156		PX14	PD:nppukp	Configurable I/O	Y
		QLINK_L_REQUEST			QLink port L request	
U35	GPIO_157		PX14	PD:nppukp	Configurable I/O	N
		QLINK_L_ENABLE			QLink port L enable	
U36	GPIO_158		PX14	PD:nppukp	Configurable I/O	N
		QLINK_WMSS_RESET_N			SDR modem subsystem reset output	
		BOOT_CONFIG[0]			Boot configuration bit 0	
U37	GPIO_159		PX14	PD:nppukp	Configurable I/O	Y
		QLINK_B_REQUEST			QLink port B request	
U38	GPIO_160		PX14	PD:nppukp	Configurable I/O	N
		QLINK_B_ENABLE			QLink port B enable	
C28	GPIO_161		PX708	PD:nppukp	Configurable I/O	N
B30	GPIO_162		PX708	PD:nppukp	Configurable I/O	Y
C14	GPIO_163		PX705	PD:nppukp	Configurable I/O	Y
		CCI_TIMER2			Camera control interface timer 2	
B15	GPIO_164		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER3			Camera control interface timer 3	
		CCI_I2C_SCL3			Camera I2C clock 3	
BB2	GPIO_165		PX14	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_0			eGPIO - LPASS I/O 0	
		LPASS_0:SWR_TX_CLK			SoundWire transmit clock	
		LPASS_0:LPI_I2S0_SCK			LPI I2S 0 clock	
BB3	GPIO_166		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_1			eGPIO - LPASS I/O 1	
		LPASS_1:SWR_TX_DATA0			SoundWire transmit data 0	
		LPASS_1:LPI_I2S0_WS			LPI I2S 0 serial data word select	
BC2	GPIO_167		PX14	PD:nppukp	Configurable I/O	N
		LPASS_2			eGPIO - LPASS I/O 2	
		LPASS_2:SWR_TX_DATA1			SoundWire transmit data 1	
		LPASS_2:LPI_I2S0_DATA0			LPI I2S 0 serial data channel 0	
BA2	GPIO_168		PX14	PD:nppukp	Configurable I/O	N
		LPASS_3			eGPIO - LPASS I/O 3	
		LPASS_3:SWR_RX_CLK			SoundWire receive clock	
		LPASS_3:LPI_I2S0_DATA1			LPI I2S 0 serial data channel 1	
BA1	GPIO_169		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_4			eGPIO - LPASS I/O 4	
		LPASS_4:SWR_RX_DATA0			SoundWire receive data 0	
		LPASS_4:LPI_I2S0_DATA2			LPI I2S 0 serial data channel 2	
BA3	GPIO_170		PX14	PD:nppukp	Configurable I/O	N
		LPASS_5			eGPIO - LPASS I/O 5	
		LPASS_5:SWR_RX_DATA1			SoundWire receive data 1	
		LPASS_5:EXT_MCLK1_C			External MCLK1 C	
		LPASS_5:LPI_I2S0_DATA3			LPI I2S 0 serial data channel 3	
BD5	GPIO_171		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_6			eGPIO - LPASS I/O 6	
		LPASS_6:LPI_DMIC0_CLK			DMIC 0 clock	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_6:LPI_I2S1_CLK			LPI I2S 1 clock	
BA5	GPIO_172		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_7			eGPIO - LPASS I/O 7	
		LPASS_7:LPI_DMIC0_DATA			DMIC 0 data	
		LPASS_7:LPI_I2S1_WS			LPI I2S 1 serial data word select	
BB4	GPIO_173		PX702	PD:nppukp	Configurable I/O	N
		LPASS_8			eGPIO - LPASS I/O 8	
		LPASS_8:LPI_DMIC1_CLK			DMIC 1 clock	
		LPASS_8:LPI_I2S1_DATA0			LPI I2S 0 serial data channel 0	
BB5	GPIO_174		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_9			eGPIO - LPASS I/O 9	
		LPASS_9:LPI_DMIC1_DATA			DMIC 1 data	
		LPASS_9:LPI_I2S1_DATA1			LPI I2S 1 serial data channel 1	
		LPASS_9:EXT_MCLK1_B			External MCLK1 B	
BA6	GPIO_175		PX701	PD:nppukp	Configurable I/O	N
		LPASS_10			eGPIO - LPASS I/O 10	
		LPASS_10:LPI_I2S2_CLK			LPI I2S 2 clock	
		LPASS_10:WSA_SWR_CLK			SoundWire clock for WSA	
BB6	GPIO_176		PX701	PD:nppukp	Configurable I/O	Y
		LPASS_11			eGPIO - LPASS I/O 11	
		LPASS_11:LPI_I2S2_WS			LPI I2S 2 serial data word select	
		LPASS_11:WSA_SWR_DATA			SoundWire data for WSA	
BC5	GPIO_177		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_12			eGPIO - LPASS I/O 12	
		LPASS_12:LPI_DMIC2_CLK			DMIC 2 clock	
		LPASS_12:LPI_I2S3_CLK			LPI I2S 3 clock	
BD4	GPIO_178		PX702	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_13			eGPIO - LPASS I/O 13	
		LPASS_13:LPI_DMIC2_DATA			DMIC 2 data	
		LPASS_13:LPI_I2S3_WS			LPI I2S 3 serial data word select	
		LPASS_13:EXT_MCLK1_A			External MCLK1 A	
BB1	GPIO_179		PX14	PD:nppukp	Configurable I/O	N
		LPASS_14			eGPIO - LPASS I/O 14	
		LPASS_14:SWR_TX_DATA2			SoundWire transmit data 2	
		LPASS_14:EXT_MCLK1_D			External MCLK1 D	
BC6	GPIO_180		PX701	PD:nppukp	Configurable I/O	N
		LPASS_15			eGPIO - LPASS I/O 15	
		LPASS_15:LPI_I2S2_DATA0			LPI I2S 2 serial data channel 0	
		LPASS_15:WSA2_SWR_CLK			SoundWire clock for WSA	
BD6	GPIO_181		PX701	PD:nppukp	Configurable I/O	Y
		LPASS_16			eGPIO - LPASS I/O 16	
		LPASS_16:LPI_I2S2_DATA1			LPI I2S 2 serial data channel 1	
		LPASS_16:WSA2_SWR_DATA			SoundWire data for WSA	
BD3	GPIO_182		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_17			eGPIO - LPASS I/O 17	
		LPASS_17:LPI_DMIC3_CLK			DMIC 3 clock	
		LPASS_17:LPI_I2S3_DATA0			LPI I2S 3 serial data channel 0	
BC4	GPIO_183		PX702	PD:nppukp	Configurable I/O	N
		LPASS_18			eGPIO - LPASS I/O 18	
		LPASS_18:LPI_DMIC3_DATA			DMIC 3 data	
		LPASS_18:LPI_I2S3_DATA1			LPI I2S 3 serial data channel 1	
AJ2	GPIO_184		PX14	PD:nppukp	Configurable I/O	N
		LPASS_19			eGPIO - LPASS I/O 19	
		LPASS_19:LPI_I2S4_CLK			LPI I2S 4 clock	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_19:SLIMBUS_CLK			SLIMbus clock	
		LPASS_19:QCA_SWR_CLK			SoundWire clock for WCN	
AJ1	GPIO_185		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_20			eGPIO - LPASS I/O 20	
		LPASS_20:LPI_I2S4_WS			LPI I2S 4 serial data word select	
		LPASS_20:SLIMBUS_DATA			SLIMbus data	
		LPASS_20:QCA_SWR_DATA			SoundWire data for WCN	
BC3	GPIO_186		PX14	PD:nppukp	Configurable I/O	N
		LPASS_21			eGPIO - LPASS I/O 21	
		LPASS_21:LPI_I2S4_DATA0			LPI I2S 4 serial data channel 0	
AY3	GPIO_187		PX14	PD:nppukp	Configurable I/O	N
		LPASS_22			eGPIO - LPASS I/O 22	
		LPASS_22:LPI_I2S4_DATA1			LPI I2S 4 serial data channel 1	
		LPASS_22:EXT_MCLK1_E			External MCLK1 E	
AY2	GPIO_188		PX703	PD:nppukp	Configurable I/O	Y
		SSC_0			eGPIO - SSC I/O 0	
		SSC_0:SSC_QUPV3_SE0_0				
AW2	GPIO_189		PX703	PD:nppukp	Configurable I/O	N
		SSC_1			eGPIO - SSC I/O 1	
		SSC_1:SSC_QUPV3_SE0_1				
AW1	GPIO_190		PX703	PD:nppukp	Configurable I/O	Y
		SSC_2			eGPIO - SSC I/O 2	
		SSC_2:SSC_QUPV3_SE1_0				
AY1	GPIO_191		PX703	PD:nppukp	Configurable I/O	Y
		SSC_3			eGPIO - SSC I/O 3	
		SSC_3:SSC_QUPV3_SE1_1				
AW3	GPIO_192		PX703	PD:nppukp	Configurable I/O	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_4			eGPIO - SSC I/O 4	
		SSC_4:SSC_QUPV3_SE2_0				
AV2	GPIO_193		PX703	PD:nppukp	Configurable I/O	Y
		SSC_5			eGPIO - SSC I/O 5	
		SSC_5:SSC_QUPV3_SE2_1				
AV1	GPIO_194		PX703	PD:nppukp	Configurable I/O	N
		SSC_6			eGPIO - SSC I/O 6	
		SSC_6:SSC_QUPV3_SE2_2				
		SSC_6:SSC_QUPV3_SE4_4				
		SSC_6:SSC_GPIO_6_CLK				
AU3	GPIO_195		PX703	PD:nppukp	Configurable I/O	N
		SSC_7			eGPIO - SSC I/O 7	
		SSC_7:SSC_QUPV3_SE2_3				
		SSC_7:SSC_QUPV3_SE4_5				
		SSC_7:SSC_GPIO_7_CLK				
AT1	GPIO_196		PX703	PD:nppukp	Configurable I/O	Y
		SSC_8			eGPIO - SSC I/O 8	
		SSC_8:SSC_QUPV3_SE3_0				
		SSC_8:SSC_QUPV3_SE2_4				
AV3	GPIO_197		PX703	PD:nppukp	Configurable I/O	Y
		SSC_9			eGPIO - SSC I/O 9	
		SSC_9:SSC_QUPV3_SE3_1				
		SSC_9:SSC_QUPV3_SE2_5				
AU2	GPIO_198		PX703	PD:nppukp	Configurable I/O	Y
		SSC_10			eGPIO - SSC I/O 10	
		SSC_10:SSC_QUPV3_SE4_0				
		SSC_10:SSC_GPIO_10_CLK				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AU1	GPIO_199		PX703	PD:nppukp	Configurable I/O	Y
		SSC_11			eGPIO - SSC I/O 11	
		SSC_11:SSC_QUPV3_SE4_1				
		SSC_11:SSC_GPIO_11_CLK				
AT3	GPIO_200		PX703	PD:nppukp	Configurable I/O	Y
		SSC_12			eGPIO - SSC I/O 12	
		SSC_12:SSC_QUPV3_SE4_2				
		SSC_12:SSC_GPIO_12_CLK				
AT2	GPIO_201		PX703	PD:nppukp	Configurable I/O	Y
		SSC_13			eGPIO - SSC I/O 13	
		SSC_13:SSC_QUPV3_SE4_3				
		SSC_13:SSC_GPIO_13_CLK				
AK1	GPIO_202		PX14	PD:nppukp	Configurable I/O	Y
		SSC_14				
		SSC_14:SSC_QUPV3_SE5_2			eGPIO - SSC I/O 14	
		SSC_14:SSC_QUPV3_SE5_0				
		SSC_14:SSC_QUPV3_SE1_2				
AM1	GPIO_203		PX14	PD:nppukp	Configurable I/O	Y
		SSC_15			eGPIO - SSC I/O 15	
		SSC_15:SSC_QUPV3_SE5_3				
		SSC_15:SSC_QUPV3_SE5_1				
		SSC_15:SSC_QUPV3_SE1_3				
AN1	GPIO_204		PX14	PD:nppukp	Configurable I/O	Y
		SSC_16			eGPIO - SSC I/O 16	
		SSC_16:SSC_QUPV3_SE6_0				
		SSC_16:SSC_QUPV3_SE6_2				
		SSC_16:SSC_QUPV3_SE10_2				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AL1	GPIO_205		PX14	PD:nppukp	Configurable I/O	Y
		SSC_17			eGPIO - SSC I/O 17	
		SSC_17:SSC_QUPV3_SE6_1				
		SSC_17:SSC_QUPV3_SE6_3				
		SSC_17:SSC_QUPV3_SE10_3				
AP1	GPIO_206		PX713	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE8_L0			I2C hub 0 SE 8 lane 0	
		SSC_24			eGPIO - SSC I/O 24	
		SSC_24:SSC_QUPV3_SE10_0				
		SSC_24:SSC_GPIO_24_CLK				
AN2	GPIO_207		PX713	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE8_L1			I2C hub 0 SE 8 lane 1	
		SSC_25			eGPIO - SSC I/O 25	
		SSC_25:SSC_QUPV3_SE10_1				
		SSC_25:SSC_GPIO_25_CLK				
AR2	GPIO_208		PX703	PD:nppukp	Configurable I/O	N
		SSC_18			eGPIO - SSC I/O 18	
		SSC_18:SSC_QUPV3_SE7_2				
		SSC_18:SSC_QUPV3_SE7_0				
		SSC_18:SSC_GPIO_18_CLK				
AR1	GPIO_209		PX703	PD:nppukp	Configurable I/O	Y
		SSC_19			eGPIO - SSC I/O 19	
		SSC_19:SSC_QUPV3_SE7_3				
		SSC_19:SSC_QUPV3_SE7_1				
		SSC_19:SSC_GPIO_19_CLK				
AH1	GPIO_210		PX716	PD:nppukp	Configurable I/O	N
		SSC_26			eGPIO - SSC I/O 26	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_26:SSC_QUPV3_SE11_0				
		SSC_26:SSC_GPIO_26_CLK				
AG2	GPIO_211		PX716	PD:nppukp	Configurable I/O	N
		SSC_27			eGPIO - SSC I/O 27	
		SSC_27:SSC_QUPV3_SE11_1				
		SSC_27:SSC_GPIO_27_CLK				
AG1	GPIO_212		PX716	PD:nppukp	Configurable I/O	N
		SSC_28			eGPIO - SSC I/O 28	
		SSC_28:SSC_QUPV3_SE11_2				
		SSC_28:SSC_GPIO_28_CLK				
AE2	GPIO_213		PX716	PD:nppukp	Configurable I/O	N
		SSC_29			eGPIO - SSC I/O 29	
		SSC_29:SSC_QUPV3_SE11_3				
		SSC_29:SSC_GPIO_29_CLK				
AF1	GPIO_214		PX716	PD:nppukp	Configurable I/O	N
		SSC_44			eGPIO - SSC I/O 44	
		SSC_44:LPI_GPIO2				

Table 2-4 MSM bottom pin descriptions: Power-supply pins

Pin number	Pin name	Functional description
A17, A24, BE16, BE25	LPDDR5X_VDD1	LPDDR5X core1 power
A5, A6, A7, A31, A32, A33, BE5, BE6, BE7, BE32, BE33, BE34	LPDDR5X_VDD2H	LPDDR5X core2/input buffer power
A20, A21, A22, BE18, BE19, BE20	LPDDR5X_VDD2L	LPDDR5X core2/input buffer power
A14, A15, A26, A27, BE11, BE12, BE27, BE28	LPDDR5X_VDDQ	LPDDR5X I/O buffer power
AR11	VDDSENSE_APC0_CX	VDD sense for APC0_CX
AJ11	VDDSENSE_APC1_CX	VDD sense for APC1_CX
AM26	VDDSENSE_GFX	VDD sense for GFX
L9	VDDSENSE_MM	VDD sense for MM
N31	VDDSENSE_MODEM	VDD sense for MODEM
P24	VDDSENSE_NSP1	VDD sense for NSP1
M18	VDDSENSE_NSP2	VDD sense for NSP2
AL8, AL10, AL12, AL14, AL16, AL18, AM5, AM7, AM9, AM11, AM13, AM15, AM17, AN18, AP5, AP11, AP13, AR12, AR18, AT11, AT13, AV5, AV11, AV13, AW6, AW8, AW14, AW16, AW18, AY5, AY7, AY15, AY17	VDD_APC0_CX	Power for Oryon application processor
AM8, AM16, AN10, AN12, AR10, AT5, AU10, AU12, AU18, AW7, AW15	VDD_APC0_MX	Power for Oryon application processor memory
AB7, AB9, AB11, AB13, AB15, AB17, AC8, AC12, AC14, AC16, AC18, AD7, AD19, AE14, AE16, AE18, AF7, AF19, AG14, AG16, AH7, AH19, AJ8, AJ12, AJ14, AJ16, AJ18, AK7, AK9, AK11, AK13, AK15, AK17	VDD_APC1_CX	Power for Oryon application processor
AC10, AD15, AD17, AF15, AF17, AG18, AH15, AH17, AJ10	VDD_APC1_MX	Power for Oryon application processor memory
J6	VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits
H6	VDD_A_CSI_01_1P2	Power for MIPI CSI01 1.2 V analog circuits
P6	VDD_A_CSI_24_0P9	Power for MIPI CSI24 0.9 V analog circuits
R6	VDD_A_CSI_24_1P2	Power for MIPI CSI24 1.2 V analog circuits
L6	VDD_A_CSI_35_0P9	Power for MIPI CSI35 0.9 V analog circuits
M6	VDD_A_CSI_35_1P2	Power for MIPI CSI35 1.2 V analog circuits
G17	VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits
F18	VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits
G19	VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V
G9, G10, G12, G13	VDD_A_EBI_0	Power for EBI0 PHY
E11	VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits
AW9, AW10, AW12, AW13	VDD_A_EBI_1	Power for EBI1 PHY
BA11	VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits
G27, G28, G30, G31	VDD_A_EBI_2	Power for EBI2 PHY
E29	VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
AW28, AW29, AW30, AW32, AW33	VDD_A_EBI_3	Power for EBI3 PHY
BA31	VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits
AG34	VDD_A_EUSB_CORE	Power for eUSB2.0 core circuits
AF34	VDD_A_EUSB_1P2	Power for eUSB2.0 1.2 V circuits
U34	VDD_A_GNSS_ADC_1P2	Power for GNSS ADC circuits
AH5	VDD_A_PCIE_0_CORE	Power for PCIE0 core circuits
AG5	VDD_A_PCIE_0_1P2	Power for PCIE0 1.2 V circuit
L34, M34	VDD_A_QLINK_0_B_0P9	Power for QLink0 port B (0.9 V)
K34	VDD_A_QLINK_0_B_1P2	Power for QLink0 port B (1.2 V)
N34	VDD_A_QLINK_0_B_CK_0P9	Power for QLink0 port B clock circuits
R34, T34	VDD_A_QLINK_0_L_0P9	Power for QLink0 port L (0.9 V)
P34	VDD_A_QLINK_0_L_CK_0P9	Power for QLink0 port L clock circuits
F7	VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875 V circuits
F16	VDD_A_QREFS_0P875_2	Reference voltage for QREFS 0.875 V circuits
F25	VDD_A_QREFS_0P875_3	Reference voltage for QREFS 0.875 V circuits
W34	VDD_A_QREFS_0P875_5	Reference voltage for QREFS 0.875 V circuits
AC35	VDD_A_QREFS_0P875_6	Reference voltage for QREFS 0.875 V circuits
AC34	VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V circuits
V6	VDD_A_QREFS_TX_0P875	Reference voltage for QREFS 0.875 V circuits
W6	VDD_A_QREFS_TX_1P2	Reference voltage for QREFS 1.2 V circuits
W29	VDD_A_SP_SENSOR	Power for SP sensor analog circuits
AH34, AJ34, AJ35	VDD_A_UFS_CORE	Power for UFS core circuits
AG33	VDD_A_UFS_1P2	Power for UFS 1.2 V circuits
AE34	VDD_A_USB_SS_DP_CORE	Power for the USB SuperSpeed and DisplayPort core analog circuits
AD34	VDD_A_USB_SS_DP_1P2	Power for the USB SuperSpeed and DisplayPort 1.2 V analog circuits
AA20, AA22, AA24, AA26, AB23, AB34, AC24, AD23, AE20, AE22, AG20, AG22, AK19, AK21, AM19, AM21, AP19, AP21, AT19, AT21, AV21, AW34, P15, T7, T15, U8, W22, W26, Y23, Y25, Y27	VDD_CX	Power for digital core circuits
G11	VDD_D_EBI_0	Power for EBI0 digital circuits
AW11	VDD_D_EBI_1	Power for EBI1 digital circuits
G29	VDD_D_EBI_2	Power for EBI2 digital circuits
AW31	VDD_D_EBI_3	Power for EBI3 digital circuits

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
AB27, AB33, AC28, AC30, AC32, AD25, AD27, AD29, AD31, AD33, AE24, AF27, AG26, AH29, AH31, AH33, AJ26, AJ28, AJ30, AJ32, AK27, AK33, AL22, AL24, AL34, AM23, AM25, AM27, AN22, AN26, AN28, AN30, AN32, AN34, AP27, AP29, AP31, AP33, AR22, AR26, AR34, AT33, AU22, AU26, AU34, AV23, AV25, AV27, AV29, AV33, AW24, AW26	VDD_GFX	Power for graphics
AA33, AC26, AE26, AE33, AH27, AK22, AL26, AM33, AP22, AT27, AV31, AW22	VDD_GFX_MXC	Power for graphics memory
F9, F10, F12, F13	VDD_IO_EBI_0	Power for the EBI_0 I/O circuits
AY9, AY10, AY12, AY13	VDD_IO_EBI_1	Power for the EBI1 I/O circuits
F27, F28, F30, F31	VDD_IO_EBI_2	Power for the EBI2 I/O circuits
AY28, AY29, AY30, AY32, AY33	VDD_IO_EBI_3	Power for the EBI_3 I/O circuits
AD5, W5, AU4, AY21, AY26, AT36, AN35, E26, F14	VDD_IX	Power for dual voltage pads
AA6, AA8, AC6, AE6, AG6, AJ6, AL6, W8, Y7, AB19, AC22, AH21, AU20	VDD_LPI_CX	Power for LPI digital core circuits
AB5, AE5, AK5, V7, V9, Y9, AC20, AB25, AJ22, AV19	VDD_LPI_MX	Power for LPI memory circuits
Y33	VDD_LPI_MX_NAV	Power for LPI on chip memory-NAV
G8, H7, H9, H13, J8, J10, J12, J14, K7, K9, K13, L8, L10, L12, L14, M7, M9, N8, N10, N12, N14, P7, P9, R8, R10, R12, R14, T9, U10, U12, U14, W10, W12, W14, W16, W18, Y11, Y13, Y15	VDD_MM	Power for multimedia subsystem circuits
G32, G34, H29, H31, H33, J34, K27, K33, M29, M31, M33, N28, N30, P27, P33, T33, U28, U30, U32, V29, V31, V33	VDD_MODEM	Power for modem circuits
AB21, AD21, AF21, AJ20, AL20, AN20, AR20, AW20, F34, M13, P13, R26, T13, T25, V13, V15, V17, V19, V21, V25, W20, Y21	VDD_MX_A	Power for memory circuits
AA10, AA12, AA14, AA16, AA18, F23, F33, H11, J27, K11, M11, M28, N32, P11, T11, T27, U22, V11, V23, V27, W24, Y17, Y19	VDD_MX_C	Power for memory circuits
G22, G24, G26, H23, H25, H27, J22, J26, L22, L26, M27, N22, N26, P23, P25, R22, R24, T23, U24	VDD_NSP1	Power for NSP1
F20, F21, G16, G18, G20, H15, H21, K15, K21, L16, L18, L20, M15, M17, M19, M21, N16, P17, P21, R16, T17, T21, U16	VDD_NSP2	Power for NSP2
V34	VDD_PX0	Power for pad group 0
R5	VDD_PX11	Power for pad group 11
W30	VDD_PX13	Power for pad group 13
AC5, U6, Y5, AV4, AY22, AY24, AL35, AU36, AA34, D27, E15, G6	VDD_PX14	Power for pad group 14
AW4	VDD_PX701	Power for pad group 701

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
AT4	VDD_PX702	Power for pad group 702
AF5	VDD_PX703	Power for pad group 703
AY27	VDD_PX704	Power for pad group 704
G14	VDD_PX705	Power for pad group 705
F15	VDD_PX706	Power for pad group 706
F26	VDD_PX708	Power for pad group 708
AU35	VDD_PX709	Power for pad group 709
AY25	VDD_PX710	Power for pad group 710
AV35	VDD_PX711	Power for pad group 711
AY35	VDD_PX712	Power for pad group 712
AA4	VDD_PX713	Power for pad group 713
AY4	VDD_PX714	Power for pad group 714
AR35	VDD_PX715	Power for pad group 715
Y4	VDD_PX716	Power for pad group 716
AT35	VDD_PX717	Power for pad group 717
AP35	VDD_PX718	Power for pad group 718
AY23	VDD_PX719	Power for pad group 719
AY19	VDD_PX720	Power for pad group 720
V5	VDD_PX721	Power for pad group 721
W4	VDD_PX722	Power for pad group 722
AY34, U26	VDD_QFPROM	Power for programming the QFPROM
W28	VDD_QFPROM_SP	Power for programming the QFPROM for secure processor unit
AT12	VSSSENSE_APC0_CX	GND sense for APC0_CX
AK10	VSSSENSE_APC1_CX	GND sense for APC1_CX
AN27	VSSSENSE_GFX	GND sense for GFX
M10	VSSSENSE_MM	GND sense for MM
M32	VSSSENSE_MODEM	GND sense for MODEM
R25	VSSSENSE_NSP1	GND sense for NSP1
L17	VSSSENSE_NSP2	GND sense for NSP2

Table 2-5 MSM bottom pin descriptions: Ground pins

Pin number	Pin name	Functional description
A4, A9, A16, A19, A23, A25, A28, A30, A34, A36, AA2, AA3, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA21, AA23, AA25, AA27, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB24, AB26, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC29, AC31, AC33, AC38, AC39, AD6, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD28, AD30, AD32, AD35, AD36, AD37, AE1, AE3, AE4, AE7, AE15, AE17, AE19, AE21, AE23, AE25, AE27, AE37, AE38, AE39, AF2, AF6, AF16, AF18, AF20, AF22, AF26, AF33, AF35, AF36, AF37, AG3, AG4, AG7, AG15, AG17, AG19, AG21, AG27, AG37, AG38, AG39, AH2, AH6, AH14, AH16, AH18, AH20, AH22, AH26, AH28, AH30, AH32, AH35, AH36, AH37, AJ3, AJ4, AJ5, AJ7, AJ9, AJ13, AJ15, AJ17, AJ19, AJ21, AJ27, AJ29, AJ31, AJ33, AJ36, AJ38, AJ39, AK2, AK4, AK6, AK8, AK12, AK14, AK16, AK18, AK20, AK26, AK34, AK35, AK37, AK38, AL2, AL5, AL7, AL9, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL33, AL36, AL37, AL39, AM2, AM4, AM6, AM10, AM12, AM14, AM18, AM20, AM22, AM24, AM34, AM35, AM37, AM38, AM39, AN3, AN4, AN5, AN11, AN13, AN19, AN21, AN29, AN31, AN33, AN36, AN38, AN39, AP2, AP10, AP12, AP18, AP20, AP26, AP28, AP30, AP32, AP34, AP37, AP38, AR3, AR4, AR5, AR13, AR19, AR21, AR27, AR33, AR36, AR37, AR39, AT10, AT18, AT20, AT22, AT26, AT34, AT38, AU5, AU11, AU13, AU19, AU21, AU27, AU33, AV10, AV12, AV18, AV20, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, AW5, AW17, AW19, AW21, AW23, AW25, AW27, AW35, AY6, AY8, AY11, AY14, AY16, AY18, AY20, AY31, B7, B9, B11, B17, B19, B21, B23, B25, B26, B31, B34, B36, BA4, BA9, BA10, BA12, BA13, BA17, BA21, BA25, BA28, BA29, BA30, BA32, BA33, BA34, BB10, BB11, BB12, BB13, BB28, BB29, BB30, BB31, BC10, BC11, BC12, BC13, BC28, BC29, BC30, BD10, BD11, BD12, BD13, BD28, BD29, BE4, BE8, BE10, BE13, BE15, BE17, BE22, BE24, BE26, BE29, BE31, BE35, C2, C3, C4, C7, C11, C17, C19, C21, C23, C26, C31, C32, C33, C34, C35, C36, C38, D1, D2, D7, D11, D16, D21, D26, D29, D30, D31, D33, D35, D37, E5, E6, E7, E8, E9, E10, E12, E13, E14, E16, E21, E25, E27, E28, E30, E31, E33, E35, E37, E38, E39, F1, F2, F5, F6, F8, F11, F17, F19, F22, F24, F29, F32, F35, F36, F37, G5, G7, G15, G21, G23, G25, G33, G35, G38, G39, H5, H8, H10, H12, H14, H22, H24, H26, H28, H30, H32, H34, H36, H37, J1, J2, J5, J7, J9, J11, J13, J15, J21, J33, J35, J38, J39, K5, K6, K8, K10, K12, K14, K22, K26, K36, K37, L1, L2, L3, L4, L5, L7, L11, L13, L15, L19, L21, L27, L33, L35, L38, L39, M5, M8, M12, M14, M16, M20, M22, M26, M30, M35, M36, M37, N1, N2, N5, N6, N7, N9, N11, N13, N15, N17, N21, N27, N29, N33, N37, P5, P8, P10, P12, P14, P16, P22, P26, P35, P36, P37, R7, R9, R11, R13, R15, R17, R21, R23, R27, R33, R37, T1, T2, T5, T8, T10, T12, T14, T16, T22, T24, T26, T35, T36, T37, U5, U7, U9, U11, U13, U17, U21, U23, U25, U27, U29, U31, U33, V3, V4, V8, V10, V12, V14, V16, V18, V20, V22, V24, V26, V28, V30, V32, W7, W9, W11, W13, W15, W17, W19, W21, W23, W25, W27, W31, W35, Y6, Y12, Y14, Y16, Y18, Y20, Y22, Y24, Y26	GND	Ground

Table 2-6 MSM bottom pin descriptions: Not connected pins

Pin number	Pin name	Functional description
A1, A2, A3, A37, A38, A39, B1, B2, B38, B39, BC1 BD1, BD2 BD39, BE1, BE2, BE3, BE37, BE38, BE39, C1, C39	NC	No connect; not connected internally.
A11, AA19, AB22, AB38, AC27, AF14, AL11, B29, BA15, BB15, BC14, BC39, BD9, BD14, BD30, BD38, U15, V2 , Y8, Y10	DNC	Do not connect; connected internally, do not connect externally.

2.3 Pin assignments: MSM top

2.3.1 Pin map: MSM top

The SM8750/SM8750P is available in the MPSP1512. See Mechanical information for package details and Pin assignments: MSM bottom for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in below.

The text within the below image is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in Pin map: MSM bottom.

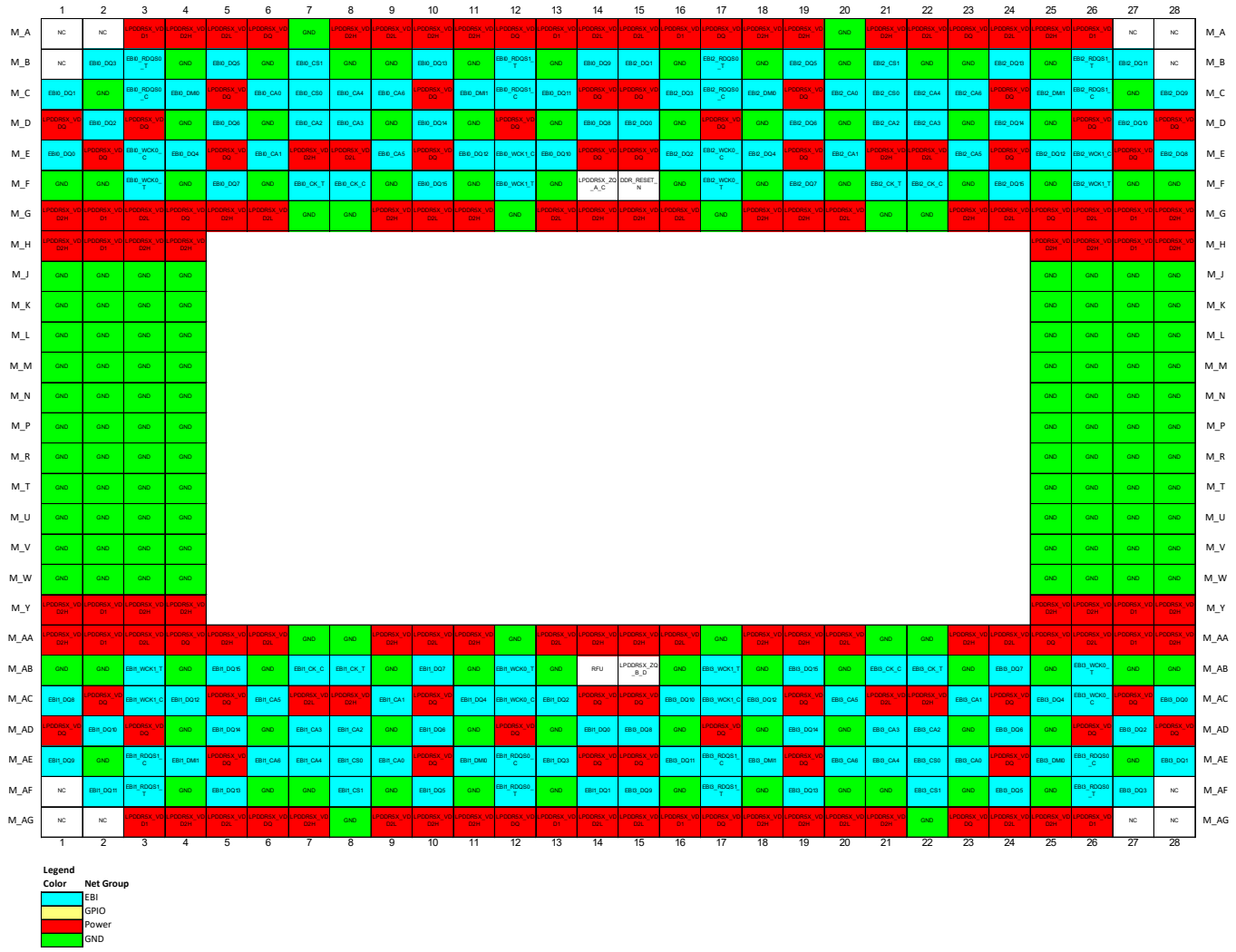

Figure 2-3 SM8750 top pin LPDDR5X assignments (top view)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in Table 2-7 through Table 2-11

Table 2-7 MSM top pin descriptions – general pins

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_C6	EBI0_CA0	EBI	DO	EBI0 LPDDR5X command/address bit 0
M_AE9	EBI1_CA0	EBI	DO	EBI1 LPDDR5X command/address bit 0
M_C20	EBI2_CA0	EBI	DO	EBI2 LPDDR5X command/address bit 0
M_AE23	EBI3_CA0	EBI	DO	EBI3 LPDDR5X command/address bit 0
M_E6	EBI0_CA1	EBI	DO	EBI0 LPDDR5X command/address bit 1
M_AC9	EBI1_CA1	EBI	DO	EBI1 LPDDR5X command/address bit 1
M_E20	EBI2_CA1	EBI	DO	EBI2 LPDDR5X command/address bit 1
M_AC23	EBI3_CA1	EBI	DO	EBI3 LPDDR5X command/address bit 1
M_D7	EBI0_CA2	EBI	DO	EBI0 LPDDR5X command/address bit 2
M_AD8	EBI1_CA2	EBI	DO	EBI1 LPDDR5X command/address bit 2
M_D21	EBI2_CA2	EBI	DO	EBI2 LPDDR5X command/address bit 2
M_AD22	EBI3_CA2	EBI	DO	EBI3 LPDDR5X command/address bit 2
M_D8	EBI0_CA3	EBI	DO	EBI0 LPDDR5X command/address bit 3
M_AD7	EBI1_CA3	EBI	DO	EBI1 LPDDR5X command/address bit 3
M_D22	EBI2_CA3	EBI	DO	EBI2 LPDDR5X command/address bit 3
M_AD21	EBI3_CA3	EBI	DO	EBI3 LPDDR5X command/address bit 3
M_C8	EBI0_CA4	EBI	DO	EBI0 LPDDR5X command/address bit 4
M_AE7	EBI1_CA4	EBI	DO	EBI1 LPDDR5X command/address bit 4
M_C22	EBI2_CA4	EBI	DO	EBI2 LPDDR5X command/address bit 4
M_AE21	EBI3_CA4	EBI	DO	EBI3 LPDDR5X command/address bit 4
M_E9	EBI0_CA5	EBI	DO	EBI0 LPDDR5X command/address bit 5
M_AC6	EBI1_CA5	EBI	DO	EBI1 LPDDR5X command/address bit 5
M_E23	EBI2_CA5	EBI	DO	EBI2 LPDDR5X command/address bit 5

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_AC20	EBI3_CA5	EBI	DO	EBI3 LPDDR5X command/address bit 5
M_C9	EBI0_CA6	EBI	DO	EBI0 LPDDR5X command/address bit 6
M_AE6	EBI1_CA6	EBI	DO	EBI1 LPDDR5X command/address bit 6
M_C23	EBI2_CA6	EBI	DO	EBI2 LPDDR5X command/address bit 6
M_AE20	EBI3_CA6	EBI	DO	EBI3 LPDDR5X command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5X differential clock (C)
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5X differential clock (C)
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5X differential clock (C)
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5X differential clock (C)
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5X differential clock (T)
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5X differential clock (T)
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5X differential clock (T)
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5X differential clock (T)
M_C7	EBI0_CS0	EBI	DO	EBI0 LPDDR5X chip select 0
M_AE8	EBI1_CS0	EBI	DO	EBI1 LPDDR5X chip select 0
M_C21	EBI2_CS0	EBI	DO	EBI2 LPDDR5X chip select 0
M_AE22	EBI3_CS0	EBI	DO	EBI3 LPDDR5X chip select 0
M_B7	EBI0_CS1	EBI	DO	EBI0 LPDDR5X chip select 1
M_AF8	EBI1_CS1	EBI	DO	EBI1 LPDDR5X chip select 1
M_B21	EBI2_CS1	EBI	DO	EBI2 LPDDR5X chip select 1
M_AF22	EBI3_CS1	EBI	DO	EBI3 LPDDR5X chip select 1
M_C4	EBI0_DMI0	EBI	DO	EBI0 LPDDR5X data mask for byte 0
M_AE11	EBI1_DMI0	EBI	DO	EBI1 LPDDR5X data mask for byte 0
M_C18	EBI2_DMI0	EBI	DO	EBI2 LPDDR5X data mask for byte 0
M_AE25	EBI3_DMI0	EBI	DO	EBI3 LPDDR5X data mask for byte 0
M_C11	EBI0_DMI1	EBI	DO	EBI0 LPDDR5X data mask for byte 1
M_AE4	EBI1_DMI1	EBI	DO	EBI1 LPDDR5X data mask for byte 1

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_C25	EBI2_DMI1	EBI	DO	EBI2 LPDDR5X data mask for byte 1
M_AE18	EBI3_DMI1	EBI	DO	EBI3 LPDDR5X data mask for byte 1
M_E1	EBI0_DQ0	EBI	B	EBI0 LPDDR5X data bit 0
M_AD14	EBI1_DQ0	EBI	B	EBI1 LPDDR5X data bit 0
M_D15	EBI2_DQ0	EBI	B	EBI2 LPDDR5X data bit 0
M_AC28	EBI3_DQ0	EBI	B	EBI3 LPDDR5X data bit 0
M_E13	EBI0_DQ10	EBI	B	EBI0 LPDDR5X data bit 10
M_AD2	EBI1_DQ10	EBI	B	EBI1 LPDDR5X data bit 10
M_D27	EBI2_DQ10	EBI	B	EBI2 LPDDR5X data bit 10
M_AC16	EBI3_DQ10	EBI	B	EBI3 LPDDR5X data bit 10
M_C13	EBI0_DQ11	EBI	B	EBI0 LPDDR5X data bit 11
M_AF2	EBI1_DQ11	EBI	B	EBI1 LPDDR5X data bit 11
M_B27	EBI2_DQ11	EBI	B	EBI2 LPDDR5X data bit 11
M_AE16	EBI3_DQ11	EBI	B	EBI3 LPDDR5X data bit 11
M_E11	EBI0_DQ12	EBI	B	EBI0 LPDDR5X data bit 12
M_AC4	EBI1_DQ12	EBI	B	EBI1 LPDDR5X data bit 12
M_E25	EBI2_DQ12	EBI	B	EBI2 LPDDR5X data bit 12
M_AC18	EBI3_DQ12	EBI	B	EBI3 LPDDR5X data bit 12
M_B10	EBI0_DQ13	EBI	B	EBI0 LPDDR5X data bit 13
M_AF5	EBI1_DQ13	EBI	B	EBI1 LPDDR5X data bit 13
M_B24	EBI2_DQ13	EBI	B	EBI2 LPDDR5X data bit 13
M_AF19	EBI3_DQ13	EBI	B	EBI3 LPDDR5X data bit 13
M_D10	EBI0_DQ14	EBI	B	EBI0 LPDDR5X data bit 14
M_AD5	EBI1_DQ14	EBI	B	EBI1 LPDDR5X data bit 14
M_D24	EBI2_DQ14	EBI	B	EBI2 LPDDR5X data bit 14
M_AD19	EBI3_DQ14	EBI	B	EBI3 LPDDR5X data bit 14
M_F10	EBI0_DQ15	EBI	B	EBI0 LPDDR5X data bit 15

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_AB5	EBI1_DQ15	EBI	B	EBI1 LPDDR5X data bit 15
M_F24	EBI2_DQ15	EBI	B	EBI2 LPDDR5X data bit 15
M_AB19	EBI3_DQ15	EBI	B	EBI3 LPDDR5X data bit 15
M_C1	EBI0_DQ1	EBI	B	EBI0 LPDDR5X data bit 1
M_AF14	EBI1_DQ1	EBI	B	EBI1 LPDDR5X data bit 1
M_B15	EBI2_DQ1	EBI	B	EBI2 LPDDR5X data bit 1
M_AE28	EBI3_DQ1	EBI	B	EBI3 LPDDR5X data bit 1
M_D2	EBI0_DQ2	EBI	B	EBI0 LPDDR5X data bit 2
M_AC13	EBI1_DQ2	EBI	B	EBI1 LPDDR5X data bit 2
M_E16	EBI2_DQ2	EBI	B	EBI2 LPDDR5X data bit 2
M_AD27	EBI3_DQ2	EBI	B	EBI3 LPDDR5X data bit 2
M_B2	EBI0_DQ3	EBI	B	EBI0 LPDDR5X data bit 3
M_AE13	EBI1_DQ3	EBI	B	EBI1 LPDDR5X data bit 3
M_C16	EBI2_DQ3	EBI	B	EBI2 LPDDR5X data bit 3
M_AF27	EBI3_DQ3	EBI	B	EBI3 LPDDR5X data bit 3
M_E4	EBI0_DQ4	EBI	B	EBI0 LPDDR5X data bit 4
M_AC11	EBI1_DQ4	EBI	B	EBI1 LPDDR5X data bit 4
M_E18	EBI2_DQ4	EBI	B	EBI2 LPDDR5X data bit 4
M_AC25	EBI3_DQ4	EBI	B	EBI3 LPDDR5X data bit 4
M_B5	EBI0_DQ5	EBI	B	EBI0 LPDDR5X data bit 5
M_AF10	EBI1_DQ5	EBI	B	EBI1 LPDDR5X data bit 5
M_B19	EBI2_DQ5	EBI	B	EBI2 LPDDR5X data bit 5
M_AF24	EBI3_DQ5	EBI	B	EBI3 LPDDR5X data bit 5
M_D5	EBI0_DQ6	EBI	B	EBI0 LPDDR5X data bit 6
M_AD10	EBI1_DQ6	EBI	B	EBI1 LPDDR5X data bit 6
M_D19	EBI2_DQ6	EBI	B	EBI2 LPDDR5X data bit 6
M_AD24	EBI3_DQ6	EBI	B	EBI3 LPDDR5X data bit 6

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_F5	EBI0_DQ7	EBI	B	EBI0 LPDDR5X data bit 7
M_AB10	EBI1_DQ7	EBI	B	EBI1 LPDDR5X data bit 7
M_F19	EBI2_DQ7	EBI	B	EBI2 LPDDR5X data bit 7
M_AB24	EBI3_DQ7	EBI	B	EBI3 LPDDR5X data bit 7
M_D14	EBI0_DQ8	EBI	B	EBI0 LPDDR5X data bit 8
M_AC1	EBI1_DQ8	EBI	B	EBI1 LPDDR5X data bit 8
M_E28	EBI2_DQ8	EBI	B	EBI2 LPDDR5X data bit 8
M_AD15	EBI3_DQ8	EBI	B	EBI3 LPDDR5X data bit 8
M_B14	EBI0_DQ9	EBI	B	EBI0 LPDDR5X data bit 9
M_AE1	EBI1_DQ9	EBI	B	EBI1 LPDDR5X data bit 9
M_C28	EBI2_DQ9	EBI	B	EBI2 LPDDR5X data bit 9
M_AF15	EBI3_DQ9	EBI	B	EBI3 LPDDR5X data bit 9
M_C3	EBI0_RDQS0_C	EBI	DI	EBI0 LPDDR5X differential read data strobe for byte 0 (C)
M_AE12	EBI1_RDQS0_C	EBI	DI	EBI1 LPDDR5X differential read data strobe for byte 0 (C)
M_C17	EBI2_RDQS0_C	EBI	DI	EBI2 LPDDR5X differential read data strobe for byte 0 (C)
M_AE26	EBI3_RDQS0_C	EBI	DI	EBI3 LPDDR5X differential read data strobe for byte 0 (C)
M_B3	EBI0_RDQS0_T	EBI	DI	EBI0 LPDDR5X differential read data strobe for byte 0 (T)
M_AF12	EBI1_RDQS0_T	EBI	DI	EBI1 LPDDR5X differential read data strobe for byte 0 (T)
M_B17	EBI2_RDQS0_T	EBI	DI	EBI2 LPDDR5X differential read data strobe for byte 0 (T)
M_AF26	EBI3_RDQS0_T	EBI	DI	EBI3 LPDDR5X differential read data strobe for byte 0 (T)
M_C12	EBI0_RDQS1_C	EBI	DI	EBI0 LPDDR5X differential read data strobe for byte 1 (C)
M_AE3	EBI1_RDQS1_C	EBI	DI	EBI1 LPDDR5X differential read data strobe for byte 1 (C)
M_C26	EBI2_RDQS1_C	EBI	DI	EBI2 LPDDR5X differential read data strobe for byte 1 (C)
M_AE17	EBI3_RDQS1_C	EBI	DI	EBI3 LPDDR5X differential read data strobe for byte 1 (C)
M_B12	EBI0_RDQS1_T	EBI	DI	EBI0 LPDDR5X differential read data strobe for byte 1 (T)
M_AF3	EBI1_RDQS1_T	EBI	DI	EBI1 LPDDR5X differential read data strobe for byte 1 (T)
M_B26	EBI2_RDQS1_T	EBI	DI	EBI2 LPDDR5X differential read data strobe for byte 1 (T)

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_AF17	EBI3_RDQS1_T	EBI	DI	EBI3 LPDDR5X differential read data strobe for byte 1 (T)
M_F15	DDR_RESET_N	PX1	DO	LPDDR5X reset (shared by EBIs)
M_E3	EBI0_WCK0_C	EBI	DO	EBI0 LPDDR5X differential data clock for byte 0 (C)
M_AC12	EBI1_WCK0_C	EBI	DO	EBI1 LPDDR5X differential data clock for byte 0 (C)
M_E17	EBI2_WCK0_C	EBI	DO	EBI2 LPDDR5X differential data clock for byte 0 (C)
M_AC26	EBI3_WCK0_C	EBI	DO	EBI3 LPDDR5X differential data clock for byte 0 (C)
M_F3	EBI0_WCK0_T	EBI	DO	EBI0 LPDDR5X differential data clock for byte 0 (T)
M_AB12	EBI1_WCK0_T	EBI	DO	EBI1 LPDDR5X differential data clock for byte 0 (T)
M_F17	EBI2_WCK0_T	EBI	DO	EBI2 LPDDR5X differential data clock for byte 0 (T)
M_AB26	EBI3_WCK0_T	EBI	DO	EBI3 LPDDR5X differential data clock for byte 0 (T)
M_E12	EBI0_WCK1_C	EBI	DO	EBI0 LPDDR5X differential data clock for byte 1 (C)
M_AC3	EBI1_WCK1_C	EBI	DO	EBI1 LPDDR5X differential data clock for byte 1 (C)
M_E26	EBI2_WCK1_C	EBI	DO	EBI2 LPDDR5X differential data clock for byte 1 (C)
M_AC17	EBI3_WCK1_C	EBI	DO	EBI3 LPDDR5X differential data clock for byte 1 (C)
M_F12	EBI0_WCK1_T	EBI	DO	EBI0 LPDDR5X differential data clock for byte 1 (T)
M_AB3	EBI1_WCK1_T	EBI	DO	EBI1 LPDDR5X differential data clock for byte 1 (T)
M_F26	EBI2_WCK1_T	EBI	DO	EBI2 LPDDR5X differential data clock for byte 1 (T)
M_AB17	EBI3_WCK1_T	EBI	DO	EBI3 LPDDR5X differential data clock for byte 1 (T)
M_F14	LPDDR5X_ZQ_A_C		Reference	ZQ calibration reference (channels A and C)
M_AB15	LPDDR5X_ZQ_B_D		Reference	ZQ calibration reference (channels B and D)

[a] See Table 2-1 for parameter and acronym definitions

Table 2-8 MSM top pin descriptions – power-supply pins

Pin number	Pin name	Functional description
M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16, M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27	LPDDR5X_VDD1	LPDDR5X core1 power
M_A4, M_A8, M_A10, M_A11, M_A18, M_A19, M_A21, M_A25, M_AA1, M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_E21, M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_Y25, M_Y26, M_Y28	LPDDR5X_VDD2H	LPDDR5X core2/input buffer power
M_A5, M_A9, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10, M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_G20, M_G24, M_G26	LPDDR5X_VDD2L	LPDDR5X core2/input buffer power
M_A6, M_A12, M_A17, M_A23, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10, M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_E27, M_G4, M_G25	LPDDR5X_VDDQ	LPDDR5X I/O buffer power

Table 2-9 MSM top pin descriptions – ground pins

Pin number	Pin name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground

Table 2-10 MSM top pin descriptions – not connected pins

Pin number	Pin name	Functional description
M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally.

Table 2-11 MSM top pin descriptions – reserved pins

Pin number	Pin name	Functional description
M_AB14	RFU	Reserved pins

3 Electrical specifications

3.1 Absolute maximum ratings

This information will be included in future revisions of this document.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-1).

Table 3-1 Operating conditions for voltage rails with AVS Type-1

Parameter [a]		Min	Max	Unit
Power supply voltages				
VDD_APC0_CX	Qualcomm Oryon application processor	TBD	TBD	V
VDD_APC0_MX	Qualcomm Oryon application processor memory	TBD	TBD	V
VDD_APC1_CX	Qualcomm Oryon application processor	TBD	TBD	V
VDD_APC1_MX	Qualcomm Oryon application processor memory	TBD	TBD	V
VDD_GFX	Graphics	TBD	TBD	V
VDD_GFX_MXC	Graphics memory	TBD	TBD	V
VDD_CX VDD_D_EBI_0 VDD_D_EBI_1 VDD_D_EBI_2 VDD_D_EBI_3	Digital core circuits EBI0 PHY digital circuits EBI1 PHY digital circuits EBI2 PHY digital circuits EBI3 PHY digital circuits	TBD	TBD	V
	Retention	TBD	TBD	
VDD_LPI_CX	Low power island core	TBD	TBD	V
VDD_LPI_MX VDD_LPI_MX_NAV	Low power island memory	TBD	TBD	V
VDD_MM	Multimedia subsystem circuits	TBD	TBD	V
VDD_MODEM	Modem	TBD	TBD	V
VDD_MX_A VDD_MX_C	On-chip memory On-chip power-collapsible memory	TBD	TBD	V
	Retention	TBD	TBD	
VDD_NSP1	NSP1	TBD	TBD	V
VDD_NSP2	NSP2	TBD	TBD	V
VDD_A_EBI_0 VDD_A_EBI_1 VDD_A_EBI_2 VDD_A_EBI_3 VDD_A_EBI_0_PLL_0P9	EBI0 PHY circuits EBI1 PHY circuits EBI2 PHY circuits EBI3 PHY circuits EBI0 PLL circuits	TBD	TBD	V

Table 3-1 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [a]		Min	Max	Unit
VDD_A_EBI_1_PLL_0P9	EBI1 PLL circuits			
VDD_A_EBI_2_PLL_0P9	EBI2 PLL circuits			
VDD_A_EBI_3_PLL_0P9	EBI3 PLL circuits			

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-2 Operating conditions

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_CSI_01_0P9 VDD_A_CSI_35_0P9 VDD_A_PCIE_0_CORE	MIPI CSI0, CSI1 0.9 V circuits MIPI CSI3, CSI5 0.9 V circuits PCIe0 core circuits	TBD	0.88	TBD	V
VDD_A_CSI_24_0P9 VDD_A_DSI_01_0P9 VDD_A_DSI_01_PLL_0P9 VDD_A_QREFS_0P875_1 VDD_A_QREFS_0P875_2 VDD_A_QREFS_0P875_3 VDD_A_QREFS_0P875_5 VDD_A_QREFS_0P875_6 VDD_A_QREFS_TX_0P875	MIPI CSI2, CSI4 0.9 V circuits MIPI DSI0, DSI1 0.9 V circuits MIPI DSI0, DSI1 PLL 0.9 V circuits QREFS 0.875 V circuits	TBD	0.88	TBD	V
VDD_A_UFS_CORE	UFS core circuits	TBD	0.912	TBD	V
VDD_A_QLINK_0_B_0P9 VDD_A_QLINK_0_B_CK_0P9	Qlink0_B 0.9 V circuits Qlink0_B clock circuits	TBD	0.912	TBD	V
VDD_A_QLINK_0_L_0P9 VDD_A_QLINK_0_L_CK_0P9	Qlink0_L 0.9 V circuits Qlink0_L clock circuits	TBD	0.88	TBD	V
VDD_A_USB_SS_DP_CORE VDD_A_EUSB_CORE	USB SS and DisplayPort core circuits eUSB core circuits	TBD	0.88	TBD	V
VDD_A_CSI_01_1P2 VDD_A_CSI_24_1P2 VDD_A_CSI_35_1P2 VDD_A_DSI_01_1P2 VDD_A_PCIE_0_1P2 VDD_A_EUSB_1P2 VDD_A_UFS_1P2 VDD_A_USB_SS_DP_1P2 VDD_A_QLINK_0_B_1P2 VDD_A_GNSS_ADC_1P2 VDD_A_QREFS_1P2 VDD_A_QREFS_TX_1P2	MIPI CSI0, CSI1 1.2 V circuits MIPI CSI2, CSI4 1.2 V circuits MIPI CSI3, CSI5 1.2 V circuits MIPI DSI 1.2 V circuits PCIe0 1.2 V circuits eUSB 1.2 V circuits UFS 1.2 V circuits USB SS and DisplayPort 1.2 V circuits Qlink0 1.2 V circuits GNSS ADC 1.2 V circuits QREFS 1.2 V circuits	TBD	1.2	TBD	V
VDD_PX0	Digital pad circuits - SPMI, RESIN_N - 1.2 V	TBD	1.2	TBD	V
VDD_PX11	Digital pad circuits - CXO - 1.2 V	TBD	1.2	TBD	V

Table 3-2 Operating conditions (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
VDD_PX13	Digital pad circuits - SPU - 1.8 V	TBD	1.8	TBD	V
VDD_PX14	Digital pad circuits - SDC2, RESOUT_N, PS_HOLD, SLEEP_CLK, MODE - 1.2 V	TBD	1.2	TBD	V
VDD_IX	Digital pad circuits - dual voltage pad (0.9 V)	TBD	0.9	TBD	V
VDD_PX701 - VDD_PX706 VDD_PX708 - VDD_PX722	Digital pad circuits - dual voltage* (1.2 V/1.8 V) * Per pad group, intended power supply should be connected properly - either 1.2 V or 1.8 V	TBD TBD	1.2 1.8	TBD TBD	V
VDD_QFPROM VDD_QFPROM_SP	Programming QFPROM Programming QFPROM and SPU	TBD	1.8	TBD	V
VDD_IO_EBI_0	EBI0 I/O memory circuits				
VDD_IO_EBI_1	EBI1 I/O memory circuits				
VDD_IO_EBI_2	EBI2 I/O memory circuits				
VDD_IO_EBI_3	EBI3 I/O memory circuits				
LPDDR5X_VDDQ	PoP DDR pads (I/O buffer) [c]				
	LPDDR5X spec range 1 [d]	TBD	0.5	TBD	V
	LPDDR5X spec range 2 [e]	TBD	0.3	TBD	V
LPDDR5X_VDD1	PoP DDR pads (core 1) [c]	–	–	–	V
LPDDR5X_VDD2H	PoP DDR pads (core 2/input buffer) [c]	–	–	–	V
LPDDR5X_VDD2L	PoP DDR pads (core 2/input buffer) [c]	–	–	–	V
Thermal conditions					
T	Device operating temperature (0.55 mm package height device)	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C
T	Device operating temperature (0.60 mm package height device)	$T_{ambient}$ = -30	–	$T_{junction}$ = +105	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.
[c] See the LPDDR5/5X standard (JESD209-5C) and vendor's data sheets for the recommended DC operating conditions (min/typ/max voltages and PDN specification) of VDD2H/VDD2L/VDD1/VDDQ
[d] LPDDR5X spec range 1 is intended for I/O operation with both ODT enabled and disabled.
[e] LPDDR5X spec range 2 is intended for I/O operation with both ODT disabled.

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8750/SM8750P Chipset Power Delivery Network Specification* (80-64994-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8750 with SDR875 Linux Android Current Consumption Data Application Note* (80-64994-7A).

3.5 Digital logic characteristics

This information will be included in future revisions of this document.

3.6 Timing characteristics

This information will be included in future revisions of this document.

3.7 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5X SDRAM memory that is attached to the top of the SM8750/SM8750P chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8750 Recommendations* (80-VP300-24).

3.8 Multimedia

This information will be included in future revisions of this document.

3.9 Connectivity

This information will be included in future revisions of this document.

3.10 Internal functions

This information will be included in future revisions of this document.

3.11 Power management interface

This information will be included in future revisions of this document.

4 Mechanical information

4.1 Device physical dimensions

The SM8750/SM8750P device is available in the MPSP1512 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1512 has a 15.95 mm by 14.0 mm body, with a maximum height of 0.60 mm or 0.55 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1512 outline drawing is shown in Figure 4-2.

NOTE Click the following link to download the *Package Outline Drawing, MPSP1512, 15.95 × 14.0 × 0.60 mm, ST94, M197, SB127, NSPPB 496, PL1, MEP* (NT90-31844-2) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-31844-2

After successfully logging in, the document is downloaded.

NOTE Click the following link to download the *Package Outline Drawing, MPSP1512, 15.95 × 14.0 × 0.55 mm, ST94, M147, SB127, NSPPB 496, PL1, MEP* (NT90-31844-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-31844-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

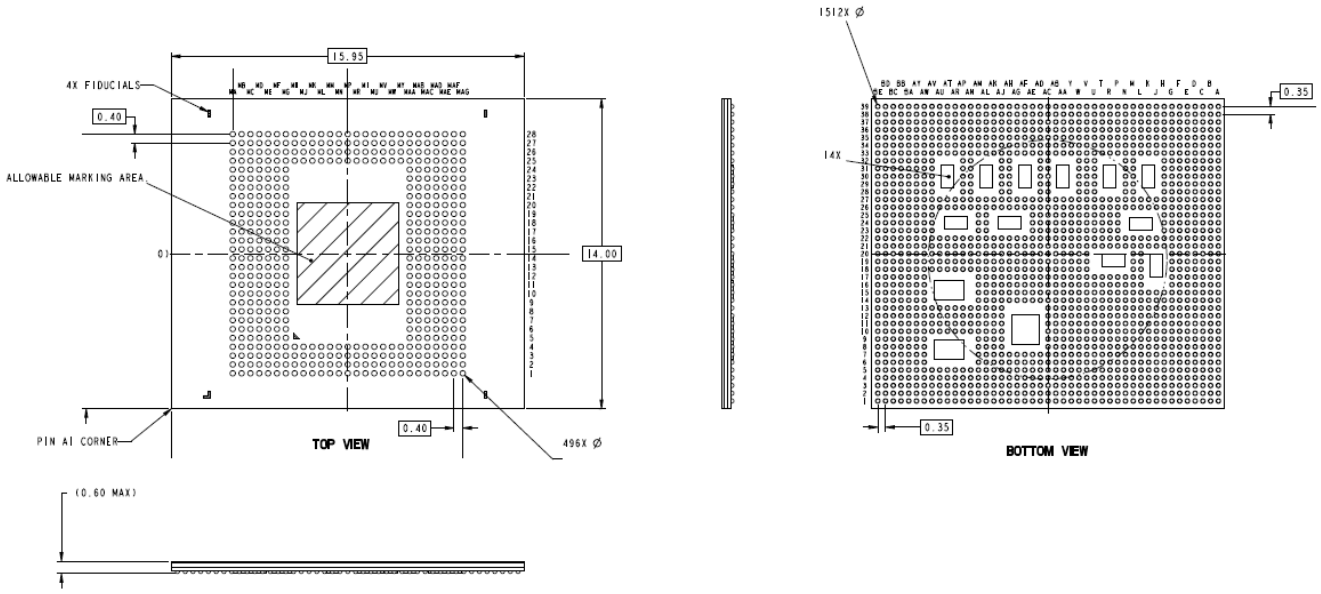

Figure 4-1 MPSP1512 outline drawing (for 0.60 mm device)

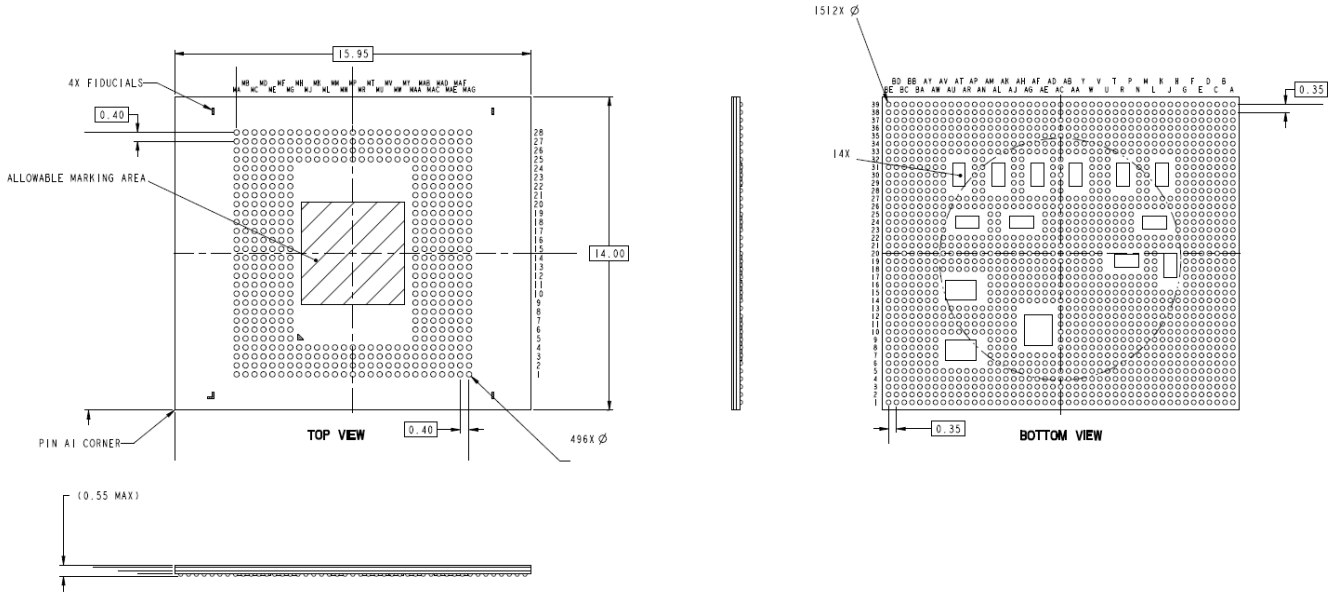

Figure 4-2 MPSP1512 outline drawing (for 0.55 mm device)

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

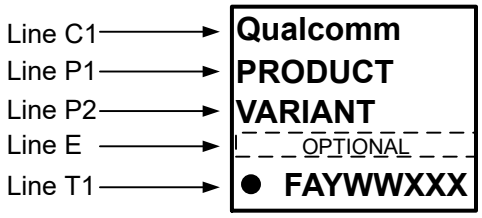

Figure 4-3 SM8750 device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ SM8750
P2	VARIANT	PRR-BB ▪ See Table 4-3 for the assigned values.
E	Blank or random	Optional information
T1	FAYWWXXX	F = foundry company code ▪ F = F for TSMC A = assembly site code ▪ A = X (Amkor, Japan) ▪ A = C (Amkor, Korea) Y = single/last digit of year WW = two-digit work week of current year XXX = lot serial number
	●	Ball A1 indicator

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-2.

Table 4-2 Example device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8750	-6	-MPSP	1512			-TR	-00	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8750-6-MPSP1512-MT-00-0-AB

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

For availability and information about daisy chain parts, contact the Qualcomm Sales team for support.

Table 4-2 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-3.

4.4 Device identification for each sample type

Table 4-3 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	FEATURE_ID [b]	Device identification register (JTAG ID)	Source configuration code (S) [c]	Comments	Sample date
SM8750	ES	600-AB	0x2B	0x0 028C 0E1	0	SM8750 (600-0-AB), MPSP1512, SM8750, CPU/GPU/AI cores, LPDDR5X, Modem for Sub-6 and mmW, 0.55 mm package height	2/15/2024
SM8750	ES	100-AB	0x30	0x0 028C 0E1	0	SM8750 (100-0-AB), MPSP1512, SM8750, CPU/GPU/AI cores, LPDDR5X, Modem for Sub-6 and mmW, 0.60 mm package height	3/20/2024

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
[b] See Table 4-5. FEATURE_ID combined with device identification register defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all the qualified die fabrication-source/assembly site combinations available when the particular sample type was shipped. S values are defined in Table 4-4.

Table 4-4 Source configuration codes

S value	F value = F	A value = C	A value = X
0	TSMC	Amkor, Korea	Amkor, Japan

FEATURE_ID and device identification register details are summarized in Table 4-5 and Table 4-6.

Table 4-5 QFPROM JTAG register (0x221C20C8)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants. See Table 4-3.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the device identification register (see Table 4-3 and Table 4-6).

The device identification register allows the user to determine the device's manufacturer, part number, and version via the test access port (TAP). The 32-bit device identification register is read through the JTAG interface and is summarized in Table 4-6.

Table 4-6 Device identification register (JTAG_ID, 0x221C8744)

Bit location	Description	Value
bits [31:28]	Version data (may change with sample type)	0x0
bits [27:12]	Part number (changes with device)	028C
bits [11:1]	Manufacturer identity code (administered by JEDEC)	070 (QTI code)
bit [0]	Device identification register start bit	Always = 1

4.5 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-7.

Table 4-7 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM8750/SM8750P rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8750/SM8750P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.6 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the

SM8750 0.60 mm Max LPDDR5X 16 GB Package Thermal Model Icepak (HS11-64994-7HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-64994-7HW

SM8750 0.60 mm Max LPDDR5X 16 GB Package Thermal Model Flowtherm (HS11-64994-8HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-64994-8HW

After successfully logging on, the document is downloaded.

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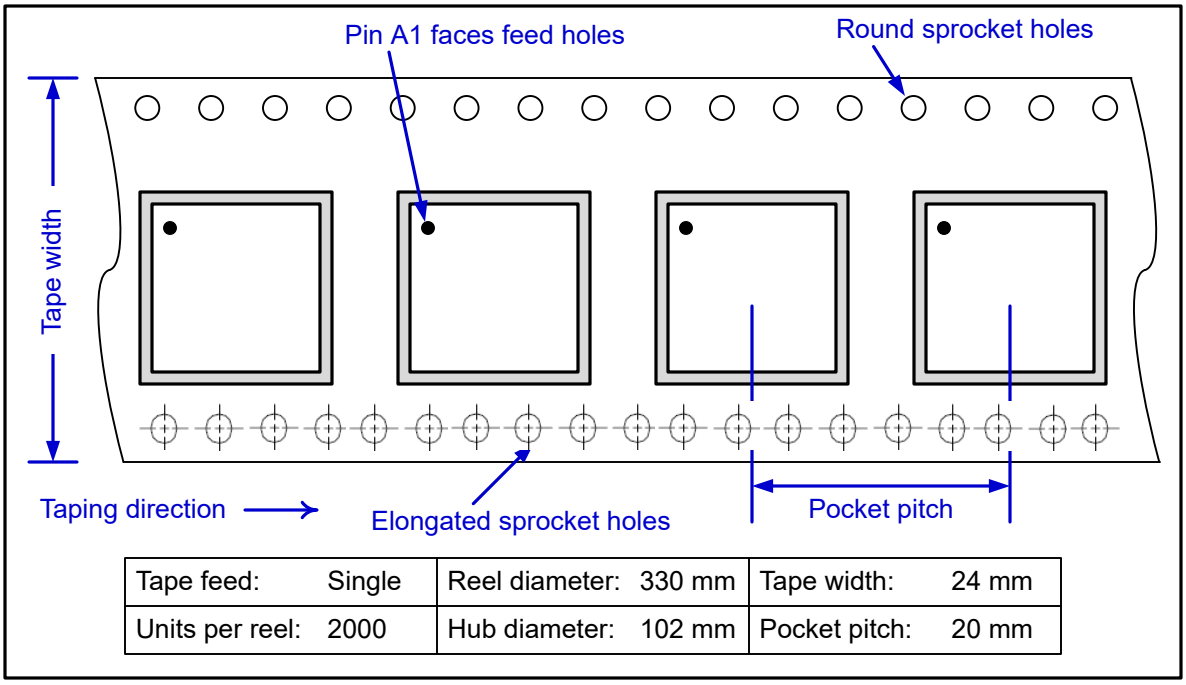
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8750/SM8750P tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown below.

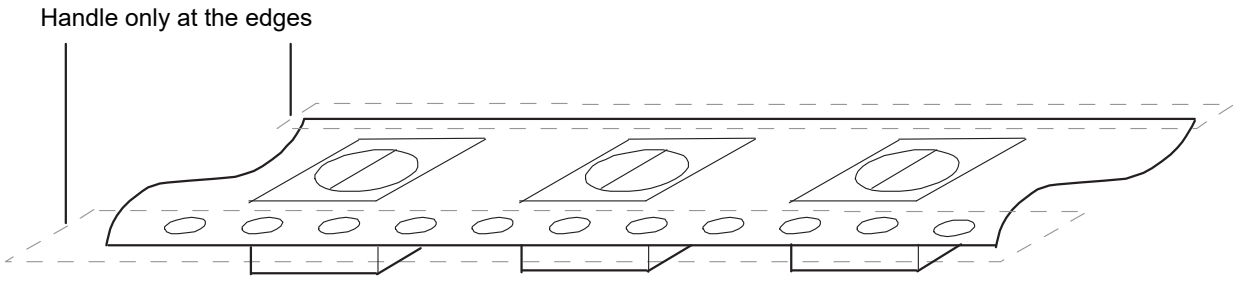


Figure 5-2 Tape handling

5.1.2 Matrix tray information - available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See Figure 5-3 for matrix-tray key attributes. See Table 5-1 for matrix-tray key dimensions.

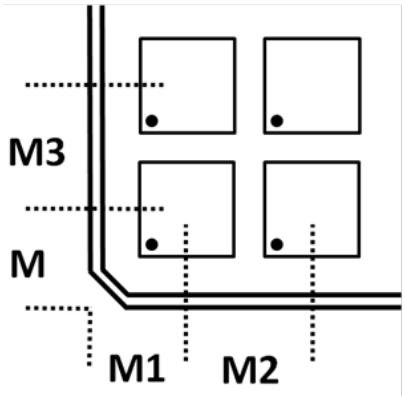


Figure 5-3 Matrix-tray key attributes

Table 5-1 Matrix-tray key dimensions

Key dimensions	
Array	6 × 15 (90)
M	15.45 mm
M1	14.00 mm
M2	20.50 mm
M3	21.00 mm

5.2 Storage

5.2.1 Bagged storage conditions

SM8750/SM8750P devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out of bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Device moisture sensitivity level.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM8750/SM8750P if the conditions specified in Bagged storage conditions and Out of bag duration have **not been exceeded.**

It is **necessary** to bake the SM8750/SM8750P if any condition specified in Bagged storage conditions or Out of bag duration has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

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6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy chain components.

Daisy chain PCB routing recommendations are available for download.

NOTE Click the following link to download the *Daisy Chain Interconnect, MPSP1512, 15.95 × 14.0 mm* (DS90-31844-R1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-31844-R1

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6.4 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability. Board-level reliability data is available for download.

NOTE Click the following link to download the *Board Level Reliability, MPSP1512 (BR80-31844-1)* from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/BR80-31844-1

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6.5 High temperature warpage

QTI measures package warpage across SMT reflow. High temperature warpage data is available for download.

NOTE Click the following link to download the *High Temperature Warpage, MPSP1512 (WR80-31844-1)* from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/WR80-31844-1

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7 Part reliability

This information will be included in future revisions of this document.

8 Samples and known issues

8.1 Sample testing

8.1.1 Engineering samples (ES)

These devices undergo limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples should not be used for product-level qualification.

8.1.2 Commercial samples (CS)

These devices undergo full production-level testing, and meet the specifications and features described in the device specification, except as otherwise noted in this document. They have passed device-level qualification. Commercial samples are suitable for performance testing, and also for product-level production and qualification.

8.2 Known issues

8.2.1 Summary of known issues

All known issues for each revision of the SM8750/SM8750P device are summarized in Table 8-2. The text within the Issue column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur. An X in one or more of the sample type columns indicates that the issue occurs in the corresponding sample type.

The following information is provided for each issue:

- Issue description
- Impact to system performance
- Possible workarounds to minimize impact

Table 8-1 Functional area descriptions

Functional area	Description
Modem	Modem subsystem
MMSS	Multimedia subsystem
CPUSS	CPU subsystem
DDRSS	DDR subsystem
GPUSS	GPU subsystem
LPAI	Low-power AI subsystem
PSS	Peripheral subsystem
RPM	Resource and power management
SPSS	Secure processor subsystem
TME	Trust management engine

Table 8-1 Functional area descriptions (cont.)

Functional area	Description
WCSS	Wireless connectivity subsystem
General	General area

Table 8-2 Known issues – all sample types and revisions

Issue number and issue description	Functional area [a]	Workaround	SM8750-AB ES PRR = 600 [b]	SM8750-AB ES PRR = 100 [b]
Issue 1 – F_{MAX} limitation in ES	General	None available, information only	X	X
Issue 2 – Power is not optimized in ES	General	None available, information only	X	X
Issue 3 – Performance is not optimized in ES	General	None available, information only	X	X

[a] The functional areas are defined in Table 8-1
[b] P and RR values are detailed in the Variant column of Table 4-3.

8.2.2 Issues – description, impact, and workaround

Issue 1 – F_{MAX} limitation in ES

Description	F_{MAX} for ES samples is different from CS target frequencies.
Impact	ES samples may operate at lower frequencies and higher voltages for some cores and subsystems.
Workaround	The target FMAX will be achieved by CS in a future hardware revision.

Return to Table 8-2

Issue 2 – Power is not optimized in ES

Description	Power is not optimized in ES
Impact	ES devices do not have all the planned hardware and software features enabled. Therefore, these devices do not represent the final product's performance.
Workaround	Power optimization will be enabled in a future hardware revision.

Return to Table 8-2

Issue 3 – Performance is not optimized in ES

Description	Performance is not optimized in ES
Impact	ES devices do not have all the planned hardware and software features enabled. Therefore, these devices do not represent the final product's performance.
Workaround	Performance optimization will be enabled in a future hardware revision.

Return to Table 8-2

9 Revision history

Revision	Date	Description
AA	July 2023	Initial release
AB	October 2023	■ Table 1-1 *SM8750/SM8750P features*: □ Under *Digital signal processing and artificial intelligence* feature, renamed "ML ISP" to "AI ISP" □ Updated camera and EVA features ■ Table 3-1 *Operating conditions for voltage rails with AVS Type-1*: Added this table ■ Table 3-2 *Operating conditions*: Added this table
AC	December 2023	■ Figure 1-1 *SM8750 + SDR875 (sub-6/mmW solution) functional block diagram and example application*: Added '1.2 V only' text for the path between GRFC/RFFE and Tuner blocks ■ Figure 1-2 *SM8750 + SDR753 (sub-6 solution) functional block diagram and example application*: Added '1.2 V only' text for the path between GRFC/RFFE and Tuner blocks ■ Table 1-1 *SM8750/SM8750P features*: Updated the internal panel resolution and external panel support ■ Figure 2-2 *SM8750 bottom pin assignments (top view)*: Updated BD38 and BC39 pins as DNC ■ Table 2-2 *MSM bottom pin descriptions – general pins*: Updated the functional description for D17 and E17 pins ■ Table 2-6 *MSM bottom pin descriptions: Not connected pins*: Added BD38 and BC39 pins to DNC
AD	February 14, 2024	■ Key features: Updated the low-power AI feature ■ Table 1-1 *SM8750/SM8750P features*: Added Low-power AI subsystem feature capability ■ Added the following sections under Chapter 3 *Electrical specifications*: □ Section 3.1 Absolute maximum ratings □ Section 3.3 Power delivery network specification □ Section 3.4 Average operating current □ Section 3.5 Digital logic characteristics □ Section 3.6 Timing characteristics □ Section 3.7 Memory support □ Section 3.8 Multimedia □ Section 3.9 Connectivity □ Section 3.10 Internal functions □ Section 3.11 Power management interface ■ Added the following sections under Chapter 4 *Mechanical information*: □ Section 4.2 Part marking □ Section 4.3 Device ordering information □ Section 4.4 Device identification for each sample type □ Section 4.5 Device moisture sensitivity level □ Section 4.6 Thermal characteristics ■ Chapter 5 Carrier, storage, and handling information: Added this chapter ■ Chapter 6 PCB mounting guidelines: Added this chapter ■ Chapter 8 Samples and known issues: Added this chapter
AE	February 23, 2024	■ Key features: Added 0.60 mm device package dimensions ■ SM8750/SM8750P high-level block diagram and MPSP1512 outline drawing: Added 0.60 mm device ourline drawing

Revision	Date	Description
		■ Table 1-1 *SM8750/SM8750P features*: □ Added 0.60 mm device package dimensions □ Added WLAN/Bluetooth feature capability ■ Table 3-2 *Operating conditions*: Added device operating temperature ■ Section 4.1 *Device physical dimensions*: Added 0.60 mm device package drawing document and download link ■ Figure 4-1 *MPSP1512 outline drawing (for 0.60 mm device)*: Added the package outline drawing for 0.60 mm device ■ Table 4-3 *Device identification details*: Added ES sample details for 100-AB variant
AF	March 25, 2024	■ Table 4-3 *Device identification details*: Added ES sample date for 100-AB variant ■ Table 8-2 *Known issues – all sample types and revisions*: Updated the issues for PRR = 100 ES sample
AG	March 26, 2024	■ Table 4-3 *Device identification details*: Updated the feature ID for 600-AB ES sample

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