

Qualcomm Technologies, Inc.

Device description

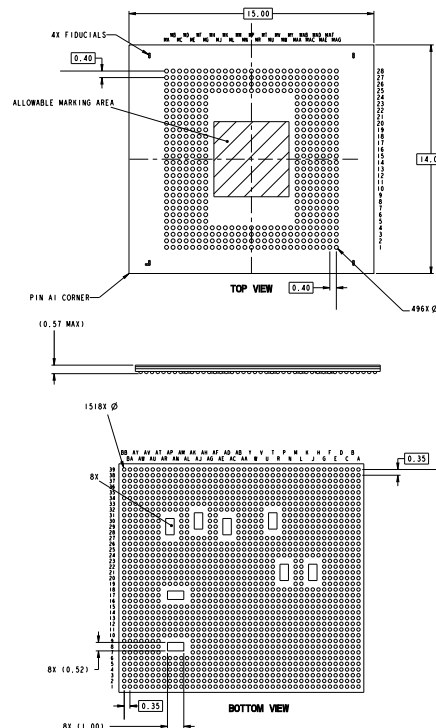
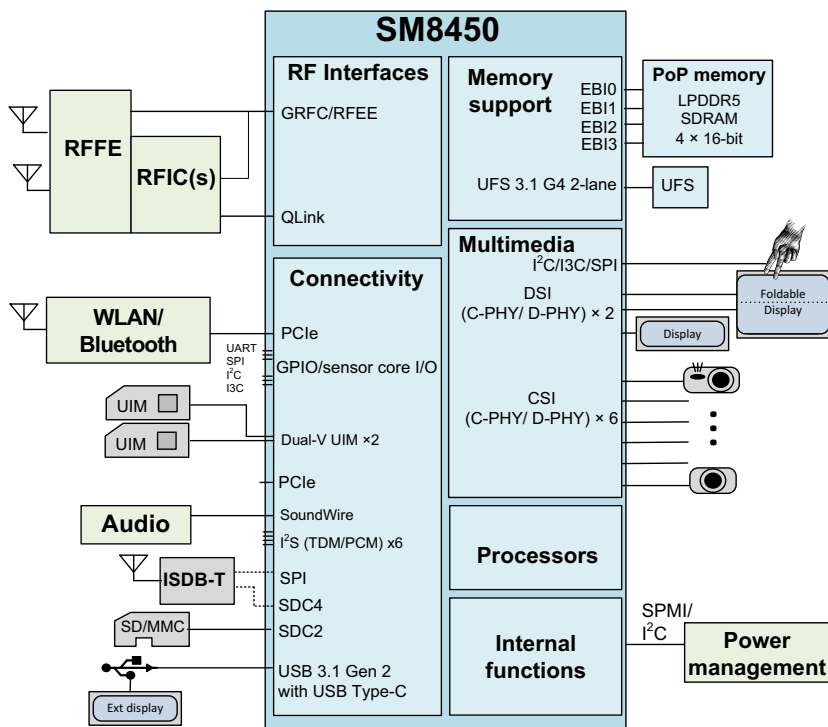
The SM8450 device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with a 4 LPX process, for superior performance and power efficiency. SM8450 includes the following key components:

- Qualcomm® Kryo™ 780 CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 730 GPU for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ 680 Image Signal Processor for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 1195 DPU for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 GHz bands (Rel 16 integrated modem)

Key features (see Section 1.2 for details)

- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9380/WCD9385 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Snapdragon Sensors Core Technology for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU260) for advanced secure use cases
- Qualcomm® Hexagon™ Tensor Processor (HTP) with Hexagon Vector eXtensions (HVX) and Hexagon Matrix eXtensions (HMx)
- Qualcomm® FastConnect™ 6900 System with WCN685x, 802.11ax, 2 × 2 MIMO, Bluetooth 5.2
- Quad-channel package-on-package (PoP) high-speed LPDDR5 SDRAM
- 14.0 × 15.0 mm MPSP1518 PoP

SM8450 high-level block diagram and MPSP1518 outline drawing



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1 Introduction

Document updates

See the [Revision history](#) for details on the changes included in this revision.

1.1 Functional block diagram

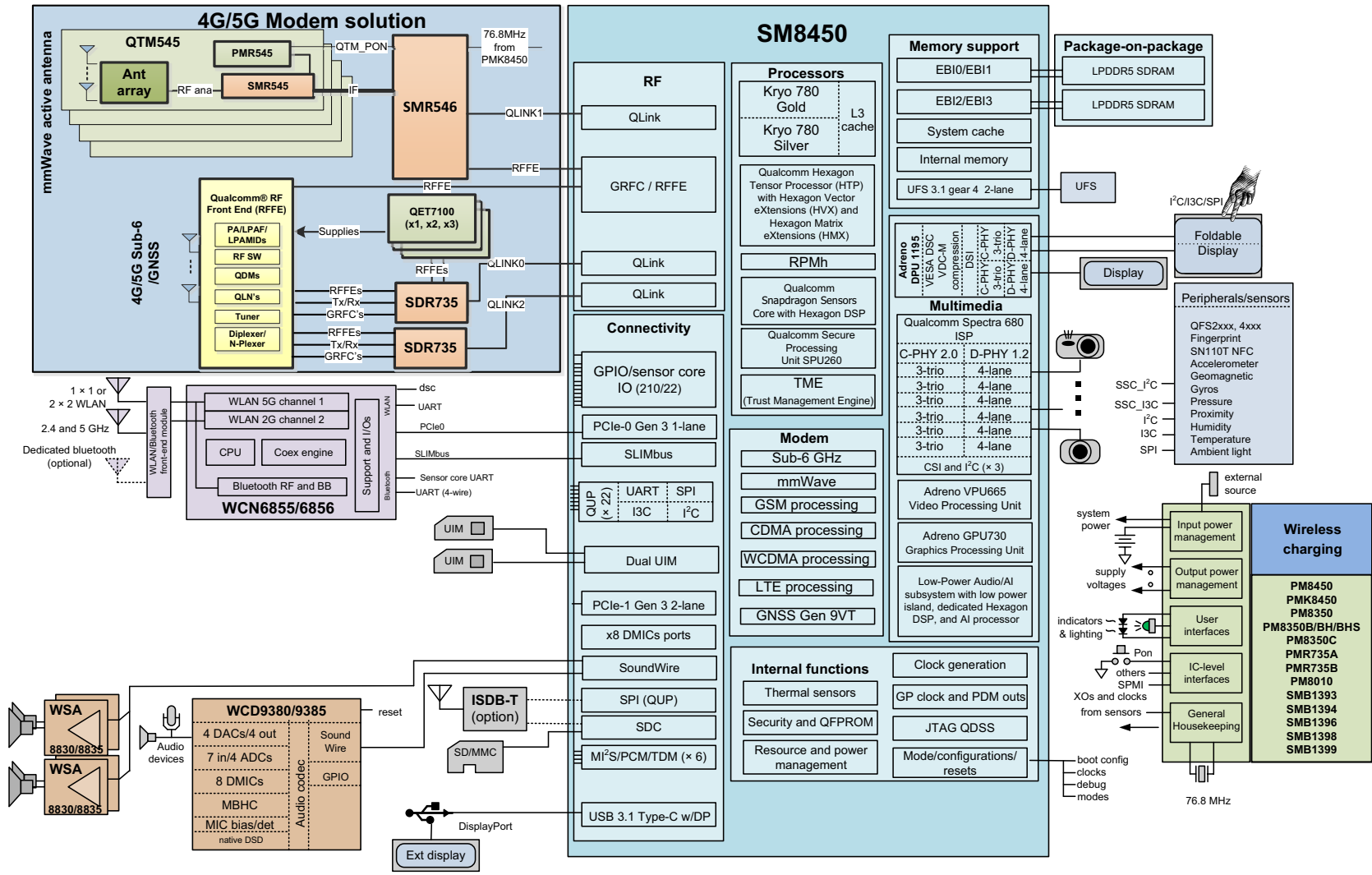


Figure 1-1 SM8450 functional block diagram and example application

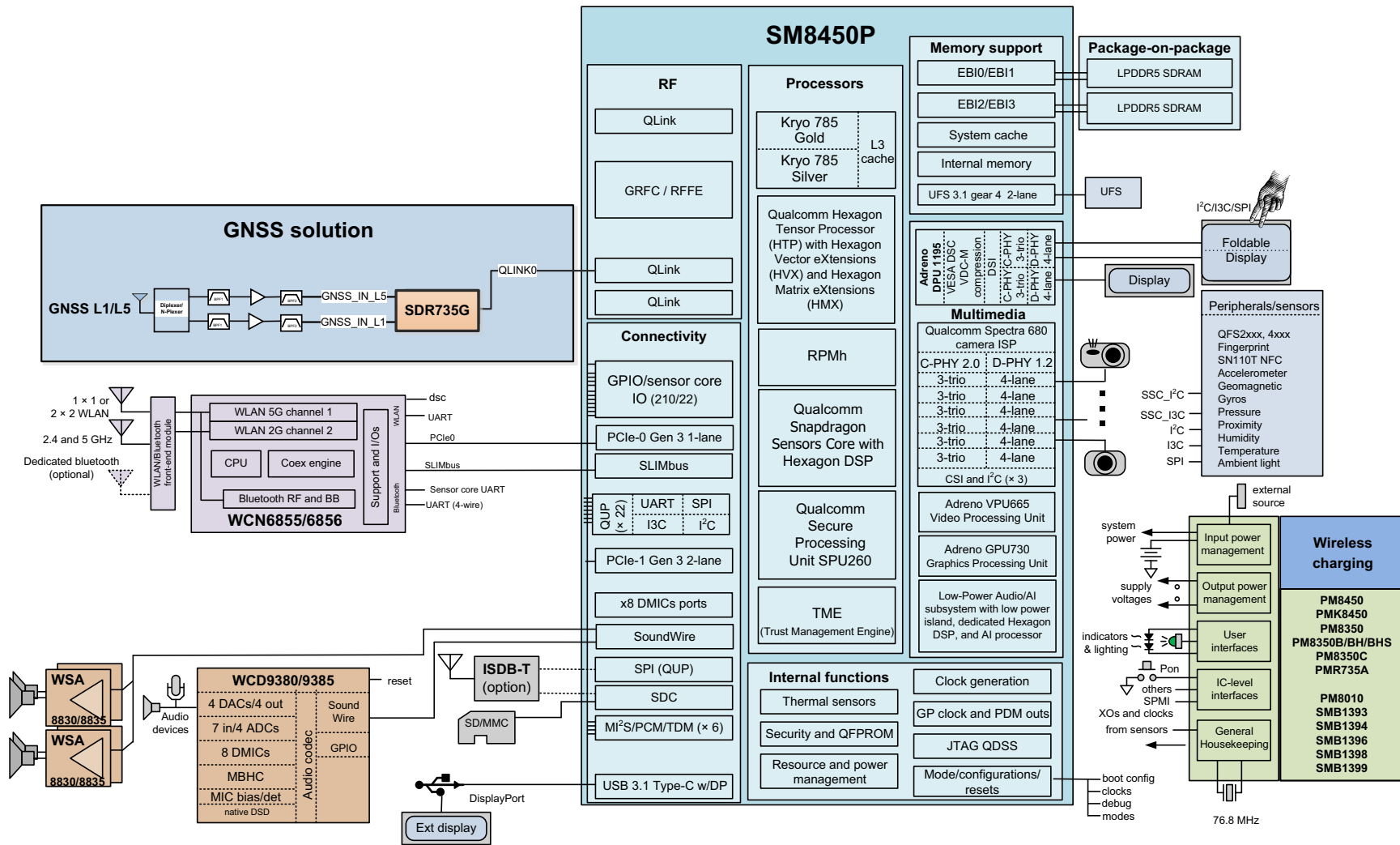


Figure 1-2 SM8450P functional block diagram and example application

1.2 SM8450 features

NOTE: Some of the hardware features integrated within the SM8450 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8450 features.

Table 1-1 SM8450 features

Feature	SM8450 capability		
Processors			
Applications	Kryo 780 CPU subsystem		
	<ul style="list-style-type: none"> ■ Prime and high-performance cores for intensive tasks ■ Quad power-efficient cores 		
	Cores	F_{max}	Cache per core
	1 - Kryo Prime	3 GHz	1 MB L2
	3 - Kryo Gold	2.5 GHz	512 KB L2
4 - Kryo Silver	1.8 GHz	128 KB L2	
Note: Each two Kryo Silver cores share one 128 KB L2 cache.			

Table 1-1 SM8450 features (cont.)

Feature	SM8450 capability
Digital signal processing and artificial intelligence	<ul style="list-style-type: none"> ■ Hexagon tensor processor <ul style="list-style-type: none"> □ V69 AI-optimized Tensor Processor □ Six threads Scalar DSP + 4x HVX vector co-processors □ Vector tightly-couple co-processor optimized for pixel processing □ Larger HMX (INT8/A16W8) □ Increase in VTCM □ BW compression □ 1.5x 8 bit and 16 bit TOPs improvement □ Higher peak and batch = 1 performance □ Improved power efficiency ■ Benefit/use cases: <ul style="list-style-type: none"> □ Noise reduction □ Super resolution □ ML ISP □ HDR □ Image enhancement □ Segmentation □ Depth estimation □ Classification/detection ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. ■ The audio Hexagon DSP is dedicated to the audio subsystem with support for always-on low-power use cases. It incorporates a dedicated AI processor for offloading neural network use cases to improve the performance and minimize power consumption. ■ The sensor Hexagon DSP in the Snapdragon Sensors Core Technology supports always-on, low-power use cases. ■ All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements. ■ Hexagon Tensor Processor dedicated neural processing unit for neural network (NN) use cases. It incorporates an NN matrix engine to ensure efficient execution of various neural networks and their parameters. ■ Hexagon Tensor Processor may be used for typical imaging, video, audio, and data-based NN use cases.
Always-on system	<p>Always-on subsystem with always-on processor</p> <p>Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication</p>

Table 1-1 SM8450 features (cont.)

Feature	SM8450 capability
Snapdragon Sensors Core LPI	Hexagon v66 DSP – 845 MHz normal; 1.2 GHz turbo/2.5 MB memory <ul style="list-style-type: none"> ■ Data acquisition engine (DAE) ■ Context change detector 4.0 (CCD) ■ Eight dedicated buses (One I3C, three I²C, one SPI, two UART, and one API I²C) ■ I3C IBI ■ Pedometer 3.0 ■ Activity recognition 1.0 ■ Qualcomm Sensing HUB 2.0 ■ Sensors supported: <ul style="list-style-type: none"> □ Accel/Gyro □ Magnetometer □ Ambient Light/Proximity □ Pressure □ Humidity/Temp □ SAR □ Hall □ Plus others per customer inputs
Modem Location	3G/4G/5G – mmWave and sub-6 GHz bands (Rel 16) Gen 9 VT v5 LocTech 21 SW
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR5 SDRAM (4 × 16-bit) designed for a 3200 MHz (LPDDR5) 4 MB system cache
External memory Via UFS Via SDC	UFS 3.1 gear 4 Rate B, 1x 2-lane ICE with 2000 MB/s read and 1600 MB/s Write Booster (Note: Write Booster performance depends on UFS) SD v3.0 4 bit for SD card
Multimedia	
Display	DPU 1195: <ul style="list-style-type: none"> ■ Maximum resolution for internal panel: Support up to UHD (3026 × 2160) at 120 Hz, 30 bpp ■ Supports dual MIPI DSI ports, with support for split-link for fold use case. ■ External panel support: DisplayPort v1.4a with MST (2x 4K60 10-bit or 1x 8K30 with DSC) ■ Compression support: VDC-M for internal panel and DSC v1.2 ■ Processing: rounded corner, Demura engine and SPR ■ Power-saving: panel self-refresh using LLC ■ FP16 support to improve rendering pipeline efficiency, reduce DDR traffic, reduce power consumption, offload tone-mapping process from GPU

Table 1-1 SM8450 features (cont.)

Feature	SM8450 capability
Camera support	<ul style="list-style-type: none"> ■ Qualcomm Spectra 680 Image Signal Processor <ul style="list-style-type: none"> □ Qualcomm Spectra 680 ISP supports connectivity to multiple cameras due to six included C-PHY/D-PHY interfaces. Furthermore, up to five cameras may operate concurrently due to the Qualcomm Spectra 680's 3 IFEs and 2 IFE-lites ■ Always on Camera (AON Camera) support <ul style="list-style-type: none"> □ CSI4 with PM8010 SPMI interface and 19.2 MHz CAM_MCLK_4 (GPIO_104) ■ HW interface <ul style="list-style-type: none"> □ Triple 36 MP ISPs □ Six combo-PHYs with four lanes each □ D-PHY 1.2 and C-PHY 2.0 □ 19.2 MHz (x8) camera clock support GPIO [107:100] ■ 2x throughput <ul style="list-style-type: none"> □ 108 MP @ 30 fps ZSL with in-ISP pixel binning □ 64 MP @ 30 fps ZSL with two IFEs combined, without in-ISP binning □ 200 MP non-ZSL snapshot capture - note: 113 MP with MFNR □ 12 MP @ 240 fps fast shutter sensor support - PHY and RAW dump ■ Key improvements: <ul style="list-style-type: none"> □ QCFA sensor support w/ HW remosaic, HDR and binning □ Fast sensor switching for smooth camera transition experience □ Major IQ improvements to deliver DSLR experience □ VBSE (Video Bokeh and Special Effect) □ LCAC for wide-angle chromatic aberration correction □ Highlight recovery white balance □ MMF (Massive Multi Frame) processing for extreme low light □ HDR10+ statistics □ GTM (Global Tone Mapping) for FD (Face Detection) □ Staggered HDR for snapshot, video, preview ■ ZSL example: <ul style="list-style-type: none"> □ (28 M + 28 M + 28 M) @ 30 fps - triple camera □ (64 M + 25 M) @ 30 fps - dual camera □ 108 M @ 30 fps - single camera (binned in the ISP) ■ MFHDR HW for snapshot, video, preview ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port ■ C-PHY v2.0: 6 Gbps/trio (41.14Gbps) on three trios per port <ul style="list-style-type: none"> □ Connect up to 12x/18x camera, 5x concurrent
Adreno video processing unit (VPU)	<p>Adreno VPU 665</p> <p>UHD video processing unit</p> <p>Video decode up to 4K240/8K60</p> <p>Video encode up to 4K120/8K30</p> <p>Concurrent 4K60 decode and 4K60 encode for wireless display</p> <p>Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, and MPEG-2 formats</p> <p>Native encode support for H.265 Main 10, H.265 Main, H.264 High formats</p>

Table 1-1 SM8450 features (cont.)

Feature	SM8450 capability
Connectivity	
Qualcomm universal peripheral (QUP) ports	Qualcomm universal peripheral (QUP) v3 support. 22 QUP serial engine Seven lanes each for 4-QUPs and four lanes each for the 18-QUPs <ul style="list-style-type: none"> ■ UART ■ I²C ■ I3C ■ SPI
USB	One USB 3.1 ports: gen2 10 Gbps (DP + data), support Type-C with DisplayPort v1.4a
PCIe	1-lane Gen 3 2-lane Gen 3
Secure digital interfaces	<ul style="list-style-type: none"> ■ Two 4-bit ports (SDC2 and SDC4) ■ SDC2: dual-voltage; SD 3.0 ■ SDC4:1.8 V only, SDIO 3.0
Touchscreen support	Capacitive panels via ext IC (I ² C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm [®] Fingerprint Sensors for under glass, under metal, or under OLED display QFS2630, QFS4008
ISDBT/DMB support	Via external ISDBT/DMB device (SDC or SPI)
Configurable GPIOs	
Number of GPIO ports	210 – GPIO_0 to GPIO_209
Internal functions	
Security	
Crypto	AES-GCM, "HW ECC & RSA" (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP certifiable
QFPROM	Fuse bits available for OEM use
Access Control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure Boot with Sec Tools 2.0; easy to use tool set
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm [®] Trusted Execution Environment (QTEE v5.3)
DRM	DRM Widevine V16 L1, HDCP v2.3
QTEE services	QTEE services ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
SPU	SPU260 for SoC Independent TCB
TME	Introduce TME (Trust Management Engine) for SOC Root of Trust
Boot sequence	1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) rest of subsystems Emergency boot over USB 3.1

Table 1-1 SM8450 features (cont.)

Feature	SM8450 capability
PLLs and clocks	<ul style="list-style-type: none"> ■ 78.4 MHz X'tal ■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	2-channel 2-line SPMI; plus other lines, as needed, via GPIOs, I ² C
Wireless connectivity WLAN Bluetooth	PCIe interface SLIMbus/UART interface
Fabrication technology and package	
Digital die	4 LPX process
PoP – small, thermally efficient package	14.0 × 15.0 × 0.57 mm
WLAN/BT/FM RF PMIC Codec	WCN6855, WCN6856 SDR735 (4G/Sub-6/GNSS), SDR735G (GNSS), SMR546/QTM545 (mmW) PM8450, PMK8450, PM8350, PM8350B/BH/BHS, PM8350C, PM8010 × 2, PMR735A, PMR735B WCD9380/WCD9385, WSA8830/WSA8835

2 Pin definitions

The SM8450 is the lower device within a PoP system, as shown and explained in [Figure 2-1](#).

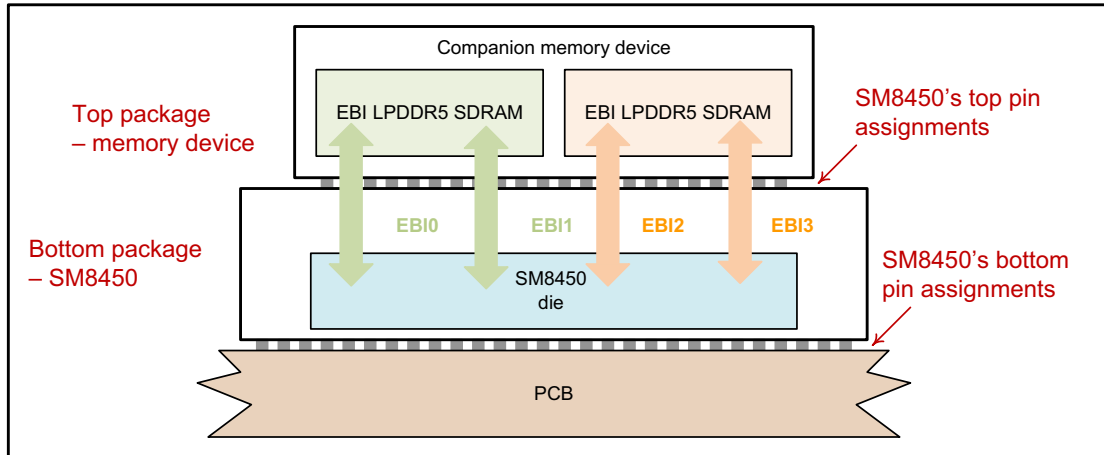


Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8450 bottom pins ([Section 2.2](#))
- SM8450 top pins ([Section 2.3](#))

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
PX0	Pad group 0 (SPMI, RESIN); 1.8 V
PX2	Pad group 2 (SDC2 IO); 1.8 V
PX3	Pad group 3 (most peripheral IO); 1.8 V
PX5	Pad group 5 (UICC 1); 1.8 V/2.85 V
PX6	Pad group 6 (UICC 2); 1.8 V/2.85 V
PX701	Pad group 701 (IO pad); 1.8 V
PX702	Pad group 702 (IO pad); 1.8 V
PX10	Pad group 10 (UFS IO); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
PX13	Pad group 13 (Secure processor); 1.85 V

2.2 Pin assignments: MSM bottom

2.2.1 Pin map: MSM bottom

The SM8450 is available in the MPSP1518 package. Its bottom surface is equivalent to an MPSP1518 that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See [Chapter 4](#) for package details and [Section 2.3](#) for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in [Figure 2-2](#).

The text within [Figure 2-2](#) is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in — the resolution is sufficient for comfortable reading.
- Download the *SM8450 Pin Assignment and GPIO Configuration Spreadsheet* (80-11140-1A). This Microsoft Excel spreadsheet lists all SM8450 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-11140-1A) from the Qualcomm® CreatePoint website.

<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-11140-1A>

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

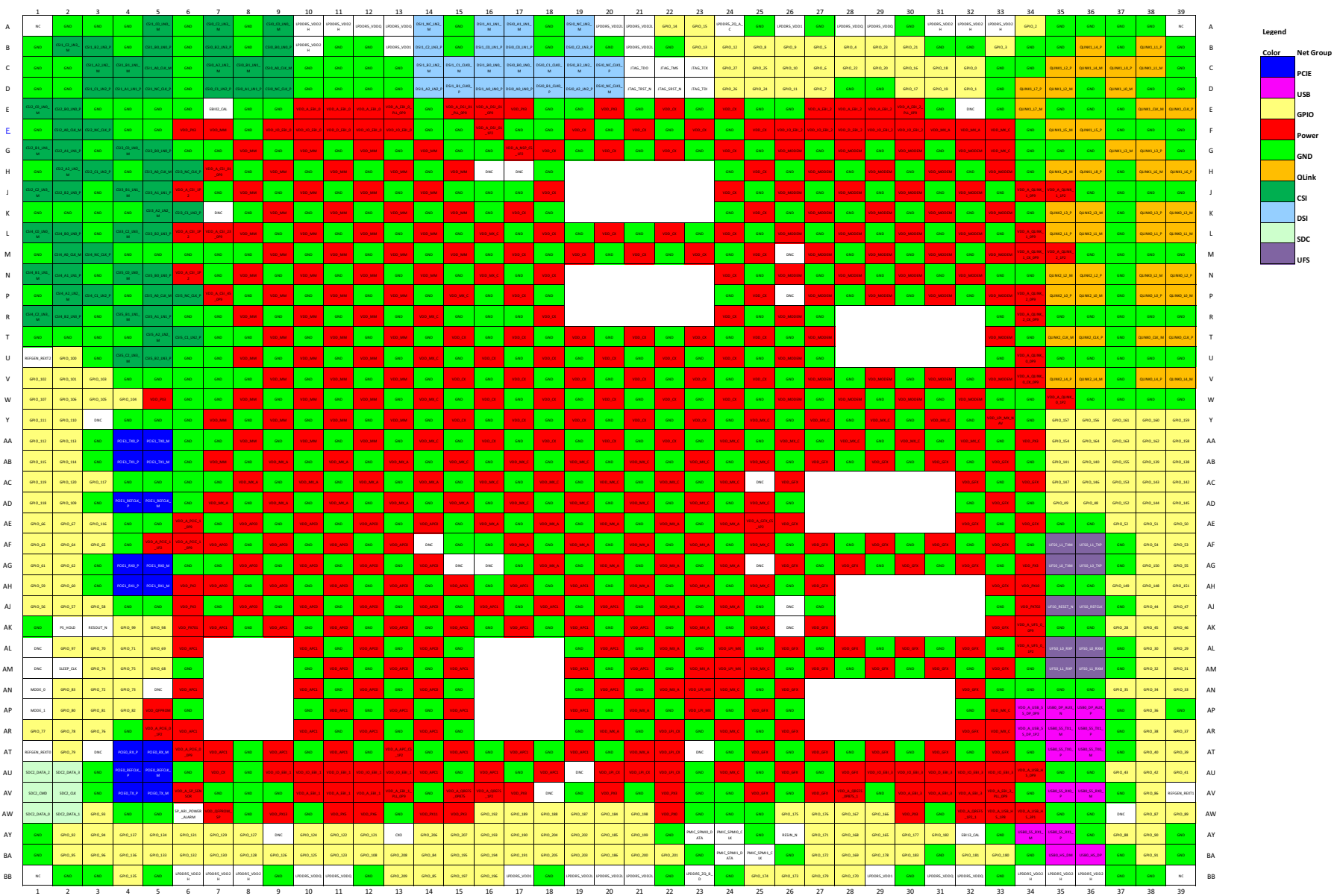


Figure 2-2 SM8450 bottom pin assignments (top view)

2.2.2 Pin descriptions: MSM bottom

The bottom pins are described in [Table 2.2](#) through [Table 2-4](#).

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
D9	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - positive MIPI CSI 0 (C-PHY), no connect
C9	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - minus MIPI CSI 0 (C-PHY), trio lane 0 – A
B9	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - positive MIPI CSI 0 (C-PHY), trio lane 0 – B
A9	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - minus MIPI CSI 0 (C-PHY), trio lane 0 – C
D8	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - positive MIPI CSI 0 (C-PHY), trio lane 1 – A
C8	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - minus MIPI CSI 0 (C-PHY), trio lane 1 – B
D7	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - positive MIPI CSI 0 (C-PHY), trio lane 1 – C
C7	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - minus MIPI CSI 0 (C-PHY), trio lane 2 – A
B7	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - positive MIPI CSI 0 (C-PHY), trio lane 2 – B
A7	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - minus MIPI CSI 0 (C-PHY), trio lane 2 – C
D5	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - positive MIPI CSI 1 (C-PHY), no connect
C5	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - minus MIPI CSI 1 (C-PHY), trio lane 0 – A
B5	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - positive MIPI CSI 1 (C-PHY), trio lane 0 – B
A5	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - minus MIPI CSI 1 (C-PHY), trio lane 0 – C
D4	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - positive MIPI CSI 1 (C-PHY), trio lane 1 – A
C4	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - minus MIPI CSI 1 (C-PHY), trio lane 1 – B
D3	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - positive MIPI CSI 1 (C-PHY), trio lane 1 – C
C3	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - minus MIPI CSI 1 (C-PHY), trio lane 2 – A
B3	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - positive MIPI CSI 1 (C-PHY), trio lane 2 – B
B2	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - minus MIPI CSI 1 (C-PHY), trio lane 2 – C

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
F3	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - positive MIPI CSI 2 (C-PHY), no connect
F2	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - minus MIPI CSI 2 (C-PHY), trio lane 0 – A
E2	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - positive MIPI CSI 2 (C-PHY), trio lane 0 – B
E1	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - minus MIPI CSI 2 (C-PHY), trio lane 0 – C
G2	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - positive MIPI CSI 2 (C-PHY), trio lane 1 – A
G1	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - minus MIPI CSI 2 (C-PHY), trio lane 1 – B
H3	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - positive MIPI CSI 2 (C-PHY), trio lane 1 – C
H2	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - minus MIPI CSI 2 (C-PHY), trio lane 2 – A
J2	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - positive MIPI CSI 2 (C-PHY), trio lane 2 – B
J1	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - minus MIPI CSI 2 (C-PHY), trio lane 2 – C
H6	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - positive MIPI CSI 3 (C-PHY), no connect
H5	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - minus MIPI CSI 3 (C-PHY), trio lane 0 – A
G5	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - positive MIPI CSI 3 (C-PHY), trio lane 0 – B
G4	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - minus MIPI CSI 3 (C-PHY), trio lane 0 – C
J5	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - positive MIPI CSI 3 (C-PHY), trio lane 1 – A
J4	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - minus MIPI CSI 3 (C-PHY), trio lane 1 – B
K6	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - positive MIPI CSI 3 (C-PHY), trio lane 1 – C
K5	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - minus MIPI CSI 3 (C-PHY), trio lane 2 – A
L5	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - positive MIPI CSI 3 (C-PHY), trio lane 2 – B
L4	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - minus MIPI CSI 3 (C-PHY), trio lane 2 – C
M3	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - positive MIPI CSI 4 (C-PHY), no connect
M2	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - minus MIPI CSI 4 (C-PHY), trio lane 0 – A

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
L2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - positive MIPI CSI 4 (C-PHY), trio lane 0 - B
L1	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - minus MIPI CSI 4 (C-PHY), trio lane 0 - C
N2	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - positive MIPI CSI 4 (C-PHY), trio lane 1 - A
N1	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - minus MIPI CSI 4 (C-PHY), trio lane 1 - B
P3	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 - positive MIPI CSI 4 (CPHY), trio lane 1 - C
P2	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 - minus MIPI CSI 4 (C-PHY), trio lane 2 - A
R2	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - positive MIPI CSI 4 (C-PHY), trio lane 2 - B
R1	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - minus MIPI CSI 4 (C-PHY), trio lane 2 - C
P6	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - positive MIPI CSI 5 (C-PHY), no connect
P5	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - minus MIPI CSI 5 (C-PHY), trio lane 0 - A
N5	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - positive MIPI CSI 5 (C-PHY), trio lane 0 - B
N4	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - minus MIPI CSI 5 (C-PHY), trio lane 0 - C
R5	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - positive MIPI CSI 5 (C-PHY), trio lane 1 - A
R4	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - minus MIPI CSI 5 (C-PHY), trio lane 1 - B
T6	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - positive MIPI CSI 5 (C-PHY), trio lane 1 - C
T5	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - minus MIPI CSI 5 (C-PHY), trio lane 2 - A
U5	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - positive MIPI CSI 5 (C-PHY), trio lane 2 - B
U4	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - minus MIPI CSI 5 (C-PHY), trio lane 2 - C
E7	EBI02_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI02_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
AY32	EBI13_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI13_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
A24	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	AI	ZQ calibration reference: The ZQ_A_C pin should be connected to VDDQ (S3H/PM8450) through a 240 Ω ±1% resistor. See LPDDR5 specification.

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
BB23	LPDDR5_ZQ_B_D	LPDDR5_VDDQ	AI	ZQ calibration reference: The ZQ_B_D pin should be connected to VDDQ (S3H/PM8450) through a 240 Ω \pm 1% resistor. See LPDDR5 specification.
D17	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - positive MIPI DSI 0 (C-PHY), trio lane 0 - A
C17	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - minus MIPI DSI 0 (C-PHY), trio lane 0 - B
B17	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - positive MIPI DSI 0 (C-PHY), trio lane 0 - C
A17	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - minus MIPI DSI 0 (C-PHY), trio lane 1 - A
D18	DSI0_B1_CLK0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - positive MIPI DSI 0 (C-PHY), trio lane 1 - B
C18	DSI0_C1_CLK0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - minus MIPI DSI 0 (C-PHY), trio lane 1 - C
D19	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - positive MIPI DSI 0 (C-PHY), trio lane 2 - A
C19	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - minus MIPI DSI 0 (C-PHY), trio lane 2 - B
B19	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - positive MIPI DSI 0 (C-PHY), trio lane 2 - C
A19	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - minus MIPI DSI 0 (C-PHY), NC
C20	DSI0_NC_CLK1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - positive MIPI DSI 0 (C-PHY), NC
D20	DSI0_NC_CLK1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - minus MIPI DSI 0 (C-PHY), NC
D16	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - positive MIPI DSI 1 (C-PHY), trio lane 0 - A
C16	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - minus MIPI DSI 1 (C-PHY), trio lane 0 - B
B16	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - positive MIPI DSI 1 (C-PHY), trio lane 0 - C
A16	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - minus MIPI DSI 1 (C-PHY), trio lane 1 - A
D15	DSI1_B1_CLK0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0 - positive MIPI DSI 1 (C-PHY), trio lane 1 - B
C15	DSI1_C1_CLK0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0 - minus MIPI DSI 1 (C-PHY), trio lane 1 - C
D14	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - positive MIPI DSI 1 (C-PHY), trio lane 2 - A
C14	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - minus MIPI DSI 1 (C-PHY), trio lane 2 - B

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
B14	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - positive MIPI DSI 1 (C-PHY), trio lane 2 – C
A14	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - minus MIPI DSI 1 (C-PHY), NC
D22	JTAG_SRST_N	PX3	DISH-PU	JTAG reset for debug
C23	JTAG_TCK	PX3	DIS-PU	JTAG clock input
D23	JTAG_TDI	PX3	DIS-PU	JTAG data input
C21	JTAG_TDO	PX3	DO-Z	JTAG data output
C22	JTAG_TMS	PX3	DI-PU:npdpk	JTAG mode select input
D21	JTAG_TRST_N	PX3	DI-PD:npukp	JTAG reset
AU5	PCIE0_REFCLK_M	-	AO	PCIe 0 Gen 3 reference clock - minus
AU4	PCIE0_REFCLK_P	-	AO	PCIe 0 Gen 3 reference clock - plus
AT5	PCIE0_RX_M	-	AI	PCIe 0 Gen 3 receive - minus
AT4	PCIE0_RX_P	-	AI	PCIe 0 Gen 3 receive - plus
AV5	PCIE0_TX_M	-	AO	PCIe 0 Gen 3 transmit - minus
AV4	PCIE0_TX_P	-	AO	PCIe 0 Gen 3 transmit - plus
AD5	PCIE1_REFCLK_M	-	AO	PCIe 1 Gen 3 reference clock - minus
AD4	PCIE1_REFCLK_P	-	AO	PCIe 1 Gen 3 reference clock - plus
AG5	PCIE1_RX0_M	-	AI	PCIe 1 Gen 3 receive - minus
AG4	PCIE1_RX0_P	-	AI	PCIe 1 Gen 3 receive - plus
AH5	PCIE1_RX1_M	-	AI	PCIe 1 Gen 3 receive - minus
AH4	PCIE1_RX1_P	-	AI	PCIe 1 Gen 3 receive - plus
AA5	PCIE1_TX0_M	-	AO	PCIe 1 Gen 3 transmit - minus
AA4	PCIE1_TX0_P	-	AO	PCIe 1 Gen 3 transmit - plus
AB5	PCIE1_TX1_M	-	AO	PCIe 1 Gen 3 transmit - minus
AB4	PCIE1_TX1_P	-	AO	PCIe 1 Gen 3 transmit - plus
T38	QLINK0_CLK_M	-	AI, AO	QLink0 clock - minus
T39	QLINK0_CLK_P	-	AI, AO	QLink0 clock - positive
N38	QLINK0_L2_M	-	AI, AO	QLink0 lane 2 - minus
N39	QLINK0_L2_P	-	AI, AO	QLink0 lane 2 - positive
K39	QLINK0_L3_M	-	AI, AO	QLink0 lane 3 - minus
K38	QLINK0_L3_P	-	AI, AO	QLink0 lane 3 - positive
V39	QLINK0_L4_M	-	AI, AO	QLink0 lane 4 - minus
V38	QLINK0_L4_P	-	AI, AO	QLink0 lane 4 - positive
P39	QLINK0_L0_M	-	AI, AO	QLink0 lane 0 - minus
P38	QLINK0_L0_P	-	AI, AO	QLink0 lane 0 - positive
L39	QLINK0_L1_M	-	AI, AO	QLink0 lane 1 - minus
L38	QLINK0_L1_P	-	AI, AO	QLink0 lane 1 - positive
E38	QLINK1_CLK_M	-	AI, AO	QLink1 clock - minus
E39	QLINK1_CLK_P	-	AI, AO	QLink1 clock - positive

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
C36	QLINK1_L4_M	-	AI, AO	QLink1 lane 4 - minus
B36	QLINK1_L4_P	-	AI, AO	QLink1 lane 4 - positive
E34	QLINK1_L7_M	-	AI, AO	QLink1 lane 7 - minus
D34	QLINK1_L7_P	-	AI, AO	QLink1 lane 7 - positive
F35	QLINK1_L5_M	-	AI, AO	QLink1 lane 5 - minus
F36	QLINK1_L5_P	-	AI, AO	QLink1 lane 5 - positive
H38	QLINK1_L6_M	-	AI, AO	QLink1 lane 6 - minus
H39	QLINK1_L6_P	-	AI, AO	QLink1 lane 6 - positive
H35	QLINK1_L8_M	-	AI, AO	QLink1 lane 8 - minus
H36	QLINK1_L8_P	-	AI, AO	QLink1 lane 8 - positive
D37	QLINK1_L0_M	-	AI, AO	QLink1 lane 0 - minus
C37	QLINK1_L0_P	-	AI, AO	QLink1 lane 0 - positive
D35	QLINK1_L2_M	-	AI, AO	QLink1 lane 2 - minus
C35	QLINK1_L2_P	-	AI, AO	QLink1 lane 2 - positive
C38	QLINK1_L1_M	-	AI, AO	QLink1 lane 1 - minus
B38	QLINK1_L1_P	-	AI, AO	QLink1 lane 1 - positive
G37	QLINK1_L3_M	-	AI, AO	QLink1 lane 3 - minus
G38	QLINK1_L3_P	-	AI, AO	QLink1 lane 3 - positive
T35	QLINK2_CLK_M	-	AI, AO	QLink2 clock - minus
T36	QLINK2_CLK_P	-	AI, AO	QLink2 clock - positive
N35	QLINK2_L2_M	-	AI, AO	QLink2 lane 2 - minus
N36	QLINK2_L2_P	-	AI, AO	QLink2 lane 2 - positive
K36	QLINK2_L3_M	-	AI, AO	QLink2 lane 3 - minus
K35	QLINK2_L3_P	-	AI, AO	QLink2 lane 3 - positive
V36	QLINK2_L4_M	-	AI, AO	QLink2 lane 4 - minus
V35	QLINK2_L4_P	-	AI, AO	QLink2 lane 4 - positive
P36	QLINK2_L0_M	-	AI, AO	QLink2 lane 0 - minus
P35	QLINK2_L0_P	-	AI, AO	QLink2 lane 0 - positive
L36	QLINK2_L1_M	-	AI, AO	QLink2 lane 1 - minus
L35	QLINK2_L1_P	-	AI, AO	QLink2 lane 1 - positive
AV2	SDC2_CLK	PX2	DO	Secure digital controller 2 clock
AV1	SDC2_CMD	PX2	B	Secure digital controller 2 command
AW1	SDC2_DATA_0	PX2	B	Secure digital controller 2 data bit 0
AW2	SDC2_DATA_1	PX2	B	Secure digital controller 2 data bit 1
AU1	SDC2_DATA_2	PX2	B	Secure digital controller 2 data bit 2
AU2	SDC2_DATA_3	PX2	B	Secure digital controller 2 data bit 3
BA25	PMIC_SPMI1_CLK	PX0	DO	Slave and PBUS interface 1 for PMICs – clock
BA24	PMIC_SPMI1_DATA	PX0	BH-PD:nppukp	Slave and PBUS interface 1 for PMICs – data
AY24	PMIC_SPMI0_CLK	PX0	DO	Slave and PBUS interface 0 for PMICs – clock

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
AY23	PMIC_SPMIO_DATA	PX0	BH-PD:nppukp	Slave and PBUS interface 0 for PMICs – data
AY13	CXO	PX11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
AN1	MODE_0	PX3	DI-S PD	Mode control bit 0 – unconnected for native mode
AP1	MODE_1	PX3	DI-S PD	Mode control bit 1 – unconnected for native mode
AK2	PS_HOLD	PX3	DO	Power-supply hold signal to PMIC
AT1	REFGEN_REXT0	-	AI, AO	Reference Voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
AV39	REFGEN_REXT1	-	AI, AO	Reference Voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
U1	REFGEN_REXT2	-	AI, AO	Reference Voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
AY26	RESIN_N	PX0	DI	Reset input
AK3	RESOUT_N	PX3	DO	Reset output
AM2	SLEEP_CLK	PX3	DI	Sleep clock
AW6	SP_ARI_POWER_ALARM	PX13	DI	Power alarm
AL36	UFS0_L0_RXM	-	AI	UFS 0 lane 0 receive - minus
AL35	UFS0_L0_RXP	-	AI	UFS 0 lane 0 receive - plus
AG35	UFS0_L0_TXM	-	AO	UFS 0 lane 0 transmit - minus
AG36	UFS0_L0_TXP	-	AO	UFS 0 lane 0 transmit - plus
AM36	UFS0_L1_RXM	-	AI	UFS 0 lane 1 receive - minus
AM35	UFS0_L1_RXP	-	AI	UFS 0 lane 1 receive - plus
AF35	UFS0_L1_TXM	-	AO	UFS 0 lane 1 transmit - minus
AF36	UFS0_L1_TXP	-	AO	UFS 0 lane 1 transmit - plus
AJ36	UFS0_REFCLK	PX10	DO	UFS 0 reference clock
AJ35	UFS0_RESET_N	PX10	DO	UFS reset
AP35	USB0_DP_AUX_N	-	AI, AO	USB 0 DisplayPort aux negative
AP36	USB0_DP_AUX_P	-	AI, AO	USB 0 DisplayPort aux - plus
BA35	USB0_HS_DM	-	AI, AO	USB 0 high-speed data - minus
BA36	USB0_HS_DP	-	AI, AO	USB 0 high-speed data - plus
AV36	USB0_SS_RX0_M	-	AI	USB super-speed receive 0 - minus
AV35	USB0_SS_RX0_P	-	AI	USB super-speed receive 0 - plus
AY34	USB0_SS_RX1_M	-	AI	USB super-speed receive 0 - minus
AY35	USB0_SS_RX1_P	-	AI	USB super-speed receive 0 - plus
AT36	USB0_SS_TX0_M	-	AO	USB super-speed transmit 0 - minus
AT35	USB0_SS_TX0_P	-	AO	USB super-speed transmit 0 - plus
AR35	USB0_SS_TX1_M	-	AO	USB super-speed transmit 0 - minus
AR36	USB0_SS_TX1_P	-	AO	USB super-speed transmit 0 - plus

1. See [Table 2-1](#) for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See [Table 2-2](#) for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
 - Input versus output
 - Pull-up or pull-down
- External connections
 - Unused inputs
 - Connections to high-impedance (tri-state) outputs
 - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that includes a worksheet for all SM8450 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the pin assignment spreadsheet (80-11140-1A) from the Qualcomm® CreatePoint website.

<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-11140-1A>

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
C32	GPIO_0	QUP_L0[0]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
D32	GPIO_1	QUP_L1[0]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
A34	GPIO_2	QUP_L2[0] QDSS_CTI_TRIG0_OUT_MIRB	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger output 0 B	Y
B33	GPIO_3	QUP_L3[0]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
B28	GPIO_4	QUP_L0[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
B27	GPIO_5	QUP_L1[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
C27	GPIO_6	QUP_L2[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
D27	GPIO_7	QUP_L3[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
B25	GPIO_8	QUP_L0[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
B26	GPIO_9	QUP_L1[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
C26	GPIO_10	QUP_L2[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
D26	GPIO_11	QUP_L3[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
B24	GPIO_12	QUP_L0[3]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
B23	GPIO_13	QUP_L1[3]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
A22	GPIO_14	QUP_L2[3]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
A23	GPIO_15	QUP_L3[3]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
C30	GPIO_16	QUP_L0[4]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
D30	GPIO_17	QUP_L1[4]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
C31	GPIO_18	QUP_L2[4]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
D31	GPIO_19	QUP_L3[4]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
C29	GPIO_20	QUP_L0[6] GP_PDM_MIRB[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 General-purpose PDM output 2 B	N
B30	GPIO_21	QUP_L1[6] GP_PDM_MIRB[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 General-purpose PDM output 1 B	Y
C28	GPIO_22	QUP_L2[6] GP_PDM_MIRB[0]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 General-purpose PDM output 0 B	N
B29	GPIO_23	QUP_L3[6]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
D25	GPIO_24	QUP_L0[7] QUP_L4_6_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
C25	GPIO_25	QUP_L1[7] QUP_L5_6_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	N
D24	GPIO_26	QUP_L2[7] QUP_L6_6_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
C24	GPIO_27	QUP_L3[7]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AK37	GPIO_28	QUP_L0[8] IBI_I3C_QUP8_SDA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP8 In-Band interrupt I3C SDA	Y
AL39	GPIO_29	QUP_L1[8] IBI_I3C_QUP8_SCL	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP8 In-Band interrupt I3C SCL	N
AL38	GPIO_30	QUP_L2[8]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AM39	GPIO_31	QUP_L3[8]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AM38	GPIO_32	QUP_L0[9] IBI_I3C_QUP9_SDA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP9 In-Band interrupt I3C SDA	Y
AN39	GPIO_33	QUP_L1[9] IBI_I3C_QUP9_SCL	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP9 In-Band interrupt I3C SCL	N
AN38	GPIO_34	QUP_L2[9]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AN37	GPIO_35	QUP_L3[9]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AP38	GPIO_36	QUP_L0[10]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AR39	GPIO_37	QUP_L1[10]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AR38	GPIO_38	QUP_L2[10]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AT39	GPIO_39	QUP_L3[10]	PX702	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AT38	GPIO_40	QUP_L0[11] QUP_L4_10_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
AU39	GPIO_41	QUP_L1[11] QUP_L5_10_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
AU38	GPIO_42	QUP_L2[11] QUP_L6_10_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	N
AU37	GPIO_43	QUP_L3[11]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AJ38	GPIO_44	QUP_L0[12]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AK38	GPIO_45	QUP_L1[12]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AK39	GPIO_46	QUP_L2[12] MDP_VSYNC_S_MIRB	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 MDP vertical sync – secondary B	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AJ39	GPIO_47	QUP_L3[12] DP_HOT_PLUG_DETECT MDP_VSYNC_P_MIRB FORCED_USB_BOOT	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 DisplayPort hot plug detect MDP vertical sync – primary B Forced USB boot	Y
AD36	GPIO_48	QUP_L0[13] QSPI_DATA[2] SDC4_DATA[2]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI data Secure digital controller 4 data bit [2]	N
AD35	GPIO_49	QUP_L1[13] QSPI_DATA[3] SDC4_DATA[3]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI data Secure digital controller 4 data bit [3]	N
AE39	GPIO_50	QUP_L2[13] QSPI_CLK SDC4_CLK	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad SPI clock Secure digital controller 4 clock	Y
AE38	GPIO_51	QUP_L3[13] QSPI_CS_N_1 SDC4_CMD	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI chip select 1 Secure digital controller 4 command	Y
AE37	GPIO_52	QUP_L0[14] QSPI_DATA[0] SDC4_DATA[0]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI data Secure digital controller 4 data bit [0]	N
AF39	GPIO_53	QUP_L1[14] QSPI_DATA[1] SDC4_DATA[1] GP_MN	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI data Secure digital controller 4 data bit [1] General-purpose M/N:D counter output	N
AF38	GPIO_54	QUP_L2[14] QSPI_CS_N_0	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 Quad-SPI chip select 0	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AG39	GPIO_55	QUP_L3[14]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AJ1	GPIO_56	QUP_L0[15] IBI_I3C_QUP15_SDA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP15 In-Band interrupt I3C SDA	Y
AJ2	GPIO_57	QUP_L1[15] IBI_I3C_QUP15_SCL	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP15 In-Band interrupt I3C SCL	N
AJ3	GPIO_58	QUP_L2[15] QUP_L4_18_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	N
AH1	GPIO_59	QUP_L3[15] QUP_L5_18_CS BOOT_CONFIG[4]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3 Boot configuration bit 4	Y
AH2	GPIO_60	QUP_L0[16] IBI_I3C_QUP16_SDA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP16 In-Band interrupt I3C SDA	Y
AG1	GPIO_61	QUP_L1[16] IBI_I3C_QUP16_SCL	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QUP16 In-Band interrupt I3C SCL	N
AG2	GPIO_62	QUP_L2[16] QUP_L6_18_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
AF1	GPIO_63	QUP_L3[16] QUP_L4_19_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
AF2	GPIO_64	QUP_L0[17]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AF3	GPIO_65	QUP_L1[17]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AE1	GPIO_66	QUP_L2[17] QUP_L5_19_CS	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3	Y
AE2	GPIO_67	QUP_L3[17] QUP_L6_19_CS BOOT_CONFIG[1]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 For QUP assignment/mapping information, see Table 2-3 Boot configuration bit 1	Y
AM5	GPIO_68	QUP_L0[18]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AL5	GPIO_69	QUP_L1[18]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AL3	GPIO_70	QUP_L2[18]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AL4	GPIO_71	QUP_L3[18]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AN3	GPIO_72	QUP_L0[19]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AN4	GPIO_73	QUP_L1[19]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AM3	GPIO_74	QUP_L2[19]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AM4	GPIO_75	QUP_L3[19]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AR3	GPIO_76	QUP_L0[20]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AR1	GPIO_77	QUP_L1[20]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AR2	GPIO_78	QUP_L2[20]	PX3	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	N
AT2	GPIO_79	QUP_L3[20]	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3	Y
AP2	GPIO_80	QUP_L0[21] QDSS_CTI_TRIG0_OUT_MIRA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger output 0 A	Y
AP3	GPIO_81	QUP_L1[21] QDSS_CTI_TRIG1_OUT_MIRA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger output 1 A	Y
AP4	GPIO_82	QUP_L2[21] QDSS_CTI_TRIG1_IN_MIRA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger input 1 A	Y
AN2	GPIO_83	QUP_L3[21] QDSS_CTI_TRIG0_IN_MIRA	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger input 0 A	Y
BA14	GPIO_84	QUP_L2[5] QDSS_CTI_TRIG0_IN_MIRB	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger input 0 B	Y
BB14	GPIO_85	QUP_L3[5] QDSS_CTI_TRIG1_IN_MIRB	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 QDSS trigger input 1 B	Y
AV38	GPIO_86	MDP_VSYNC_P_MIRA GCC_GP1_CLK_MIRB	PX3	PD:nppukp	Configurable I/O MDP vertical sync – primary A General-purpose Clock 1 B	Y
AW38	GPIO_87	MDP_VSYNC_S_MIRA GCC_GP2_CLK_MIRB	PX3	PD:nppukp	Configurable I/O MDP vertical sync – secondary A General-purpose Clock 2 B	Y
AY37	GPIO_88	MDP_VSYNC_E GCC_GP3_CLK_MIRB	PX3	PD:nppukp	Configurable I/O MDP vertical sync – external General-purpose Clock 3 B	Y
AW39	GPIO_89		PX3	PD:nppukp	Configurable I/O	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AY38	GPIO_90		PX3	PD:nppukp	Configurable I/O	Y
BA38	GPIO_91	USB_PHY_PS	PX3	PD:nppukp	Configurable I/O USB PHY port select: USB CC direction 1.8 V push-pull tri-state output indicating USB Type-C connector orientation (CC1 or CC2 connection)	Y
AY2	GPIO_92	SD_CARD_DET_N	PX3	PD:nppukp	Configurable I/O SD card detect	Y
AW3	GPIO_93	SD_WRITE_PROTECT QDSS_CTI_TRIG1_OUT_MIRB	PX3	PD:nppukp	Configurable I/O Secure digital card write protection QDSS trigger output 1 B	N
AY3	GPIO_94	PCIE0_RST_N	PX3	PD:nppukp	Configurable I/O PCIe reset	N
BA2	GPIO_95	PCIE0_CLKREQN	PX3	PU:nppdkp	Configurable I/O PCIe clock request	Y
BA3	GPIO_96	PCIE0_WAKE_N	PX3	PD:nppukp	Configurable I/O PCIe wake	Y
AL2	GPIO_97	PCIE1_RST_N	PX701	PD:nppukp	Configurable I/O PCIe reset	N
AK5	GPIO_98	PCIE1_CLKREQN	PX701	PU:nppdkp	Configurable I/O PCIe clock request	Y
AK4	GPIO_99	PCIE1_WAKE_N	PX701	PD:nppukp	Configurable I/O PCIe wake	Y
U2	GPIO_100	CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB[0]	PX3	PD:nppukp	Configurable I/O Camera 0 MCLK 19.2 MHz/ 24 MHz QDSS trace data 0 B	N
V2	GPIO_101	CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB[1]	PX3	PD:nppukp	Configurable I/O Camera 1 MCLK 19.2 MHz/ 24 MHz QDSS trace data 1 B	N
V1	GPIO_102	CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB[2]	PX3	PD:nppukp	Configurable I/O Camera 2 MCLK 19.2 MHz/ 24 MHz QDSS trace data 2 B	N
V3	GPIO_103	CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB[3]	PX3	PD:nppukp	Configurable I/O Camera 3 MCLK 19.2 MHz/ 24 MHz QDSS trace data 3 B	N
W4	GPIO_104	CAM_MCLK4 QDSS_GPIO_TRACEDATA_LOCB[4]	PX3	PD:nppukp	Configurable I/O Camera 4 MCLK 19.2 MHz/ 24 MHz QDSS trace data 4 B	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
W3	GPIO_105	CAM_MCLK5 QDSS_GPIO_TRACEDATA_LOCB[5]	PX3	PD:nppukp	Configurable I/O Camera 5 MCLK 19.2 MHz/ 24 MHz QDSS trace data 5 B	N
W2	GPIO_106	CAM_MCLK6 QDSS_GPIO_TRACEDATA_LOCB[11]	PX3	PD:nppukp	Configurable I/O Camera 6 MCLK 19.2 MHz/ 24 MHz QDSS trace data 11 B	N
W1	GPIO_107	CAM_MCLK7 QDSS_GPIO_TRACEDATA_LOCB[12]	PX3	PD:nppukp	Configurable I/O Camera 7 MCLK 19.2 MHz/ 24 MHz QDSS trace data 12 B	N
BA12	GPIO_108	AON_CAM_RESET	PX3	PD:nppukp	Configurable I/O	N
AD2	GPIO_109	CCI_ASYNC_IN0	PX3	PD:nppukp	Configurable I/O Camera control interface async 0	N
Y2	GPIO_110	CCI_I2C_SDA0 QDSS_GPIO_TRACEDATA_LOCB[7]	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 0 serial data QDSS trace data	N
Y1	GPIO_111	CCI_I2C_SCL0 QDSS_GPIO_TRACEDATA_LOCB[8]	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 0 clock QDSS trace data	N
AA1	GPIO_112	CCI_I2C_SDA1 QDSS_GPIO_TRACECLK_LOCB	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 1 serial data QDSS trace clock B	N
AA2	GPIO_113	CCI_I2C_SCL1 QDSS_GPIO_TRACECTL_LOCB	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 1 clock QDSS trace control B	N
AB2	GPIO_114	CCI_I2C_SDA2 QDSS_GPIO_TRACEDATA_LOCB[9]	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 2 serial data QDSS trace data B9	N
AB1	GPIO_115	CCI_I2C_SCL2 QDSS_GPIO_TRACEDATA_LOCB[10]	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 2 clock QDSS trace data	Y
AE3	GPIO_116	CCI_TIMER0	PX3	PD:nppukp	Configurable I/O Camera 0 control interface timer	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AC3	GPIO_117	CCI_TIMER1 QDSS_GPIO_TRACEDATA_LOCB[6]	PX3	PD:nppukp	Configurable I/O Camera 1 control interface timer QDSS trace data B6	Y
AD1	GPIO_118	CCI_TIMER2 QDSS_GPIO_TRACEDATA_LOCB[13]	PX3	PD:nppukp	Configurable I/O Camera 2 control interface timer QDSS trace data B 13	Y
AC1	GPIO_119	CCI_TIMER3 CCI_ASYNC_IN1 QDSS_GPIO_TRACEDATA_LOCB[14]	PX3	PD:nppukp	Configurable I/O Camera 3 control interface timer Camera control interface async 1 QDSS trace data B 14	Y
AC2	GPIO_120	CCI_TIMER4 CCI_ASYNC_IN2 QDSS_GPIO_TRACEDATA_LOCB[15]	PX3	PD:nppukp	Configurable I/O Camera 4 control interface timer Camera control interface async 2 QDSS trace data B 15	N
AY12	GPIO_121	I2S2_SCK	PX3	PD:nppukp	Configurable I/O I2S 2 clock	N
AY11	GPIO_122	I2S2_DATA0	PX3	PD:nppukp	Configurable I/O I2S 2 serial data channel 0	N
BA11	GPIO_123	I2S2_WS	PX3	PD:nppukp	Configurable I/O I2S 2 serial data word select	N
AY10	GPIO_124	I2S2_DATA1 SEC_I2S_MCLK AUDIO_REF_CLK	PX3	PD:nppukp	Configurable I/O I2S 2 serial data channel 1 Secondary I2S master clock Audio reference clock	N
BA10	GPIO_125	PRI_I2S_MCLK	PX3	PD:nppukp	Configurable I/O Primary I2S master clock	N
BA9	GPIO_126	I2S0_SCK GP_PDM_MIRA[0]	PX3	PD:nppukp	Configurable I/O I2S 0 clock General-purpose PDM output 0 A	N
AY8	GPIO_127	I2S0_DATA0 GP_PDM_MIRA[1]	PX3	PD:nppukp	Configurable I/O I2S 0 serial data channel 0 General-purpose PDM output 1 A	N
BA8	GPIO_128	I2S0_DATA1 GP_PDM_MIRA[2]	PX3	PD:nppukp	Configurable I/O I2S 0 serial data channel 1 General-purpose PDM output 2A	N
AY7	GPIO_129	I2S0_WS	PX3	PD:nppukp	Configurable I/O I2S 0 serial data word select	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BA7	GPIO_130	UIM0_DATA	PX5	PD:nppukp	Configurable I/O UIM0 data	N
AY6	GPIO_131	UIM0_CLK	PX5	PD:nppukp	Configurable I/O UIM0 clock	N
BA6	GPIO_132	UIM0_RESET	PX5	PD:nppukp	Configurable I/O UIM0 reset	N
BA5	GPIO_133	UIM0_PRESENT	PX3	PD:nppukp	Configurable I/O UIM0 presence detection	Y
AY5	GPIO_134	UIM1_DATA GCC_GP1_CLK_MIRA	PX6	PD:nppukp	Configurable I/O UIM1 data General-purpose Clock 1 A	N
BB4	GPIO_135	UIM1_CLK GCC_GP2_CLK_MIRA	PX6	PD:nppukp	Configurable I/O UIM1 clock General-purpose Clock 2 A	N
BA4	GPIO_136	UIM1_RESET GCC_GP3_CLK_MIRA	PX6	PD:nppukp	Configurable I/O UIM1 reset General-purpose Clock 3 A	N
AY4	GPIO_137	UIM1_PRESENT	PX3	PD:nppukp	Configurable I/O UIM1 presence detection	Y
AB39	GPIO_138	RFFE0_CLK GRFC0	PX3	PD:nppukp	Configurable I/O RF front end 0 interface clock Generic RF controller bit 0	N
AB38	GPIO_139	RFFE0_DATA GRFC1	PX3	PD:nppukp	Configurable I/O RF front end 0 interface data Generic RF controller bit 1	N
AB36	GPIO_140	RFFE1_CLK GRFC2	PX3	PD:nppukp	Configurable I/O RF front end 1 interface clock Generic RF controller bit 2	N
AB35	GPIO_141	RFFE1_DATA GRFC3	PX3	PD:nppukp	Configurable I/O RF front end 1 interface data Generic RF controller bit 3	N
AC39	GPIO_142	RFFE2_CLK GRFC4	PX3	PD:nppukp	Configurable I/O RF front end 2 interface clock Generic RF controller bit 4	N
AC38	GPIO_143	RFFE2_DATA GRFC5	PX3	PD:nppukp	Configurable I/O RF front end 2 interface data Generic RF controller bit 5	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AD38	GPIO_144	RFFE3_CLK GRFC6	PX3	PD:nppukp	Configurable I/O RF front end 3 interface clock Generic RF controller bit 6	N
AD39	GPIO_145	RFFE3_DATA GRFC7	PX3	PD:nppukp	Configurable I/O RF front end 3 interface data Generic RF controller bit 7	N
AC36	GPIO_146	RFFE4_CLK GRFC8	PX3	PD:nppukp	Configurable I/O RF front end 4 interface clock Generic RF controller bit 8	N
AC35	GPIO_147	RFFE4_DATA GRFC9	PX3	PD:nppukp	Configurable I/O RF front end 4 interface data Generic RF controller bit 9	N
AH38	GPIO_148	WLAN_COEX_UART1_RX	PX3	PD:nppukp	Configurable I/O Interface between WCN6855/6856 and SM8450/SM8450P	Y
AH37	GPIO_149	WLAN_COEX_UART1_TX BOOT_CONFIG[5]	PX3	PD:nppukp	Configurable I/O Interface between WCN6855/6856 and SM8450/SM8450P Boot configuration bit 5	N
AG38	GPIO_150	GRFC10	PX3	PD:nppukp	Configurable I/O Generic RF controller bit 10	Y
AH39	GPIO_151	GRFC11	PX3	PD:nppukp	Configurable I/O Generic RF controller bit 11	N
AD37	GPIO_152	GRFC12	PX3	PD:nppukp	Configurable I/O Generic RF controller bit 12	N
AC37	GPIO_153	GRFC0_MIRA	PX3	PD:nppukp	Configurable I/O Generic RF controller bit	Y
AA35	GPIO_154		PX3	PD:nppukp	Configurable I/O	Y
AB37	GPIO_155		PX3	PD:nppukp	Configurable I/O	Y
Y36	GPIO_156	QLINK0_REQUEST	PX3	PD:nppukp	Configurable I/O QLINK 0 REQUEST for SDR735_0, SDR0_QLINK0_REQ	Y
Y35	GPIO_157	QLINK0_ENABLE	PX3	PD:nppukp	Configurable I/O QLINK 0 ENABLE 0 for SDR735_0, SDR0_QLINK0_EN	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AA39	GPIO_158	QLINK0_WMSS_RESET_N BOOT_CONFIG[2]	PX3	PD:nppukp	Configurable I/O QLINK 0 modem subsystem reset output for SDR735_0, SDR0_QLINK0_WMSS_RESET_N Boot configuration bit 2	N
Y39	GPIO_159	QLINK1_REQUEST	PX3	PD:nppukp	Configurable I/O QLINK 1 REQUEST for SMR546, QLINK1_REQ	Y
Y38	GPIO_160	QLINK1_ENABLE	PX3	PD:nppukp	Configurable I/O QLINK 1 ENABLE for SMR546, QLINK1_EN	N
Y37	GPIO_161	QLINK1_WMSS_RESET_N BOOT_CONFIG[3]	PX3	PD:nppukp	Configurable I/O QLINK 1 modem subsystem reset output for SMR546 WMSS_RESETN pin, QLINK1_WMSS_RESET_N Boot configuration bit 3	N
AA38	GPIO_162	QLINK2_REQUEST	PX3	PD:nppukp	Configurable I/O QLINK 2 REQUEST for SDR735_1, SDR1_QLINK2_REQ	Y
AA37	GPIO_163	QLINK2_ENABLE	PX3	PD:nppukp	Configurable I/O QLINK 2 ENABLE 2 for SDR735_1, SDR1_QLINK2_EN	N
AA36	GPIO_164	QLINK2_WMSS_RESET_N BOOT_CONFIG[0]	PX3	PD:nppukp	Configurable I/O QLINK 2 modem subsystem reset output for SDR735_1, SDR1_QLINK2_WMSS_RESET_N Boot configuration bit 0	N
AY29	GPIO_165	LPASS_0 SWR_TX_CLK LPI_QUA_I2S_SCK	PX3	PD:nppukp	Configurable I/O LPASS I/O 0 SoundWire transmit clock LPI I2S clock	N
AW29	GPIO_166	LPASS_1 SWR_TX_DATA0 LPI_QUA_I2S_WS	PX3	PD:nppukp	Configurable I/O LPASS I/O 1 SoundWire transmit data 0 LPI I2S serial data word select	Y
AW28	GPIO_167	LPASS_2 SWR_TX_DATA1 LPI_QUA_I2S_DATA0	PX3	PD:nppukp	Configurable I/O LPASS I/O 2 SoundWire transmit data 1 LPI I2S serial data channel 0	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AY28	GPIO_168	LPASS_3 SWR_RX_CLK LPI_QUA_I2S_DATA1	PX3	PD:nppukp	Configurable I/O LPASS I/O 3 SoundWire receive clock LPI I2S serial data channel 1	N
BA28	GPIO_169	LPASS_4 SWR_RX_DATA0 LPI_QUA_I2S_DATA2	PX3	PD:nppukp	Configurable I/O LPASS I/O 4 SoundWire receive data 0 LPI I2S serial data channel 2	Y
BB28	GPIO_170	LPASS_5 SWR_RX_DATA1 EXT_MCLK1_C LPI_QUA_I2S_DATA3	PX3	PD:nppukp	Configurable I/O LPASS I/O 5 SoundWire receive data 1 External MCLK 1C LPI I2S serial data channel 3	N
AY27	GPIO_171	LPASS_6 LPI_DMIC1_CLK LPI_I2S1_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 6 DMIC1 clock LPI I2S 1 clock	Y
BA27	GPIO_172	LPASS_7 LPI_DMIC1_DATA LPI_I2S1_WS	PX3	PD:nppukp	Configurable I/O LPASS I/O 7 DMIC1 data LPI I2S 1 serial data word select	Y
BB26	GPIO_173	LPASS_8 LPI_DMIC2_CLK LPI_I2S1_DATA0	PX3	PD:nppukp	Configurable I/O LPASS I/O 8 DMIC2 clock LPI I2S 1 serial data channel 0	N
BB25	GPIO_174	LPASS_9 LPI_DMIC2_DATA LPI_I2S1_DATA1 EXT_MCLK1_B	PX3	PD:nppukp	Configurable I/O LPASS I/O 9 DMIC2 data LPI I2S 1 serial data channel 1 External MCLK 1 B	Y
AW26	GPIO_175	LPASS_10 LPI_I2S2_CLK WSA_SWR_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 10 LPI I2S 2 clock SoundWire clock for WSA	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AW27	GPIO_176	LPASS_11 LPI_I2S2_WS WSA_SWR_DATA	PX3	PD:nppukp	Configurable I/O LPASS I/O 11 LPI I2S 2 serial data serial data word select SoundWire data for WSA	Y
AY30	GPIO_177	LPASS_12 LPI_DMIC3_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 12 DMIC 3 clock	Y
BA29	GPIO_178	LPASS_13 LPI_DMIC3_DATA EXT_MCLK1_A	PX3	PD:nppukp	Configurable I/O LPASS I/O 13 DMIC3 data External MCLK 1 A	N
BB27	GPIO_179	LPASS_14 SWR_TX_DATA2 EXT_MCLK1_D	PX3	PD:nppukp	Configurable I/O LPASS I/O 14 SoundWire transmit data 2 External MCLK 1 D	N
BA33	GPIO_180	LPASS_15 LPI_I2S2_DATA0 WSA2_SWR_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 15 LPI I2S 2 serial data channel 0 SoundWire clock for WSA2	N
BA32	GPIO_181	LPASS_16 LPI_I2S2_DATA1 WSA2_SWR_DATA	PX3	PD:nppukp	Configurable I/O LPASS I/O 16 LPI I2S 2 serial data channel 1 SoundWire data for WSA2	Y
AY31	GPIO_182	LPASS_17 LPI_DMIC4_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 17 DMIC 4 clock	Y
BA30	GPIO_183	LPASS_18 LPI_DMIC4_DATA	PX3	PD:nppukp	Configurable I/O LPASS I/O 18 DMIC4 data	N
AW20	GPIO_184	LPASS_19 LPI_I2S3_CLK SLIMBUS_CLK	PX3	PD:nppukp	Configurable I/O LPASS I/O 19 LPI I2S 3 clock LPASS SLIMbus clock	N
AY20	GPIO_185	LPASS_20 LPI_I2S3_WS SLIMBUS_DATA	PX3	PD:nppukp	Configurable I/O LPASS I/O 20 LPI I2S 3 serial data serial data word select LPASS SLIMbus data	Y

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BA20	GPIO_186	LPASS_21 LPI_I2S3_DATA0	PX3	PD:nppukp	Configurable I/O LPASS I/O 21 LPI I2S 3 serial data channel 0	N
AW19	GPIO_187	LPASS_22 LPI_I2S3_DATA1 EXT_MCLK1_E	PX3	PD:nppukp	Configurable I/O LPASS I/O 22 LPI I2S 3 serial data channel 1 External MCLK 1 E	Y
AW18	GPIO_188	QDSS_GPIO_TRACEDATA_LOCA[0] SSC_0	PX3	PD:nppukp	Configurable I/O QDSS trace data 0 A SSC IO 0	Y
AW17	GPIO_189	QDSS_GPIO_TRACEDATA_LOCA[1] SSC_1	PX3	PD:nppukp	Configurable I/O QDSS trace data 1 A SSC_IO 1	N
AY17	GPIO_190	QDSS_GPIO_TRACEDATA_LOCA[2] SSC_2	PX3	PD:nppukp	Configurable I/O QDSS trace data A 2 SSC IO 2	Y
BA17	GPIO_191	QDSS_GPIO_TRACEDATA_LOCA[3] SSC_3	PX3	PD:nppukp	Configurable I/O QDSS trace data A 3 SSC IO 3	N
AW16	GPIO_192	QDSS_GPIO_TRACEDATA_LOCA[4] SSC_4	PX3	PD:nppukp	Configurable I/O QDSS trace data 4 A SSC_IO 4	Y
AY16	GPIO_193	QDSS_GPIO_TRACEDATA_LOCA[5] SSC_5	PX3	PD:nppukp	Configurable I/O QDSS trace data 5 A SSC_IO 5	N
BA16	GPIO_194	QDSS_GPIO_TRACEDATA_LOCA[6] SSC_6	PX3	PD:nppukp	Configurable I/O QDSS trace data 6 A SSC IO 6	N
BA15	GPIO_195	QDSS_GPIO_TRACEDATA_LOCA[7] SSC_7	PX3	PD:nppukp	Configurable I/O QDSS trace data 7 A SSC_IO 7	Y
BB16	GPIO_196	QDSS_GPIO_TRACECTL_LOCA SSC_8	PX3	PD:nppukp	Configurable I/O QDSS trace control A SSC IO 8	N
BB15	GPIO_197	QDSS_GPIO_TRACECLK_LOCA SSC_9	PX3	PD:nppukp	Configurable I/O QDSS trace clock A SSC IO 9	N

Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics ¹		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AW21	GPIO_198	QDSS_GPIO_TRACEDATA_LOCA[8] SSC_10	PX3	PD:nppukp	Configurable I/O QDSS trace data 8 A SSC IO 10	N
AY21	GPIO_199	QDSS_GPIO_TRACEDATA_LOCA[9] SSC_11	PX3	PD:nppukp	Configurable I/O QDSS trace data 9 A SSC IO 11	N
BA21	GPIO_200	QDSS_GPIO_TRACEDATA_LOCA[10] SSC_12	PX3	PD:nppukp	Configurable I/O QDSS trace data 10 A SSC IO 12	N
BA22	GPIO_201	QDSS_GPIO_TRACEDATA_LOCA[11] SSC_13	PX3	PD:nppukp	Configurable I/O QDSS trace data 11 A SSC IO 13	Y
AY19	GPIO_202	QDSS_GPIO_TRACEDATA_LOCA[12] SSC_14	PX3	PD:nppukp	Configurable I/O QDSS trace data 12 A SSC IO 14	N
BA19	GPIO_203	QDSS_GPIO_TRACEDATA_LOCA[13] SSC_15	PX3	PD:nppukp	Configurable I/O QDSS trace data 13 A SSC IO15	Y
AY18	GPIO_204	QDSS_GPIO_TRACEDATA_LOCA[14] SSC_16	PX3	PD:nppukp	Configurable I/O QDSS trace data 14 A SSC IO 16	N
BA18	GPIO_205	QDSS_GPIO_TRACEDATA_LOCA[15] SSC_17	PX3	PD:nppukp	Configurable I/O QDSS trace data 15 A SSC IO 17	Y
AY14	GPIO_206	QUP_L0[5] SSC_18	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 SSC IO 18	N
AY15	GPIO_207	QUP_L1[5] SSC_19	PX3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-3 SSC IO 19	N
BA13	GPIO_208	CCI_I2C_SDA3 SSC_20	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 3 serial data SSC IO 20	N
BB13	GPIO_209	CCI_I2C_SCL3 SSC_21	PX3	PD:nppukp	Configurable I/O Dedicated camera control interface I2C 3 clock SSC IO 21	N

1. See [Table 2-1](#) for the parameter and acronym definitions.

Table 2-3 QUP lane to GPIO mapping

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I ² C	I3C	SPI ¹	UART	HS-UART
QUP[0]	L0	GPIO_0	SDA		MISO	CTS	
	L1	GPIO_1	SCL		MOSI	RFR	
	L2	GPIO_2			SCLK	TX	
	L3	GPIO_3			CS_0	RX	
QUP[1]	L0	GPIO_4	SDA		MISO	CTS	
	L1	GPIO_5	SCL		MOSI	RFR	
	L2	GPIO_6			SCLK	TX	
	L3	GPIO_7			CS_0	RX	
QUP[2]	L0	GPIO_8	SDA		MISO	CTS	
	L1	GPIO_9	SCL		MOSI	RFR	
	L2	GPIO_10			SCLK	TX	
	L3	GPIO_11			CS_0	RX	
QUP[3]	L0	GPIO_12	SDA		MISO	CTS	
	L1	GPIO_13	SCL		MOSI	RFR	
	L2	GPIO_14			SCLK	TX	
	L3	GPIO_15			CS_0	RX	
QUP[4]	L0	GPIO_16	SDA		MISO	CTS	
	L1	GPIO_17	SCL		MOSI	RFR	
	L2	GPIO_18			SCLK	TX	
	L3	GPIO_19			CS_0	RX	
QUP[5] ²	L0	GPIO_206	SDA		MISO	CTS	
	L1	GPIO_207	SCL		MOSI	RFR	
	L2	GPIO_84			SCLK	TX	
	L3	GPIO_85			CS_0	RX	
QUP[6]	L0	GPIO_20	SDA		MISO	CTS	CTS
	L1	GPIO_21	SCL		MOSI	RFR	RFR
	L2	GPIO_22			SCLK	TX	TX
	L3	GPIO_23			CS_0	RX	RX
	L4	GPIO_24			CS_1		
	L5	GPIO_25			CS_2		
	L6	GPIO_26			CS_3		

Table 2-3 QUP lane to GPIO mapping (cont.)

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I ² C	I ³ C	SPI ¹	UART	HS-UART
QUP[7]	L0	GPIO_24	SDA		MISO	CTS	CTS
	L1	GPIO_25	SCL		MOSI	RFR	RFR
	L2	GPIO_26			SCLK	TX	TX
	L3	GPIO_27			CS_0	RX	RX
QUP[8]	L0	GPIO_28	SDA	SDA	MISO	CTS	
	L1	GPIO_29	SCL	SCL	MOSI	RFR	
	L2	GPIO_30			SCLK	TX	
	L3	GPIO_31			CS_0	RX	
QUP[9]	L0	GPIO_32	SDA	SDA	MISO	CTS	
	L1	GPIO_33	SCL	SCL	MOSI	RFR	
	L2	GPIO_34			SCLK	TX	
	L3	GPIO_35			CS_0	RX	
QUP[10]	L0	GPIO_36	SDA		MISO	CTS	
	L1	GPIO_37	SCL		MOSI	RFR	
	L2	GPIO_38			SCLK	TX	
	L3	GPIO_39			CS_0	RX	
	L4	GPIO_40			CS_1		
	L5	GPIO_41			CS_2		
	L6	GPIO_42			CS_3		
QUP[11]	L0	GPIO_40	SDA		MISO	CTS	
	L1	GPIO_41	SCL		MOSI	RFR	
	L2	GPIO_42			SCLK	TX	
	L3	GPIO_43			CS_0	RX	
QUP[12]	L0	GPIO_44	SDA		MISO	CTS	CTS
	L1	GPIO_45	SCL		MOSI	RFR	RFR
	L2	GPIO_46			SCLK	TX	TX
	L3	GPIO_47			CS_0	RX	RX
QUP[13]	L0	GPIO_48	SDA		MISO	CTS	CTS
	L1	GPIO_49	SCL		MOSI	RFR	RFR
	L2	GPIO_50			SCLK	TX	TX
	L3	GPIO_51			CS_0	RX	RX
QUP[14]	L0	GPIO_52	SDA		MISO	CTS	CTS
	L1	GPIO_53	SCL		MOSI	RFR	RFR
	L2	GPIO_54			SCLK	TX	TX
	L3	GPIO_55			CS_0	RX	RX

Table 2-3 QUP lane to GPIO mapping (cont.)

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I ² C	I ³ C	SPI ¹	UART	HS-UART
QUP[15]	L0	GPIO_56	SDA	SDA	MISO	CTS	
	L1	GPIO_57	SCL	SCL	MOSI	RFR	
	L2	GPIO_58			SCLK	TX	
	L3	GPIO_59			CS_0	RX	
QUP[16]	L0	GPIO_60	SDA	SDA	MISO	CTS	
	L1	GPIO_61	SCL	SCL	MOSI	RFR	
	L2	GPIO_62			SCLK	TX	
	L3	GPIO_63			CS_0	RX	
QUP[17]	L0	GPIO_64	SDA		MISO	CTS	
	L1	GPIO_65	SCL		MOSI	RFR	
	L2	GPIO_66			SCLK	TX	
	L3	GPIO_67			CS_0	RX	
QUP[18]	L0	GPIO_68	SDA		MISO	CTS	
	L1	GPIO_69	SCL		MOSI	RFR	
	L2	GPIO_70			SCLK	TX	
	L3	GPIO_71			CS_0	RX	
	L4	GPIO_58			CS_1		
	L5	GPIO_59			CS_2		
	L6	GPIO_62			CS_3		
QUP[19]	L0	GPIO_72	SDA		MISO	CTS	CTS
	L1	GPIO_73	SCL		MOSI	RFR	RFR
	L2	GPIO_74			SCLK	TX	TX
	L3	GPIO_75			CS_0	RX	RX
	L4	GPIO_63			CS_1		
	L5	GPIO_66			CS_2		
	L6	GPIO_67			CS_3		
QUP[20]	L0	GPIO_76	SDA		MISO	CTS	CTS
	L1	GPIO_77	SCL		MOSI	RFR	RFR
	L2	GPIO_78			SCLK	TX	TX
	L3	GPIO_79			CS_0	RX	RX
QUP[21]	L0	GPIO_80	SDA		MISO	CTS	CTS
	L1	GPIO_81	SCL		MOSI	RFR	RFR
	L2	GPIO_82			SCLK	TX	TX
	L3	GPIO_83			CS_0	RX	RX

1. SM8450 QUP SPI interfaces are master only.

2. QUP[5] SPI interface supports speed up to 25 MHz. All other SPI interfaces support up to 50 MHz.

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins

Pad #	Pad name	Functional description
A1, A39, BB1, BB39	NC	No connect; not connected internally.
AL1, AM1, AF14, AG15, AU19, AV18, AJ26, AK26, K7, P26, M26, AG16, AG25, AC25, H17, H16, AT23, E32, AY9, AN5, AT3, AW37, Y3	DNC	Do not connect; connected internally, do not connect externally.
A2, A3, A4, A6, A8, A15, A18, A25, A27, A30, A35, A36, A37, A38, AA3, AA6, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AB3, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB28, AB30, AB32, AB34, AC4, AC5, AC6, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC33, AD3, AD6, AD8, AD10, AD12, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD32, AD34, AE4, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE33, AE35, AE36, AF4, AF8, AF10, AF12, AF15, AF16, AF18, AF20, AF22, AF24, AF26, AF28, AF30, AF32, AF34, AF37, AG3, AG6, AG7, AG9, AG11, AG13, AG17, AG19, AG21, AG23, AG27, AG29, AG31, AG33, AG37, AH3, AH8, AH10, AH12, AH14, AH16, AH18, AH20, AH22, AH24, AH26, AH35, AH36, AJ4, AJ5, AJ7, AJ9, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ33, AJ37, AK1, AK8, AK10, AK12, AK14, AK16, AK18, AK20, AK22, AK24, AK35, AK36, AL11, AL13, AL15, AL19, AL21, AL23, AL25, AL27, AL29, AL31, AL33, AL37, AM6, AM10, AM12, AM14, AM20, AM22, AM26, AM28, AM30, AM32, AM34, AM37, AN11, AN13, AN15, AN19, AN21, AN25, AN33, AN34, AN35, AN36, AP6, AP10, AP12, AP14, AP20, AP22, AP24, AP26, AP32, AP37, AP39, AR4, AR11, AR13, AR15, AR19, AR21, AR23, AR25, AR37, AT8, AT10, AT12, AT14, AT16, AT18, AT20, AT24, AT26, AT28, AT30, AT32, AT34, AT37, AU3, AU6, AU8, AU15, AU17, AU23, AU25, AU27, AU35, AU36, AV3, AV7, AV8, AV9, AV14, AV19, AV21, AV23, AV24, AV26, AV29, AV34, AV37, AW4, AW5, AW8, AW10, AW13, AW23, AW24, AW25, AW31, AW35, AW36, AY1, AY22, AY25, AY33, AY36, AY39, B1, B4, B6, B8, B11, B12, B15, B18, B20, B22, B31, B32, B34, B35, B37, B39, BA1, BA23, BA26, BA31, BA34, BA37, BA39, BB2, BB3, BB5, BB9, BB12, BB18, BB22, BB24, BB30, BB33, BB37, BB38, C1, C2, C6, C10, C11, C12, C13, C33, C34, C39, D1, D2, D6, D10, D11, D12, D13, D28, D29, D33, D36, D38, D39, E3, E4, E5, E6, E8, E9, E14, E18, E19, E21, E23, E25, E26, E31, E33, E35, E36, E37, F1, F4, F5, F8, F14, F15, F17, F18, F20, F22, F24, F34, F37, F38, F39, G3, G6, G7, G9, G11, G13, G15, G16, G19, G21, G23, G25, G27, G29, G31, G34, G35, G36, G39, H1, H4, H8, H10, H12, H14, H18, H24, H26, H28, H30, H32, H34, H37, J3, J7, J9, J11, J13, J15, J16, J17, J25, J27, J29, J31, J33, J36, J37, J38, J39, K1, K2, K3, K4, K8, K10, K12, K14, K16, K18, K24, K26, K28, K30, K32, K34, K37, L3, L9, L11, L13, L15, L17, L19, L21, L23, L25, L27, L29, L31, L33, L37, M1, M4, M5, M6, M7, M8, M10, M12, M14, M16, M18, M20, M22, M24, M28, M30, M32, M36, M37, M38, M39, N3, N7, N9, N11, N13, N15, N17, N25, N27, N29, N31, N33, N34, N37, P1, P4, P8, P10, P12, P14, P16, P18, P24, P28, P30, P32, P37, R3, R6, R7, R9, R11, R13, R15, R16, R17, R25, R27, R33, R35, R36, R37, R38, R39, T1, T2, T3, T4, T7, T8, T10, T12, T14, T16, T18, T20, T22, T24, T26, T34, T37, U3, U6, U7, U9, U11, U13, U15, U17, U19, U21, U23, U25, U27, U33, U35, U36, U37, U38, U39, V4, V5, V6, V7, V8, V10, V12, V14, V16, V18, V20, V22, V24, V26, V28, V30, V32, V37, W6, W7, W9, W11, W13, W15, W17, W19, W21, W23, W25, W27, W29, W31, W33, W34, W36, W37, W38, W39, Y4, Y5, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y22, Y24, Y26, Y28, Y30, Y32, Y34	GND	Ground
AE8, AE10, AE12, AE14, AF7, AF9, AF11, AF13, AG8, AG10, AG12, AG14, AH7, AH9, AH11, AH13, AJ8, AJ10, AJ12, AJ14, AK11, AK13, AL12, AL14, AM11, AM13, AN12, AN14	VDD_APC0	Power for the Kryo Silver application processor

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AH15, AH17, AH19, AJ16, AJ18, AJ20, AK7, AK9, AK15, AK17, AK19, AK21, AL6, AL10, AL20, AM15, AM19, AM21, AN6, AN10, AN20, AP11, AP13, AP15, AP19, AR6, AR10, AR12, AR14, AT7, AT9, AT11, AT15, AT17, AT19, AU14, AU16, AU18	VDD_APC1	Power for the Kryo Gold application processor
AT13	VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V circuits
H7	VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits
J6, L6, N6	VDD_A_CSI_1P2	Power for MIPI CSI 1.2 V analog circuits
L7	VDD_A_CSI_23_0P9	Power for MIPI CSI23 0.9 V analog circuits
P7	VDD_A_CSI_45_0P9	Power for MIPI CSI45 0.9 V analog circuits
E16	VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits
F16	VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits
E15	VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V analog circuits
E10, E11, E12	VDD_A_EBI_0	Power for EBI0 PHY analog circuits
E13	VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits
AV10, AV11, AV12	VDD_A_EBI_1	Power for EBI1 PHY analog circuits
AV13	VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits
E27, E28, E29	VDD_A_EBI_2	Power for EBI2 PHY analog circuits
E30	VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits
AV30, AV31, AV32	VDD_A_EBI_3	Power for EBI3 PHY analog circuits
AV33	VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits
AE25	VDD_A_GFX_CS_1P2	Power for GFX Current Sensor 1.2 V analog circuits
G17	VDD_A_NSP_CS_1P2	Power for NSP Current Sensor 1.2 V analog circuits
AT6	VDD_A_PCIE_0_0P9	Power for PCIe0, 0.9 V analog circuits
AR5	VDD_A_PCIE_0_1P2	Power for PCIe0, 1.2 V analog circuits
AE6, AF6	VDD_A_PCIE_1_0P9	Power for PCIe1, 0.9 V analog circuits
AF5	VDD_A_PCIE_1_1P2	Power for PCIe1, 1.2 V analog circuits
U34	VDD_A_QLINK_0_0P9	Power for Qlink 0, 0.9 V analog circuits
W35	VDD_A_QLINK_0_1P2	Power for Qlink 0, 1.2 V analog circuits
V34	VDD_A_QLINK_0_CK_0P9	Power for Qlink 0 clock, 0.9 V analog circuits
J34, L34	VDD_A_QLINK_1_0P9	Power for Qlink 1 0.9 V analog circuits
J35	VDD_A_QLINK_1_1P2	Power for Qlink 1, 1.2 V analog circuits
M34	VDD_A_QLINK_1_CK_0P9	Power for Qlink 1, clock 0.9 V analog circuits
P34	VDD_A_QLINK_2_0P9	Power for Qlink 2, 0.9 V analog circuits
M35	VDD_A_QLINK_2_1P2	Power for Qlink 2, 1.2 V analog circuits
R34	VDD_A_QLINK_2_CK_0P9	Power for Qlink 2, clock 0.9 V analog circuits
AV15	VDD_A_QREFS_0P875	Reference voltage for the QREFS 0.875 V analog circuits

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AV28	VDD_A_QREFS_0P875_1	Reference voltage for the QREFS 0.875 V analog circuits
AV16	VDD_A_QREFS_1P2	Reference voltage for the QREFS 1.2 V analog circuits
AW32	VDD_A_QREFS_1P2_1	Reference voltage for the QREFS 1.2 V analog circuits
AV6	VDD_A_SP_SENSOR	Power for SP sensor analog circuits
AK34	VDD_A_UFS_0_0P9	Power for the UFS 0.9 V analog circuits
AL34	VDD_A_UFS_0_1P2	Power for the UFS 1.2 V analog circuits
AU34	VDD_A_USB_HS_0P9	Power for the USB high-speed 0.9 V analog circuits
AW33	VDD_A_USB_HS_1P8	Power for the USB high-speed 1.8 V analog circuits
AW34	VDD_A_USB_HS_3P1	Power for the USB high-speed 3.1 V analog circuits
AP34	VDD_A_USB_SS_DP_0P9	Power for USB SS and DisplayPort 0.9 V analog circuits
AR34	VDD_A_USB_SS_DP_1P2	Power for USB SS and DisplayPort 1.2 V analog circuits
AA16, AA18, AA20, AA22, AU7, E22, E24, F19, F21, F23, F25, G18, G20, G22, G24, H25, J18, J24, K17, K25, L18, L20, L22, L24, M17, M19, M21, M23, M25, N18, N24, P17, P25, R18, R24, T15, T17, T19, T21, T23, T25, U16, U18, U20, U22, U24, V15, V17, V19, V21, V23, V25, W16, W18, W20, W22, W24, Y15, Y17, Y19, Y21, Y23	VDD_CX	Power for digital core circuits
F11	VDD_D_EBI_0	Power for the EBI_0 digital circuits
AU11	VDD_D_EBI_1	Power for the EBI_1 digital circuits
F28	VDD_D_EBI_2	Power for the EBI_2 digital circuits
AU31	VDD_D_EBI_3	Power for the EBI_3 digital circuits
AB27, AB29, AB31, AB33, AC26, AC32, AC34, AD33, AE26, AE32, AE34, AF27, AF29, AF31, AF33, AG26, AG28, AG30, AG32, AH27, AH33, AK27, AK33, AL26, AL28, AL30, AL32, AM27, AM29, AM31, AM33, AN26, AN32, AP25, AR26, AR32, AT25, AT27, AT29, AT31, AT33, AU26, AU28, AV25, AV27	VDD_GFX	Power for graphics
F9, F10, F12, F13	VDD_IO_EBI_0	Power for the EBI_0 IO circuits
AU9, AU10, AU12, AU13	VDD_IO_EBI_1	Power for the EBI_1 IO circuits
F26, F27, F29, F30	VDD_IO_EBI_2	Power for the EBI_2 IO circuits
AU29, AU30, AU32, AU33	VDD_IO_EBI_3	Power for the EBI_3 IO circuits
AR22, AT22, AU20, AU21, AU22	VDD_LPI_CX	Power for LPI digital core circuits
AL24, AM24, AN23, AP23	VDD_LPI_MX	Power for low-power island memory circuits
Y33	VDD_LPI_MX_NAV	Power for low-power island memory circuits
H9, H11, H13, H15, J8, J10, J12, J14, K9, K11, K13, K15, L8, L10, L12, L14, M9, M11, M13, M15, N8, N10, N12, N14, P9, P11, P13, R8, R10, R12, T9, T11, T13, U8, U10, U12, V9, V11, V13, W8, W10, W12, Y7, Y9, Y11, Y13, AA8, AA10, AA12, AB7, F7, G8, G10, G12, G14	VDD_MM	Power for multimedia subsystem circuits

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
G26, G28, G30, G32, H27, H29, H31, H33, J26, J28, J30, J32, K27, K29, K31, K33, L26, L28, L30, L32, M27, M29, M31, M33, N26, N28, N30, N32, P27, P29, P31, P33, R26, T27, T33, U26, V27, V29, V31, V33, W26, W28, W30, W32	VDD_MODEM	Power for modem circuits
AB9, AB11, AB13, AC8, AC10, AC12, AC14, AD7, AD9, AD11, AD13, AD15, AE16, AE18, AE20, AE22, AE24, AF17, AF19, AF21, AF23, AG18, AG20, AG22, AG24, AH21, AH23, AJ22, AJ24, AK23, AL22, AM23, AN22, AP21, AR20, AT21, F31, F32	VDD_MX_A	Power for on-chip memory
AA14, AA24, AA26, AA28, AA30, AA32, AB15, AB17, AB19, AB21, AB23, AB25, AC16, AC18, AC20, AC22, AC24, AD17, AD19, AD21, AD23, AD25, AF25, AH25, AK25, AM25, AN24, AP33, AR24, AR33, AU24, F33, G33, L16, N16, P15, R14, U14, W14, Y25, Y27, Y29, Y31	VDD_MX_C	Power for on-chip memory
AW22	VDD_PX0	Power for pad group 0
AH34	VDD_PX10	Power for pad group 10
AW14	VDD_PX11	Power for pad group 11
AW9	VDD_PX13	Power for pad group 13
AH6	VDD_PX2	Power for pad group 2
AA34, AG34, AJ6, AV17, AV20, AV22, AW15, AW30, E17, E20, F6, W5	VDD_PX3	Power for pad group 3
AW11	VDD_PX5	Power for pad group 5
AW12	VDD_PX6	Power for pad group 6
AK6	VDD_PX701	Power for pad group 701
AJ34	VDD_PX702	Power for pad group 702
AP5	VDD_QFPROM	Power for programming the QFPROM
AW7	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit
A26, B13, BB17, BB29	LPDDR5_VDD1	Power for PoP DDR memory core – 1.8 V Nom (bottom LPDDR5_VDD1)
BB34, BB35, BB36, A10, A11, A31, A32, A33, B10, BB6, BB7, BB8	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core – 1.05 V Nom (bottom LPDDR5_VDD2H)
A20, A21, B21, BB19, BB20, BB21	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core – 0.9 V Nom (bottom LPDDR5_VDD2L)
A12, A13, A28, A29, BB10, BB11, BB31, BB32	LPDDR5_VDDQ	Power for PoP DDR pads 0.5 V Nom (bottom LPDDR5_VDDQ)

2.3 Pin assignments: MSM top

2.3.1 Pin map: MSM top

The SM8450 is available in the MPSP1518. See [Chapter 4](#) for package details and [Section 2.2](#) for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in [Figure 2-3](#).

The text within [Figure 2-3](#) is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in [Section 2.2.1](#).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28					
M_A	NC	NC	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	NC	NC	M_A				
M_B	NC	EBI_DQ_3	EBI_R0DQ_T_0	GND	EBI_DQ_5	GND	EBI_CS_1	GND	GND	EBI_DQ_11	GND	EBI_R0DQ_T_1	GND	EBI_DQ_9	EBI_DQ_1	GND	EBI_R0DQ_T_0	GND	EBI_DQ_5	GND	EBI_CS_1	GND	GND	EBI_DQ_13	GND	EBI_R0DQ_T_1	EBI_DQ_11	NC	M_B				
M_C	EBI_DQ_1	GND	EBI_R0DQ_C_0	EBI_DMI_0	LPDDR5_VDDQ	EBI_CA_0	EBI_CS_0	EBI_CA_4	EBI_CA_8	LPDDR5_VDDQ	EBI_DMI_1	EBI_R0DQ_C_1	EBI_DQ_11	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI_DQ_3	EBI_R0DQ_C_0	EBI_DMI_0	LPDDR5_VDDQ	EBI_CA_0	EBI_CS_0	EBI_CA_4	EBI_CA_8	LPDDR5_VDDQ	EBI_DMI_1	EBI_R0DQ_C_1	GND	EBI_DQ_9	M_C				
M_D	LPDDR5_VDDQ	EBI_DQ_2	LPDDR5_VDDQ	GND	EBI_DQ_6	GND	EBI_CA_2	EBI_CA_3	GND	EBI_DQ_14	GND	LPDDR5_VDDQ	GND	EBI_DQ_8	EBI_DQ_0	GND	LPDDR5_VDDQ	GND	EBI_DQ_6	GND	EBI_CA_2	EBI_CA_3	GND	EBI_DQ_14	GND	LPDDR5_VDDQ	EBI_DQ_10	LPDDR5_VDDQ	M_D				
M_E	EBI_DQ_0	LPDDR5_VDDQ	EBI_WCK_C_0	EBI_DQ_4	LPDDR5_VDDQ	EBI_CA_1	LPDDR5_VDD2H	LPDDR5_VDD2L	EBI_CA_5	LPDDR5_VDDQ	EBI_DQ_12	EBI_WCK_C_1	EBI_DQ_10	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI_DQ_2	EBI_WCK_C_0	EBI_DQ_4	LPDDR5_VDDQ	EBI_CA_1	LPDDR5_VDD2H	LPDDR5_VDD2L	EBI_CA_5	LPDDR5_VDDQ	EBI_DQ_12	EBI_WCK_C_1	LPDDR5_VDDQ	EBI_DQ_8	M_E				
M_F	GND	GND	EBI_WCK_T_0	GND	EBI_DQ_7	GND	EBI_CA_T	EBI_CA_C	GND	EBI_DQ_15	GND	EBI_WCK_T_1	GND	LPDDR5_ZQ_A_C	SDR_RESET_N	GND	EBI_WCK_T_1	GND	EBI_DQ_7	GND	EBI_CA_T	EBI_CA_C	GND	EBI_DQ_15	GND	EBI_WCK_T_1	GND	GND	M_F				
M_G	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDDQ	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_G				
M_H	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ																			LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_H		
M_J	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	M_J	
M_K	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_K
M_L	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_L
M_M	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_M
M_N	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_N
M_P	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_P
M_R	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_R
M_T	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_T
M_U	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_U
M_V	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_V
M_W	GND	GND	GND	GND																			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	M_W
M_Y	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ																			LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_Y		
M_AA	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_AA				
M_AB	GND	GND	EBI_WCK_T_1	GND	EBI_DQ_15	GND	EBI_CA_C	EBI_CA_T	GND	EBI_DQ_7	GND	EBI_WCK_T_0	GND	RFU	LPDDR5_ZQ_B_D	GND	EBI_WCK_T_1	GND	EBI_DQ_15	GND	EBI_CA_C	EBI_CA_T	GND	EBI_DQ_7	GND	EBI_WCK_T_0	GND	GND	M_AB				
M_AC	EBI_DQ_8	LPDDR5_VDDQ	EBI_WCK_C_1	EBI_DQ_12	LPDDR5_VDDQ	EBI_CA_3	LPDDR5_VDD1	LPDDR5_VDD2H	EBI_CA_3	LPDDR5_VDDQ	EBI_DQ_4	EBI_WCK_C_0	EBI_DQ_2	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI_DQ_10	EBI_WCK_C_1	EBI_DQ_12	LPDDR5_VDDQ	EBI_CA_5	LPDDR5_VDD1	LPDDR5_VDD2H	EBI_CA_3	LPDDR5_VDDQ	EBI_DQ_4	EBI_WCK_C_0	LPDDR5_VDDQ	EBI_DQ_9	M_AC				
M_AD	LPDDR5_VDDQ	EBI_DQ_10	LPDDR5_VDDQ	GND	EBI_DQ_14	GND	EBI_CA_3	EBI_CA_2	GND	EBI_DQ_6	GND	LPDDR5_VDDQ	GND	EBI_DQ_0	EBI_DQ_8	GND	LPDDR5_VDDQ	GND	EBI_DQ_14	GND	EBI_CA_3	EBI_CA_2	GND	EBI_DQ_6	GND	LPDDR5_VDDQ	EBI_DQ_2	LPDDR5_VDDQ	M_AD				
M_AE	EBI_DQ_9	GND	EBI_R0DQ_C_1	EBI_DMI_1	LPDDR5_VDDQ	EBI_CA_6	EBI_CA_4	EBI_CS_0	EBI_CA_0	LPDDR5_VDDQ	EBI_DMI_0	EBI_R0DQ_C_0	EBI_DQ_3	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI_DQ_11	EBI_R0DQ_C_1	EBI_DMI_1	LPDDR5_VDDQ	EBI_CA_6	EBI_CA_4	EBI_CS_0	EBI_CA_0	LPDDR5_VDDQ	EBI_DMI_0	EBI_R0DQ_C_0	GND	EBI_DQ_1	M_AE				
M_AF	NC	EBI_DQ_11	EBI_R0DQ_T_1	GND	EBI_DQ_13	GND	GND	EBI_CS_1	GND	EBI_DQ_5	GND	EBI_R0DQ_T_0	GND	EBI_DQ_1	EBI_DQ_9	GND	EBI_R0DQ_T_1	GND	EBI_DQ_13	GND	GND	EBI_CS_1	GND	EBI_DQ_5	GND	EBI_R0DQ_T_0	EBI_DQ_3	NC	M_AF				
M_AG	NC	NC	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	GND	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	NC	NC	M_AG			

Legend

Color	Net Group
Light Blue	LPDDR5_VDD1
Red	LPDDR5_VDD2H
Yellow	LPDDR5_VDD2L
Orange	LPDDR5_VDDQ
Cyan	EBI
Pink	ZQ_B_D, ZQ_A_C, RESET_N
White	NC, RFU
Green	GND

Figure 2-3 SM8450 top pin LPDDR5 assignments (top view)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in [Table 2-5](#) and [Table 2-6](#).

Table 2-5 MSM top pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
M_F15	DDR_RESET_N	PX1	DO	LPDDR5 reset (shared by EBIs)
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock - negative
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock - positive
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9
M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 - positive
M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 - positive
M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 - negative

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 - negative
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - positive
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - positive
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - negative
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - negative
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0
M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 1
M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5 command/address bit 2
M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 3
M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 4
M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 5
M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock - negative
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock - positive
M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5 chip select 0
M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5 chip select 1
M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR5 data mask for byte 0
M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR5 data mask for byte 1
M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0
M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1
M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10
M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11
M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12
M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13
M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14
M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15
M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2
M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3
M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4
M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5
M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6
M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7
M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8
M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9
M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 - positive
M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 - positive

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 - negative
M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 - negative
M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 - positive
M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 - positive
M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 - negative
M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 - negative
M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5 command/address bit 0
M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5 command/address bit 1
M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5 command/address bit 2
M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5 command/address bit 3
M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5 command/address bit 4
M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5 command/address bit 5
M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5 differential clock - negative
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5 differential clock - positive
M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5 chip select 0
M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5 chip select 1
M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR5 data mask for byte 0
M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR5 data mask for byte 1
M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5 data bit 0
M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5 data bit 1
M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5 data bit 10
M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5 data bit 11
M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5 data bit 12
M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5 data bit 13
M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5 data bit 14
M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5 data bit 15
M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5 data bit 2
M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5 data bit 3
M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5 data bit 4
M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5 data bit 5
M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5 data bit 6
M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5 data bit 7
M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5 data bit 8
M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5 data bit 9
M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 - positive

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 - positive
M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 - negative
M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 - negative
M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 - positive
M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 - positive
M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 - negative
M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 - negative
M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5 command/address bit 0
M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5 command/address bit 1
M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5 command/address bit 2
M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5 command/address bit 3
M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5 command/address bit 4
M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5 command/address bit 5
M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5 differential clock - negative
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5 differential clock - positive
M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5 chip select 0
M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5 chip select 1
M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR5 data mask for byte 0
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR5 data mask for byte 1
M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5 data bit 0
M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5 data bit 1
M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5 data bit 10
M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5 data bit 11
M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5 data bit 12
M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5 data bit 13
M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5 data bit 14
M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5 data bit 15
M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5 data bit 2
M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5 data bit 3
M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5 data bit 4
M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5 data bit 5
M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5 data bit 6
M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5 data bit 7
M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5 data bit 8
M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5 data bit 9

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics ¹		Functional description
		Voltage	Type	
M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 - positive
M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 - positive
M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 - negative
M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 - negative
M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 - positive
M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 - positive
M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 - negative
M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 - negative
M_F14	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	Reference	LPDDR5 ZQ calibration for channels A and C
M_AB15	LPDDR5_ZQ_B_D	LPDDR5_VDDQ	Reference	LPDDR5 ZQ calibration for channels B and D

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-6 MSM top pin descriptions – ground, NC, and power-supply pins

Pad #	Pad name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground
M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally
M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27, M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16	LPDDR5_VDD1	Power for PoP DDR memory core – 1.8 V Nom (top LPDDR5_VDD1)

Table 2-6 MSM top pin descriptions – ground, NC, and power-supply pins (cont.)

Pad #	Pad name	Functional description
M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_A4, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_A8, M_E21, M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_A10, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_A11, M_Y25, M_Y26, M_Y28, M_A18, M_A19, M_A21, M_A25, M_AA1	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core – 1.05 V Nom (top LPDDR5_VDD2H)
M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_A5, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_A9, M_G20, M_G24, M_G26, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core – 0.9 V Nom (top LPDDR5_VDD2L)
M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_A6, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_A12, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_A17, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_A23, M_E27, M_G4, M_G25, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10	LPDDR5_VDDQ	Power for PoP DDR pads 0.5 V Nom (top LPDDR5_VDDQ)
M_AB14	RFU	Reserved

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor	-0.3	1.2485	V
VDD_APC1	Qualcomm Kryo Gold application processor	-0.3	1.2485	V
VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits	-0.3	1.386	V
VDD_A_CSI_01_0P9 VDD_A_CSI_23_0P9 VDD_A_CSI_45_0P9	Power for MIPI CSI 0.9 V analog circuits	-0.3	1.012	V
VDD_A_CSI_1P2	Power for MIPI CSI 1.2 V analog circuits	-0.3	1.386	V
VDD_A_DSI_01_0P9 VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI 0.9 V analog circuits Power for MIPI DSI PLL 0.9 V analog circuits	-0.3	1.012	V
VDD_A_DSI_01_1P2	Power for MIPI DSI 1.2 V analog circuits	-0.3	1.386	V
VDD_A_EBI0 VDD_A_EBI1 VDD_A_EBI2 VDD_A_EBI3 VDD_A_PLL_EBI0 VDD_A_PLL_EBI1 VDD_A_PLL_EBI2 VDD_A_PLL_EBI3	EBI PHY and PLL circuits	-0.3	1.133	V
VDD_A_GFX_CS_1P2	Power for GFX current sensor 1.2 V analog circuits	-0.3	1.386	V
VDD_A_NSP_CS_1P2	Power for NSP current sensor 1.2 V analog circuits	-0.3	1.386	V
VDD_A_PCIE_0_0P9	Power for PCIe0 0.9 V analog circuits	-0.3	1.012	V
VDD_A_PCIE_1_0P9	Power for PCIe1 0.9 V analog circuits	-0.3	1.012	V
VDD_A_PCIE_0_1P2 VDD_A_PCIE_1_1P2	Power for PCIe 1.2 V circuits	-0.3	1.386	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_QLINK_0_0P9 VDD_A_QLINK_2_0P9 VDD_A_QLINK_0_CK_0P9 VDD_A_QLINK_2_CK_0P9	Power for QLINK 0.9 V analog circuits Power for QLINK clock 0.9 V analog circuits	-0.3	1.012	V
VDD_A_QLINK_1_0P9 VDD_A_QLINK_1_CK_0P9	Power for QLINK1 0.9 V analog circuits Power for QLINK1 clock 0.9 V analog circuits	-0.3	1.0538	V
VDD_A_QLINK_0_1P2 VDD_A_QLINK_1_1P2 VDD_A_QLINK_2_1P2	Power for QLINK 1.2 V analog circuits	-0.3	1.386	V
VDD_A_QREFS_0P875 VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875 V analog circuits	-0.3	1.012	V
VDD_A_QREFS_1P2 VDD_A_QREFS_1P2_1	Reference voltage for QREFS 1.2 V analog circuits	-0.3	1.386	V
VDD_A_SP_SENSOR	Power or SP sensor analog circuits	-0.3	1.012	V
VDD_A_UFS_0_0P9	Power for UFS 0.9 V analog circuits	-0.3	1.012	V
VDD_A_UFS_0_1P2	Power for UFS 1.2 V analog circuits	-0.3	1.386	V
VDD_A_USB_HS_0P9	Power for USB high-speed 0.9 V analog circuits	-0.3	1.012	V
VDD_A_USB_HS_1P8	Power for USB high-speed 1.8 V analog circuits	-0.3	2.178	V
VDD_A_USB_HS_3P1	Power for USB high-speed 3.1 V analog circuits	-0.3	3.993	V
VDD_A_USB_SS_DP_0P9	Power for USB super-speed and DisplayPort 0.9 V analog circuits	-0.3	1.056	V
VDD_A_USB_SS_DP_1P2	Power for USB super-speed and DisplayPort 1.2 V analog circuits	-0.3	1.386	V
VDD_CX	Digital core	-0.3	1.2485	V
VDD_D_EBI0 VDD_D_EBI1 VDD_D_EBI2 VDD_D_EBI3	EBI PHY digital circuits	-0.3	1.2485	V
VDD_GFX	Graphics	-0.3	1.133	V
VDD_IO_EBI0 VDD_IO_EBI1 VDD_IO_EBI2 VDD_IO_EBI3	EBI I/O memory circuits	-0.3	0.627	V
VDD_LPI_CX	Power for LPI digital core circuits	-0.3	1.133	V
VDD_LPI_MX VDD_LPI_MX_NAV	Power for LPI memory circuits	-0.3	1.078	V
VDD_MM	Multimedia subsystem circuits	-0.3	1.133	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_MODEM	Modem subsystem	-0.3	1.133	V
VDD_MX_A VDD_MX_C	On-chip memory	-0.3	1.078	V
VDD_PX0	Power for Pad Group 0 - control signals	-0.3	2.145	V
VDD_PX2	Power for Pad Group 2 - SDC2 pads	-0.3	3.52	V
VDD_PX3	Power for Pad Group 3 - most I/O pads	-0.3	2.145	V
VDD_PX5	Power for Pad Group 5 - UIM1 pads	-0.3	3.52	V
VDD_PX6	Power for Pad Group 6 - UIM2 pads	-0.3	3.52	V
VDD_PX10	Power for Pad Group 10 - UFS pads	-0.3	1.419	V
VDD_PX11	Power for Pad Group 11 - CXO pads	-0.3	1.419	V
VDD_PX13	Power for Pad Group 13 - Secure Processor Unit (SPU)	-0.3	2.09	V
VDD_PX701	Power for Pad Group 701 - I/O pads	-0.3	2.145	V
VDD_PX702	Power for Pad Group 702 - I/O pads	-0.3	2.145	V
VDD_QFPROM VDD_QFPROM_SP	Power for programming QFPROM Power for programming QFPROM Secure Processor Unit	-0.3	2.09	V
LPDDR5_VDDQ ¹	Power for PoP LPDDR5 memory IO pads	-0.3	0.627	V
LPDDR5_VDD1 ¹	Power for PoP LPDDR5 memory core	-0.3	2.09	V
LPDDR5_VDD2H ¹	Power for PoP LPDDR5 memory core	–	–	V
LPDDR5_VDD2L ¹	Power for PoP LPDDR5 memory core	–	–	V
T _s	Storage temperature ^{2 3}	-55	150	°C
ESD protection – see Section 7.1 .				
Thermal conditions – see Section 4.5 .				

1. See the LPDDR5 data sheet for the absolute maximum DC ratings for minimum and maximum voltages of VDDQ, VDD1, VDD2H and VDD2L.
2. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
3. For devices shipped in tape and reel, the storage temperature range is [-35°C to +15°C] and relative humidity (RH) < 90%. QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter ¹		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor Active	0.485	1.135	V
VDD_APC1	Qualcomm Kryo Gold application processor Active	0.5	1.135	V
VDD_A_EBI0 VDD_A_EBI1 VDD_A_EBI2 VDD_A_EBI3 VDD_A_PLL_EBI0 VDD_A_PLL_EBI1 VDD_A_PLL_EBI2 VDD_A_PLL_EBI3	EBI PHY and PLL circuits Active	0.64	1.03	V
VDD_CX VDD_D_EBI0 VDD_D_EBI1 VDD_D_EBI2 VDD_D_EBI3	Digital core and EBI PHY digital circuits Active Retention	0.485 0.352	1.135 0.48	V V
VDD_GFX	Graphics Active	0.485	1.03	V
VDD_MM	Multimedia subsystem circuits Active	0.485	1.03	V
VDD_MODEM	Modem subsystem Active	0.485	1.03	V
VDD_MX_A VDD_MX_C	On-chip memory Active Retention	0.695 0.504	0.98 0.68	V V
VDD_LPI_CX	Low power island core Active Retention	0.485 0.352	1.03 0.58	V V
VDD_LPI_MX VDD_LPI_MX_NAV	Low power island memory Active Retention	0.695 0.508	0.98 0.684	V V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-3 Operating conditions for non AVS voltage rails

Parameter ¹		Min	Typ ²	Max	Unit
Power supply voltages					
VDD_A_CSI_01_OP9 VDD_A_CSI_23_OP9 VDD_A_CSI_45_OP9	Power for MIPI CSI 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_CSI_1P2	Power for MIPI CSI 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_DSI_01_OP9 VDD_A_DSI_01_PLL_OP9	Power for MIPI DSI 0.9 V analog circuits Power for MIPI DSI PLL 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_DSI_01_1P2	Power for MIPI DSI 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_PCIE_0_OP9	Power for PCIe0 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_PCIE_1_OP9	Power for PCIe1 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_PCIE_0_1P2 VDD_A_PCIE_1_1P2	Power for PCIe 1.2 V circuits	1.14	1.2	1.26	V
VDD_A_QLINK_0_OP9 VDD_A_QLINK_2_OP9 VDD_A_QLINK_0_CK_OP9 VDD_A_QLINK_2_CK_OP9	Power for QLink0/2 0.9 V analog circuits Power for QLink 0/2clock 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_QLINK_1_OP9 VDD_A_QLINK_1_CK_OP9	Power for QLink1 0.9 V analog circuits Power for QLink1 Clock 0.9 V analog circuits	0.866	0.912	0.958	V
VDD_A_QLINK_0_1P2 VDD_A_QLINK_1_1P2 VDD_A_QLINK_2_1P2	Power for QLink0/1/2 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_UFS_0_OP9	Power for UFS 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_UFS_0_1P2	Power for UFS 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_USB_HS_0P9	Power for USB high-speed 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_USB_HS_1P8	Power for USB high-speed 1.8 V analog circuits	1.62	1.8	1.98	V
VDD_A_USB_HS_3P1	Power for USB high-speed 3.1 V analog circuits	2.97	3.072	3.63	V
VDD_A_USB_SS_DP_OP9	Power for USB super-speed and DisplayPort 0.9 V analog circuits	0.86	0.912	0.96	V
VDD_A_USB_SS_DP_1P2	Power for USB super-speed and DisplayPort 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_QREFS_0P875 VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875 V analog circuits	0.83	0.88	0.92	V
VDD_A_QREFS_1P2 VDD_A_QREFS_1P2_1	Reference voltage for QREFS 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_SP_SENSOR	Power for the SP sensor analog circuit.	0.83	0.88	0.92	V
VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_GFX_CS_1P2	Power for GFX current sensor 1.2 V analog circuits	1.14	1.2	1.26	V

Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter ¹		Min	Typ ²	Max	Unit
Power supply voltages					
VDD_A_NSP_CS_1P2	Power for NSP current sensor 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_IO_EBI	EBI I/O memory circuits LPDDR5 spec range 1 ^{3 5} LPDDR5 spec range 2 ^{4 5}	0.47 0.27	0.5 0.3	0.57 0.37	V
VDD_PX0	Power for Pad Group 0 - control signals	1.7	1.8	1.95	V
VDD_PX2	Power for Pad Group 1 - SDC2 pads	1.7 2.72	1.8 3.0	1.9 3.2	V
VDD_PX3	Power for Pad Group 3 - most I/O pads	1.7	1.8	1.95	V
VDD_PX5	Power for Pad Group 5 - UIM1 pads	1.7 2.72	1.8 3.0	1.9 3.2	V
VDD_PX6	Power for Pad Group 6 - UIM2 pads	1.7 2.72	1.8 3.0	1.9 3.2	V
VDD_PX10	Power for Pad Group 10 - UFS pads	1.12	1.2	1.29	V
VDD_PX11	Power for Pad Group 11 - CXO pad	1.17	1.2	1.29	V
VDD_PX13	Power for Pad Group 13 - Secure Processor Unit (SPU)	1.7	1.8	1.9	V
VDD_PX701	Power for Pad Group 701 - I/O pads	1.7	1.8	1.95	V
VDD_PX702	Power for Pad Group 702 - I/O pads	1.7	1.8	1.95	V
VDD_QFPROM VDD_QFPROM_SP	Power for programming QFPROM Power for programming QFPROM Secure Processor Unit	1.7	1.8	1.9	V
LPDDR5_VDDQ	Power for PoP LPDDR5 memory IO pads LPDDR5 spec range 1 ^{3 5} LPDDR5 spec range 2 ^{4 5}	0.47 0.27	0.5 0.3	0.57 0.37	V
LPDDR5_VDD1	Power for PoP LPDDR5 memory core	1.7	1.8	1.95	V
LPDDR5_VDD2H	Power for PoP LPDDR5 memory core	– ⁶	– ⁶	– ⁶	V
LPDDR5_VDD2L	Power for PoP LPDDR5 memory core	– ⁶	– ⁶	– ⁶	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. LPDDR5 spec range 1 is intended for IO operation with both ODT enabled and disabled.
4. LPDDR5 spec range 1 is intended for IO operation with both ODT disabled
5. For more information, please check LPDDR5 PDN specification defined by JEDEC Solid State Technology Association (JESD209-5B)
6. See the LPDDR5 data sheets for the recommended DC operating conditions (min/typ/max voltages) of VDD2H/VDD2L/VDD1/VDDQ

3.2.1 Thermal conditions

Table 3-4 Thermal conditions

Parameter	Description	Min	Typ	Max	Units
Thermal conditions					
T _J	Device operating junction temperature	T _{ambient} = -30	–	T _{junction} = +95	°C

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8450 Chipset Power Delivery Network Specification* (80-11140-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8450 Linux Android Current Consumption Data Application Note* (80-11140-7).

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM8450 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I²C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-5 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V _{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PX3	VDD_PX3 + 0.3	V
V _{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3	0.35 × VDD_PX3	V
V _{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PX3	VDD_PX3 + 0.3	V
V _{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3	0.3 × VDD_PX3	V
V _{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V _{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I _{IH}	Input high leakage current ¹	–	10	μA

Table 3-5 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
I _{IL}	Input low leakage current ¹	-1	–	μA
I _{OZH}	High-level, tri-state leakage current ¹	–	10	μA
I _{OZL}	Low-level, tri-state leakage current ¹	-1	10	μA
R _{PD}	Pull-down resistance	20K	60K	Ω
R _{PU}	Pull-up resistance	20K	60K	Ω
R _{KP}	Bus keeper resistor	20K	60K	Ω
V _{OH}	High-level output voltage	VDD_PX3 - 0.45	VDD_PX3	V
V _{OL}	Low-level output voltage	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH}, and I_{OZL} values are based on characterization of corner devices over temperature.

Table 3-6 SDC2 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V _{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V _{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V _{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I _{IH}	Input high leakage current	–	–	10	μA
I _{IL}	Input low leakage current	-10	–	–	μA
I _{OZH}	High-level, tri-state leakage current	–	–	10	μA
I _{OZL}	Low-level, tri-state leakage current	-10	–	–	μA
R _{PULL-UP}	Pull-up resistance	10	–	100	kΩ
R _{PULL-DOWN}	Pull-down resistance	10	–	100	kΩ
R _{KEEPER-UP}	Keeper-up resistance	10	–	100	kΩ
R _{KEEPER-DOWN}	Keeper-down resistance	10	–	100	kΩ
V _{OH}	High-level output voltage	0.75 × VDD_PX2	–	VDD_PX2	V
V _{OL}	Low-level output voltage	0.0	–	0.125 × VDD_PX2	V

Table 3-7 SDC2 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V _{IH}	High-level input voltage	1.27	–	2	V
V _{IL}	Low-level input voltage	-0.3	–	0.58	V
V _{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I _{IH}	Input high leakage current	–	–	5	μA
I _{IL}	Input low leakage current	-5	–	–	μA
I _{OZH}	High-level, tri-state leakage current	–	–	5	μA
I _{OZL}	Low-level, tri-state leakage current	-5	–	–	μA

Table 3-7 SDC2 1.8 V mode DC specifications (cont.)

Parameter	Description	Min	Typ	Max	Units
R _{PULL-UP}	Pull-up resistance	10	–	100	kΩ
R _{PULL-DOWN}	Pull-down resistance	10	–	100	kΩ
R _{KEEPER-UP}	Keeper-up resistance	10	–	100	kΩ
R _{KEEPER-DOWN}	Keeper-down resistance	10	–	100	kΩ
V _{OH}	High-level output voltage	1.4	–	–	V
V _{OL}	Low-level output voltage	–	–	0.45	V

Table 3-8 UIM 3 V mode DC specifications (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Units
V _{IH}	High-level input voltage ¹	0.7 × VDD_PXx	–	VDD_PXx + 0.3	V
V _{IL}	Low-level input voltage ¹	-0.3	–	0.2 × VDD_PXx	V
V _{HYS}	Schmitt hysteresis voltage ²	100	–	–	mV
I _{IH}	Input high leakage current	-20	–	20	μA
I _{IL}	Input low leakage current	–	–	1000	μA
I _{OZH}	High-level, tri-state leakage current	–	–	10	μA
I _{OZL}	Low-level, tri-state leakage current	-10	–	–	μA
R _{PULL-UP}	Pull-up resistance	10	–	100	kΩ
R _{PULL-DOWN}	Pull-down resistance	10	–	100	kΩ
R _{KEEPER-UP}	Keeper-up resistance	10	–	100	kΩ
R _{KEEPER-DOWN}	Keeper-down resistance	10	–	100	kΩ
V _{OH}	High-level output voltage ³	0.8 × VDD_PXx	–	VDD_PXx	V
V _{OL}	Low-level output voltage ⁴	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.

2. V_{HYS} is not a required specification for UIM.

3. UIM specifies V_{OH} = 0.8 × VDD_PXx (RST) and 0.7 × VDD_PXx (CLK, I/O). The worst-case V_{OH} is used in this table.

4. UIM specifies V_{OL} = 0.2 × VDD_PXx (RST, CLK) and 0.4 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-9 UIM 1.8 V mode DC specifications (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Units
V _{IH}	High-level input voltage ¹	0.7 × VDD_PXx	–	VDD_PXx + 0.3	V
V _{IL}	Low-level input voltage ¹	-0.3	–	0.2 × VDD_PXx	V
V _{HYS}	Schmitt hysteresis voltage ²	100	–	–	mV
I _{IH}	Input high leakage current	-20	–	20	μA
I _{IL}	Input low leakage current	–	–	1000	μA

Table 3-9 UIM 1.8 V mode DC specifications (VDD_PX5 and VDD_PX6) (cont.)

Parameter	Description	Min	Typ	Max	Units
I _{OZH}	High-level, tri-state leakage current	–	–	5	μA
I _{OZL}	Low-level, tri-state leakage current	-5	–	–	μA
R _{PULL-UP}	Pull-up resistance	10	–	100	kΩ
R _{PULL-DOWN}	Pull-down resistance	10	–	100	kΩ
R _{KEEPER-UP}	Keeper-up resistance	10	–	100	kΩ
R _{KEEPER-DOWN}	Keeper-down resistance	10	–	100	kΩ
V _{OH}	High-level output voltage ³	0.8 × VDD_PXx	–	VDD_PXx	V
V _{OL}	Low-level output voltage ⁴	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UIM.
3. UIM specifies V_{OH} = 0.8 × VDD_PXx (RST) and 0.7 × VDD_PXx (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UIM specifies V_{OL} = 0.2 × VDD_PXx (RST, CLK) and 0.3 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-10 UFS clock DC characteristics (VDD_PX10)

Parameter	Description	Min	Max	Units
V _{OL}	Low-level output voltage	0	0.25 × VDD_PX10	V
V _{OH}	High-level output voltage	0.75 × VDD_PX10	VDD_PX10	V
R _{PULL-UP}	Pull-up resistance	20	–	kΩ
R _{PULL-DOWN}	Pull-down resistance	20	–	kΩ
I _{OZH}	High-level, tri-state leakage current	–	10	μA
I _{OZL}	Low-level, tri-state leakage current	-10	–	μA

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM8450 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in [Section 3.6.2](#).

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in [Figure 3-1](#).






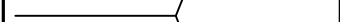

Waveform	Description
	Don't care or bus is driven
	Signal is changing from low to high
	Signal is changing from high to low
	Bus is changing from invalid to valid
	Bus is changing from valid to keeper
	Bus is changing from Hi-Z to valid
	Denotes multiple clock periods

Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
 - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
 - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SM8450 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in [Figure 3-2](#).

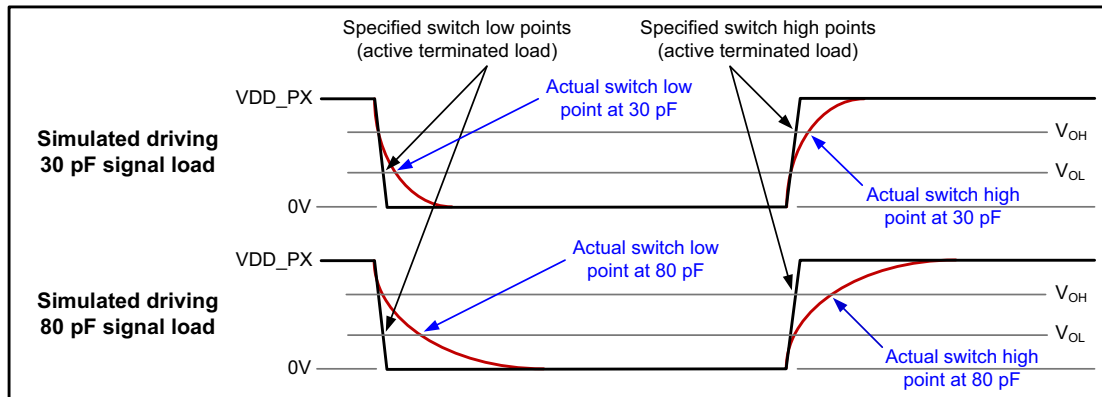


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8450 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SM8450 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DDPX_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH} .

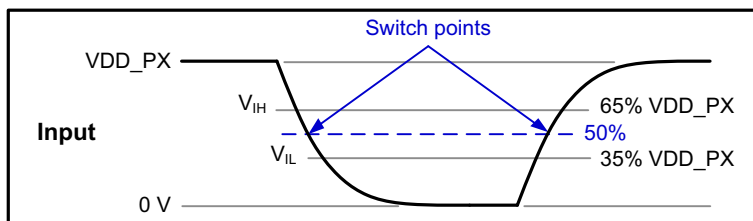


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL} (max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- $V_{OH} \sim V_{DDPX_x} - 50 \text{ mV}$ or more
- $V_{OL} \sim 50 \text{ mV}$ or less

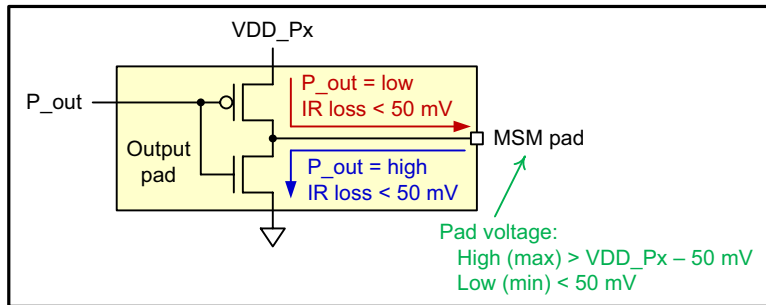


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and $V_{DDPX_x} - 50$ mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at $2/3 \times [V_{OL} \text{ (max)} - 50 \text{ mV}]$, and 1.5 mA or more at $1/3 \times [V_{OL} \text{ (max)} - 50 \text{ mV}]$. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at $1/2 \times [V_{DDPX_x} - 50 \text{ mV} + V_{OH} \text{ (min)}]$.

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (T_{RISE}) and fall time (T_{FALL}) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5 SDRAM memory that is attached to the top of the SM8450 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8450 Recommendations* (80-VP300-18).

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SM8450 device supports up to six D-PHY or C-PHY camera interfaces.

Table 3-11 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
<i>MIPI Alliance Specification for CSI-2 v3.0</i>	Following features are not supported: <ul style="list-style-type: none"> ■ Raw6/7 data formats ■ All DPCM formats ■ LRTE with EPD over DPHY ■ EoTp ■ USL ■ sROI
<i>MIPI Alliance Specification for D-PHY v1.2</i>	None
<i>MIPI Alliance Specification for C-PHY v2.0</i>	Following features are not supported: <ul style="list-style-type: none"> ■ Bidirectional lanes ■ Alternate low power (ALP) mode

3.8.1.1 Camera MLCK

The SM8450 camera master clocks (CAM_MCLK[7:0]) supports 19.2/24 MHz with jitter specification < 400 ps.

3.8.2 Audio support

The SM8450 supports the WCD9380/WCD9385 audio codec IC to provide the system's audio functions. SM8450 audio-related interface options with the WCD include:

- Digital microphone: [Section 3.9.7](#)
- SWR: [Section 3.9.8](#)
- I²S: [Section 3.9.10](#)
- PCM/TDM: [Section 3.9.11](#)
- I²C/I3C: [Section 3.9.13](#)
- SPI: [Section 3.9.14](#)

See the *WCD9380/WCD9385 Audio Codec Device Specification* (80-PL335-1) for performance characteristics.

3.8.3 Display support

The SM8450 device supports up to two D-PHY or C-PHY displays.

Table 3-12 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
<i>MIPI Alliance Specification for Display Serial Interface v1.3.1</i>	Following features are not supported: <ul style="list-style-type: none"> ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission
<i>MIPI Alliance Specification for Display Serial Interface 2 v2.0</i>	Following features are not supported: <ul style="list-style-type: none"> ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission ■ Packed pixel stream, 20-bit YCbCr 4:2:2 format
<i>MIPI Alliance Specification for D-PHY v1.2</i>	None
<i>MIPI Alliance Specification for C-PHY v1.1</i>	None

3.8.4 DMB support

The SM8450 supports an external DMB solution using the following interface options:

- SPI: [Section 3.9.14](#)
- SD: [Section 3.9.1](#)

3.9 Connectivity

The connectivity functions supported by the SM8450 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- Digital microphone PDM interface
- SoundWire (SWR) interface
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I²S) interfaces

- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Touchscreen connections
- Through proper configuration of the 22 QUP ports:
 - Universal asynchronous receiver/transmitter (UART) ports
 - Inter-integrated circuit (I²C) interfaces
 - Serial peripheral interface (SPI) ports
 - Dedicated I²C interfaces for camera (CCI I²C)
 - I3C

Pertinent specifications for these functions are detailed in the following subsections.

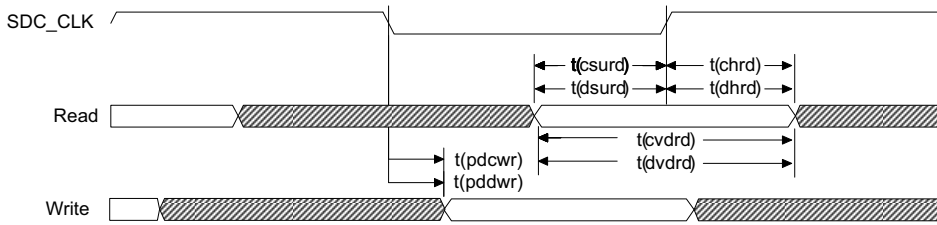
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

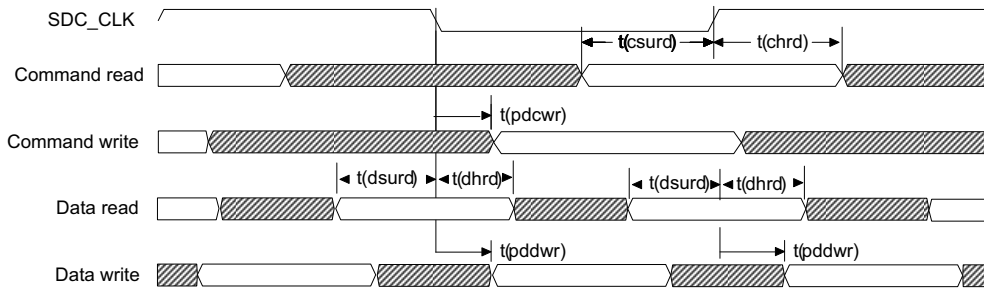
Table 3-13 Supported SD standards and exceptions

Applicable standard	Feature exceptions
<i>Secure Digital: Physical layer Specification version 3.0</i>	None
<i>SDIO Card Specification version 3.0</i>	None

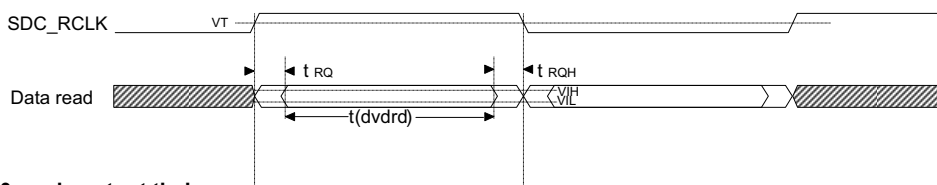
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

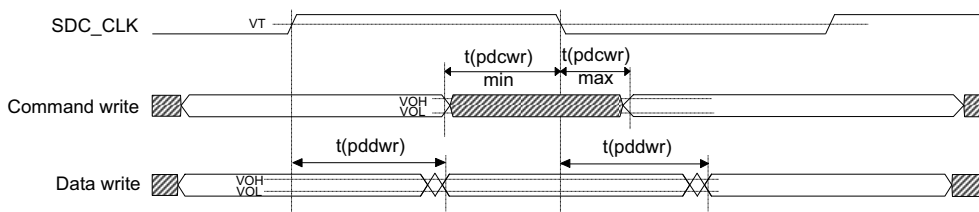


Figure 3-5 SD interface timing

NOTE: SD interface timing parameters can be found at the standards mentioned above.

3.9.2 USB interfaces

Table 3-14 Supported USB standards and exceptions

Applicable standard	Feature exceptions
<i>Universal Serial Bus Specification, Revision 3.1</i> (August 11, 2014 or later)	U1 and U2 stages are not enabled in USB3 Gen1 and Gen2 Device Mode due to interoperability concerns
<i>UTMI Specification Version 1.05, released on 3/29/2001</i>	None
<i>On-The-Go and Embedded Host Supplement to the USB 3.0 Specification</i> (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.9.3 DisplayPort

Table 3-15 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
<i>VESA DisplayPort V1.4a</i>	None

3.9.4 PCIe interface

Table 3-16 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
<i>PCI Express Base Specification Revision 3.0</i>	None

3.9.5 UFS interface

Table 3-17 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
<i>Universal Flash Storage (UFS), Version 3.1</i>	None

3.9.6 UIM interface

Table 3-18 Supported UIM standards and exceptions

Applicable standard	Feature exceptions
<i>ISO/IEC 7816-3</i>	Class A

3.9.7 Digital microphone PDM interface

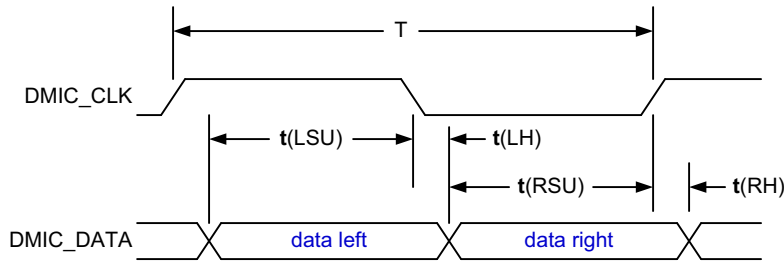


Figure 3-6 Digital microphone PDM interface timing

Table 3-19 Digital microphone timing

Parameter		Min	Typ	Max	Units
1/T	DMIC clock frequency	0.6	–	12.288	MHz
	DMIC clock duty cycle	45	–	55	%
t(LSU)	Data left setup time to clock falling edge	10	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	ns

3.9.8 SoundWire (SWR) interface

Table 3-20 Supported SWR standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for SoundWire Version 1.2	None

SM8450 SoundWire PHY timing parameters, as specified in [Table 3-21](#), are compliant to clock and data specifications.

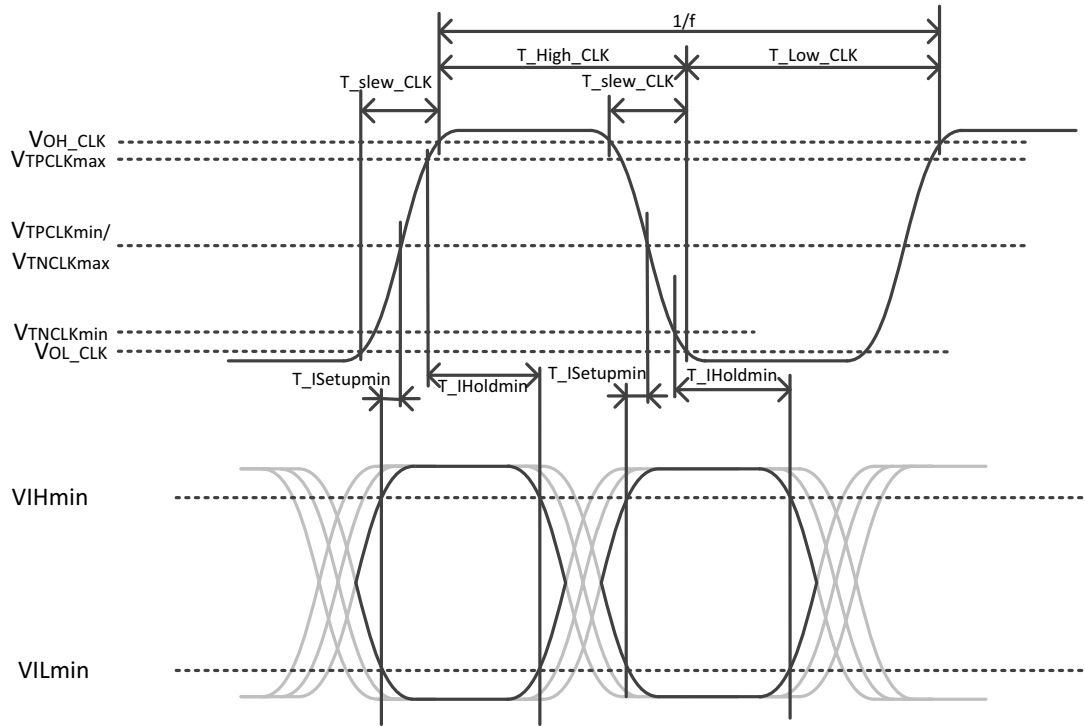


Figure 3-7 PHY timing – clock output/input and data input

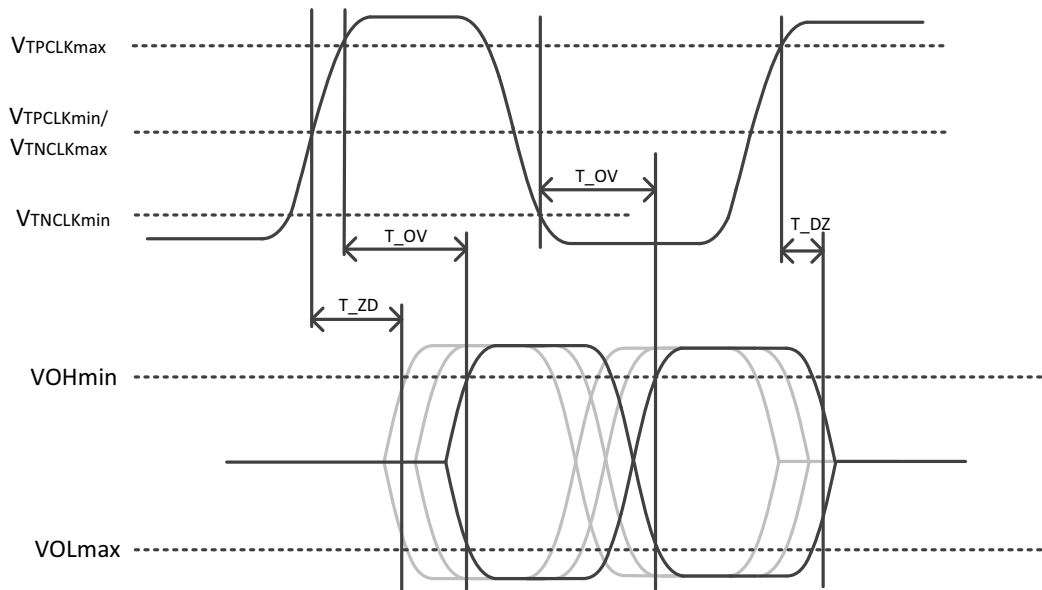


Figure 3-8 PHY timing – clock output and data output

Table 3-21 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Units
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	25.6	ns
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	3	–	ns
t_IHold_min_Data_1V8	Input hold time	–	4	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from $t_{Low_Clock}/(t_{Low_Clock} + t_{High_Clock})$	46% of the SWR CLK	54% of the SWR CLK	ns

3.9.9 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
<i>MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 2.0</i>	None

3.9.10 I²S interfaces

There are two I²S interface types supported by the SM8450:

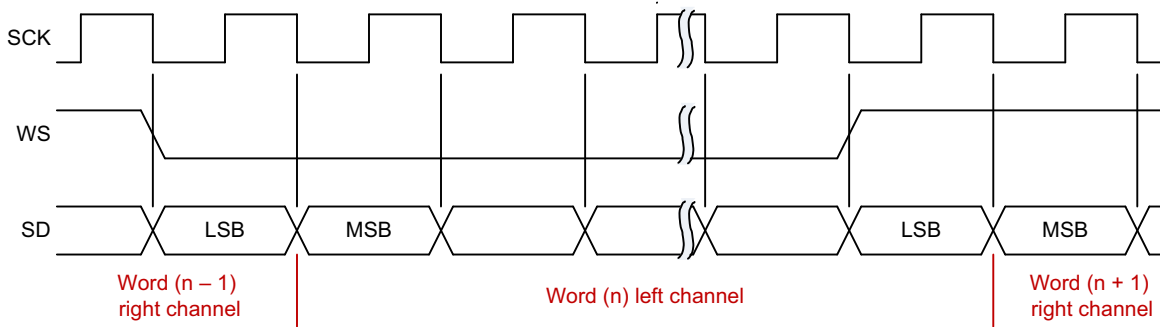
- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI²S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-23 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
<i>Philips I²S Bus Specifications revised June 5, 1996</i>	None

High-level I²S timing



I²S timing details – Tx and Rx

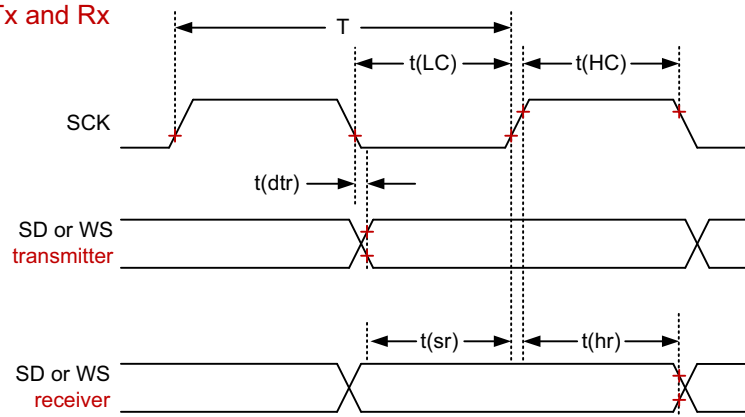


Figure 3-9 I²S timing diagram

Table 3-24 I²S interface timing parameters

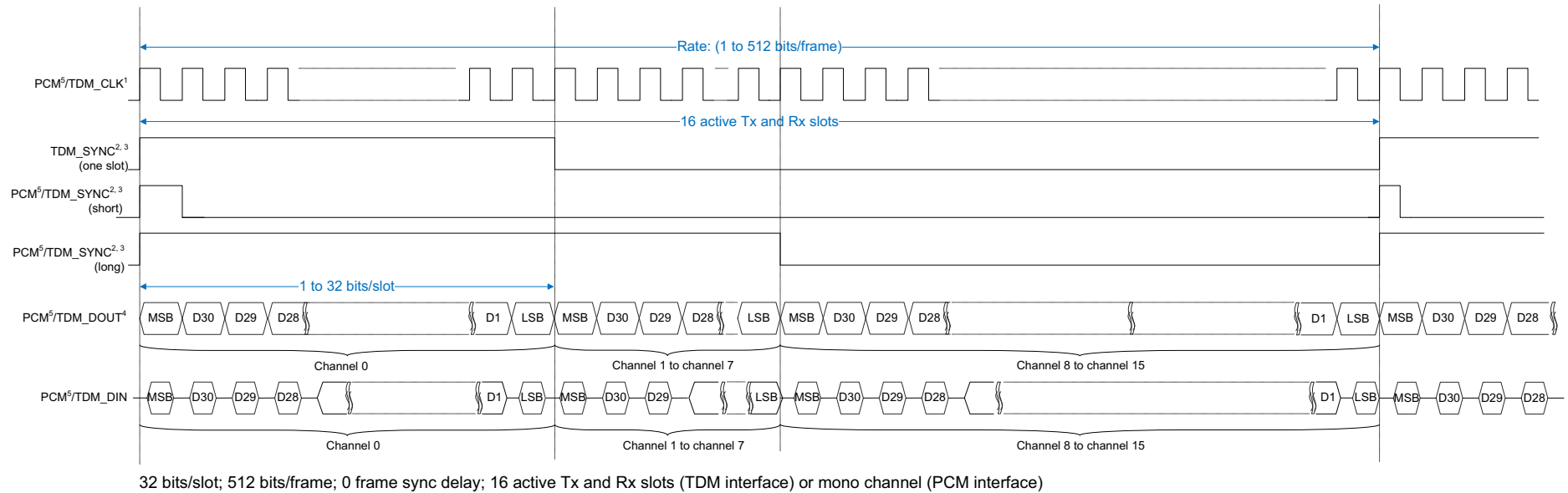
Parameter		Comments ¹	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns

Table 3-24 I²S interface timing (cont.) parameters

Parameter		Comments ¹	Min	Typ	Max	Unit
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

1. Load capacitance is between 10 pF and 40 pF

3.9.11 PCM/TDM interfaces



Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
 - If data size < slot size, remaining data bits are padded with zeroes.
 - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
 - Supports only mono channel.
 - Does not support one-slot mode.
 - PCM_SYNC period is equivalent to 1 frame.

Figure 3-10 PCM/TDM audio format with different sync modes

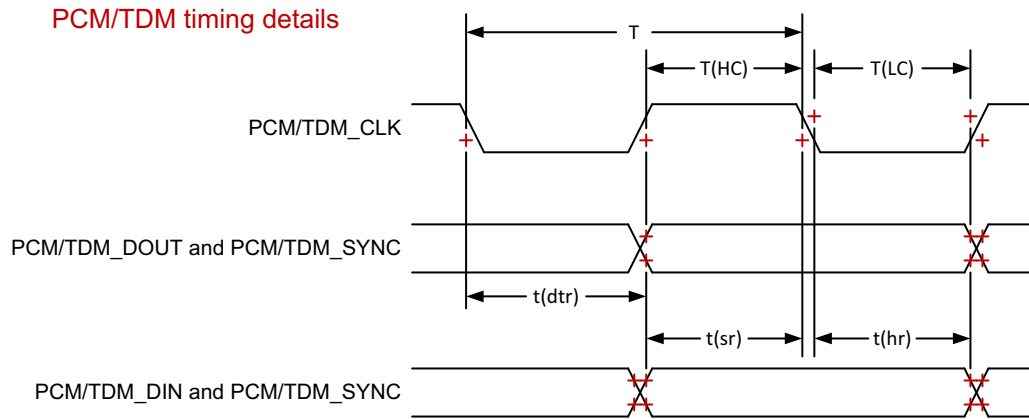


Figure 3-11 PCM/TDM timing diagram

Table 3-25 PCM/TDM interface timing parameters

Parameter ¹		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		$0.45 \times T$	$0.55 \times T$	ns
t(LC)	Clock low		$0.45 \times T$	$0.55 \times T$	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns
Slave mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		$0.45 \times T$	$0.55 \times T$	ns
t(LC)	Clock low		$0.45 \times T$	$0.55 \times T$	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns

1. Load capacitance is between 10 pF to 40 pF.

3.9.12 Touchscreen connections

Touchscreen panels are supported using I²C buses (Section 3.9.13) and GPIOs configured as discrete digital inputs (Section 3.5). Additional specifications are not required.

3.9.13 I²C/I³C interface

Table 3-26 Supported I²C/I³C standards and exceptions

Applicable standard	Feature exceptions
<i>I²C Specification, version 3.0</i>	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
<i>I³C specification, version 1.0</i>	Ternary, multi-master, HCI are not supported.

3.9.14 Serial peripheral interface

The SM8450 supports SPI as a master only. Any one of the 22 QUP ports can be configured as an SPI master.

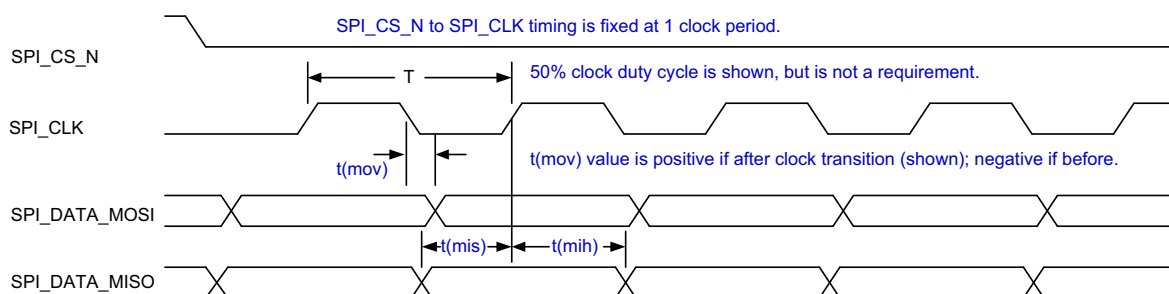


Figure 3-12 SPI master timing diagram

Table 3-27 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) ¹	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

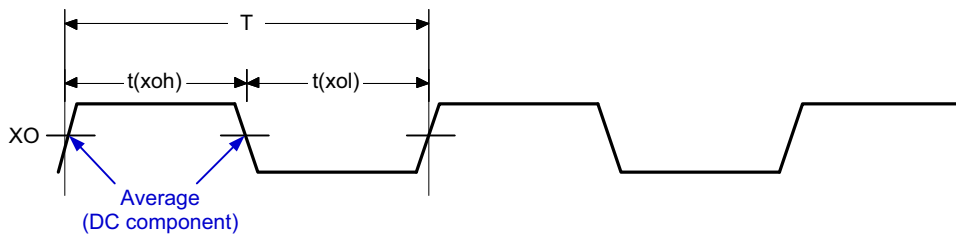


Figure 3-13 XO timing parameters

Table 3-28 CXO timing parameters

Parameter		Comments ¹	Min	Typ	Max	Unit
$t(xoh)$	XO logic high	–	22.6	–	29.5	ns
$t(xol)$	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
$1/T$	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See Section 3.6.3 76.8 MHz XO crystal requirements of PMK8350/PMK8450/PMK8475 Data Sheet (80-PT197-1) for more information.

3.10.1.2 Sleep clock

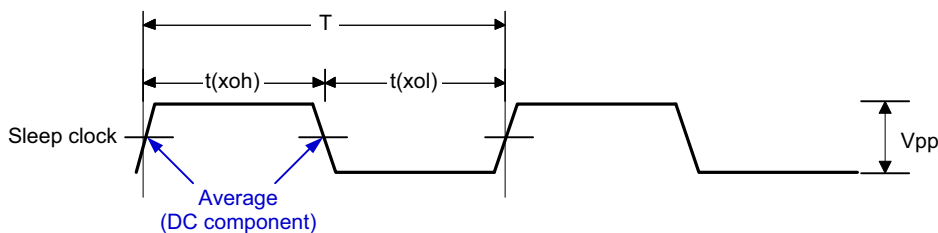


Figure 3-14 Sleep-clock timing parameters

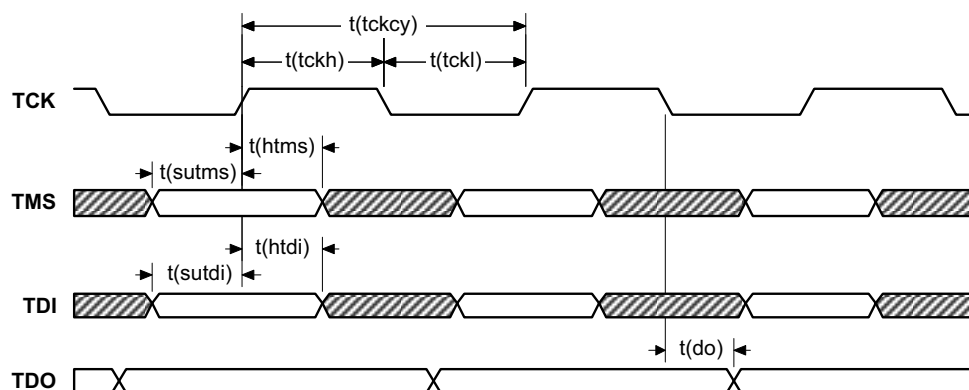
Table 3-29 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	μs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	μs
T	Sleep-clock period	–	–	30.521	–	μs
F	Sleep-clock frequency	$F = 1/T$	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in [Section 3.5](#).

3.10.3 JTAG

**Figure 3-15 JTAG interface timing diagram****Table 3-30 JTAG interface timing characteristics**

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

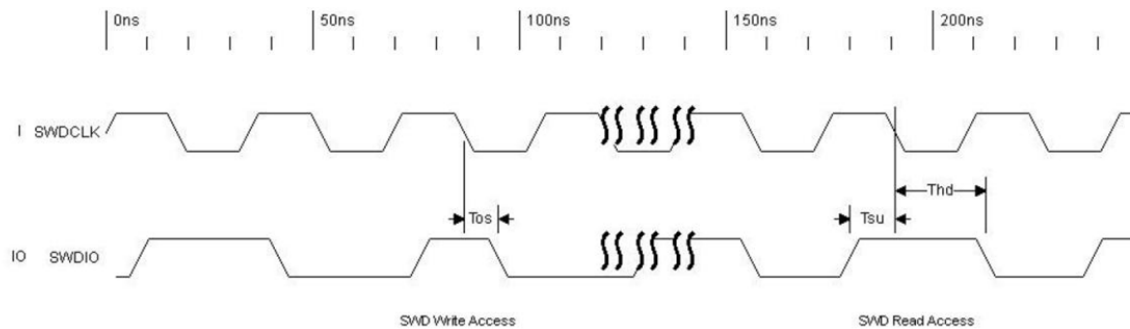


Figure 3-16 SWD write and read AC timing diagram

Table 3-31 SWD write and read AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T-7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

NOTE: SWDCLK runs at 20 MHz or lower.

3.11 Power management interface

The digital I/Os must meet the logic-level requirements specified in [Section 3.5](#).

3.11.1 System power management interface (SPMI)

Table 3-32 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM8450 is available in the MPSP1518 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1518 has a 15.0 mm by 14.0 mm body, with a maximum height of 0.57 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1518 outline drawing is shown in [Figure 4-1](#).

NOTE: Click the following link to download the *Package Outline Drawing, MPSP1518, 15.0 × 14.0 × 0.57 mm, ST94, M127, SB167, PB 496NSP, PL1, MEP* (NT90-PT611-3) from the CreatePoint website.

<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PT611-3>

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the **Related Files** line that is located directly underneath the PDF link.

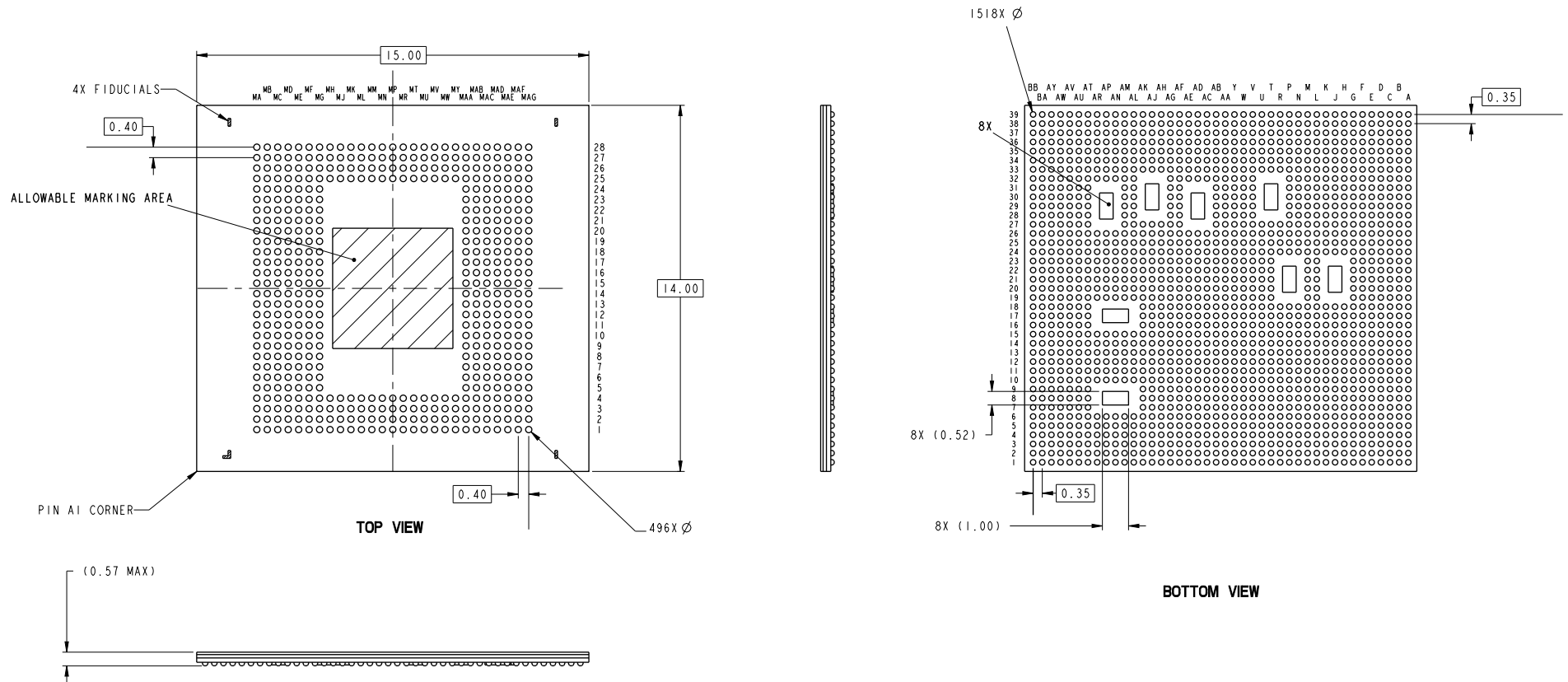


Figure 4-1 MPSP1518 outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

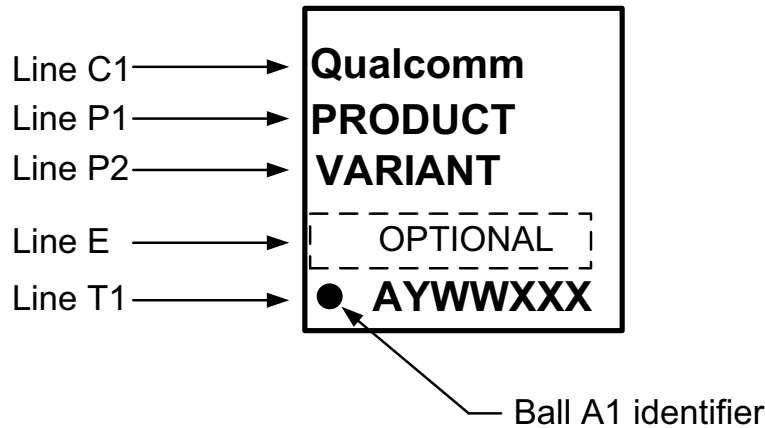


Figure 4-2 SM8450/SM8450P device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name <ul style="list-style-type: none"> ■ SM8450 ■ SM8450P
P2	VARIANT	PRR-BB <ul style="list-style-type: none"> ■ See Table 4-4 for the assigned values.
E	Blank or random	Optional information
T1	AYWWXXX	A = assembly site code <ul style="list-style-type: none"> ■ A = C (Amkor, Korea) ■ A = X (Shinko, Japan) Y = single/last digit of year WW = two digit work week of current year XXX = serial number
	•	Ball A1 indicator

NOTE: For complete marking definitions of all SM8450/SM8450P variants and revisions, see the *SM8450/SM8450P Device Revision Guide* (80-11140-4).

The 28-bit QFPROM JTAG register is summarized in [Table 4-2](#).

Table 4-2 Related register (0x221C21B8)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	Feature ID is used for differentiating SKUs/variants
bits [19:0]	JTAG_ID	These bits map to [31:12] of the JTAG_ID register (0x221C8744). Fuse bit 0 maps to bit 12 of JTAG_ID

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in [Table 4-3](#).

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID ¹
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8450	-1	-MPSP	1518			-TR	-00	-0	-AC

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8450-1-MPSP1518-TR-00-0-AC

NOTE: The shipping package is either TR (tape and reel) or MT (matrix tray).

Device identification details for all samples available to date are summarized in [Table 4-4](#).

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code ¹	FEATURE_ID ²	Hardware revision number	Source configuration code (S) ³	Comments	Sample date
SM8450	ES1	100-AC	0x2	0x0 0187 0E1	0	SM8450, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.59 mm height	04/30/2021
SM8450P	ES1	100-AC	0x1	0x0 0188 0E1	0	SM8450P, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, no modem, 0.59 mm height	04/30/2021
SM8450	ES2	102-AC	0x4	0x2 0187 0E1	0	SM8450, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.57 mm height	8/31/2021
SM8450P	ES2	102-AC	0x2	0x2 0188 0E1	0	SM8450P, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, no modem, 0.57 mm height	8/31/2021
SM8450	CS ⁴	103-AC	0x5	0x3 0187 0E1	0	SM8450, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, no AON camera, 800 MHz mmW, 200 MHz Sub-6 with ULCA, LTE, 0.57 mm height	09/30/2021
SM8450P	CS ⁴	103-AC	0x3	0x3 0188 0E1	0	SM8450P, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, no AON camera, no modem, 0.57 mm height	09/30/2021
SM8450	CS ⁴	103-AD	0x8	0x3 0187 0E1	0	SM8450, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, 800 MHz mmW, 200 MHz Sub-6 with ULCA, LTE, 0.57 mm height	09/30/2021
SM8450P	CS ⁴	103-AD	0x5	0x3 0188 0E1	0	SM8450P, MPSP1518, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, no modem, 0.57 mm height	09/30/2021

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See [Table 4-2](#). FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
3. S is the source configuration code that identifies all the qualified die fabrication-source and assembly site combinations available when the particular sample type was shipped. S values are defined in [Table 4-5](#).
4. These are the devices affected as per PCN05208. The updates made are reflected in [Section 5.1.1 Tape and reel information](#).

Table 4-5 Source configuration codes

S value	Die	F value = J	A value = C	A value = X
0	Digital	Samsung	Amkor, Korea	Shinko, Japan

4.3.2 Serial number

For instructions on how to read serial number, see the *How to get 64bit Serial Number in TA* (KBA-210829225022).

NOTE: Click the following link to download the *How to get 64bit Serial Number in TA* (KBA-210829225022) from the CreatePoint website.

<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/KBA-210829225022>

After successfully logging on, the document is downloaded.

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4.3.3 Daisy chain devices

The SM8450/SM8450P daisy chain ordering part number is TP-MPSP1518-1 (0.59 mm height) for ES1 package and TP-MPSP1518-2 (0.57 mm height) for ES2 and CS package.

For the daisy chain interconnect information, see *Daisy Chain Interconnect, MPSP1518, 15.0 × 14.0 mm* (DS90-PT611-S1).

NOTE: For LPDDR5 daisy chain ordering part number, contact the LPDDR manufacturer.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in [Table 4-6](#).

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SM8450/SM8450P rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. *The SM8450/SM8450P devices are classified as MSL3; the qualification temperature was 255°C.* This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA} , validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the
SM8450 LPDDR5 8GB PACKAGE THERMAL MODEL ICEPAK
(HS11-11140-5HW)
<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-11140-5HW>
SM8450 LPDDR5 8GB PACKAGE THERMAL MODEL FLOTHERM
(HS11-11140-6HW)
<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-11140-6HW>

After successfully logging on, the document is downloaded.

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5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8450 tape carrier is shown in [Figure 5-1](#), including the proper part orientation, maximum number of devices per reel, and key dimensions.

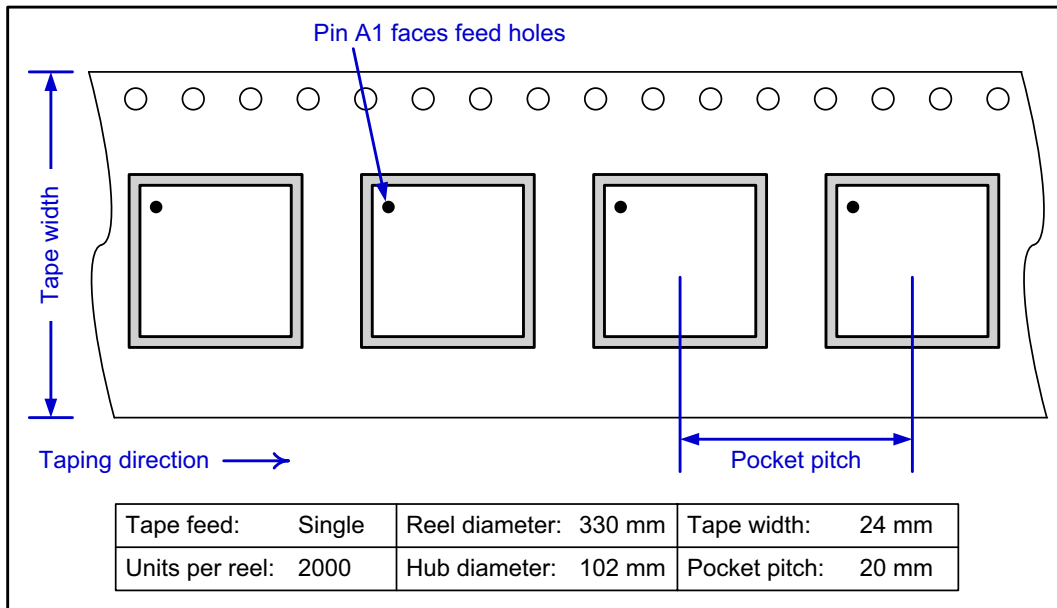


Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in [Figure 5-2](#).

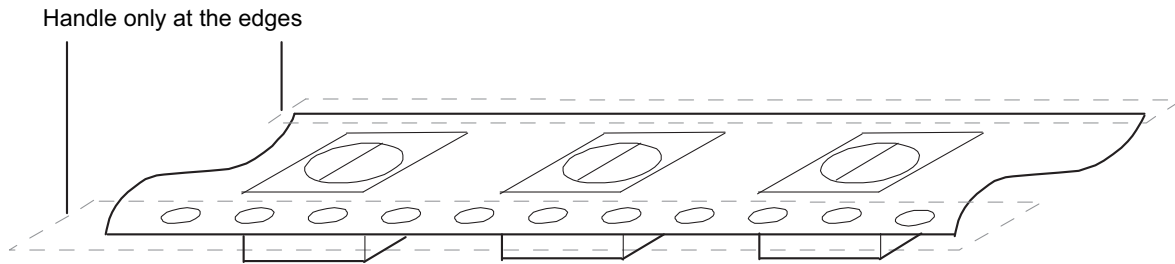


Figure 5-2 Tape handling

5.1.2 Matrix tray information – available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See [Figure 5-3](#) for matrix-tray key attributes and dimensions.

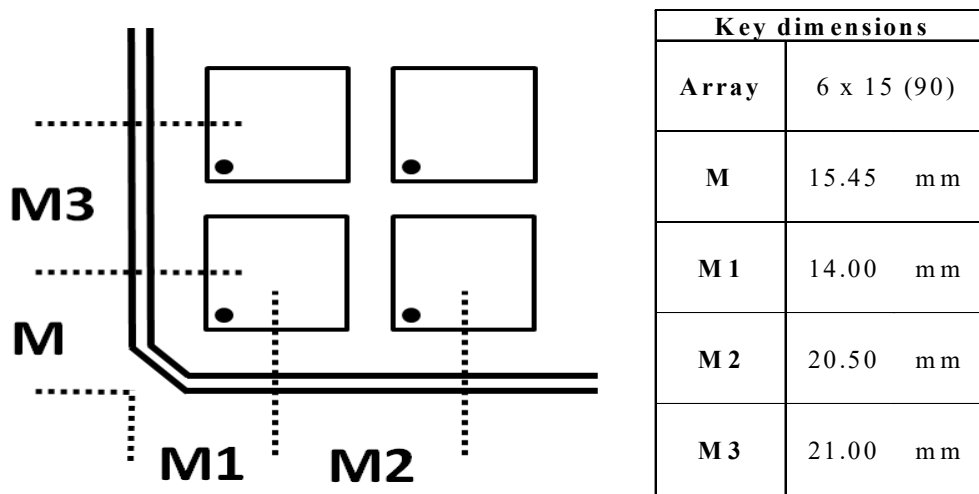


Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Storage

5.2.1 Bagged storage conditions

SM8450 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in [Section 4.4](#).

5.3 Handling

Tape handling was described in [Section 5.1.1](#). Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM8450 if the conditions specified in [Section 5.2.1](#) and [Section 5.2.2](#) have **not been exceeded**.

It is **necessary** to bake the SM8450 if any condition specified in [Section 5.2.1](#) or [Section 5.2.2](#) has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

<https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1>

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualification summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	1270	Pass
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	513	< 100
Mean time to failure (MTTF) $t = 1/\lambda$ in million hours (Total samples from three different wafer lots)	513	> 10
ESD — Human body model (HBM) rating per JS001 (Total samples from one wafer lot)	21	Pass; ± 1 kV
ESD — Charged device model (CDM) rating per C101 (Total samples from one wafer lot) All pins passed +/-250 V except EBI passed -200 V	3	Pass; ± 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ± 100 mA; temperature: 105°C (Total samples from one wafer lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at $1.5 \times V_{ddmax}$ per device specification; temperature: 105°C (Total samples from one wafer lot)	6	Pass

Table 7-2 SM8450-LPDDR5 package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Shinko Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C (Total samples from three different assembly lots)	693	693	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 700 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C (Total samples from three different assembly lots)	120	120	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (Total samples from three different assembly lots)	231	231	Pass
Flammability UL-STD-94 Note: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

7.2 Device characteristics

Table 7-3 Device characteristics

Device name	SM8450/SM8450P
Package type	MPSP1518
Package body size	15.0 mm × 14.0 mm × 0.57 mm
Lead composition	SAC125/Ni
Fab process	4 LPX
Fab sites	Samsung
Assembly sites	<ul style="list-style-type: none">■ Amkor, Korea■ Shinko, Japan
Solder ball pitch	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	November 2020	Initial release
AB	February 2021	<ul style="list-style-type: none"> ■ Table 1-1 SM8450 features: Updated the Hexagon tensor processor capabilities and SSC mapping ■ Table 2-1 I/O description (pad type) parameters: Updated the PX2 description ■ Figure 2-2 SM8450 bottom pin assignments (top view): Updated the UFS pin name ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: <ul style="list-style-type: none"> □ Removed references to BOOT_CONFIG[6:11] □ Updated the QUP assignment/mapping information table references □ Updated the pad voltages for GPIO_36, GPIO_37, GPIO_38, GPIO_39, GPIO_40, GPIO_41, GPIO_42, GPIO_43, GPIO_97, GPIO_98, GPIO_99 ■ Table 2-3 QUP lane to GPIO mapping: Added this table ■ Section 4.2 Part marking: Added this section ■ Section 4.3 Device ordering information: Added this section ■ Section 4.4 Device moisture sensitivity level: Added this section ■ Section 4.5 Thermal characteristics: Added this section ■ Chapter 5 Carrier, storage, and handling information: Added this chapter ■ Chapter 6 PCB mounting guidelines: Added this chapter
AC	March 26, 2021	<ul style="list-style-type: none"> ■ Cover: Updated the outline drawing ■ Section 1.1 Functional block diagram: Updated the block diagram to include the modem block ■ Table 1-1 SM8450 features: Updated the package thickness from 0.59 mm to 0.57 mm ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: Added a configurable function for GPIO_92: SD_CARD_DET_N ■ Table 3-2 Operating conditions for non AVS voltage rails: Updated the typical voltage values of some power rails ■ Section 4.1 Device physical dimensions: Updated the package thickness from 0.59 mm to 0.57 mm and NT90 document number ■ Figure 4-1 MPSP1518 outline drawing: Updated the package outline drawing ■ Chapter 7 Part reliability: Added the ESD test results for ES parts

Revision	Date	Description
AD	March 31, 2021	<ul style="list-style-type: none"> ■ Figure 1-1 SM8450 functional block diagram and example application: Updated PCIe Gen 4 to PCIe Gen 3 ■ Figure 1-2 SM8450P functional block diagram and example application: Updated PCIe Gen 4 to PCIe Gen 3 ■ Table 1-1 SM8450 features: Updated PCIe Gen 4 to PCIe Gen 3 ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: Added configurable functions to GPIO_94, GPIO_96, GPIO_97, GPIO_99
AE	April 13, 2021	<ul style="list-style-type: none"> ■ Table 1-1 SM8450 features: Replaced BurstWrite with Write Booster for UFS memory ■ Section 4.3.2 Daisy chain devices: Added the daisy chain ordering part number ■ Table 4-4 Device identification details: Updated the sample type
AF	April 14, 2021	<ul style="list-style-type: none"> ■ Figure 1-1 SM8450 functional block diagram and example application: Replaced USC with TME ■ Figure 1-2 SM8450P functional block diagram and example application: Replaced USC with TME ■ Table 1-1 SM8450 features: Replaced USC with TME ■ Table 4-4 Device identification details: Updated the sample comments
AG	May 2021	<ul style="list-style-type: none"> ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: Updated the pad number for GPIO_105
AH	June 2021	<ul style="list-style-type: none"> ■ Section 4.3.2 Daisy chain devices: Added a note for LPDDR5 daisy chain ordering
Revision AI was omitted in accordance with QTI document conventions		
AJ	July 8, 2021	<ul style="list-style-type: none"> ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: Updated the pad type for GPIO_34 ■ Section 4-4 Device identification details: Updated this table for ES2 samples
AK	July 14, 2021	<ul style="list-style-type: none"> ■ Table 1-1 SM8450 features: Updated the audio features
AL	July 27, 2021	<ul style="list-style-type: none"> ■ Figure 1-1 SM8450 functional block diagram and example application: Added UIM block ■ Table 1-1 SM8450 features: Added a note for Write Booster performance
AM	August 10, 2021	<ul style="list-style-type: none"> ■ Figure 4-4 Device identification details: Updated this table for CS samples
AN	September 8, 2021	<ul style="list-style-type: none"> ■ Table 1-1 SM8450 features: Added the core frequency and cache information. Updated DisplayPort v1.4a. ■ Section 3.1 Absolute maximum ratings: Added this section ■ Section 3.5 Digital logic characteristics: Added this section ■ Section 3.6 Timing characteristics: Added this section ■ Section 3.8 Multimedia: Added this section ■ Section 3.9 Connectivity: Added this section ■ Section 3.10 Internal functions: Added this section ■ Section 3.11 Power management interface: Added this section ■ Section 4.3.2 Daisy chain devices: Added CS details
Revision AO was omitted in accordance with QTI document conventions		

Revision	Date	Description
AP	September 21, 2021	<ul style="list-style-type: none"> ■ Table 3-1 Absolute maximum ratings: Updated the voltage values ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Updated the voltage values ■ Table 3-3 Operating conditions for non AVS voltage rails: Updated the voltage values ■ Table 3-27 CXO timing parameters: Updated this table ■ Table 3-28 Sleep-clock timing parameters: Updated this table ■ Section 4.3.2 Serial number: Added this section ■ Figure 5-1 Carrier tape drawing with part orientation: Updated the units per reel and hub diameter ■ Table 7-1 Silicon reliability results: Updated this table
Revision AQ was omitted in accordance with QTI document conventions		
AR	September 30, 2021	<ul style="list-style-type: none"> ■ Table 3-4 Thermal conditions: Added this table ■ Table 4-4 Device identification details: Updated this table for CS samples
Revision AS was omitted in accordance with QTI document conventions		
AT	October 6, 2021	<ul style="list-style-type: none"> ■ Table 7-1 Silicon reliability results: Updated the reliability results ■ Table 7-2 SM8450-LPDDR5 package reliability results: Updated the reliability results
AU	October 14, 2021	<ul style="list-style-type: none"> ■ Table 7-2 SM8450-LPDDR5 package reliability results: Updated the reliability results
AV	October 18, 2021	<ul style="list-style-type: none"> ■ Table 3-5 DC specification of 1.8 V GPIOs: Updated this table ■ Table 7-2 SM8450-LPDDR5 package reliability results: Updated the reliability results
AW	October 19, 2021	<ul style="list-style-type: none"> ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Added retention mode for VDD_LPI_CX and VDD_LPI_MX
Revision AX was omitted in accordance with QTI document conventions		
AY	October 22, 2021	<ul style="list-style-type: none"> ■ Updated Table 7-2: SM8450-LPDDR5 package reliability results
Revision AZ was omitted in accordance with QTI document conventions		
BA	October 27, 2021	<ul style="list-style-type: none"> ■ Table 2-2 MSM bottom pin descriptions – general-purpose input/output ports: Updated the functional description of GPIO_100, GPIO_101, GPIO_102, GPIO_103, GPIO_104, GPIO_105, GPIO_106, GPIO_107 ■ Table 3-3 Operating conditions for non AVS voltage rails: Added additional voltage values for VDD_IO_EBI and LPDDR5_VDDQ and added a note ■ Section 3.8.1.1 Camera MLCK: Added this section
BB	November 2021	<ul style="list-style-type: none"> ■ Table 4-4 Device identification details: Added a note for CS samples ■ Section 4.3.3 Daisy chain devices: Added the daisy chain interconnect information ■ Section 5.1.1 Tape and reel information: Updated the units per reel and hub size as per PCN05208
BC	January 2022	<ul style="list-style-type: none"> ■ Table 1-1 SM8450 features: Updated core frequency ■ Table 4-4 Device identification details: Updated device comments
BD	February 4, 2022	<ul style="list-style-type: none"> ■ Table 3-1 Absolute maximum ratings: Updated the absolute maximum rating of some power rails ■ Table 3-3 Operating conditions for non AVS voltage rails: Updated the voltage values to meet the PMIC software setting
BE	February 9, 2022	<ul style="list-style-type: none"> ■ Global: Updated process description ■ Table 4-5 Source configuration codes: Added assembly sites
BF	February 23, 2022	<ul style="list-style-type: none"> ■ Table 4-4 Device identification details: Updated modem information

For additional information or to submit technical questions, go to <https://createpoint.qti.qualcomm.com>

Document release date: February 23, 2022

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