Device description

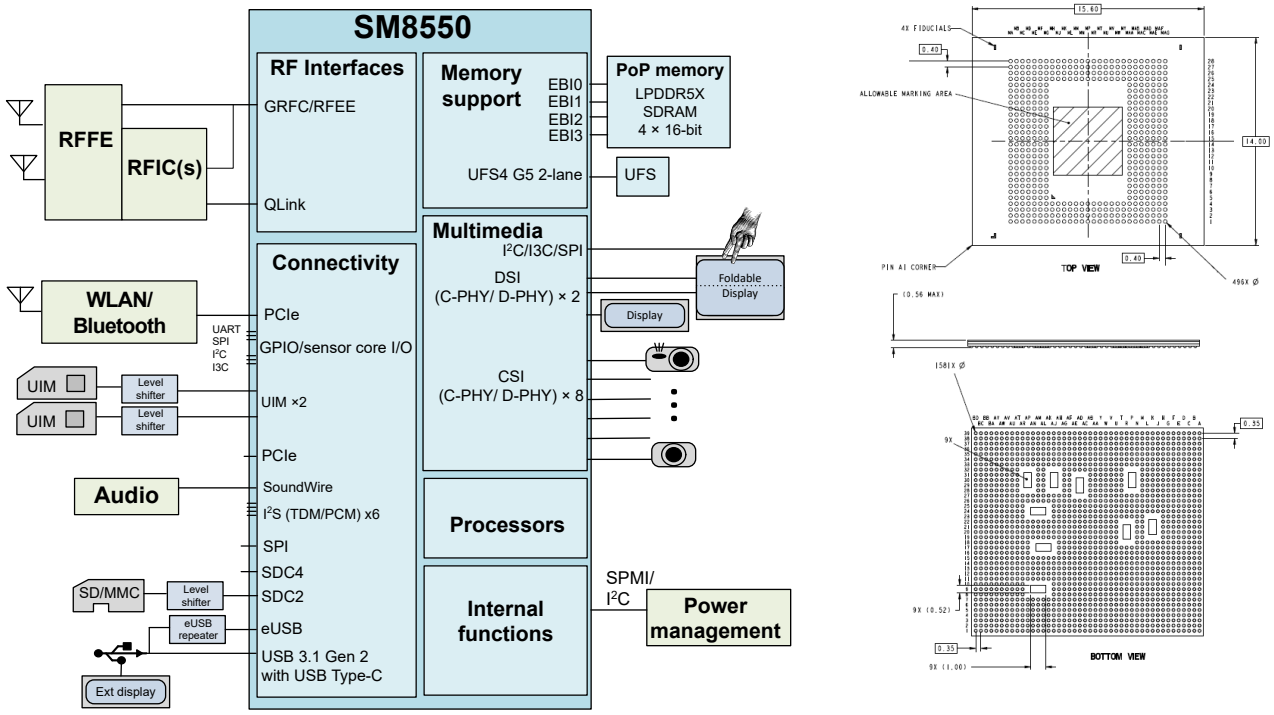
The SM8550/SM8550P device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with a 4 nm process, for superior performance and power efficiency. SM8550/ SM8550P includes the following key components:

- Qualcomm® Kryo™ CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 740 GPU for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ Image Signal Processor for the ultimate photography and videography experiences
- Adreno VPU 8550 for high-quality, ultra HD video encode and decode
- Adreno 1295 DPU for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 GHz bands (Rel 16 integrated modem)

Key features

- Low Power AI (LPAI) subsystem with dedicated DSP and AI accelerator (eNPU) supporting always-on audio, sensors, contextual data streams, and Always-on camera
- Qualcomm Aqstic™ Audio Technologies WCD9380/ WCD9385 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Secure Processing Unit for advanced secure use cases
- Qualcomm® Hexagon™ Tensor Processor (HTP) with Hexagon Vector eXtensions (HVX) and Hexagon Matrix eXtensions (HMX)
- Qualcomm® FastConnect™ 7800 System with WCN785x, 802.11be, 2 × 2 MIMO, Bluetooth 5.3
- Quad-channel package-on-package (PoP) high-speed LPDDR5X SDRAM
- 15.6 × 14.0 × 0.56 mm MPSP1581 PoP

SM8550/SM8550P high-level block diagram and MPSP1581 outline drawing



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Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

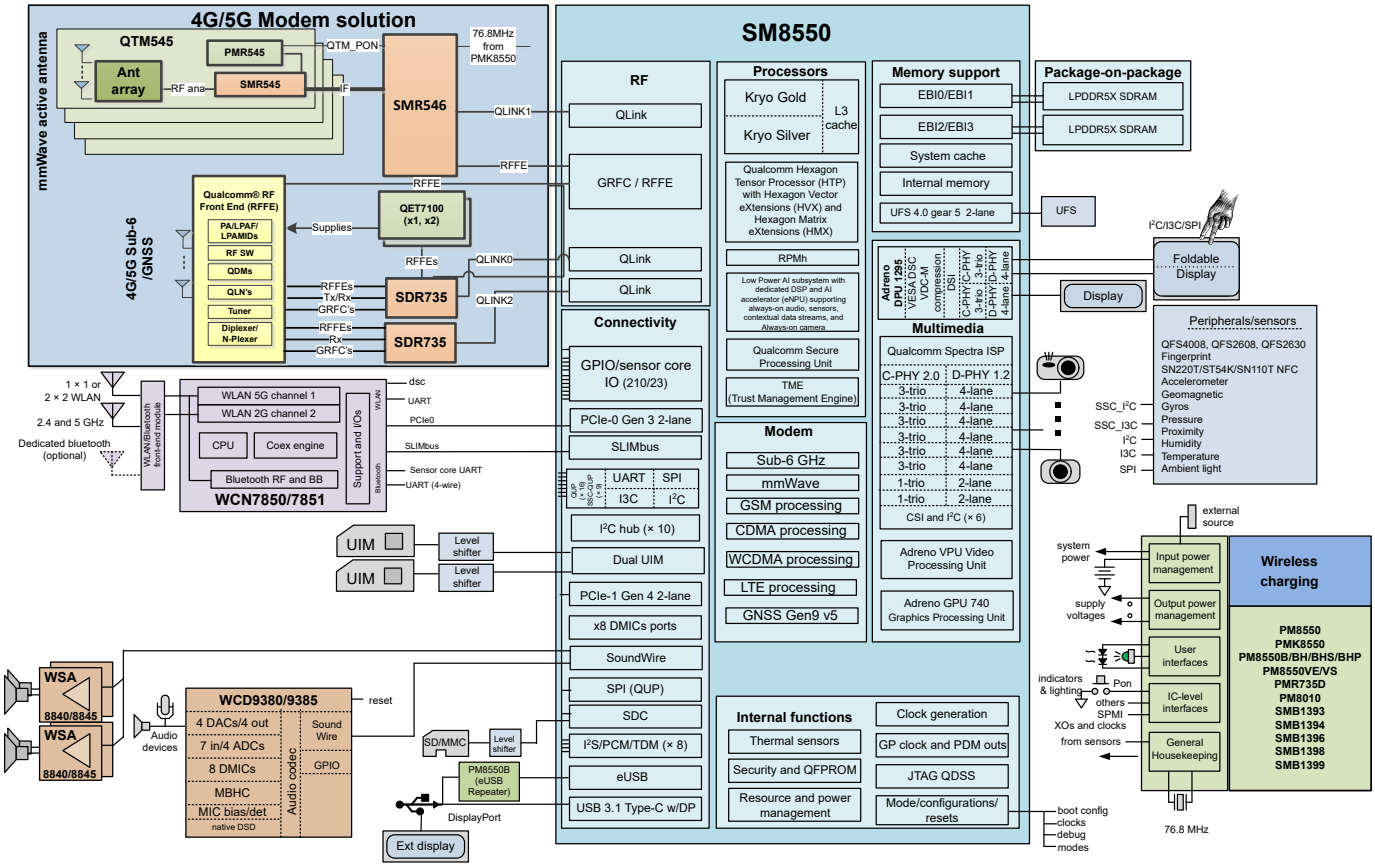


Figure 1-1 SM8550 functional block diagram and example application

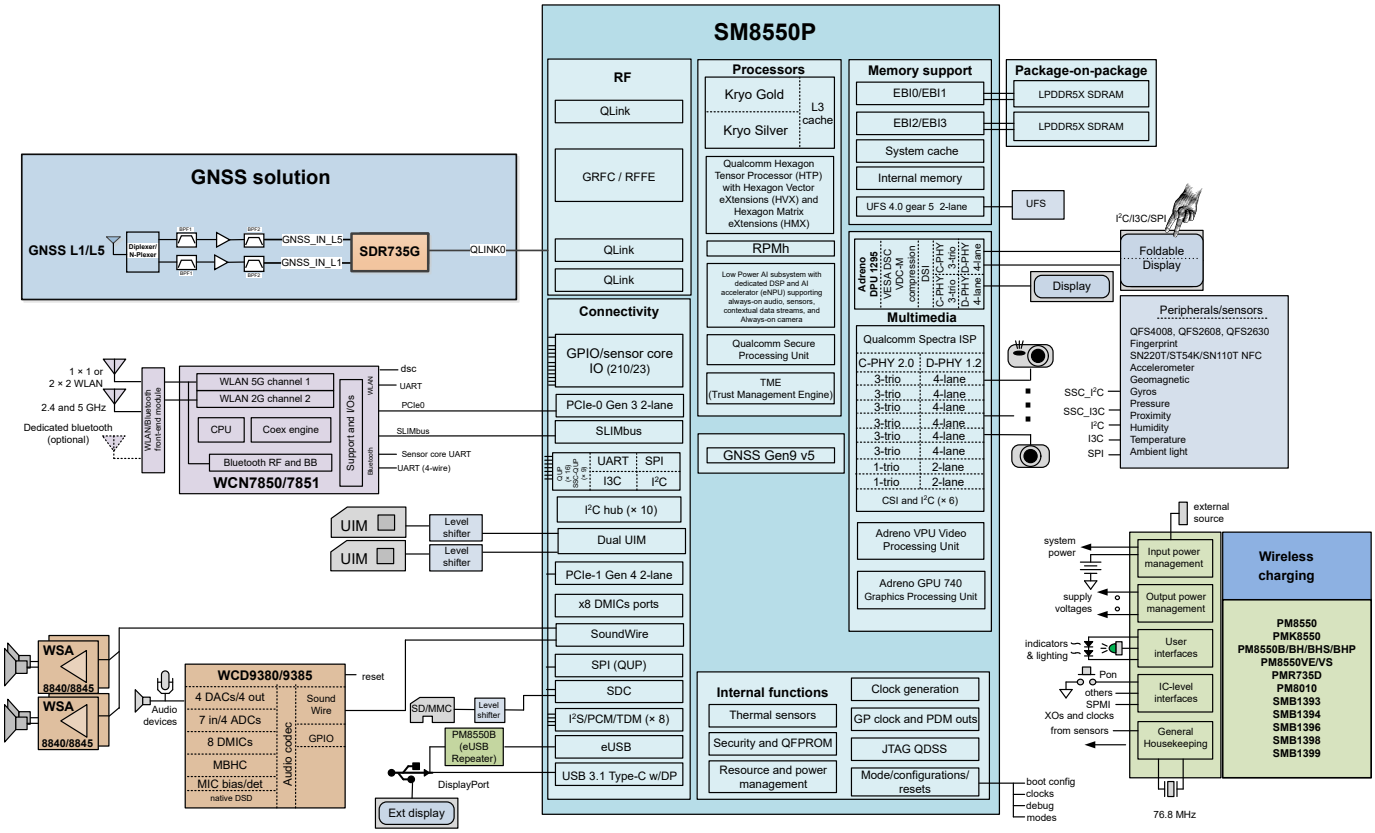


Figure 1-2 SM8550P functional block diagram and example application

1.2 SM8550/SM8550P features

NOTE Some of the hardware features integrated within the SM8550/SM8550P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8550/ SM8550P features.

Table 1-1 SM8550/SM8550P features

Feature	SM8550/SM8550P capability
Processors	
Applications	Kryo CPU subsystem ■ Prime and high-performance cores for intensive tasks ■ Power-efficient cores
Digital signal processing and artificial intelligence	■ Hexagon tensor processor ▫ V73 AI-optimized tensor processor ▫ Six threads scalar DSP ▫ 4x HVX Vector tightly-couple co-processor optimized for pixel processing ▫ 1x HMX Matrix tightly-couple co-processor optimized for deep neural network processing, MAC arithmetic formats include INT8, A16W8, and FP16 ▫ Large VTCM ▫ BW compression ▫ Focus on depth-wise networks ▫ Focus on power efficiency ■ AI use cases: ▫ Noise reduction ▫ Super resolution ▫ ML ISP ▫ HDR ▫ Image enhancement ▫ Segmentation ▫ Depth estimation ▫ Classification/detection ■ For imaging, video, audio, and data-based NN use cases. ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. ■ The audio/sensors Hexagon DSP is dedicated to the Low Power AI subsystem with support for always-on, low-power use cases. It incorporates a dedicated AI processor for offloading neural network use cases to improve the performance and minimize power consumption. ■ All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
Low Power AI subsystem	Merged low power island, for always-on audio/voice, sensors, sensing hub, and Always-on camera ■ Hexagon V73M 2Cluster – 4 Thread DSP ■ 5.5 MB of LPI memory ■ AI Processor (eNPU) v3, to accelerate neural networking use cases ■ Qualcomm Sensing Hub 3.0
Sensors hardware	■ Data acquisition engine (DAE) ■ Context change detector 5.0 (CCD)
Sensors interfaces	■ Nine dedicated buses (1 I3C, 1 I3C/I^2C, 2 SPI, 3 I^2C, 2 UART) ■ 3x I3C IBI for DAE and DSP ■ Sensors supported in Qualcomm POR: ▫ Accel/Gyro ▫ Magnetometer ▫ Ambient Light/Proximity ▫ Pressure ▫ Humidity/Temp ▫ SAR ▫ Hall ▫ Plus others per customer inputs
Audio and voice hardware	■ Hardware linear echo cancellation accelerator ■ DSP-offload for audio playback (analog, Bluetooth Audio, USB Digital Audio)
Audio interfaces	SLIMbus for WCN785x SoundWire ■ SoundWire interface (two Tx and two Rx data for codec) WCD9380/WCD9385, PMIC Haptics, SoundWire MICs ■ Two dedicated SoundWire interfaces to support up to four WSA884x for smart speaker amplifier DMICs ■ Four DMIC ports support up to eight DMICs ■ Up to four DMICs for low-power voice activation Six I^2S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application One I^2S supports four data lanes for up to eight channels Tx/Rx application TDM/PCM: Up to 32 channels at 48 kHz per individual interface (Qualcomm Technologies, Inc. (QTI) I^2S supports both TDM and PCM modes.)

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
Audio and voice algorithms	Voice UI ■ Snapdragon Voice Activation keyword detection ■ Echo cancellation and noise suppression (ECNS) Voice call ■ AI-based noise suppression ■ Far-end noise suppression Audio record ■ Ambient noise suppression ■ HDR record
Codec	Integrated within the WCD9380/WCD9385 high fidelity audio codec
Speaker amplifier	Integrated within the WSA8840/WSA8845 class-H, low noise smart amplifier
Modem	3G/4G/5G – mmWave and sub-6 GHz bands (Rel 16) only for SM8550
Location	Gen9 v5 Location SW v22 GPS L1/L5/L2C, GLO G1, BDS B1I/B1C/B2A/B2B, GAL E1/E5A/E5B, QZSS L1/L5/L2C, NavIC L5
Memory support	
System memory via EBI on PoP	Four-channel PoP high-speed memory – LPDDR5X SDRAM (4 × 16-bit) designed for a 3750 MHz (LPDDR5), system cache
Storage Via UFS Via SDC	UFS 4.0 gear 5 Rate A, 1x 2-lane ICE with 3800 MB/s read and 3500 MB/s write SD v3.0 4 bit for SD card
Multimedia	
Display	DPU1295: ■ Maximum resolution for internal panel: Support up to 3480 × 2160 at 120 Hz, 3360 × 1600 at 144 Hz ■ Supports dual MIPI DSI ports, with support for split-link for fold use case. ■ External panel support: DisplayPort v1.4 with MST (2x 4K60 10-bit or 1x 8K30 with DSC) ■ Compression support: VDC-M for internal panel and DSC v1.2 ■ Processing: HDR10/10+, wide color gamut, scaling (source and destination), detail enhancement, local tone mapping, SPR and demura, color accuracy, rounded corner ■ Power-saving: panel self-refresh using LLC

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
Camera support	■ Qualcomm spectra image signal processor ▫ Qualcomm spectra ISP supports connectivity to multiple cameras due to eight included C-PHY/D-PHY interfaces. Furthermore, up to five cameras may operate concurrently due to the Qualcomm Spectra's 3 IFEs and 2 IFE-lites ■ AI assisted camera with object-based pixel processing ■ Always-on camera support ▫ CSI4 with PM8010 SPMI interface and CAM_MCLK_4 (GPIO_104) ■ HW interface ▫ Triple 36 MP ISPs ▫ Six combo-PHYs with four lanes for D-PHY/three trios for C-PHY each, two combo-PHYs (CSI6 and CSI7) with two lanes for D-PHY/one trio for C-PHY each ▫ D-PHY v1.2: 2.5 Gbps/lane ▫ C-PHY v2.0: 13.68 Gbps/trio ▫ Connect up to 14x/20x cameras, 5x concurrent ■ Throughput ▫ 108 MP @ 30 fps ZSL with in-ISP pixel binning ▫ 64 MP @ 30 fps ZSL with two IFEs combined, without in-ISP binning ▫ 200 MP non-ZSL snapshot capture ▫ 12 MP @ 240 fps fast shutter sensor support - PHY and RAW dump ■ Key improvements: ▫ Improved sensor feature support including 2x2, 3x3, 4x4 color filter patterns and flexible HDR sensor support with smooth mode transition ▫ Improved local tone mapping (LTM), minimizing halo artifacts and improving face detection accuracy ▫ Color 2D look-up table (LUT) enhanced to improve saturation and noise ▫ Lens shading correction (LSC) improved to handle higher resolution and wider lens field of view ▫ Auto focus improvements to handle larger sensor resolutions and low light conditions ▫ Advanced auto exposure (AEC) statistics, improving exposure consistency regardless of light source position ■ ZSL example: ▫ (36 M + 36 M + 36 M) @ 30 fps - triple camera ▫ (64 M + 36 M) @ 30 fps - dual camera ▫ 108 M @ 30 fps - single camera ■ MFHDR HW for snapshot, video, preview ■ Staggered HDR (sHDR, digital overlap, and non-overlap) HW for snapshot, video, and preview
Adreno video processing unit (VPU)	Adreno VPU 8550

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
	UHD video processing unit Video decode up to 4K240/8K60 Video encode up to 4K120/8K30 Concurrent 4K60 decode and 4K60 encode for wireless display AV1 decode Native decode support for H.265 Main 10, H.265 Main, H.264 High, and VP9 profile 2 Native encode support for H.265 Main 10, H.265 Main, H.264 high formats
Adreno graphic processing unit (GPU)	Adreno GPU 740 – 4K 120 fps UI Ray tracing OpenGL ES 3.2, Vulkan 1.2 OpenCL 3.0 full profile Adreno NN direct GMEM as General Purpose Memory - GMEM write for compute Concurrent processing to improve efficiency - concurrent binning Workload Reduction - Image based variable rate shading Full virtualization support
Connectivity	
I/Os	Dual voltage (1.2 V/1.8 V) support. For details, see Pin definitions.
Qualcomm universal peripheral (QUP) ports	Qualcomm universal peripheral (QUP) v3 support. 16 QUP serial engines + 9 SSC-QUP serial engines ■ UART ■ I^2C ■ I3C ■ SPI 10 I^2C hubs
USB	■ One USB 3.1 ports: gen2 10 Gbps (DP + data), support Type-C with DisplayPort v1.4, embedded USB (eUSB) 2.0 ■ eUSB requires external repeater over eD+/eD-
UIM	Two 1.8 V/3 V SIM card using external level shifter
PCIe	2-lane Gen 3 2-lane Gen 4

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4) ■ SDC2: 1.2 V only; SD 3.0 ■ 1.8 V/3 V SD card operation using external level shifter ■ SDC4: dual-voltage, SDIO 3.0
Touchscreen support	■ Capacitive panels via ext IC (I^2C,I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display QFS4008, QFS2608, QFS2630
Configurable GPIOs	
Number of GPIOs	210 – GPIO_0 to GPIO_209
Internal functions (Security)	
Crypto	AES-GCM,"HW ECC & RSA" (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP 140-3 certifiable, PRNG compliant to NIST 800-90B
QFPROM	Fuse bits available for OEM use
Access Control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure boot/debug security with Sec Tools 2.0; easy to use tool set
Key management	Hardware key manager
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.3)
Hypervisor	Qualcomm® Type-1 Hypervisor enables multiple trusted VMs (TVMs)
DSP security	DSP secure domain
QTEE and TVM services	DRM Widevine V17 L1, HDCP v2.3, Qualcomm® Content Protection, camera security framework, Trusted UI framework, connection security (cellular and Wi-Fi), trusted location, QC WES device attestation service, QC WES secure provisioning service, QC WES 3rd party feature licensing service
SPU	SPU for SoC independent TCB
Boot	See *SM8550 Boot and CoreBSP Architecture Overview* (80-TBD-11) for the details of boot sequence. Emergency boot over USB 3.1
PLLs and clocks	■ 76.8 MHz X'tal ■ Multiple clock regimes; watchdog and sleep timers ■ Input: 38.4 MHz CXO ■ General-purpose outputs: M/N counter and PDM

Table 1-1 SM8550/SM8550P features (cont.)

Feature	SM8550/SM8550P capability
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	SPMI; also I^2C as needed
Wireless connectivity WLAN Bluetooth	 PCIe interface SLIMbus/UART interface
Fabrication technology, package, and major companion ICs	
Digital die	4 nm process
Package	1581 MPSP
PoP– small, thermally efficient package	15.6 × 14.0 × 0.56 mm
WLAN/BT RF PMIC Audio	WCN7850, WCN7851 SDR735 (4G/Sub-6/GNSS), SDR735G (GNSS), SMR546/QTM545 (mmW) PM8550, PMK8550, PM8550B/BH/BHS, PM8550VE/VS, PM8010 × 2, PMR735D WCD9380/WCD9385, WSA8840/WSA8845

2 Pin definitions

The SM8550/SM8550P is the lower device within a PoP system, as shown and explained in Figure 2-1.

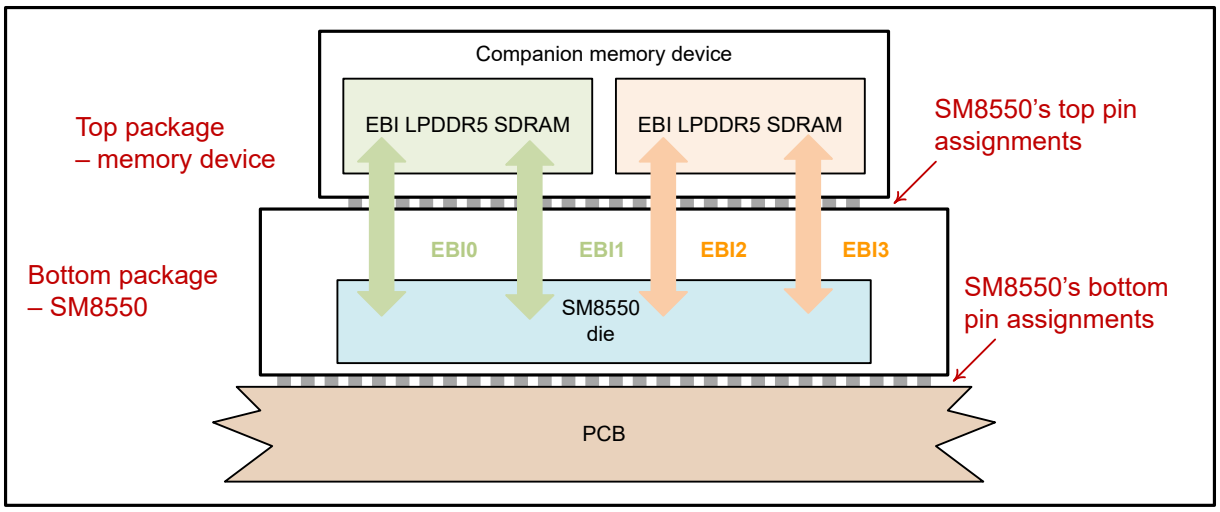


Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8550 bottom pins (Pin assignments: MSM bottom)
- SM8550 top pins (Pin assignments: MSM top)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits – 1.2 V unless otherwise noted	
PX0	Pad group 0 (SPMI0)
PX3	Pad group 3 (SPMI1, Modem, Audio SWR, Always-on camera control); 1.8 V
PX5	Pad group 5 (UIM0/UIM1)
PX7xx	Pad group 7xx (IO pad); 1.2 V/1.8 V
PX10	Pad group 10 (UFS IO)
PX11	Pad group 11 (CXO)
PX13	Pad group 13 (Secure processor); 1.85 V
PX14	Pad group 14 (SDC2, RESIN_N, PS_HOLD, SLEEP_CLK, MODE)

2.2 Pin assignments: MSM bottom

2.2.1 Pin map: MSM bottom

The SM8550/SM8550P is available in the MPSP1581 package. Its bottom surface is equivalent to an MPSP1581 that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Mechanical information for package details and Pin assignments: MSM top for information about the top pin assignments.

A high-level view of the pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM8550 Pin Assignment and GPIO Configuration Spreadsheet* (80-33265-1A). This Microsoft Excel spreadsheet lists all SM8550/SM8550P pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the *SM8550/SM8550P Pin Assignment and GPIO Configuration Spreadsheet* (80-33265-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-33265-1A

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

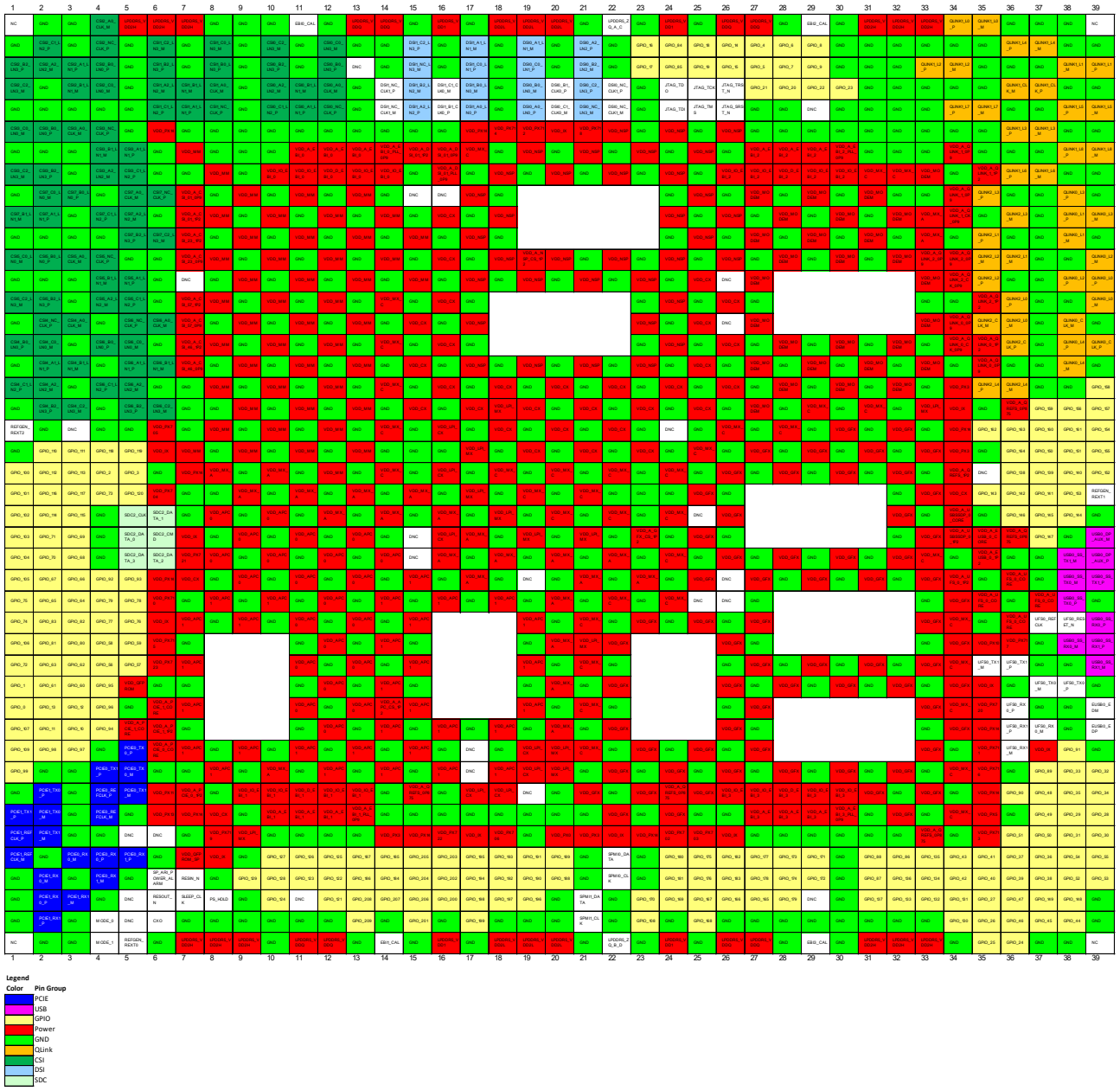


Figure 2-2 SM8550 bottom pin assignments (top view)

2.2.2 Pin descriptions: MSM bottom

The bottom pins are described in Table 2-2 through Table 2-4.

Table 2-2 MSM bottom pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D12	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - minus MIPI CSI 0 (C-PHY), trio lane 0 – A
E11	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - plus MIPI CSI 0 (C-PHY), trio lane 1 – A
D10	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - minus MIPI CSI 0 (C-PHY), trio lane 2 – A
C12	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - plus MIPI CSI 0 (C-PHY), trio lane 0 – B
D11	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - minus MIPI CSI 0 (C-PHY), trio lane 1 – B
C10	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - plus MIPI CSI 0 (C-PHY), trio lane 2 – B
B12	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - minus MIPI CSI 0 (C-PHY), trio lane 0 – C
E10	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - plus MIPI CSI 0 (C-PHY), trio lane 1 – C
B10	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - minus MIPI CSI 0 (C-PHY), trio lane 2 – C
E12	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - plus MIPI CSI 0 (C-PHY), no connect
D8	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - minus MIPI CSI 1 (C-PHY), trio lane 0 – A
E7	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - plus MIPI CSI 1 (C-PHY), trio lane 1 – A

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D6	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - minus MIPI CSI 1 (C-PHY), trio lane 2 – A
C8	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - plus MIPI CSI 1 (C-PHY), trio lane 0 – B
D7	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - minus MIPI CSI 1 (C-PHY), trio lane 1 – B
C6	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - plus MIPI CSI 1 (C-PHY), trio lane 2 – B
B8	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - minus MIPI CSI 1 (C-PHY), trio lane 0 – C
E6	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - plus MIPI CSI 1 (C-PHY), trio lane 1 – C
B6	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - minus MIPI CSI 1 (C-PHY), trio lane 2 – C
E8	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - plus MIPI CSI 1 (C-PHY), no connect
A4	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - minus MIPI CSI 2 (C-PHY), trio lane 0 – A
C3	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - plus MIPI CSI 2 (C-PHY), trio lane 1 – A
C2	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - minus MIPI CSI 2 (C-PHY), trio lane 2 – A
C4	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - plus MIPI CSI 2 (C-PHY), trio lane 0 – B
D3	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - minus MIPI CSI 2 (C-PHY), trio lane 1 – B
C1	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - plus MIPI CSI 2 (C-PHY), trio lane 2 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D4	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - minus MIPI CSI 2 (C-PHY), trio lane 0 – C
B2	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - plus MIPI CSI 2 (C-PHY), trio lane 1 – C
D1	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - minus MIPI CSI 2 (C-PHY), trio lane 2 – C
B4	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - plus MIPI CSI 2 (C-PHY), no connect
F3	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - minus MIPI CSI 3 (C-PHY), trio lane 0 – A
G5	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - plus MIPI CSI 3 (C-PHY), trio lane 1 – A
H4	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - minus MIPI CSI 3 (C-PHY), trio lane 2 – A
F2	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - plus MIPI CSI 3 (C-PHY), trio lane 0 – B
G4	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - minus MIPI CSI 3 (C-PHY), trio lane 1 – B
H2	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - plus MIPI CSI 3 (C-PHY), trio lane 2 – B
F1	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - minus MIPI CSI 3 (C-PHY), trio lane 0 – C
H5	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - plus MIPI CSI 3 (C-PHY), trio lane 1 – C
H1	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - minus MIPI CSI 3 (C-PHY), trio lane 2 – C
F4	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - plus MIPI CSI 3 (C-PHY), no connect

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
R3	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - minus MIPI CSI 4 (C-PHY), trio lane 0 – A
U2	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - plus MIPI CSI 4 (C-PHY), trio lane 1 – A
V2	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 - minus MIPI CSI 4 (C-PHY), trio lane 2 – A
T1	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - plus MIPI CSI 4 (C-PHY), trio lane 0 – B
U3	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - minus MIPI CSI 4 (C-PHY), trio lane 1 – B
W2	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - plus MIPI CSI 4 (C-PHY), trio lane 2 – B
T2	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - minus MIPI CSI 4 (C-PHY), trio lane 0 – C
V1	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 - plus MIPI CSI 4 (C-PHY), trio lane 1 – C
W3	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - minus MIPI CSI 4 (C-PHY), trio lane 2 – C
R2	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - plus MIPI CSI 4 (C-PHY), no connect
M3	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - minus MIPI CSI 5 (C-PHY), trio lane 0 – A
N5	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - plus MIPI CSI 5 (C-PHY), trio lane 1 – A
P4	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - minus MIPI CSI 5 (C-PHY), trio lane 2 – A
M2	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - plus MIPI CSI 5 (C-PHY), trio lane 0 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
N4	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - minus MIPI CSI 5 (C-PHY), trio lane 1 – B
P2	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - plus MIPI CSI 5 (C-PHY), trio lane 2 – B
M1	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - minus MIPI CSI 5 (C-PHY), trio lane 0 – C
P5	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - plus MIPI CSI 5 (C-PHY), trio lane 1 – C
P1	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - minus MIPI CSI 5 (C-PHY), trio lane 2 – C
M4	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - plus MIPI CSI 5 (C-PHY), no connect
R6	CSI6_A0_CLK_M	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential clock - minus MIPI CSI 6 (C-PHY), trio lane 0 – A
U5	CSI6_A1_LN1_P	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 1 - plus MIPI CSI 6 (C-PHY), trio lane 1 – A
V5	CSI6_A2_LN2_M	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 2 - minus MIPI CSI 6 (C-PHY), trio lane 2 – A
T4	CSI6_B0_LN0_P	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 0 - plus MIPI CSI 6 (C-PHY), trio lane 0 – B
U6	CSI6_B1_LN1_M	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 1 - minus MIPI CSI 6 (C-PHY), trio lane 1 – B
W5	CSI6_B2_LN3_P	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 3 - plus MIPI CSI 6 (C-PHY), trio lane 2 – B
T5	CSI6_C0_LN0_M	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 0 - minus MIPI CSI 6 (C-PHY), trio lane 0 – C
V4	CSI6_C1_LN2_P	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 2 - plus MIPI CSI 6 (C-PHY), trio lane 1 – C

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
W6	CSI6_C2_LN3_M	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential lane 3 - minus MIPI CSI 6 (C-PHY), trio lane 2 – C
R5	CSI6_NC_CLK_P	CSI	AI, AO	MIPI CSI 6 (D-PHY), differential clock - plus MIPI CSI 6 (C-PHY), no connect
J5	CSI7_A0_CLK_M	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential clock - minus MIPI CSI 7 (C-PHY), trio lane 0 – A
K2	CSI7_A1_LN1_P	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 1 - plus MIPI CSI 7 (C-PHY), trio lane 1 – A
K5	CSI7_A2_LN2_M	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 2 - minus MIPI CSI 7 (C-PHY), trio lane 2 – A
J3	CSI7_B0_LN0_P	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 0 - plus MIPI CSI 7 (C-PHY), trio lane 0 – B
K1	CSI7_B1_LN1_M	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 1 - minus MIPI CSI 7 (C-PHY), trio lane 1 – B
L5	CSI7_B2_LN3_P	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 3 - plus MIPI CSI 7 (C-PHY), trio lane 2 – B
J2	CSI7_C0_LN0_M	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 0 - minus MIPI CSI 7 (C-PHY), trio lane 0 – C
K4	CSI7_C1_LN2_P	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 2 - plus MIPI CSI 7 (C-PHY), trio lane 1 – C
L6	CSI7_C2_LN3_M	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential lane 3 - minus MIPI CSI 7 (C-PHY), trio lane 2 – C
J6	CSI7_NC_CLK_P	CSI	AI, AO	MIPI CSI 7 (D-PHY), differential clock - plus MIPI CSI 7 (C-PHY), no connect
BC6	CXO	PX11	DIS	Core crystal oscillator (digital 38.4 MHz system clock)
E19	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - plus MIPI DSI 0 (C-PHY), trio lane 0 – A

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B19	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - minus MIPI DSI 0 (C-PHY), trio lane 1 – A
B21	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - plus MIPI DSI 0 (C-PHY), trio lane 2 – A
D19	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - minus MIPI DSI 0 (C-PHY), trio lane 0 – B
D20	DSI0_B1_CLK0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - plus MIPI DSI 0 (C-PHY), trio lane 1 – B
C21	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - minus MIPI DSI 0 (C-PHY), trio lane 2 – B
C19	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - plus MIPI DSI 0 (C-PHY), trio lane 0 – C
E20	DSI0_C1_CLK0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - minus MIPI DSI 0 (C-PHY), trio lane 1 – C
D21	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - plus MIPI DSI 0 (C-PHY), trio lane 2 – C
E22	DSI0_NC_CLK1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - minus MIPI DSI 0 (C-PHY), no connect
D22	DSI0_NC_CLK1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - plus MIPI DSI 0 (C-PHY), no connect
E21	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - minus MIPI DSI 0 (C-PHY), no connect
E17	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - plus MIPI DSI 1 (C-PHY), trio lane 0 – A
B17	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - minus MIPI DSI 1 (C-PHY), trio lane 1 – A
E15	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - plus MIPI DSI 1 (C-PHY), trio lane 2 – A

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D17	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - minus MIPI DSI 1 (C-PHY), trio lane 0 – B
E16	DSI1_B1_CLK0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0 - plus MIPI DSI 1 (C-PHY), trio lane 1 – B
D15	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - minus MIPI DSI 1 (C-PHY), trio lane 2 – B
C17	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - plus MIPI DSI 1 (C-PHY), trio lane 0 – C
D16	DSI1_C1_CLK0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0 - minus MIPI DSI 1 (C-PHY), trio lane 1 – C
B15	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - plus MIPI DSI 1 (C-PHY), trio lane 2 – C
E14	DSI1_NC_CLK1_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 1 - minus MIPI DSI 1 (C-PHY), no connect
D14	DSI1_NC_CLK1_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 1 - plus MIPI DSI 1 (C-PHY), no connect
C15	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - minus MIPI DSI 1 (C-PHY), no connect
A11	EBI0_CAL	LPDDR5_VDDQ	AI	EBI0 calibration resistor
BD14	EBI1_CAL	LPDDR5_VDDQ	AI	EBI1 calibration resistor
A29	EBI2_CAL	LPDDR5_VDDQ	AI	EBI2 calibration resistor
BD29	EBI3_CAL	LPDDR5_VDDQ	AI	EBI3 calibration resistor
AN39	EUSB0_EDM	-	AI, AO	Embedded USB 0 high-speed data - minus
AP39	EUSB0_EDP	-	AI, AO	Embedded USB 0 high-speed data - plus
E26	JTAG_SRST_N	PX714	DIS-PU	JTAG reset for debug
D25	JTAG_TCK	PX714	DIS-PU	JTAG clock input
E24	JTAG_TDI	PX714	DIS-PU:nppdkp	JTAG data input

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D24	JTAG_TDO	PX714	DO-Z	JTAG data output
E25	JTAG_TMS	PX714	DI-PU:nppdkp	JTAG mode select input
D26	JTAG_TRST_N	PX714	DIS-PD:nppukp	JTAG reset
A22	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	AI	ZQ calibration reference for channels A and C
BD22	LPDDR5_ZQ_B_D	LPDDR5_VDDQ	AI	ZQ calibration reference for channels B and D
BC4	MODE_0	PX14	DIS	Mode control bit 0 – unconnected for native mode
BD4	MODE_1	PX14	DIS	Mode control bit 1 – unconnected for native mode
AV4	PCIE0_REFCLK_M	-	AI, AO	PCIe 0 Gen 3 reference clock - minus
AU4	PCIE0_REFCLK_P	-	AI, AO	PCIe 0 Gen 3 reference clock - plus
AY3	PCIE0_RX0_M	-	AI, AO	PCIe 0 Gen 3 receive - minus
AY4	PCIE0_RX0_P	-	AI, AO	PCIe 0 Gen 3 receive - plus
BA4	PCIE0_RX1_M	-	AI, AO	PCIe 0 Gen 3 receive - minus
AY5	PCIE0_RX1_P	-	AI, AO	PCIe 0 Gen 3 receive - plus
AT5	PCIE0_TX0_M	-	AI, AO	PCIe 0 Gen 3 transmit - minus
AR5	PCIE0_TX0_P	-	AI, AO	PCIe 0 Gen 3 transmit - plus
AU5	PCIE0_TX1_M	-	AI, AO	PCIe 0 Gen 3 transmit - minus
AT4	PCIE0_TX1_P	-	AI, AO	PCIe 0 Gen 3 transmit - plus
AY1	PCIE1_REFCLK_M	-	AI, AO	PCIe 1 Gen 3 reference clock - minus
AW1	PCIE1_REFCLK_P	-	AI, AO	PCIe 1 Gen 3 reference clock - plus
BA2	PCIE1_RX0_M	-	AI, AO	PCIe 1 Gen 3 receive - minus
BB2	PCIE1_RX0_P	-	AI, AO	PCIe 1 Gen 3 receive - plus
BB3	PCIE1_RX1_M	-	AI, AO	PCIe 1 Gen 3 receive - minus
BC2	PCIE1_RX1_P	-	AI, AO	PCIe 1 Gen 3 receive - plus
AV2	PCIE1_TX0_M	-	AI, AO	PCIe 1 Gen 3 transmit - minus
AU2	PCIE1_TX0_P	-	AI, AO	PCIe 1 Gen 3 transmit - plus
AW2	PCIE1_TX1_M	-	AI, AO	PCIe 1 Gen 3 transmit - minus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AV1	PCIE1_TX1_P	-	AI, AO	PCIe 1 Gen 3 transmit - plus
BB8	PS_HOLD	PX14	DO	Power-supply hold signal to PMIC
R38	QLINK0_CLK_M	-	AI, AO	Qlink0 clock - minus
T39	QLINK0_CLK_P	-	AI, AO	Qlink0 clock - plus
M39	QLINK0_L2_M	-	AI, AO	Qlink0 lane 0 - minus
N38	QLINK0_L2_P	-	AI, AO	Qlink0 lane 0 - plus
K39	QLINK0_L3_M	-	AI, AO	Qlink0 lane 1 - minus
J38	QLINK0_L3_P	-	AI, AO	Qlink0 lane 1 - plus
U38	QLINK0_L4_M	-	AI, AO	Qlink0 lane 2 - minus
T38	QLINK0_L4_P	-	AI, AO	Qlink0 lane 2 - plus
P39	QLINK0_L0_M	-	AI, AO	Qlink0 lane 0 - minus
N39	QLINK0_L0_P	-	AI, AO	Qlink0 lane 0 - plus
L38	QLINK0_L1_M	-	AI, AO	Qlink0 lane 1 - minus
K38	QLINK0_L1_P	-	AI, AO	Qlink0 lane 1 - plus
D36	QLINK1_CLK_M	-	AI, AO	Qlink1 clock - minus
D37	QLINK1_CLK_P		AI, AO	Qlink1 clock - plus
B37	QLINK1_L4_M	-	AI, AO	Qlink1 lane 0 - minus
B36	QLINK1_L4_P	-	AI, AO	Qlink1 lane 0 - plus
E35	QLINK1_L7_M	-	AI, AO	Qlink1 lane 1 - minus
E34	QLINK1_L7_P	-	AI, AO	Qlink1 lane 1 - plus
E39	QLINK1_L5_M	-	AI, AO	Qlink1 lane 2 - minus
E38	QLINK1_L5_P	-	AI, AO	Qlink1 lane 2 - plus
H37	QLINK1_L6_M	-	AI, AO	Qlink1 lane 3 - minus
H36	QLINK1_L6_P	-	AI, AO	Qlink1 lane 3 - plus
G39	QLINK1_L8_M	-	AI, AO	Qlink1 lane 4 - minus
G38	QLINK1_L8_P	-	AI, AO	Qlink1 lane 4 - plus
A35	QLINK1_L0_M	-	AI, AO	Qlink1 lane 0 - minus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
A34	QLINK1_L0_P	-	AI, AO	Qlink1 lane 0 - plus
C34	QLINK1_L2_M	-	AI, AO	Qlink1 lane 1 - minus
C33	QLINK1_L2_P	-	AI, AO	Qlink1 lane 1 - plus
C38	QLINK1_L1_M	-	AI, AO	Qlink1 lane 2 - minus
C39	QLINK1_L1_P	-	AI, AO	Qlink1 lane 2 - plus
F37	QLINK1_L3_M	-	AI, AO	Qlink1 lane 3 - minus
F36	QLINK1_L3_P	-	AI, AO	Qlink1 lane 3 - plus
R35	QLINK2_CLK_M	-	AI, AO	Qlink2 clock - minus
T36	QLINK2_CLK_P	-	AI, AO	Qlink2 clock - plus
M35	QLINK2_L2_M	-	AI, AO	Qlink2 lane 0 - minus
N35	QLINK2_L2_P	-	AI, AO	Qlink2 lane 0 - plus
K36	QLINK2_L3_M	-	AI, AO	Qlink2 lane 1 - minus
J35	QLINK2_L3_P	-	AI, AO	Qlink2 lane 1 - plus
V36	QLINK2_L4_M	-	AI, AO	Qlink2 lane 2 - minus
V35	QLINK2_L4_P	-	AI, AO	Qlink2 lane 2 - plus
R36	QLINK2_L0_M	-	AI, AO	Qlink2 lane 0 - minus
P36	QLINK2_L0_P	-	AI, AO	Qlink2 lane 0 - plus
M36	QLINK2_L1_M	-	AI, AO	Qlink2 lane 1 - minus
L35	QLINK2_L1_P	-	AI, AO	Qlink2 lane 1 - plus
BD5	REFGEN_REXT0	-	AI, AO	Reference voltage bias
AC39	REFGEN_REXT1	-	AI, AO	Reference voltage bias
Y1	REFGEN_REXT2	-	AI, AO	Reference voltage bias
BA7	RESIN_N	PX14	DI	Reset input
BB6	RESOUT_N	PX14	DO	Reset output
AD5	SDC2_CLK	PX14	B	Secure digital controller 2 clock
AE6	SDC2_CMD	PX14	B	Secure digital controller 2 command
AE5	SDC2_DATA_0	PX14	B	Secure digital controller 2 data bit 0

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AD6	SDC2_DATA_1	PX14	B	Secure digital controller 2 data bit 1
AF6	SDC2_DATA_2	PX14	B	Secure digital controller 2 data bit 2
AF5	SDC2_DATA_3	PX14	B	Secure digital controller 2 data bit 3
BB7	SLEEP_CLK	PX14	DIS	Sleep clock
BA22	SPMI0_CLK	PX0	DO	Slave and PBUS interface for PMICs – clock
AY22	SPMI0_DATA	PX0	BS-PD:nppukp	Slave and PBUS interface for PMICs – data
BC21	SPMI1_CLK	PX3	DO	Slave and PBUS interface for PMICs – clock
BB21	SPMI1_DATA	PX3	BS-PD:nppukp	Slave and PBUS interface for PMICs – data
BA6	SP_ARI_POWER_ALARM	PX13	DI	Power alarm
AJ37	UFS0_REFCLK	PX10	DO	UFS 0 reference clock
AJ38	UFS0_RESET_N	PX10	DO	UFS 0 reset
AP37	UFS0_RX0_M	-	AI, AO	UFS 0 receive 0 - minus
AN36	UFS0_RX0_P	-	AI, AO	UFS 0 receive 0 - plus
AR36	UFS0_RX1_M	-	AI, AO	UFS 0 receive 1 - minus
AP36	UFS0_RX1_P	-	AI, AO	UFS 0 receive 1 - plus
AM37	UFS0_TX0_M	-	AI, AO	UFS 0 transmit 0 - minus
AM38	UFS0_TX0_P	-	AI, AO	UFS 0 transmit 0 - plus
AL35	UFS0_TX1_M	-	AI, AO	UFS 0 transmit 1 - minus
AL36	UFS0_TX1_P	-	AI, AO	UFS 0 transmit 1 - plus
AE39	USB0_DP_AUX_M	-	AI, AO	USB 0 DisplayPort aux - minus
AF39	USB0_DP_AUX_P	-	AI, AO	USB 0 DisplayPort aux - plus
AK38	USB0_SS_RX0_M	-	AI	USB super-speed receive 0 - minus
AJ39	USB0_SS_RX0_P	-	AI	USB super-speed receive 0 - plus
AL39	USB0_SS_RX1_M	-	AI	USB super-speed receive 0 - minus
AK39	USB0_SS_RX1_P	-	AI	USB super-speed receive 0 - plus
AG38	USB0_SS_TX0_M	-	AO	USB super-speed transmit 0 - minus
AH38	USB0_SS_TX0_P	-	AO	USB super-speed transmit 0 - plus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AF38	USB0_SS_TX1_M	-	AO	USB super-speed transmit 0 - minus
AG39	USB0_SS_TX1_P	-	AO	USB super-speed transmit 0 - plus

[a] See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function - carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM8550/SM8550P GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the *SM8550/SM8550P Pin Assignment and GPIO Configuration Spreadsheet* (80-33265-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-33265-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AN1	GPIO_0		PX715	BS-PD:nppukp	Configurable I/O	Y
		CCI_I2C_SDA5			Camera 5 I^2C data	
		QUP2_SE0_L0_MIRB				
		IBI_I3C_QUP2_SE0_SDA_MIRB				
AM1	GPIO_1		PX715	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL5			Camera 5 I^2C clock	
		QUP2_SE0_L1_MIRB				
		IBI_I3C_QUP2_SE0_SCL_MIRB				
AB4	GPIO_2		PX705	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L0				
AB5	GPIO_3		PX705	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L1				
B27	GPIO_4		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L0				
C27	GPIO_5		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L1				
B28	GPIO_6		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE5_L0				
C28	GPIO_7		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE5_L1				
B29	GPIO_8		PX718	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE6_L0				
C29	GPIO_9		PX718	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE6_L1				
AP3	GPIO_10		PX723	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE7_L0				
		QDSS_CTI_TRIG0_OUT_MIRB			QDSS trigger output 0 B	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AP2	GPIO_11		PX723	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE7_L1				
		USB_PHY_PS_MIRB			USB PHY port select	
		QDSS_CTI_TRIG1_OUT_MIRB			QDSS trigger output 1 B	
AN3	GPIO_12		PX723	BS-PD:nppukp	Configurable I/O	N
AN2	GPIO_13		PX723	BS-PD:nppukp	Configurable I/O	N
B26	GPIO_14		PX712	BS-PD:nppukp	Configurable I/O	Y
C26	GPIO_15		PX718	BS-PD:nppukp	Configurable I/O	Y
B23	GPIO_16		PX712	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L0				
C23	GPIO_17		PX712	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L1				
B25	GPIO_18		PX712	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE1_L0				
C25	GPIO_19		PX712	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE1_L1				
D28	GPIO_20		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE2_L0				
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
D27	GPIO_21		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE2_L1				
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
D29	GPIO_22		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L0				
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	
D30	GPIO_23		PX718	BS-PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L1				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BD36	GPIO_24		PX716	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE7_L0				
BD35	GPIO_25		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L1				
BC35	GPIO_26		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L2				
		UIM1_PRESENT			UIM1 presence detection	
BB35	GPIO_27		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L3				
		UIM0_PRESENT			UIM0 presence detection	
AV39	GPIO_28		PX720	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L0				
		IBI_I3C_QUP1_SE0_SDA				
AV38	GPIO_29		PX720	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE0_L1				
		IBI_I3C_QUP1_SE0_SCL				
AW39	GPIO_30		PX720	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE0_L2				
AW38	GPIO_31		PX720	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L3				
AT39	GPIO_32		PX720	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L0				
		IBI_I3C_QUP1_SE1_SDA				
AT38	GPIO_33		PX720	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE1_L1				
		IBI_I3C_QUP1_SE1_SCL				
AU39	GPIO_34		PX720	BS-PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QUP1_SE1_L2				
AU38	GPIO_35		PX720	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L3				
AY37	GPIO_36		PX711	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE2_L0				
AY36	GPIO_37		PX711	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE2_L1				
BA37	GPIO_38		PX711	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE2_L2				
BA36	GPIO_39		PX711	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE2_L3				
BA35	GPIO_40		PX711	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L0				
		QUP1_SE2_L4_CS				
AY35	GPIO_41		PX711	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L1				
		QUP1_SE2_L5_CS				
BA34	GPIO_42		PX711	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE3_L2				
		QUP1_SE2_L6_CS				
AY34	GPIO_43		PX711	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L3				
		FORCED_USB_BOOT			Forced USB boot	
BC38	GPIO_44		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L0				
BC37	GPIO_45		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L1				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BC36	GPIO_46		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L2				
BB36	GPIO_47		PX716	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L3				
		DP_HOT_PLUG_DETECT			DisplayPort hot plug detect	
AU37	GPIO_48		PX717	BS-PD:nppukp	Configurable I/O	Y
		USB_PHY_PS_MIRA			USB PHY port select	
		QUP1_SE6_L0				
		QSPI_DATA[2]			Quad-SPI data	
		SDC4_DATA[2]			Secure digital controller 4 data bit [2]	
AV37	GPIO_49		PX717	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE6_L1				
		QSPI_DATA[3]			Quad-SPI data	
		SDC4_DATA[3]			Secure digital controller 4 data bit [3]	
AW37	GPIO_50		PX717	BS-PD:nppukp	Configurable I/O	N
		QUP1_SE6_L2				
		QSPI_CLK			Quad SPI clock	
		SDC4_CLK			Secure digital controller 4 clock	
AW36	GPIO_51		PX717	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L3				
		QSPI_CS_N_1			Quad-SPI chip select 1	
		SDC4_CMD			Secure digital controller 4 command	
BA38	GPIO_52		PX720	BS-PD:nppukp	Configurable I/O	N
		GRFC4_MIRB				
		QUP1_SE5_L0				
BA39	GPIO_53		PX720	BS-PD:nppukp	Configurable I/O	N
		GRFC5_MIRB				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QUP1_SE5_L1				
		GP_MN			General-purpose M/N:D counter output	
AY38	GPIO_54		PX720	BS-PD:nppukp	Configurable I/O	N
		GRFC6_MIRB				
		QUP1_SE5_L2				
AY39	GPIO_55		PX720	BS-PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L3				
AL4	GPIO_56		PX710	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L0_MIRA				
		IBI_I3C_QUP2_SE0_SDA_MIRA				
AL5	GPIO_57		PX710	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE0_L1_MIRA				
		IBI_I3C_QUP2_SE0_SCL_MIRA				
AK4	GPIO_58		PX710	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE0_L2_MIRA				
AK5	GPIO_59		PX710	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L3_MIRA				
		QDSS_GPIO_TRACEDATA_LOCB[6]			QDSS trace data 6 B	
AM3	GPIO_60		PX710	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L0				
		IBI_I3C_QUP2_SE1_SDA				
AM2	GPIO_61		PX710	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE1_L1				
		IBI_I3C_QUP2_SE1_SCL				
AL3	GPIO_62		PX710	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L2				
AL2	GPIO_63		PX710	BS-PD:nppukp	Configurable I/O	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QUP2_SE1_L3				
		QUP2_SE0_L4_CS				
AH3	GPIO_64		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE2_L0				
		TB_TRIG_SDC2				
		TGU_CH0_TRIGOUT				
		QDSS_GPIO_TRACEDATA_LOCB[4]			QDSS trace data 4 B	
AH2	GPIO_65		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE2_L1				
AG3	GPIO_66		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE2_L2				
		QUP2_SE0_L5_CS				
AG2	GPIO_67		PX704	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L3				
		QUP2_SE0_L6_CS				
AF3	GPIO_68		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE3_L0				
AE3	GPIO_69		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE3_L1				
AF2	GPIO_70		PX704	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE3_L2				
AE2	GPIO_71		PX704	BS-PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN0			Camera control interface async 0	
		QUP2_SE3_L3				
AL1	GPIO_72		PX710	BS-PD:nppukp	Configurable I/O	N
		CCI_ASYNC_IN1			Camera control interface async 1	
		QUP2_SE7_L0				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AC4	GPIO_73	CAM_DRI_IRQ	PX704	BS-PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[5]			QDSS trace data 5 B	
AJ1	GPIO_74		PX710	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA4			Camera 4 I2C Data	
		QUP2_SE7_L2				
AH1	GPIO_75		PX710	BS-PD:nppukp	Configurable I/O	Y
		CCI_I2C_SCL4			Camera 4 I2C clock	
		QUP2_SE7_L3				
		QDSS_CTI_TRIG0_IN_MIRB			QDSS trigger input 0 B	
AJ5	GPIO_76		PX721	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE6_L0				
AJ4	GPIO_77		PX721	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE6_L1				
AH5	GPIO_78		PX721	BS-PU:nppdkp	Configurable I/O	N
		QUP2_SE6_L2				
AH4	GPIO_79		PX721	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L3				
		QDSS_CTI_TRIG1_IN_MIRB			QDSS trigger input 1 B	
AK3	GPIO_80		PX721	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE5_L0				
AK2	GPIO_81		PX721	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE5_L1				
AJ3	GPIO_82		PX721	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L2				
AJ2	GPIO_83		PX721	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L3				
B24	GPIO_84		PX712	BS-PD:nppukp	Configurable I/O	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		I2CHUB0_SE9_L0				
C24	GPIO_85		PX712	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE9_L1				
AY32	GPIO_86		PX713	BS-PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA			MDP vertical sync – primary A	
		MDP_VSYNC0_OUT			MDP vertical sync 0 – out	
		MDP_VSYNC1_OUT			MDP vertical sync 1 – out	
		GCC_GP1_CLK_MIRB			General-purpose clock 1 B	
BA31	GPIO_87		PX713	BS-PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA			MDP vertical sync – secondary A	
		MDP_VSYNC2_OUT			MDP vertical sync 2 – out	
		MDP_VSYNC3_OUT			MDP vertical sync 3 – out	
		GCC_GP2_CLK_MIRB			General-purpose clock 2 B	
AY31	GPIO_88		PX713	BS-PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_E			MDP vertical sync – external	
		GCC_GP3_CLK_MIRB			General-purpose clock 3 B	
AT37	GPIO_89		PX717	BS-PD:nppukp	Configurable I/O	Y
		QSPI_DATA[0]			Quad-SPI data	
		SDC4_DATA[0]			Secure digital controller data	
AU36	GPIO_90		PX717	BS-PD:nppukp	Configurable I/O	N
		USB1_HS_AC_EN				
		QSPI_DATA[1]			Quad-SPI data	
		SDC4_DATA[1]			Secure digital controller data	
AR38	GPIO_91		PX717	BS-PD:nppukp	Configurable I/O	N
		QSPI_CS_N_0			Quad-SPI chip select 0	
AG4	GPIO_92 [b]		PX721	BS-PD:nppukp	Configurable I/O	N
		RESOUT_GPIO_N				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AG5	GPIO_93		PX14	BS-PD:nppukp	Configurable I/O	N
		SD_WRITE_PROTECT			Secure digital card write protection	
AP4	GPIO_94		PX721	BS-PD:nppukp	Configurable I/O	N
AM4	GPIO_95		PX721	BS-PU:nppdkp	Configurable I/O	Y
		PCIE0_CLK_REQ_N			PCIE0 clock request	
AN4	GPIO_96		PX721	BS-PD:nppukp	Configurable I/O	Y
AR3	GPIO_97		PX715	BS-PD:nppukp	Configurable I/O	N
AR2	GPIO_98		PX715	BS-PU:nppdkp	Configurable I/O	Y
		PCIE1_CLK_REQ_N			PCIE1 clock request	
AT1	GPIO_99		PX715	BS-PD:nppukp	Configurable I/O	Y
AB1	GPIO_100		PX705	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK0			Camera 0 MCLK	
		QDSS_GPIO_TRACEDATA_LOCB[11]			QDSS trace data 11 B	
AC1	GPIO_101		PX705	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK1			Camera 1 MCLK	
		QDSS_GPIO_TRACEDATA_LOCB[12]			QDSS trace data 12 B	
AD1	GPIO_102		PX705	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK2			Camera 2 MCLK	
		QDSS_GPIO_TRACEDATA_LOCB[0]			QDSS trace data 0 B	
AE1	GPIO_103		PX705	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK3			Camera 3 MCLK	
		QDSS_GPIO_TRACEDATA_LOCB[1]			QDSS trace data 1 B	
AF1	GPIO_104		PX704	BS-PD:nppukp	Configurable I/O	N
		CAM_AON_MCLK4				
		QDSS_GPIO_TRACEDATA_LOCB[2]			QDSS trace data 2 B	
AG1	GPIO_105		PX704	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK5			Camera 5 MCLK	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACEDATA_LOCB[3]			QDSS trace data 3 B	
AK1	GPIO_106		PX710	BS-PD:nppukp	Configurable I/O	N
		CAM_MCLK6			Camera 6 MCLK	
		QUP2_SE7_L1				
AP1	GPIO_107		PX715	BS-PD:nppukp	Configurable I/O	Y
		CAM_MCLK7			Camera 7 MCLK	
		QUP2_SE0_L3_MIRB				
BC23	GPIO_108		PX3	BS-PD:nppukp	Configurable I/O	N
AR1	GPIO_109		PX715	BS-PD:nppukp	Configurable I/O	N
		CCI_ASYNC_IN2			Camera control interface async 2	
		QUP2_SE0_L2_MIRB				
AA2	GPIO_110		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Camera 0 I2C Data	
		QDSS_GPIO_TRACEDATA_LOCB[7]			QDSS trace data 7 B	
AA3	GPIO_111		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Camera 0 I2C clock	
		QDSS_GPIO_TRACEDATA_LOCB[8]			QDSS trace data 8 B	
AB2	GPIO_112		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Camera 1 I2C data	
		QDSS_GPIO_TRACECLK_LOCB			QDSS trace clock B	
AB3	GPIO_113		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Camera 1 I2C clock	
		QDSS_GPIO_TRACECTL_LOCB			QDSS trace control B	
AD2	GPIO_114		PX704	BS-PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Camera 2 I2C Data	
		QDSS_GPIO_TRACEDATA_LOCB[9]			QDSS trace data 9 B	
AD3	GPIO_115		PX704	BS-PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		CCI_I2C_SCL2			Camera 2 I2C clock	
		QDSS_GPIO_TRACEDATA_LOCB[10]			QDSS trace data 10 B	
AC2	GPIO_116		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera 0 control interface timer	
		QDSS_GPIO_TRACEDATA_LOCB[13]			QDSS trace data 13 B	
AC3	GPIO_117		PX705	BS-PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera 1 control interface timer	
		QDSS_GPIO_TRACEDATA_LOCB[14]			QDSS trace data 14 B	
AA4	GPIO_118		PX705	BS-PD:nppukp	Configurable I/O	N
		QUP2_SE4_L2				
		CCI_TIMER2			Camera 2 control interface timer	
AA5	GPIO_119		PX705	BS-PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L3				
		CCI_TIMER3			Camera 3 control interface timer	
AC5	GPIO_120		PX704	BS-PD:nppukp	Configurable I/O	Y
		CCI_TIMER4			Camera 4 control interface timer	
		QDSS_GPIO_TRACEDATA_LOCB[15]			QDSS trace data 15 B	
		SSC_22			EGPIO - SSC IO 22	
		SSC_22:AON_CAM_RESET				
BB12	GPIO_121		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S1_SCK			I2S 1 clock	
BA12	GPIO_122		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S1_DATA0			I2S 1 serial data channel 0	
BA11	GPIO_123		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S1_WS				
BB10	GPIO_124		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S1_DATA1			I2S 1 serial data channel 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		AUDIO_EXT_MCLK1				
		AUDIO_REF_CLK			Audio reference clock	
AY12	GPIO_125		PX719	BS-PD:nppukp	Configurable I/O	N
		AUDIO_EXT_MCLK0				
AY11	GPIO_126		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S0_SCK			I2S 0 clock	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
AY10	GPIO_127		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S0_DATA0			I2S 0 serial data channel 0	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
BA10	GPIO_128		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S0_DATA1			I2S 0 serial data channel 1	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
BA9	GPIO_129		PX719	BS-PD:nppukp	Configurable I/O	N
		I2S0_WS				
BC34	GPIO_130		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM0_DATA			UIM0 data	
BB34	GPIO_131		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM0_CLK			UIM0 clock	
BB33	GPIO_132		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM0_RESET			UIM0 reset	
BB32	GPIO_133	DISP0_RESET_N	PX713	BS-PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRB			MDP vertical sync – secondary B	
BA33	GPIO_134		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM1_DATA			UIM1 data	
		GCC_GP1_CLK_MIRA			General-purpose clock 1 A	
		EUD_AUX_TDI				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AY33	GPIO_135		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM1_CLK			UIM1 clock	
		GCC_GP2_CLK_MIRA			General-purpose clock 2 A	
		EUD_AUX_TDO				
BA32	GPIO_136		PX5	BS-PD:nppukp	Configurable I/O	N
		UIM1_RESET			UIM1 reset	
		GCC_GP3_CLK_MIRA			General-purpose clock 3 A	
		EUD_AUX_SRST_N				
BB31	GPIO_137	DISP1_RESET_N	PX713	BS-PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRB			MDP vertical sync – primary B	
AB36	GPIO_138		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front end interface clock	
		GRFC0_MIRA				
		QDSS_GPIO_TRACEDATA_LOCA[0]			QDSS trace data 0 A	
AB37	GPIO_139		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front end interface data	
		GRFC1			Generic RF controller bit 1	
		QDSS_GPIO_TRACEDATA_LOCA[1]			QDSS trace data 1 A	
		BOOT_CONFIG[10]			Boot configuration bit 10	
AB38	GPIO_140		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front end interface clock	
		GRFC2			Generic RF controller bit 2	
		QDSS_GPIO_TRACEDATA_LOCA[2]			QDSS trace data 2 A	
AC37	GPIO_141		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front end interface data	
		GRFC3			Generic RF controller bit 3	
		QDSS_GPIO_TRACEDATA_LOCA[3]			QDSS trace data 3 A	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AC36	GPIO_142		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE2_CLK			RF front end interface clock	
		GRFC4_MIRA				
		QDSS_GPIO_TRACEDATA_LOCA[4]			QDSS trace data 4 A	
AC35	GPIO_143		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front end interface data	
		GRFC5_MIRA				
		QDSS_GPIO_TRACEDATA_LOCA[5]			QDSS trace data 5 A	
		BOOT_CONFIG[9]			Boot configuration bit 9	
AD38	GPIO_144		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE3_CLK			RF front end interface clock	
		GRFC6_MIRA				
		QDSS_GPIO_TRACEDATA_LOCA[6]			QDSS trace data 6 A	
AD37	GPIO_145		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE3_DATA			RF front end interface data	
		GRFC7			Generic RF controller bit 7	
		QDSS_GPIO_TRACEDATA_LOCA[7]			QDSS trace data 7 A	
		BOOT_CONFIG[8]			Boot configuration bit 8	
AD36	GPIO_146		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE4_CLK			RF front end interface clock	
		GRFC8			Generic RF controller bit 8	
AE37	GPIO_147		PX3	BS-PD:nppukp	Configurable I/O	N
		RFFE4_DATA			RF front end interface data	
		GRFC9			Generic RF controller bit 9	
BB38	GPIO_148		PX720	BS-PD:nppukp	Configurable I/O	Y
		COEX_UART1_RX			Interface between WCN7850/7851 and SM8550/SM8550P	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACECTL_LOCA			QDSS trace control A	
BB37	GPIO_149		PX720	BS-PD:nppukp	Configurable I/O	N
		COEX_UART1_TX			Interface between WCN7850/7851 and SM8550/SM8550P	
		QDSS_GPIO_TRACECLK_LOCA			QDSS trace clock A	
AA37	GPIO_150		PX3	BS-PD:nppukp	Configurable I/O	Y
		COEX_UART2_RX			Interface between WCN7850/7851 and SM8550/SM8550P	
		GRFC10			Generic RF controller bit 10	
		QDSS_GPIO_TRACEDATA_LOCA[8]			QDSS trace data 8 A	
		BOOT_CONFIG[3]			Boot configuration bit 3	
AA38	GPIO_151		PX3	BS-PD:nppukp	Configurable I/O	N
		COEX_UART2_TX			Interface between WCN7850/7851 and SM8550/SM8550P	
		GRFC11			Generic RF controller bit 11	
		QDSS_GPIO_TRACEDATA_LOCA[9]			QDSS trace data 9 A	
		BOOT_CONFIG[4]			Boot configuration bit 4	
AB39	GPIO_152		PX3	BS-PD:nppukp	Configurable I/O	N
		GRFC12			Generic RF controller bit 12	
		QDSS_GPIO_TRACEDATA_LOCA[10]			QDSS trace data 10 A	
		BOOT_CONFIG[6]			Boot configuration bit 6	
AC38	GPIO_153		PX3	BS-PD:nppukp	Configurable I/O	Y
		GRFC0_MIRB				
		NAV_GPIO2			GPS control signal 2	
		QDSS_GPIO_TRACEDATA_LOCA[11]			QDSS trace data 11 A	
		BOOT_CONFIG[7]			Boot configuration bit 7	
Y39	GPIO_154		PX3	BS-PD:nppukp	Configurable I/O	Y
		NAV_GPIO0			GPS control signal 0	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACEDATA_LOCA[12]			QDSS trace data 12 A	
		BOOT_CONFIG[5]			Boot configuration bit 5	
AA39	GPIO_155		PX3	BS-PD:nppukp	Configurable I/O	Y
		NAV_GPIO1			GPS control signal 1	
		QDSS_GPIO_TRACEDATA_LOCA[13]			QDSS trace data 13 A	
		BOOT_CONFIG[11]			Boot configuration bit 11	
W38	GPIO_156		PX3	BS-PD:nppukp	Configurable I/O	Y
		QLINK0_REQUEST			QLINK request	
		QDSS_GPIO_TRACEDATA_LOCA[14]			QDSS trace data 14 A	
W39	GPIO_157		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK0_ENABLE			QLINK ENABLE 0	
		QDSS_GPIO_TRACEDATA_LOCA[15]			QDSS trace data 15 A	
V39	GPIO_158		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK0_WMSS_RESET_N			SDR modem subsystem reset output	
		BOOT_CONFIG[2]			Boot configuration bit 2	
W37	GPIO_159		PX3	BS-PD:nppukp	Configurable I/O	Y
		QLINK1_REQUEST			QLINK REQUEST	
		QDSS_CTI_TRIG1_IN_MIRA			QDSS trigger input 1 A	
Y37	GPIO_160		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK1_ENABLE			QLINK ENABLE 1	
		QDSS_CTI_TRIG0_OUT_MIRA			QDSS trigger output 0 A	
Y38	GPIO_161		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK1_WMSS_RESET_N			SDR modem subsystem reset output	
		QDSS_CTI_TRIG1_OUT_MIRA			QDSS trigger output 1 A	
		BOOT_CONFIG[1]			Boot configuration bit 1	
Y35	GPIO_162		PX3	BS-PD:nppukp	Configurable I/O	Y
		QLINK2_REQUEST			QLINK REQUEST	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		QDSS_CTI_TRIG0_IN_MIRA			QDSS trigger input 0 A	
Y36	GPIO_163		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK2_ENABLE			QLINK ENABLE 2	
AA36	GPIO_164		PX3	BS-PD:nppukp	Configurable I/O	N
		QLINK2_WMSS_RESET_N			SDR modem subsystem reset output	
		BOOT_CONFIG[0]			Boot configuration bit 0	
BB27	GPIO_165		PX3	BS-PD:nppukp	Configurable I/O	N
		LPASS_0			EGPIO - LPASS IO 0	
		LPASS_0:SWR_TX_CLK			SoundWire transmit clock	
		LPASS_0:LPI_I2S0_SCK			LPI I2S clock	
BB26	GPIO_166		PX3	BS-PD:nppukp	Configurable I/O	Y
		LPASS_1			EGPIO - LPASS IO 1	
		LPASS_1:SWR_TX_DATA0			SoundWire transmit data 0	
		LPASS_1:LPI_I2S0_WS			LPI I2S serial data word select	
BB25	GPIO_167		PX3	BS-PD:nppukp	Configurable I/O	N
		LPASS_2			EGPIO - LPASS IO 2	
		LPASS_2:SWR_TX_DATA1			SoundWire transmit data 1	
		LPASS_2:LPI_I2S0_DATA0			LPI I2S 0 serial data channel 0	
BC25	GPIO_168		PX3	BS-PD:nppukp	Configurable I/O	N
		LPASS_3			EGPIO - LPASS IO 3	
		LPASS_3:SWR_RX_CLK			SoundWire receive clock	
		LPASS_3:LPI_I2S0_DATA1			LPI I2S 0 serial data channel 1	
BB24	GPIO_169		PX3	BS-PD:nppukp	Configurable I/O	Y
		LPASS_4			EGPIO - LPASS IO 4	
		LPASS_4:SWR_RX_DATA0			SoundWire receive data 0	
		LPASS_4:LPI_I2S0_DATA2			LPI I2S 0 serial data channel 2	
BB23	GPIO_170		PX3	BS-PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		LPASS_5			EGPIO - LPASS IO 5	
		LPASS_5:SWR_RX_DATA1			SoundWire receive data 1	
		LPASS_5:EXT_MCLK1_C			External MCLK 1 C	
		LPASS_5:LPI_I2S0_DATA3			LPI I2S 0 serial data channel 3	
AY29	GPIO_171		PX703	BS-PD:nppukp	Configurable I/O	Y
		LPASS_6			EGPIO - LPASS IO 6	
		LPASS_6:LPI_DMIC1_CLK			DMIC1 clock	
		LPASS_6:LPI_I2S1_CLK			LPI I2S 1 clock	
BA29	GPIO_172		PX703	BS-PD:nppukp	Configurable I/O	Y
		LPASS_7			EGPIO - LPASS IO 7	
		LPASS_7:LPI_DMIC1_DATA			DMIC1 data	
		LPASS_7:LPI_I2S1_WS			LPI I2S 1 serial data word select	
AY28	GPIO_173		PX703	BS-PD:nppukp	Configurable I/O	N
		LPASS_8			EGPIO - LPASS IO 8	
		LPASS_8:LPI_DMIC2_CLK			DMIC2 clock	
		LPASS_8:LPI_I2S1_DATA0			LPI I2S 1 serial data channel 0	
BA28	GPIO_174		PX703	BS-PD:nppukp	Configurable I/O	Y
		LPASS_9			EGPIO - LPASS IO 9	
		LPASS_9:LPI_DMIC2_DATA			DMIC2 data	
		LPASS_9:LPI_I2S1_DATA1			LPI I2S 1 serial data channel 1	
		LPASS_9:EXT_MCLK1_B			External MCLK 1 B	
AY25	GPIO_175		PX702	BS-PD:nppukp	Configurable I/O	N
		LPASS_10			EGPIO - LPASS IO 10	
		LPASS_10:LPI_I2S2_CLK			LPI I2S 2 clock	
		LPASS_10:WSA_SWR_CLK			SoundWire clock for WSA	
BA25	GPIO_176		PX702	BS-PD:nppukp	Configurable I/O	Y
		LPASS_11			EGPIO - LPASS IO 11	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		LPASS_11:LPI_I2S2_WS			LPI I2S 2 serial data word select	
		LPASS_11:WSA_SWR_DATA			SoundWire data for WSA	
AY27	GPIO_177		PX702	BS-PD:nppukp	Configurable I/O	Y
		LPASS_12			EGPIO - LPASS IO 12	
		LPASS_12:LPI_DMIC3_CLK			DMIC 3 clock	
		LPASS_12:LPI_I2S3_CLK			LPI I2S 3 clock	
BA27	GPIO_178		PX702	BS-PD:nppukp	Configurable I/O	N
		LPASS_13			EGPIO - LPASS IO 13	
		LPASS_13:LPI_DMIC3_DATA			DMIC3 data	
		LPASS_13:LPI_I2S3_WS			LPI I2S 3 serial data word select	
		LPASS_13:EXT_MCLK1_A			External MCLK 1 A	
BB28	GPIO_179		PX3	BS-PD:nppukp	Configurable I/O	N
		LPASS_14			EGPIO - LPASS IO 14	
		LPASS_14:SWR_TX_DATA2			SoundWire transmit data 2	
		LPASS_14:EXT_MCLK1_D			External MCLK 1 D	
AY24	GPIO_180		PX702	BS-PD:nppukp	Configurable I/O	N
		LPASS_15			EGPIO - LPASS IO 15	
		LPASS_15:LPI_I2S2_DATA0			LPI I2S 2 serial data channel 0	
		LPASS_15:WSA2_SWR_CLK			SoundWire clock for WSA2	
BA24	GPIO_181		PX702	BS-PD:nppukp	Configurable I/O	Y
		LPASS_16			EGPIO - LPASS IO 16	
		LPASS_16:LPI_I2S2_DATA1			LPI I2S 2 serial data channel 1	
		LPASS_16:WSA2_SWR_DATA			SoundWire data for WSA2	
AY26	GPIO_182		PX702	BS-PD:nppukp	Configurable I/O	Y
		LPASS_17			EGPIO - LPASS IO 17	
		LPASS_17:LPI_DMIC4_CLK			DMIC 4 clock	
		LPASS_17:LPI_I2S3_DATA0			LPI I2S 3 serial data channel 0	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BA26	GPIO_183		PX702	BS-PD:nppukp	Configurable I/O	N
		LPASS_18			EGPIO - LPASS IO 18	
		LPASS_18:LPI_DMIC4_DATA			DMIC4 data	
		LPASS_18:LPI_I2S3_DATA1			LPI I2S 3 serial data channel 1	
BA14	GPIO_184		PX722	BS-PD:nppukp	Configurable I/O	N
		LPASS_19			EGPIO - LPASS IO 19	
		LPASS_19:LPI_I2S4_CLK			LPI I2S 4 clock	
		LPASS_19:SLIMBUS_CLK			LPASS SLIMbus clock	
AY14	GPIO_185		PX722	BS-PD:nppukp	Configurable I/O	Y
		LPASS_20			EGPIO - LPASS IO 20	
		LPASS_20:LPI_I2S4_WS			LPI I2S 4 serial data word select	
		LPASS_20:SLIMBUS_DATA			LPASS SLIMbus data	
BA13	GPIO_186		PX722	BS-PD:nppukp	Configurable I/O	N
		LPASS_21			EGPIO - LPASS IO 21	
		LPASS_21:LPI_I2S4_DATA0			LPI I2S 4 serial data channel 0	
AY13	GPIO_187		PX722	BS-PD:nppukp	Configurable I/O	Y
		LPASS_22			EGPIO - LPASS IO 22	
		LPASS_22:LPI_I2S4_DATA1			LPI I2S 4 serial data channel 1	
		LPASS_22:EXT_MCLK1_E			External MCLK 1 E	
BA20	GPIO_188		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_0			EGPIO - SSC IO 0	
		SSC_0:SSC_QUP_SE0_L0				
AY20	GPIO_189		PX706	BS-PD:nppukp	Configurable I/O	N
		SSC_1			EGPIO - SSC IO 1	
		SSC_1:SSC_QUP_SE0_L1				
BA19	GPIO_190		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_2			EGPIO - SSC IO 2	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		SSC_2:SSC_QUP_SE1_L0				
AY19	GPIO_191		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_3			EGPIO - SSC IO 3	
		SSC_3:SSC_QUP_SE1_L1				
BA18	GPIO_192		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_4			EGPIO - SSC IO 4	
		SSC_4:SSC_QUP_SE2_L0				
AY18	GPIO_193		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_5			EGPIO - SSC IO 5	
		SSC_5:SSC_QUP_SE2_L1				
BA17	GPIO_194		PX706	BS-PD:nppukp	Configurable I/O	N
		SSC_6			EGPIO - SSC IO 6	
		SSC_6:SSC_QUP_SE2_L2				
		SSC_6:SSC_QUP_SE4_L4				
		SSC_6:SSC_GPIO_0_CLK				
AY17	GPIO_195		PX706	BS-PD:nppukp	Configurable I/O	N
		SSC_7			EGPIO - SSC IO 7	
		SSC_7:SSC_QUP_SE2_L3				
		SSC_7:SSC_QUP_SE4_L5				
		SSC_7:SSC_GPIO_1_CLK				
BB19	GPIO_196		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_8			EGPIO - SSC IO 8	
		SSC_8:SSC_QUP_SE3_L0				
		SSC_8:SSC_QUP_SE2_L4				
		SSC_8:SSC_GPIO_2_CLK				
BB18	GPIO_197		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_9			EGPIO - SSC IO 9	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		SSC_9:SSC_QUP_SE3_L1				
		SSC_9:SSC_GPIO_3_CLK				
BB17	GPIO_198		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_10			EGPIO - SSC IO 10	
		SSC_10:SSC_QUP_SE4_L0				
		SSC_10:SSC_GPIO_4_CLK				
BC17	GPIO_199		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_11			EGPIO - SSC IO 11	
		SSC_11:SSC_QUP_SE4_L1				
		SSC_11:SSC_GPIO_5_CLK				
BB16	GPIO_200		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_12			EGPIO - SSC IO 12	
		SSC_12:SSC_QUP_SE4_L2				
		SSC_12:SSC_GPIO_6_CLK				
BC15	GPIO_201		PX706	BS-PD:nppukp	Configurable I/O	Y
		SSC_13			EGPIO - SSC IO 13	
		SSC_13:SSC_QUP_SE4_L3				
		SSC_13:SSC_GPIO_7_CLK				
BA16	GPIO_202		PX722	BS-PD:nppukp	Configurable I/O	N
		SSC_14			EGPIO - SSC IO 14	
		SSC_14:SSC_QUP_SE5_L2				
		SSC_14:SSC_GPIO_8_CLK				
AY16	GPIO_203		PX722	BS-PD:nppukp	Configurable I/O	Y
		SSC_15			EGPIO - SSC IO 15	
		SSC_15:SSC_QUP_SE5_L3				
		SSC_15:SSC_GPIO_9_CLK				
BA15	GPIO_204		PX722	BS-PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
		SSC_16			EGPIO - SSC IO 16	
		SSC_16:SSC_QUP_SE6_L2				
		SSC_16:SSC_QUP_SE6_L0				
		SSC_16:SSC_QUP_SE1_L2				
		SSC_16:SSC_GPIO_10_CLK				
AY15	GPIO_205		PX722	BS-PD:nppukp	Configurable I/O	Y
		SSC_17			EGPIO - SSC IO 17	
		SSC_17:SSC_QUP_SE6_L3				
		SSC_17:SSC_QUP_SE6_L1				
		SSC_17:SSC_QUP_SE1_L3				
		SSC_17:SSC_GPIO_11_CLK				
BB15	GPIO_206		PX3	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE8_L0				
		SSC_18			EGPIO - SSC IO 18	
		SSC_18:SSC_QUP_SE7_L0				
BB14	GPIO_207		PX3	BS-PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE8_L1				
		SSC_19			EGPIO - SSC IO 19	
		SSC_19:SSC_QUP_SE7_L1				
BB13	GPIO_208		PX3	BS-PD:nppukp	Configurable I/O	Y
		AON_CCI_I2C_SDA3				
		SSC_20			EGPIO - SSC IO 20	
		SSC_20:SSC_QUP_SE8_L0				
BC13	GPIO_209		PX3	BS-PD:nppukp	Configurable I/O	Y
		AON_CCI_I2C_SCL3				
		SSC_21			EGPIO - SSC IO 21	
		SSC_21:SSC_QUP_SE8_L1				

[a] See Table 2-1 for parameter and acronym definitions.
[b] GPIO_92 will be with VDD_PX710 on SM8550 v2.

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins

Pad #	Pad name	Functional description
A1, A39, BD1, BD39	NC	No connect; not connected internally.
BB5, BC5, AF15, AT17, AH26, N26, J15, C13, BB11, E29, BB29, AW6, AW5, AB35, Y3, AD25, AE15, AG19, AG26, AH25, AR17, AU19, J16, N7, R26, Y24	DNC	Do not connect; connected internally, do not connect externally.

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
A2, A3, A8, A9, A10, A12, A15, A17, A21, A23, A25, A28, A30, A36, A37, A38, AA1, AA8, AA10, AA12, AA14, AA15, AA16, AA18, AA20, AA22, AA24, AA26, AA28, AA30, AA32, AA35, AB6, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AB25, AB27, AB29, AB31, AB33, AC7, AC8, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC23, AC24, AC26, AC32, AD4, AD7, AD9, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD33, AD35, AD39, AE4, AE8, AE10, AE12, AE14, AE18, AE20, AE22, AE24, AE26, AE32, AE38, AF4, AF9, AF11, AF13, AF17, AF19, AF21, AF23, AF25, AF27, AF29, AF31, AF34, AF36, AF37, AG8, AG10, AG12, AG14, AG16, AG18, AG20, AG22, AG24, AG28, AG30, AG32, AG35, AG37, AH7, AH9, AH11, AH13, AH15, AH17, AH19, AH21, AH23, AH27, AH33, AH36, AH39, AJ8, AJ10, AJ12, AJ14, AJ20, AJ22, AJ24, AJ26, AJ35, AK7, AK11, AK13, AK15, AK19, AK27, AK33, AK37, AL12, AL14, AL20, AL22, AL26, AL28, AL30, AL32, AL37, AL38, AM6, AM7, AM11, AM13, AM15, AM19, AM21, AM27, AM29, AM31, AM33, AM36, AM39, AN5, AN12, AN20, AN22, AN26, AN37, AN38, AP7, AP11, AP13, AP15, AP17, AP19, AP21, AP27, AP33, AP38, AR4, AR8, AR10, AR12, AR14, AR16, AR18, AR22, AR24, AR26, AR34, AR39, AT2, AT3, AT6, AT7, AT9, AT11, AT13, AT15, AT21, AT23, AT25, AT27, AT29, AT31, AT33, AT36, AU1, AU3, AU8, AU14, AU16, AU20, AU22, AU32, AU34, AV3, AV5, AV9, AV14, AV15, AV16, AV17, AV18, AV19, AV20, AV21, AV23, AV25, AV26, AV31, AV33, AV36, AW3, AW4, AW7, AW10, AW11, AW12, AW13, AW19, AW27, AW28, AW29, AW30, AW31, AW32, AW34, AY2, AY6, AY9, AY21, AY23, AY30, B1, B3, B5, B7, B9, B11, B13, B14, B16, B18, B20, B22, B30, B31, B32, B33, B34, B35, B38, B39, BA1, BA3, BA5, BA8, BA21, BA23, BA30, BB1, BB4, BB9, BB20, BB22, BB30, BB39, BC1, BC3, BC7, BC8, BC9, BC10, BC11, BC12, BC14, BC16, BC18, BC19, BC20, BC22, BC24, BC26, BC27, BC28, BC29, BC30, BC31, BC32, BC33, BC39, BD2, BD3, BD6, BD10, BD13, BD15, BD17, BD21, BD23, BD25, BD28, BD30, BD34, BD37, BD38, C5, C7, C9, C11, C14, C16, C18, C20, C22, C30, C31, C32, C35, C36, C37, D2, D5, D9, D13, D18, D23, D31, D32, D33, D34, D35, D38, D39, E1, E2, E3, E4, E5, E9, E13, E18, E23, E27, E28, E30, E31, E32, E33, E36, E37, F5, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F23, F25, F27, F28, F29, F30, F31, F32, F33, F34, F35, F38, F39, G1, G2, G3, G6, G8, G9, G10, G18, G20, G22, G24, G26, G31, G32, G33, G35, G36, G37, H3, H6, H7, H9, H15, H17, H19, H21, H23, H25, H34, H38, H39, J1, J4, J8, J10, J12, J14, J18, J24, J26, J28, J30, J32, J33, J36, J37, J39, K3, K6, K9, K11, K13, K15, K17, K25, K27, K29, K31, K35, K37, L1, L2, L3, L4, L8, L10, L12, L14, L16, L18, L24, L26, L28, L30, L32, L34, L36, L37, L39, M5, M6, M9, M11, M13, M15, M17, M21, M23, M25, M27, M29, M31, M37, M38, N1, N2, N3, N6, N8, N10, N12, N14, N16, N18, N20, N22, N24, N36, N37, P3, P6, P9, P11, P13, P15, P17, P23, P25, P27, P33, P34, P37, P38, R1, R4, R8, R10, R12, R14, R16, R24, R37, R39, T3, T6, T9, T11, T13, T15, T17, T23, T25, T27, T29, T31, T33, T37, U1, U4, U8, U10, U12, U14, U16, U18, U20, U22, U24, U26, U28, U30, U32, U34, U36, U37, U39, V3, V6, V7, V9, V11, V13, V15, V17, V19, V21, V23, V25, V27, V29, V31, V33, V37, V38, W1, W4, W7, W8, W10, W12, W14, W16, W20, W22, W24, W26, W28, W30, W32, W35, Y2, Y4, Y5, Y7, Y9, Y11, Y13, Y15, Y17, Y19, Y21, Y23, Y25, Y27, Y29, Y31, Y33	GND	Ground
A16, A24, BD16, BD24	LPDDR5_VDD1	Power for PoP LPDDR5 memory core

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
A5, A6, A7, A31, A32, A33, BD7, BD8, BD9, BD31, BD32, BD33	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core
A18, A19, A20, BD18, BD19, BD20	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core
A13, A14, A26, A27, BD11, BD12, BD26, BD27	LPDDR5_VDDQ	Power for PoP LPDDR5 memory core
AD8, AD10, AE9, AE11, AE13, AF8, AF10, AF12, AF14, AG9, AG11, AG13, AH12, AJ11, AJ13, AK12, AL11, AL13, AM12, AN11, AN13, AP12	VDD_APC0	Power for the Kryo Silver application processor
AG15, AH8, AH10, AH14, AH16, AH18, AJ7, AJ9, AJ15, AJ19, AK14, AL7, AL15, AL19, AM14, AN7, AN15, AN19, AP14, AP16, AP18, AR7, AR9, AR11, AR13, AR15, AT8, AT12, AT14, AT16, AT18	VDD_APC1	Power for the Kryo Gold application processor
AN14	VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits
J7	VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits
K7	VDD_A_CSI_01_1P2	Power for MIPI CSI01 1.2 V analog circuits
M7	VDD_A_CSI_23_0P9	Power for MIPI CSI23 0.9 V analog circuits
L7	VDD_A_CSI_23_1P2	Power for MIPI CSI23 1.2 V analog circuits
U7	VDD_A_CSI_46_0P9	Power for MIPI CSI46 0.9 V analog circuits
T7	VDD_A_CSI_46_1P2	Power for MIPI CSI46 1.2 V analog circuits
R7	VDD_A_CSI_57_0P9	Power for MIPI CSI57 0.9 V analog circuits
P7	VDD_A_CSI_57_1P2	Power for MIPI CSI57 1.2 V analog circuits
G16	VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits
G15	VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits
H16	VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI(01) PLL 0.9 V
G11, G12, G13	VDD_A_EBI_0	Power for EBI0 PHY
G14	VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits
AV10, AV11, AV12	VDD_A_EBI_1	Power for EBI1 PHY
AV13	VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits
G27, G28, G29	VDD_A_EBI_2	Power for EBI2 PHY
G30	VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits
AV27, AV28, AV29	VDD_A_EBI_3	Power for EBI3 PHY
AV30	VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AF35	VDD_A_EUSB_0_1P2	Power for eUSB 1.2 V analog circuits
AE35	VDD_A_EUSB_0_CORE	Power for eUSB core analog circuits
AE23	VDD_A_GFX_CS_1P2	Power for GFX current sensor
M19	VDD_A_NSP_CS_1P2	Power for NSP current sensor
AU7	VDD_A_PCIE_0_1P2	Power for PCIE0 1.2 V circuit
AR6	VDD_A_PCIE_0_CORE	Power for PCIe0 core circuits
AP6	VDD_A_PCIE_1_1P2	Power for PCIE1 1.2 V circuit
AN6, AP5	VDD_A_PCIE_1_CORE	Power for PCIe1 core circuits
R34, U35	VDD_A_QLINK_0_0P9	Power for QLink0 (0.9 V)
T35	VDD_A_QLINK_0_1P2	Power for QLink0 (1.2 V)
T34	VDD_A_QLINK_0_CK_0P9	Power for QLink0 clock circuit
G34, J34	VDD_A_QLINK_1_0P9	Power for QLink1 (0.9 V)
H35	VDD_A_QLINK_1_1P2	Power for QLink1 (1.2 V)
K34	VDD_A_QLINK_1_CK_0P9	Power for QLink1 clock circuit
M33, M34	VDD_A_QLINK_2_0P9	Power for QLink2 (0.9 V)
P35	VDD_A_QLINK_2_1P2	Power for QLink2 (1.2 V)
N34	VDD_A_QLINK_2_CK_0P9	Power for QLink2 clock circuit
AU15, AU24, AW33, AE36, W36	VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits
AB34	VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V analog circuits
AG34	VDD_A_UFS_0_1P2	Power for the UFS0 1.2 V analog circuits
AG36, AH35, AH37, AJ36	VDD_A_UFS_0_CORE	Power for the UFS0 core analog circuits
AE34	VDD_A_USBSSDP_0_1P2	Power for USB super-speed and DisplayPort 1.2 V analog circuits
AD34	VDD_A_USBSSDP_0_CORE	Power for USB super-speed and DisplayPort core analog circuits
AA19, AA21, AA23, AC34, AG7, AV8, K16, M16, N25, P16, P26, R15, R25, T16, T26, U15, U25, V16, V18, V20, V22, V24, V26, W15, W17, W19, W21, W23, W25, Y18, Y20, Y22	VDD_CX	Power for digital core circuits
H12	VDD_D_EBI_0	Power for EBI_0 digital circuits

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AU11	VDD_D_EBI_1	Power for EBI_1 digital circuits
H28	VDD_D_EBI_2	Power for EBI_2 digital circuits
AU28	VDD_D_EBI_3	Power for EBI_3 digital circuits
AA27, AA29, AA31, AA33, AB26, AB28, AB30, AB32, AC25, AC33, AD26, AD32, AE25, AE33, AF26, AF28, AF30, AF32, AG25, AG27, AG29, AG31, AG33, AH34, AJ23, AJ25, AJ27, AJ33, AK22, AK26, AK34, AL27, AL29, AL31, AL33, AM22, AM26, AM28, AM30, AM32, AM34, AN27, AN33, AP22, AP26, AP34, AR23, AR25, AR27, AR33, AT22, AT24, AT26, AT28, AT30, AT32, AU21, AU23, AU25, AU31, AU33, AV22, AV24, AV32, Y30, Y32	VDD_GFX	Power for graphics
H10, H11, H13, H14	VDD_IO_EBI_0	Power for the EBI_0 I/O circuits
AU9, AU10, AU12, AU13	VDD_IO_EBI_1	Power for the EBI_1 I/O circuits
H26, H27, H29, H30	VDD_IO_EBI_2	Power for the EBI_2 I/O circuits
AU26, AU27, AU29, AU30	VDD_IO_EBI_3	Power for the EBI_3 I/O circuits
AA6, AE7, AJ6, AY8, AW17, AW22, AW26, AM35, AR37, W34, F20	VDD_IX	Power for dual voltage pads (0.9 V)
AB16, AE16, AR19, AT19, AU17, AU18, Y16	VDD_LPI_CX	Power for LPI digital core circuits
AA17, AC17, AD18, AE19, AE21, AK21, AR20, AT20, W18, AW9, W33	VDD_LPI_MX	Power for low-power island memory circuits
AA7, AA9, AA11, AA13, AB12, G7, H8, J9, J11, J13, K8, K10, K12, K14, L9, L11, L13, L15, M8, M10, M12, M14, N9, N11, N13, N15, P8, P10, P12, R9, R11, R13, T8, T10, T12, U9, U11, U13, V8, V10, V12, W9, W11, W13, Y8, Y10, Y12	VDD_MM	Power for multimedia subsystem circuits
H33, J27, J29, J31, K28, K30, K32, L27, L29, L31, M28, M30, M32, N27, N33, R27, R33, T28, T30, T32, U27, U29, U31, U33, V28, V30, V32, W27	VDD_MODEM	Power for modem circuits
AB8, AB10, AC9, AC11, AC13, AC15, AD12, AD14, AD16, AE17, AF16, AF18, AF20, AF22, AG17, AG21, AG23, AH20, AK20, AM20, AP20, AT10, K33, L33	VDD_MX_A	Power for memory circuits
AA25, AB14, AB18, AB20, AB22, AB24, AC19, AC21, AD20, AD22, AD24, AF24, AF33, AH22, AH24, AJ21, AJ34, AL21, AL34, AN21, AN34, AR21, AT34, AV34, G17, H31, H32, P14, T14, V14, W29, W31, Y14, Y26, Y28	VDD_MX_C	Power for memory circuits
F22, F24, F26, G19, G21, G23, G25, H18, H20, H22, H24, J17, J25, K18, K24, K26, L17, L25, M18, M20, M22, M24, M26, N17, N19, N21, N23, P24, R17, R23, T24, U17, U19, U21, U23	VDD_NSP	Power for NSP circuits
AW20	VDD_PX0	Power for pad group 0
AK35	VDD_PX10	Power for pad group 10
AU6	VDD_PX11	Power for pad group 11
AV6	VDD_PX13	Power for pad group 13

Table 2-4 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AA34, AW14, AW21, V34	VDD_PX3	Power for pad group 3
AB7, AG6, AV7, AW15, AW23, AP35, AU35, Y34, F17, F6	VDD_PX14	Power for pad group 14
AV35	VDD_PX5	Power for pad group 5
AW24	VDD_PX702	Power for pad group 702
AW25	VDD_PX703	Power for pad group 703
AC6	VDD_PX704	Power for pad group 704
Y6	VDD_PX705	Power for pad group 705
AW18	VDD_PX706	Power for pad group 706
AH6	VDD_PX710	Power for pad group 710
AR35	VDD_PX711	Power for pad group 711
F19	VDD_PX712	Power for pad group 712
AW35	VDD_PX713	Power for pad group 713
F18	VDD_PX714	Power for pad group 714
AK6	VDD_PX715	Power for pad group 715
AT35	VDD_PX716	Power for pad group 716
AK36	VDD_PX717	Power for pad group 717
F21	VDD_PX718	Power for pad group 718
AW8	VDD_PX719	Power for pad group 719
AN35	VDD_PX720	Power for pad group 720
AF7	VDD_PX721	Power for pad group 721
AW16	VDD_PX722	Power for pad group 722
AL6	VDD_PX723	Power for pad group 723
AM5	VDD_QFPROM	Power for programming the QFPROM
AY7	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit

2.3 Pin assignments: MSM top

2.3.1 Pin map: MSM top

The SM8550/SM8550P is available in the MPSP1581. See Mechanical information for package details and Pin assignments: MSM bottom for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3.

The text within Figure 2-3 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in Pin map: MSM bottom.

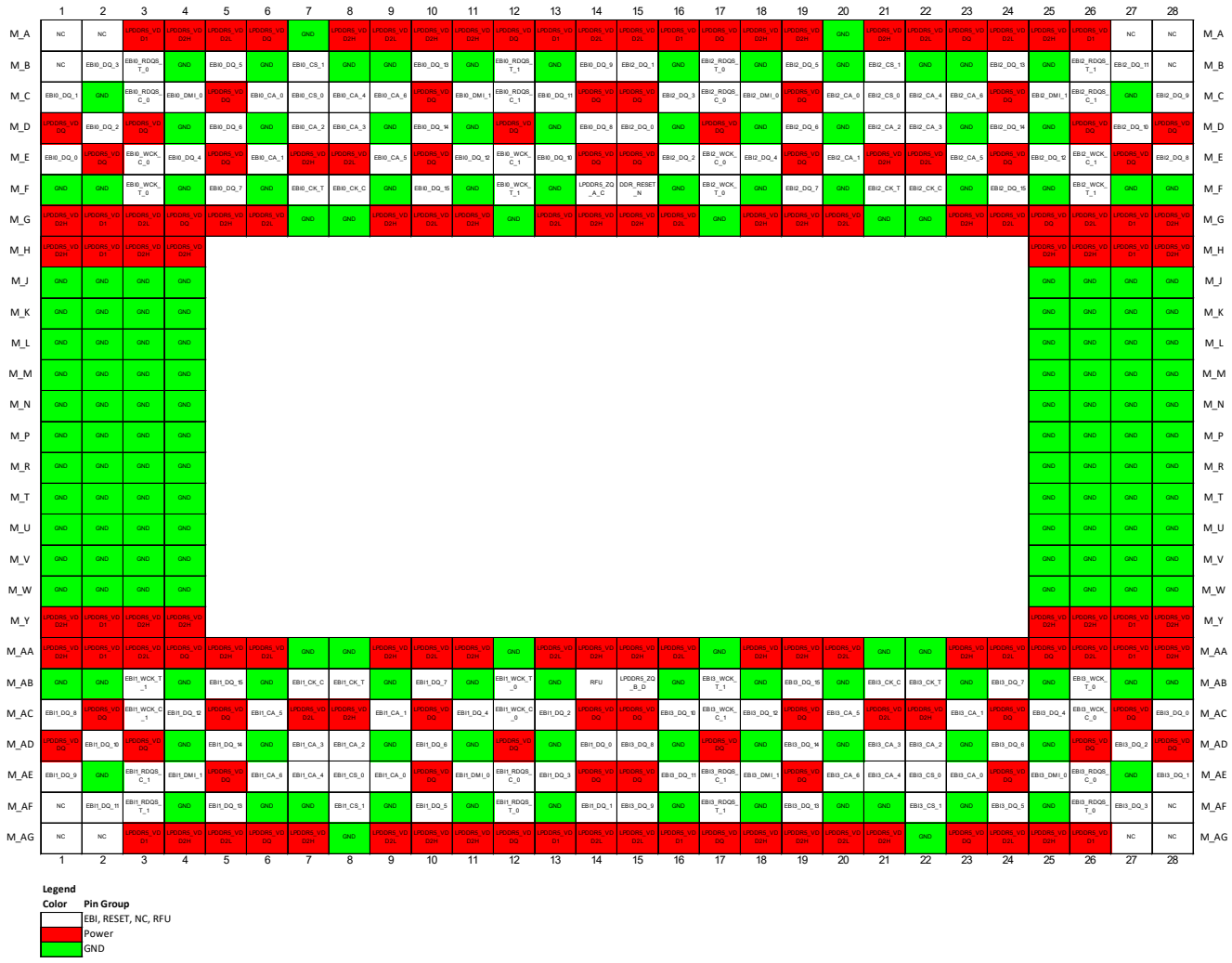


Figure 2-3 SM8550 top pin LPDDR5 assignments (top view)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in Table 2-5 and Table 2-6

Table 2-5 MSM top pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics		Functional description
		Voltage	Type	
M_F15	DDR_RESET_N	LPDDR5_VDD2H	DO	LPDDR5 reset
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock (C)
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock (T)
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics		Functional description
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9
M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 (C)
M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 (C)
M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 (T)
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 (T)
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (C)
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (C)
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (T)
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (T)
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0
M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 1
M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5 command/address bit 2
M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 3
M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 4
M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 5
M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock (C)
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock (T)
M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5 chip select 0
M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5 chip select 1
M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR5 data mask for byte 0

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics		Functional description
M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR5 data mask for byte 1
M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0
M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1
M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10
M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11
M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12
M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13
M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14
M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15
M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2
M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3
M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4
M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5
M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6
M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7
M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8
M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9
M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 (C)
M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 (C)
M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 (T)
M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 (T)
M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (C)
M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (C)
M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (T)
M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (T)
M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5 command/address bit 0
M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5 command/address bit 1

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics		Functional description
M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5 command/address bit 2
M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5 command/address bit 3
M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5 command/address bit 4
M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5 command/address bit 5
M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5 differential clock (C)
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5 differential clock (T)
M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5 chip select 0
M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5 chip select 1
M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR5 data mask for byte 0
M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR5 data mask for byte 1
M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5 data bit 0
M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5 data bit 1
M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5 data bit 10
M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5 data bit 11
M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5 data bit 12
M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5 data bit 13
M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5 data bit 14
M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5 data bit 15
M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5 data bit 2
M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5 data bit 3
M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5 data bit 4
M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5 data bit 5
M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5 data bit 6
M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5 data bit 7
M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5 data bit 8
M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5 data bit 9

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics		Functional description
M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 (C)
M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 (C)
M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 (T)
M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 (T)
M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (C)
M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (C)
M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (T)
M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (T)
M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5 command/address bit 0
M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5 command/address bit 1
M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5 command/address bit 2
M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5 command/address bit 3
M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5 command/address bit 4
M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5 command/address bit 5
M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5 differential clock (C)
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5 differential clock (T)
M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5 chip select 0
M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5 chip select 1
M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR5 data mask for byte 0
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR5 data mask for byte 1
M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5 data bit 0
M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5 data bit 1
M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5 data bit 10
M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5 data bit 11
M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5 data bit 12
M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5 data bit 13

Table 2-5 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics		Functional description
M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5 data bit 14
M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5 data bit 15
M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5 data bit 2
M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5 data bit 3
M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5 data bit 4
M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5 data bit 5
M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5 data bit 6
M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5 data bit 7
M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5 data bit 8
M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5 data bit 9
M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 (C)
M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 (C)
M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 (T)
M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 (T)
M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (C)
M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (C)
M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (T)
M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (T)
M_F14	LPDDR5_ZQ_A_C	-	Reference	ZQ calibration reference (channels A and C)
M_AB15	LPDDR5_ZQ_B_D	-	Reference	ZQ calibration reference (channels B and D)

[a] See Table 2-1 for parameter and acronym definitions[a]

Table 2-6 MSM top pin descriptions – ground, NC, and power-supply pins

Pad #	Pad name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground
M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally
M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16, M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27	LPDDR5_VDD1	Power for PoP LPDDR5 memory core
M_A4, M_A8, M_A10, M_A11, M_A18, M_A19, M_A21, M_A25, M_AA1, M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_E21, M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_Y25, M_Y26, M_Y28	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core
M_A5, M_A9, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10, M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_G20, M_G24, M_G26	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core
M_A6, M_A12, M_A17, M_A23, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10, M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_E27, M_G4, M_G25	LPDDR5_VDDQ	Power for PoP LPDDR5 memory core
M_AB14	RFU	Reserved pins

3 Electrical specifications

3.1 Absolute maximum ratings

This information will be included in future revisions of this document.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-1).

Table 3-1 Operating conditions for voltage rails with AVS Type-1

Parameter [a]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor	TBD	TBD	V
VDD_APC1	Qualcomm Kryo Gold application processor	TBD	TBD	V
VDD_GFX	Graphics	TBD	TBD	V
VDD_CX VDD_D_EBI_0 VDD_D_EBI_1 VDD_D_EBI_2 VDD_D_EBI_3	Digital core circuits EBI0 PHY digital circuits EBI1 PHY digital circuits EBI2 PHY digital circuits EBI3 PHY digital circuits	TBD	TBD	V
VDD_LPI_CX	Low power island core	TBD	TBD	V
VDD_LPI_MX	Low power island memory	TBD	TBD	V
VDD_MM	Multimedia subsystem circuits	TBD	TBD	V
VDD_MODEM	Modem	TBD	TBD	V
VDD_MX_A	On-chip memory	TBD	TBD	V
VDD_MX_C	On-chip power-collapsible memory	TBD	TBD	V
VDD_NSP	NSP	TBD	TBD	V
VDD_A_EBI_0 VDD_A_EBI_1 VDD_A_EBI_2 VDD_A_EBI_3 VDD_A_EBI_0_PLL_0P9 VDD_A_EBI_1_PLL_0P9 VDD_A_EBI_2_PLL_0P9 VDD_A_EBI_3_PLL_0P9	EBI0 PHY circuits EBI1 PHY circuits EBI2 PHY circuits EBI3 PHY circuits EBI0 PLL circuits EBI1 PLL circuits EBI2 PLL circuits EBI3 PLL circuits	TBD	TBD	V

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-2 Operating conditions for non AVS voltage rails

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_CSI_01_0P9	MIPI CSI0, CSI1 0.9V circuits	TBD	0.875	TBD	V
VDD_A_CSI_23_0P9	MIPI CSI2, CSI3 0.9 V circuits				
VDD_A_CSI_46_0P9	MIPI CSI4, CSI6 0.9 V circuits				
VDD_A_CSI_57_0P9	MIPI CSI5, CSI7 0.9 V circuits				
VDD_A_DSI_01_0P9	MIPI DSI0, DSI1 0.9 V circuits				
VDD_A_DSI_01_PLL_0P9	MIPI DSI0, DSI1 PLL 0.9 V circuits				
VDD_A_PCIE_0_CORE	PCIe0 core circuits				
VDD_A_EUSB_0_CORE	eUSB0 core circuits				
VDD_A_PCIE_1_CORE	PCIe1 core circuits	TBD	0.875	TBD	V
VDD_A_UFS_0_CORE	UFS0 core circuits	TBD	0.875	TBD	V
VDD_A_QLINK_0_0P9	Qlink0 0.9 V circuits	TBD	0.912	TBD	V
VDD_A_QLINK_2_0P9	Qlink2 0.9 V circuits				
VDD_A_QLINK_0_CK_0P9	Qlink0 clock circuits				
VDD_A_QLINK_2_CK_0P9	Qlink2 clock circuits				
VDD_A_QLINK_1_0P9	Qlink1 0.9 V circuits	TBD	0.912	TBD	V
VDD_A_QLINK_1_CK_0P9	Qlink1 clock circuits				
VDD_A_USBSSDP_0_CORE	USB0 SS and DisplayPort core circuits	TBD	0.875	TBD	V
VDD_A_CSI_01_1P2	MIPI CSI0, CSI1 1.2 V circuits	TBD	1.2	TBD	V
VDD_A_CSI_23_1P2	MIPI CSI2, CSI3 1.2 V circuits				
VDD_A_CSI_46_1P2	MIPI CSI4, CSI6 1.2 V circuits				
VDD_A_CSI_57_1P2	MIPI CSI5, CSI7 1.2 V circuits				
VDD_A_DSI_01_1P2	MIPI DSI 1.2 V circuits				
VDD_A_PCIE_0_1P2	PCIe0 1.2 V circuits				
VDD_A_PCIE_1_1P2	PCIe1 1.2 V circuits				
VDD_A_EUSB_0_1P2	eUSB0 1.2 V circuits				
VDD_A_UFS_0_1P2	UFS0 1.2 V circuits				
VDD_A_USBSSDP_0_1P2	USB0 SS and DisplayPort 1.2 V circuits				
VDD_A_QLINK_0_1P2	Qlink0 1.2 V circuits				
VDD_A_QLINK_1_1P2	Qlink1 1.2 V circuits				
VDD_A_QLINK_2_1P2	Qlink2 1.2 V circuits				
VDD_PX0	Digital pad circuits - SPMI0 - 1.2 V	TBD	1.2	TBD	V
VDD_PX3	Digital pad circuits - SPMI1, Modem, Audio SWR, Always-on camera control	TBD	1.8	TBD	V
VDD_PX5	Digital pad circuits - UIM - 1.2 V	TBD	1.2	TBD	V
VDD_PX10	Digital pad circuits - UFS clock - 1.2 V	TBD	1.2	TBD	V
VDD_PX13	Digital pad circuits - SPU	TBD	1.8	TBD	V
VDD_PX14	Digital pad circuits - SDC2, RESIN_N, PS_HOLD, SLEEP_CLK, MODE - 1.2 V	TBD	1.2	TBD	V
VDD_IX	Digital pad circuits - dual voltage pad (0.9 V)	TBD	0.9	TBD	V

Table 3-2 Operating conditions for non AVS voltage rails (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
VDD_PX702 - VDD_PX706, VDD_PX710 - VDD_PX723	Digital pad circuits - dual voltage* (1.2 V/1.8 V) * Per pad group, intended power supply should be connected properly - either 1.2 V or 1.8 V	TBD	1.2 1.8	TBD	V
VDD_PX11	Digital pad circuits - CXO	TBD	1.2	TBD	V
VDD_QFPROM VDD_QFPROM_SP	Programming QFPROM Programming QFPROM, SPU	TBD	1.8	TBD	V
VDD_A_QREFS_1P2 VDD_A_APC_CS_1P2 VDD_A_GFX_CS_1P2 VDD_A_NSP_CS_1P2	Reference voltage for QREFS 1.2 V circuits Application processor current sensor 1.2 V circuit Graphics current sensor 1.2 V circuit NSP current sensor 1.2 V circuit	TBD	1.2	TBD	V
VDD_A_QREFS_0P875	Reference voltage for QREFS circuits	TBD	0.875	TBD	V
VDD_IO_EBI_0 VDD_IO_EBI_1 VDD_IO_EBI_2 VDD_IO_EBI_3 LPDDR5_VDDQ	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP DDR pads (I/O buffer) [c] LPDDR5 spec range 1 [d] LPDDR5 spec range 2 [e]	 TBD TBD	 0.5 0.3	 TBD TBD	 V
LPDDR5_VDD1	POP DDR pads (core 1) [c]	–	–	–	V
LPDDR5_VDD2H	POP DDR pads (core 2/input buffer) [c]	–	–	–	V
LPDDR5_VDD2L	POP DDR pads (core 2/input buffer) [c]	–	–	–	V
Thermal conditions					
T_J	Device operating temperature	TBD	–	TBD	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.
[c] See the LPDDR5 standard (JESD209-5B) and vendor's data sheets for the recommended DC operating conditions (min/typ/max voltages and PDN specification) of VDD1/VDD2H/VDD2L/VDDQ
[d] LPDDR5 spec range 1 is intended for I/O operation with both ODT enabled and disabled.
[e] LPDDR5 spec range 2 is intended for I/O operation with ODT disabled.

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8550 Chipset Power Delivery Network Specification* (80-33265-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8550 Linux Android Current Consumption Data Application Note* (80-33265-7).

3.5 Digital logic characteristics

This information will be included in future revisions of this document.

3.6 Timing characteristics

This information will be included in future revisions of this document.

3.7 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5 SDRAM memory that is attached to the top of the SM8550/SM8550Pchipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8550 Recommendations* (80-VP300-21).

3.8 Multimedia

This information will be included in future revisions of this document.

3.9 Connectivity

This information will be included in future revisions of this document.:

3.10 Internal functions

This information will be included in future revisions of this document.

3.11 Power management interface

This information will be included in future revisions of this document.

4 Mechanical information

4.1 Device physical dimensions

The SM8550/SM8550P device is available in the MPSP1581 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1581 has a 15.6 mm by 14.0 mm body, with a maximum height of 0.56 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1581 outline drawing is shown in Figure 4-1

NOTE Click the following link to download the *Package Outline Drawing, MPSP1581, 15.6 × 14.0 × 0.56 mm, ST94, M147, SB130, NSPPB 496, PL1, MEP* (NT90-11746-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-11746-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

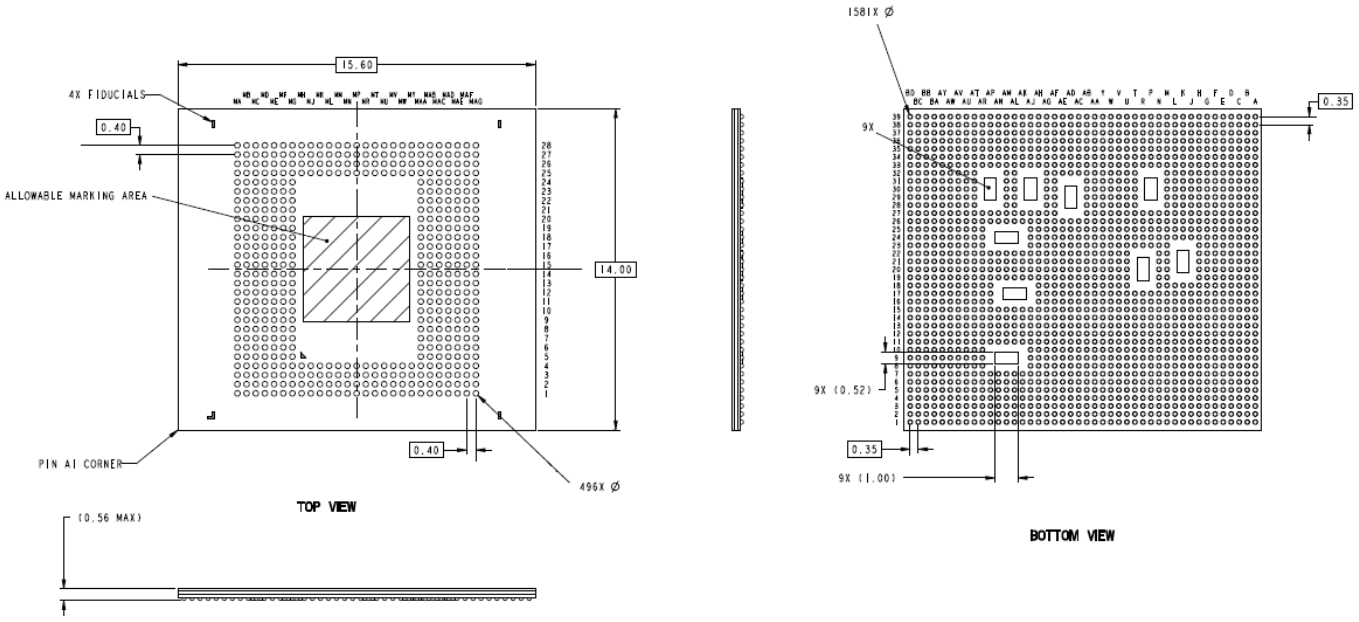


Figure 4-1 MPSP1581 outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

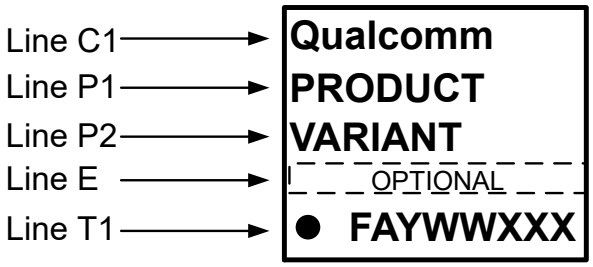


Figure 4-2 SM8550/SM8550P device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ SM8550 ▪ SM8550P
P2	VARIANT	PRR-BB ▪ See Table 4-4 for the assigned values.
E	Blank or random	Optional information
T1	FAYWWXXX	F = foundry company code ▪ F = F for TSMC A = assembly site code ▪ A = C (Amkor, Korea) ▪ A = X (Shinko, Japan) Y = single/last digit of year WW = two-digit work week of current year XXX = lot serial number
	•	Ball A1 indicator

NOTE For complete marking definitions of all SM8550/SM8550P variants and revisions, see the *SM8550/SM8550P Device Revision Guide* (80-33265-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 Related register (0x221C2098)

Bit location	Name	Description
[bits [27:20]	FEATURE_ID	Feature ID is used for differentiating SKUs/variants
bits [19:0]	JTAG_ID	These bits map to [31:12] of the JTAG_ID register (0x221C8744). Fuse bit 0 maps to bit 12 of JTAG_ID

4.3 Device identification

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8550	-0	-MPSP	1581			-TR	-01	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S)

For example

- Example 1: SM-8550-0-MPSP1581-TR-01-0-AB

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	FEATURE_ID [b]	Hardware revision number	Source configuration code (S) [c]	Comments	Sample date
SM8550	ES1	001-AB	0x6	0x1 01CA 0E1	0	SM8550 (001-0-AB), MPSP1581, 3.7 GHz LPDDR5X, AON camera, modem for Sub-6 and mmW	03/31/2022

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
[b] See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible
[c] S is the source configuration code that identifies all the qualified die fabrication-source/assembly site combinations available when the particular sample type was shipped. S values are defined in Table 4-5.

Table 4-5 Source configuration codes

S value	F value = F	A value = C	A value = X
0	TSMC	Amkor, Korea	Shinko, Japan

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

For the daisy chain interconnect information, see *Daisy Chain Interconnect, MPSP1581, 15.6 × 14.0 mm* (DS90-11746-R1).

NOTE For LPDDR5 daisy chain ordering part number, contact the LPDDR manufacturer.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM8550/SM8550P rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8550/SM8550P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the

SM8550 LPDDR5X 12GB PACKAGE THERMAL MODEL ICEPAK (HS11-33265-5HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-33265-5HW

SM8550 LPDDR5X 12GB PACKAGE THERMAL MODEL FLOTHERM (HS11-33265-6HW)

http://https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-33265-6HW

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

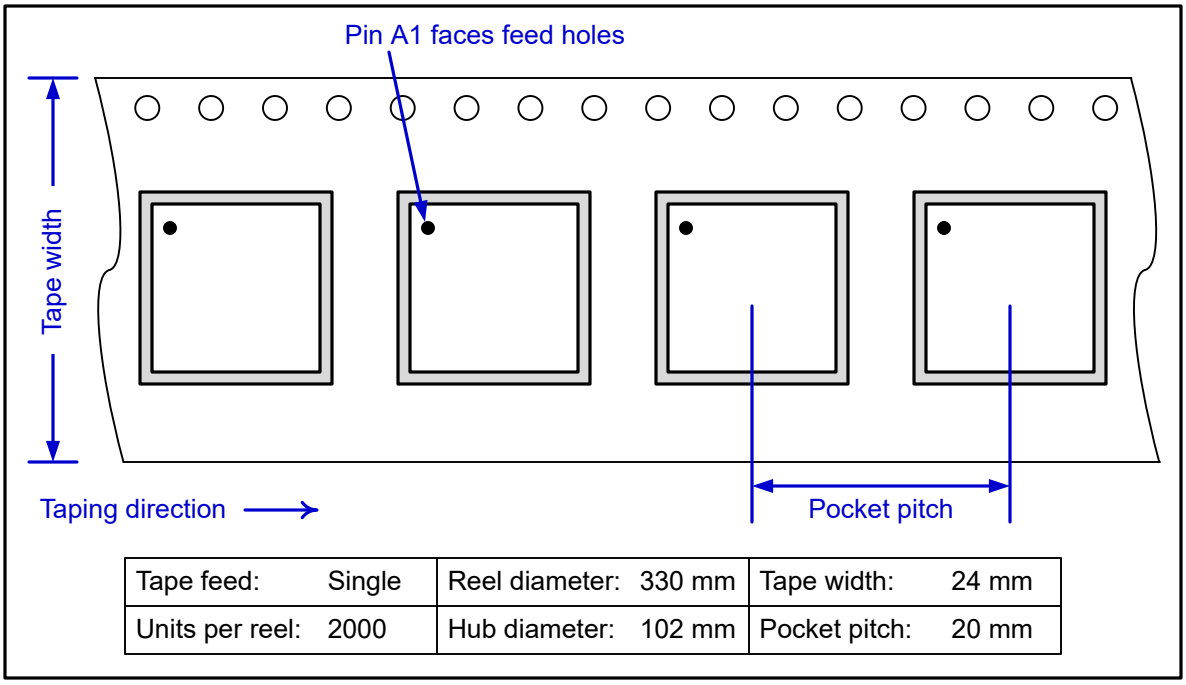
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8550/SM8550P tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

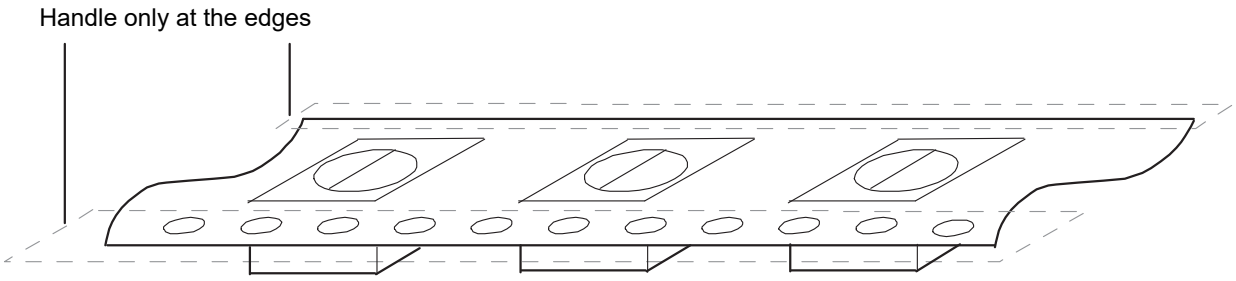


Figure 5-2 Tape handling

5.1.2 Matrix tray information - available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See Figure 5-3 for matrix-tray key attributes. See Table 5-1 for matrix-tray key dimensions.

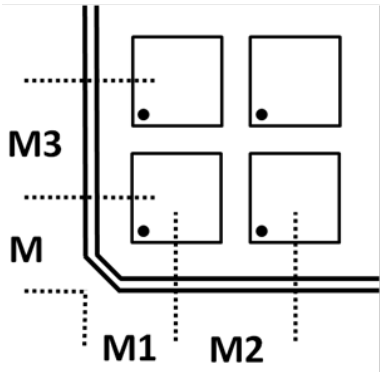


Figure 5-3 Matrix-tray key attributes

Table 5-1 Matrix-tray key dimensions

Key Dimensions	
Array	7 × 15 (105)
M	12.90 mm
M1	14.00 mm
M2	20.50 mm
M3	18.35 mm

5.2 Storage

5.2.1 Bagged storage conditions

SM8550/SM8550P devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See*IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out of bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Device moisture sensitivity level.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM8550/SM8550P if the conditions specified in Bagged storage conditions and Out of bag duration have **not been exceeded.**

It is **necessary** to bake the SM8550/SM8550P if any condition specified in Bagged storage conditions or Out of bag duration has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

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7 Part reliability

This information will be included in future revisions of this document.

8 Revision history

Revision	Date	Description
AA	September 2021	Initial release
AB	October 2021	■ Global: Updated the camera feature ■ Chapter 2 *Pin definitions*: Added this chapter
AC	November 2021	■ Cover page: Updated the high-level block diagram ■ Figure 1-1 SM8550 functional block diagram and example application: Updated the block diagram ■ Figure 1-2 SM8550P functional block diagram and example application: Updated the block diagram ■ Table 1-1 SM8550/SM8550P features: ▫ Removed DMB support ▫ Updated camera support and Fingerprint support features ■ Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports: Updated the pad voltage of GPIO_92 and added a note
AD	March 2022	■ Figure 1-1 SM8550 functional block diagram and example application: Updated the block diagram ■ Figure 1-2 SM8550P functional block diagram and example application: Updated the block diagram ■ Chapter 3 *Electrical specifications*: Added this chapter ■ Section 4.2 *Part marking*: Added this section ■ Section 4.3 *Device identification*: Added this section ■ Section 4.4 *Device moisture sensitivity level*: Added this section ■ Section 4.5 *Thermal characteristics*: Added this section ■ Chapter 5 *Carrier, storage, and handling information*: Added this chapter ■ Chapter 6 *PCB mounting guidelines*: Added this chapter
AE	April 2022	Table 4-4 *Device identification details*: Updated the hardware revision number
AF	May 2022	■ Table 1-1 *SM8550/SM8550P features*: Updated location feature capability ■ Figure 5-1 *Carrier tape drawing with part orientation*: Updated the units per reel and hub diameter

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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