PM8550B/PM8550BH/PM8550BHS/PM8550BHP

Data Sheet

80-33267-1 Rev. AH

April 21, 2023

Device description

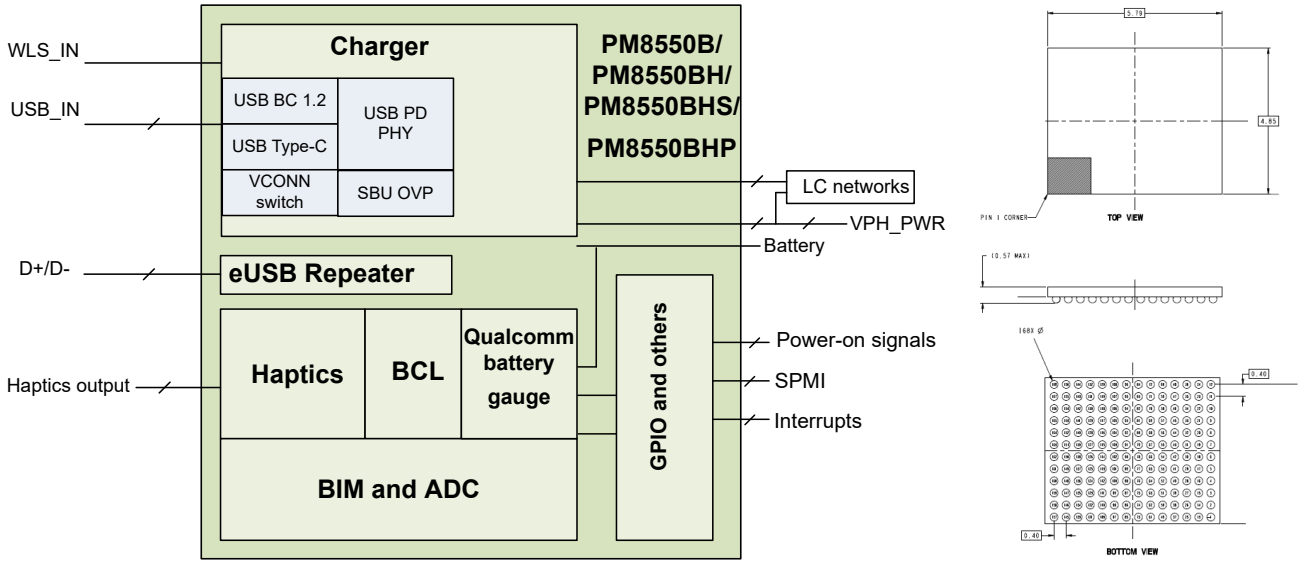
The PM8550B/PM8550BH/PM8550BHS/PM8550BHP interface PMIC, supplements the master core PM8550 PMIC and the slave core PM8550VE/PM8550VS PMIC to integrate all wireless handset power management, general housekeeping, and user interface support functions into an integrated multi-IC solution.

- Best in class high-efficiency 6 A 3-level buck/Div2 charge pump combination architecture Li-ion battery charger (> 97% peak efficiency)
- Dedicated paths for USB and wireless charging with charger operation up to 21.5 V (25 V absolute max)
- Supports up to a 6 A charge current (single path) and a 12 A charge current (dual path using SMB1396/SMB1398 companion ICs)
- Supports *USB Type-C Specification* Rev. 1.4 and *USB Power Delivery Specification* Rev. 3.0
- Supports Qualcomm® Quick Charge™ 2.0, Quick Charge 3.0, Quick Charge 4.0, and Quick Charge 5.0 technology
- Supports 2S battery with charge balancing (SMB1399 needed). See PM8550B SKUs for details.
- Simultaneous wireless charging and OTG support using haptics boost
- Simultaneous USB charging and reverse wireless charging support using haptics boost

Key features

- eUSB repeater
- Qualcomm battery gauge with 1S, 2S, and 1S2P support
- Analog-to-digital converter (ADC) subsystem with analog multiplexer (AMUX) and voltage/current analog-to-digital converter (VADC/IADC)
- Battery interface module (BIM) that includes battery serial interface (BSI) or PMIC serial interface (PSI) and battery missing detection (BMD)
- Battery current limiting (BCL) subsystem that provides both hardware and software alarms, which are used by the system for reducing battery current.
- Full H-bridge haptics driver with dedicated 5 V to 10 V programmable boost for LRA application and SoundWire interface. See PM8550B SKUs for details.
- SPMI interface
- 12 GPIOs
- 168-pin fan-out wafer-level nanoscale package (168 FOWNSP)

High-level block diagram and FOWNSP168 package outline drawing



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Document updates

See the Revision history for details on the changes included in this revision

1.1 Functional block diagram

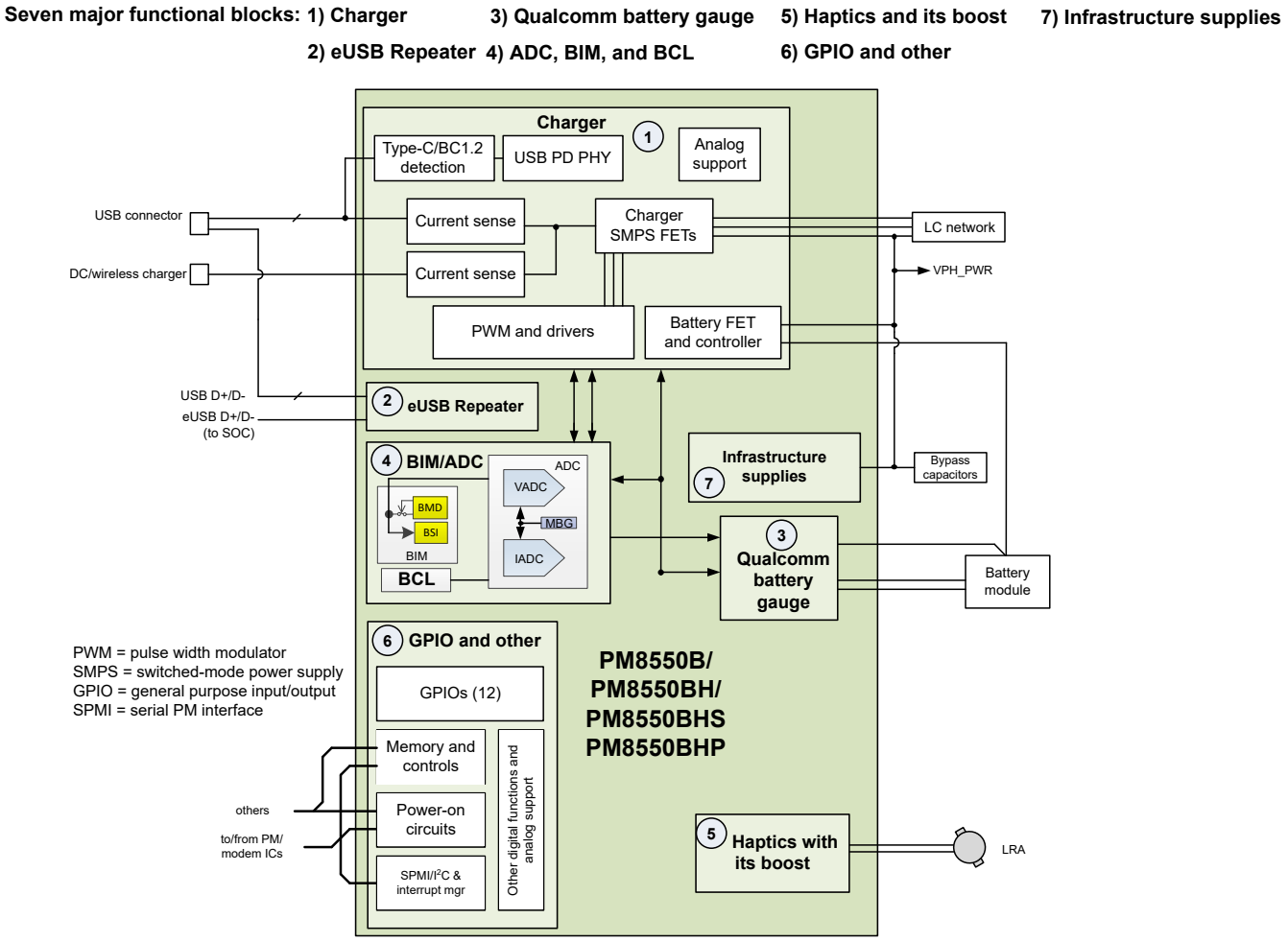

Figure 1-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP high-level functional block diagram

1.2 PM8550B/PM8550BH/PM8550BHS/PM8550BHP features

NOTE Some hardware features integrated within the PM8550B/PM8550BH/PM8550BHS/PM8550BHP device must be enabled through the IC software. See the latest revision of the applicable software release notes to identify the enabled PMIC features.

Table 1-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP features

Feature	PM8550B/PM8550BH/PM8550BHS/PM8550BHP capability
Charger	
Battery charger	■ High-efficiency 6 A 3-level buck/Div2 charge pump combination architecture Li-ion battery charger ▫ Extremely low Rds(on) MOSFETs minimizing power dissipation during charging ▫ > 97% peak efficiency ■ 100% duty cycle mode ■ Dedicated charging paths for USB and wireless charging with +3.6 V to +21.5 V operating range and absolute maximum voltage of +25 V ■ Automatic USB/wireless input path selection and priority ■ USB charging input path ▫ Optional external USB OVP FET control with 10 V VGS to minimize Rds(on) ▫ 10 mΩ FP FET to minimize power loss during high current charging ▫ USB Type-C CC logic compliant to the *USB Type-C Specification* Rev. 1.4. ▫ VCONN switch capable of delivering 1.5 W for DisplayPort alt-mode ▫ USB power delivery PHY hardware compliant to *USB Power Delivery Specification* Rev. 3.0 ▫ Quick Charge 2.0 and Quick Charge 3.0 hardware support; Quick Charge 4.0 and Quick Charge 5.0 software support ▫ Automatic power source detection (APSD) per the *USB Battery Charging Specification* Rev. 1.2 ▫ Automatic input current limit (AICL) for universal USB adapter compatibility ▫ Liquid presence detection (LPD) based on SBU1/2 impedance ▫ Universal fast charging spec support ■ Wireless charging input path ▫ Optional external WLS Blocking FET control with 10 V VGS to minimize Rds(on) ▫ 20 mΩ FP FET to sense input current ▫ Automatic input current limit (AICL) to detect input collapse ■ 6 A charge current (single path); 24 A charge current (using SMB1394 as parallel charger) with PM8550B/BH/BHP; 12 A charge current (using SMB1396 as parallel) with PM8550BHS ■ Support 2S battery charging (SMB1399 needed). Improved 2S battery charging efficiency by charging the 2S battery directly when input voltage is high. See PM8550B SKUs for details. ■ Simultaneous wireless charging and OTG support using haptics boost ■ Simultaneous USB charging and reverse wireless charging support using haptics boost ■ Reverse boost ▫ Up to 5 V, 3 A output for reverse USB OTG/Type-C source ▫ Up to 12 V, 1 A output for 10 W reverse WLS charging ▫ True OCP ▫ Ability to reverse boost directly from 2S battery for higher efficiency ■ Battery interface ▫ 5 mΩ integrated BATFET (QBAT) for optimal charging efficiency and battery life. ▫ QBAT soft-start and VPH short-circuit detection

Table 1-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP features (cont.)

Feature	PM8550B/PM8550BH/PM8550BHS/PM8550BHP capability
	▫ Input/output CurrentPath control allows system operation with deeply discharged/missing battery ▫ Battery supplemental mode (BSM) to allow battery to supplement system current exceeding what the charger buck can provide ▫ Differential battery voltage Kelvin sensing to compensate for the IR drop caused by the phone PCB and battery pack protection FETs to prolong CC charging and reduce the total charging time ▫ JEITA battery temperature management and JISC 8714 support ▫ Battery-missing detection options (in the battery interface module) ▫ Ship-mode and AFP mode ■ Intelligent charging control and thermal management ▫ Hardware autonomous charging ▫ Trickle charger ▫ Hardware-controlled thermal loop manages input current limit based on the die temperature
eUSB Repeater	
eUSB Repeater	■ *Universal Serial Bus 2.0* specification compliant ■ *Embedded USB2 (eUSB2) Physical Layer Specification 1.1* compliant ■ Dual role capable
Qualcomm battery gauge	
Qualcomm battery gauge	■ Improved SoC accuracy (~1% average SOC error) ■ Qualcomm battery gauge is a hybrid of voltage and current based SoC with optimum linear parameter estimation using extended Kalman filtering ■ 2S battery support, with charge balancing. See PM8550B SKUs for details. ■ 1S2P battery support, with individual cell gauging ■ SMB parallel charging current sensing through ICHG pins ■ BAT_THERM IR compensation eliminates variation of BAT_THERM reading with varying charge/discharge currents ■ Simplified hardware architecture with reduced states and easy configurability ■ Online battery ESR and Rslow estimation
BIM and ADC	
BIM	■ BIM module includes the battery serial interface (BSI) or PMIC serial interface (PSI) and battery missing detection (BMD) hardware for two cells. ■ BSI is a single-wire interface that can communicate with external hardware using the MIPI-BIF protocol. ■ BMD is a hardware that detects battery removal in all modes (on, off, sleep)
On-chip ADC	■ The ADC subsystem includes signal multiplexing and voltage analog-to-digital converter (VADC) ■ Support for 2S battery - 1/6 divider for higher voltage levels, mid-node monitoring, charge balancing FETs. See PM8550B SKUs for details. ■ A dedicated internal 1.875 V LDO used to bias the VADC and pull-up resistors ■ Parallel hardware interface to arbitrate ADC requests from multiple clients (Qualcomm battery gauge, charger, and BCL) ■ Qualcomm battery gauge and BCL requires Vbatt and Ibatt ■ Charger requires USB and DC input levels, thermistor values, and Vbatt/Ibatt
Haptics	

Table 1-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP features (cont.)

Feature	PM8550B/PM8550BH/PM8550BHS/PM8550BHP capability
Haptics boost and driver	■ Full H-bridge haptics driver with dedicated 5 V to 10 V programmable boost for LRA applications. See PM8550B SKUs for details. ■ SoundWire interface with LPASS ■ 2 kB memory space for FIFO and sampled waveform storage for pattern generation ■ Hardware-based arbitration for multiple haptics requests ■ Real time resistance detection ■ Closed loop auto braking ■ Enhanced protection schemes (short/open circuit detection, high voltage safety timer) ■ > 5 W wireless Tx charging with vibe ■ Off-mode vibration and virtual key support
IC-level interfaces	
Primary status and control	■ Two-line serial power management interface (MIPI SPMI) ■ Supported by SPMI
Interrupt managers	PBS 3.0 with one-time programmable (OTP) memory and user programmable
Programmable boot sequence	RAM for customizable power-on, power-off, and reset sequences
Configurable I/Os	
General-purpose input/ output (GPIO) pins	■ 12 GPIO pins, configurable as digital inputs or outputs ■ Some GPIOs have primary/alternate functions for IC-level interfacing or required controls for user interface functions if those UI functions are used.
Internal clock	Internal 19.2 MHz RC clock
Package	
Size	5.79 × 4.85 × 0.57 mm
Pin count and package type	168-pin FOWNSP (0.4 mm pitch)

1.3 PM8550B SKUs

PM8550B has the following four SKUs: PM8550B, PM8550BH, PM8550BHS, and PM8550BHP.

The table below lists the differences between the four SKUs.

SKU	Haptics boost support	Battery charging support	Qualcomm battery gauge support
PM8550B	5 V	1S	1S
PM8550BH	5 V to 10 V	1S	1S
PM8550BHS	5 V to 10 V	2S	2S
PM8550BHP	5 V to 10 V	1S	2P

2 Pin definitions

The PM8550B/PM8550BH/PM8550BHS/PM8550BHP is available in the FOWNSP168 – see Mechanical information for package details.

A high-level view of the pad assignments is shown in Figure 2-1.

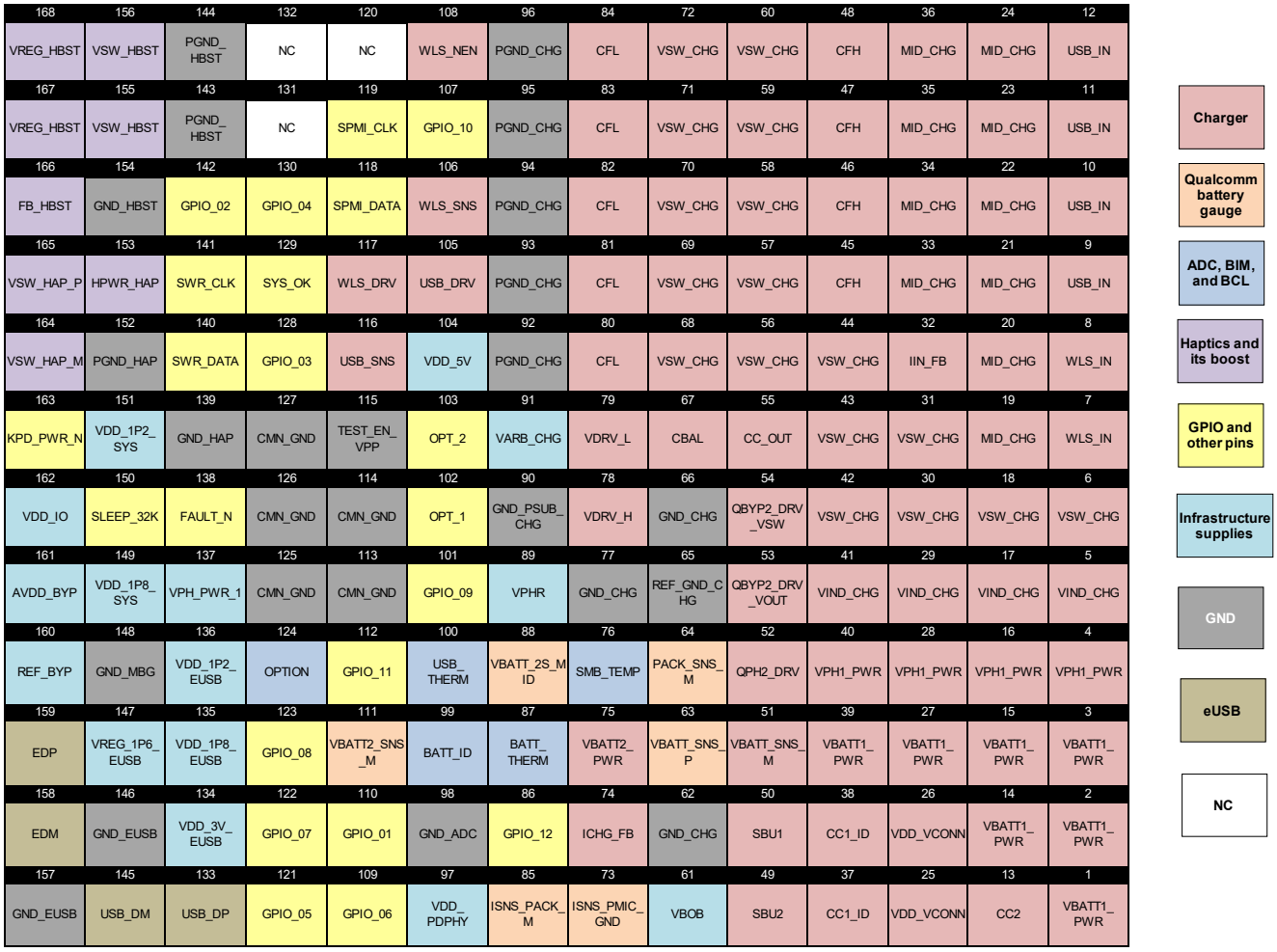

Figure 2-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP pad assignments (bottom view)

2.1 I/O parameter definitions

Table 2-1 I/O parameter (pin type) definitions

Symbol	Description
Pin attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pin that handles 10 mA or more of current flow into the device [a]
PO	Power output; a pin that handles 10 mA or more of current flow out of the device [a]
Z	High-impedance (Hi-Z) output
MV	Medium voltage
LV	Low voltage
GNDP	Power ground; a pin that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pins.
GNDC	Common ground; a pin that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates.
When configured as outputs, GPIO pins have configurable drive strengths that depend on the GPIO pin's supply voltage. See Electrical specifications for details.	

[a] The maximum current levels expected on PI and PO type pins are listed in Electrical specifications.

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional groups .

Table 2-2 Charger

Table 2-3 eUSB repeater

Table 2-4 Qualcomm battery gauge

Table 2-5 ADC, BIM, and BCL

Table 2-6 Haptics and its boost

Table 2-7 General-purpose input/output functions and other pins

Table 2-8 Infrastructure supplies

Table 2-9 Ground pads

Table 2-10 No connection pins

Table 2-2 Pin descriptions — Charger

Pin #	Pin name and/or function	Pin type [a]	Functional description
116	USB_SNS	AI	USB OVP input voltage remove sense
105	USB_DRV	AO	USB OVP FET gate drive
9, 10, 11, 12	USB_IN	PI, PO	USB power input of the charger
106	WLS_SNS	AI	WLS input voltage remote sense
117	WLS_DRV	AO	WLS blocking FET gate drive
7, 8	WLS_IN	PI, PO	Wireless (DC) power input of the charger.
108	WLS_NEN	DO	Wireless charging output enable/disable pin. Keeps wireless charger output stage disabled (forward voltage blocking) during USB charging.
19, 20, 21, 22, 23, 24, 33, 34, 35, 36	MID_CHG	PI, PO	Mid joint point of QUSB, QWLS, and charger buck input
45, 46, 47, 48	CFH	PI, PO	Flying capacitor high side node
80, 81, 82, 83, 84	CFL	PI, PO	Flying capacitor low side node
78	VDRV_H	PI, PO	Bootstrap capacitor high-side connection
79	VDRV_L	PI, PO	Bootstrap capacitor low-side connection
67	CBAL	PI, PO	Balance node for flying capacitor
53	QBYP2_DRV_VOUT	AO	3LBk/Div2 external Bypass FET gate drive 1, near VOUT_CHG side
54	QBYP2_DRV_VSW	AO	3LBk/Div2 external Bypass FET gate drive 2, near VSW_CHG side
52	QPH2_DRV	AO	External QPH2 FET gate drive
6, 18, 30, 31, 42, 43, 44, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72	VSW_CHG	PI, PO	Charger buck/boost switch node
5, 17, 29, 41	VIND_CHG	PI, PO	2S battery: Charger buck VOUT feedback 1S battery: Connect to VSW_CHG

Table 2-2 Pin descriptions — Charger (cont.)

Pin #	Pin name and/or function	Pin type [a]	Functional description
4, 16, 28, 40	VPH1_PWR	PI, PO	System power input/output node
1, 2, 3, 14, 15, 27, 39	VBATT1_PWR	PI, PO	1S battery power input and output
75	VBATT2_PWR	PI	2S battery power input for VARB and aVdd/dVdd
63	VBATT_SNS_P	AI	1S/2S battery cell voltage sensing S+; charger sense battery voltage across VBATT_SNS_P and VBATT_SNS_M
51	VBATT_SNS_M	AI	1S/2S battery cell voltage sensing S-; charger sense battery voltage across VBATT_SNS_P and VBATT_SNS_M
32	IIN_FB	AI	SMB input current signal; input to PMIC charger input current limit control loop
74	ICHG_FB	AI	SMB charge current signal; input to PMIC charger charge current limit control loop
37, 38	CC1_ID	AI, DI, DO, PO	USB Type-C CC1 pin
13	CC2	AI, DI, DO, PO	USB Type-C CC2 pin
55	CC_OUT	DO	1.2/1.8 V push-pull tri-state output indicating USB Type-C connector orientation (CC1 or CC2 connection)
50	SBU1	AI	USB Type-C SBU1 pin
49	SBU2	AI	USB Type-C SBU2 pin
25, 26	VDD_VCONN	PI	VDD source for VCONN switch; connect to VPH_PWR or VREG_BOB

[a] See Table 2-1 for pin voltage and type definitions

Table 2-3 Pin descriptions — eUSB repeater

Pin #	Pin name and/or function	Pin type [a]	Functional description
133	USB_DP	AI, DI, DO	USB D+ signal line, also for BC1.2 detection
145	USB_DM	AI, DI, DO	USB D- signal line, also for BC1.2 detection
159	EDP	DI, DO	eUSB2 port positive IO pad
158	EDM	DI, DO	eUSB2 port negative IO pad

[a] See Table 2-1 for pin voltage and type definitions

Table 2-4 Pin descriptions — Qualcomm battery gauge

Pin #	Pin name and/or function	Pin type [a]	Functional description
63	VBATT_SNS_P	AI	1S/2S battery cell voltage sensing S+; Qualcomm battery gauge senses battery voltage across VBATT_SNS_P and PACK_SNS_M
64	PACK_SNS_M	AI	Battery pack bottom node; Qualcomm battery gauge senses battery voltage across VBATT_SNS_P and PACK_SNS_M
88	VBATT_2S_MID	AI	MID of 2S battery pack. Used for cell balancing
73	ISNS_PMIC_GND	AI	External sensing plus node
85	ISNS_PACK_M	AI	External sensing minus node
111	VBATT2_SNS_M	AI	Remote sensing of second battery cell voltage S- in 1S2P configuration

[a] See Table 2-1 for pin voltage and type definitions

Table 2-5 Pin descriptions — ADC, BIM, and BCL

Pin #	Pin name and/or function	Pin type [a]	AMUX channel	Functional description
87	BATT_THERM	AI	AMUX_THM1	Battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and battery gauge.
99	BATT_ID	AI	AMUX_THM2	Battery ID – used for battery identification, battery missing and BSI communication
76	SMB_TEMP	AI	AMUX_THM3	SMB temperature sensor (current) signal input; converted to voltage then sent to ADC.
100	USB_THERM	AI	AMUX_THM4	USB Type-C connector temperature sensor
124	OPTION	AI	AMUX_THM5	Power up sequence option
107	GPIO_10	AI	AMUX_THM6	GPIO input to AMUX
110	GPIO_01	AI	AMUX1_GPIO	GPIO input to AMUX
121	GPIO_05	AI	AMUX2_GPIO	GPIO input to AMUX
109	GPIO_06	AI	AMUX3_GPIO	GPIO input to AMUX
86	GPIO_12	AI	AMUX4_GPIO	GPIO input to AMUX

[a] See Table 2-1 for pin voltage and type definitions

Table 2-6 Pin descriptions — Haptics and its boost

Pin #	Pin name and/or function	Pin type [a]	Functional description
155, 156	VSW_HBST	PO	Haptics boost switch node
166	FB_HBST	AI	Feedback sense for haptics boost output
167, 168	VREG_HBST	PO	Haptics boost power output
164	VSW_HAP_M	PO	Haptics driver M bridge output
165	VSW_HAP_P	PO	Haptics driver P bridge output
153	HPWR_HAP	PI	Haptics driver input power supply

[a] See Table 2-1 for pin voltage and type definitions

Table 2-7 Pin descriptions — general-purpose input/output functions and other pins

Pin #	Pin name	Configurable function	Pin type [a]	Functional description
Configurable GPIOs [b c]				
110	GPIO_01		MV	Configurable; default digital input with 10 µA pull-down
		FM_FORCE_USB_BOOT		Force USB boot (EDL mode)
		VBATT_2S_MID		MID2 of 2S battery pack. Used for cell balancing
142	GPIO_02		MV	Configurable; default digital input with 10 µA pull-down
		HAP_EXT_TRIG		Haptics external trigger
		DIV_CLK		Divided down HFRC clock
128	GPIO_03		MV	Configurable; default digital input with 10 µA pull-down
		UFCS DP		UFCS PHY DP communication
130	GPIO_04		MV	Configurable; default digital input with 10 µA pull-down
		UFCS DM		UFCS PHY DM communication
121	GPIO_05		MV	Configurable; default digital input with 10 µA pull-down
		HAP_VP		Haptics volume increase trigger
109	GPIO_06		MV	Configurable; default digital input with 10 µA pull-down
		HAP_VM		Haptics volume increase trigger
		BATT2_THERM		Battery temperature input to ADC for measuring 2nd battery pack temperature. It is used for charger safe operation and battery gauge.
122	GPIO_07		MV	Configurable; default digital input with 10 µA pull-down
		ISNS2_PMIC_GND		Second external Rsense GND side
123	GPIO_08		MV	Configurable; default digital input with 10 µA pull-down
		ISNS2_PACK_M		Second external Rsense pack side
101	GPIO_09		LV	Configurable; default digital input with 10 µA pull-down
107	GPIO_10		LV	Configurable; default digital input with 10 µA pull-down
		WLS_THERM		Wireless charging thermistor
112	GPIO_11		LV	Configurable; default digital input with 10 µA pull-down
		SMB_EN		Enable SMB parallel chargers
86	GPIO_12		LV	Configurable; default digital input with 10 µA pull-down
		X2D2_EN		Enable SMB parallel chargers

Table 2-7 Pin descriptions — general-purpose input/output functions and other pins (cont.)

Pin #	Pin name	Configurable function	Pin type [a]	Functional description
Other pins				
163	KPD_PWR_N		DI	Phone power key for exiting ship mode
129	SYS_OK		DO	System OK or charger detection indicator output (user programmable)
102	OPT_1		AI	Option pin 1
103	OPT_2		AI	Option pin 2
119	SPMI_CLK		DI	SPMI communication bus clock signal
118	SPMI_DATA		DI	SPMI communication bus data signal
141	SWR_CLK		DI	SoundWire clock input
140	SWR_DATA		DI, DO	SoundWire data input
150	SLEEP_32K		AI	32 kHz XO sleep clock input
138	FAULT_N		DI, DO	PMIC fault signal (bidirectional) that initiates shutdown or S3 reset to all PMICs

[a] See Table 2-1 for pin voltage and type definitions

[b] GPIOs may be configured for the following use cases:

- User interface functions
- IC-level interface functions
- General housekeeping functions

To assign a GPIO to a particular function, identify all of your application's requirements and map each GPIO to its function—carefully avoiding assignment conflicts.

[c] Not all GPIOs are connected to the RRADC. Also, there are no free channels available on the RRADC, because they are all accounted for.

Fixed supply for GPIO_09 through GPIO_12:

- 0 and 1 = VDD_1P8_SYS (1.8 V)

For GPIO_01 through GPIO_08, options include the following:

- 0 = VPH_PWR_1 (3.6 V nominal)
- 1 = VDD_1P8_SYS (1.8 V)
- 2 = VDD_1P2_SYS (1.2 V)

Table 2-8 Pin descriptions — infrastructure supplies

Pin #	Pin name and/or function	Pin type [a]	Functional description
160	REF_BYP	AO	1.25 V bandgap reference voltage
161	AVDD_BYP	AO	Bypass capacitor for dedicated LDO analog infrastructure circuits. This LDO must only be used for analog infrastructure circuits and must not be used as a general LDO output.
91	VARB_CHG	PO	Power source arbitration circuit output
104	VDD_5V	PO	5 V LDO output supply for the bootstrap capacitor
137	VPH_PWR_1	PI	General VPH_PWR supply for all modules
89	VPHR	PI	VPH_PWR connection for power FET guarding
61	VBOB	PI	BOB output that powers VARB when battery is low
149	VDD_1P8_SYS	PI	1.8 V supply from core PMIC to power I/O
162	VDD_IO	PI	1.2 V/1.8 V I/O supply
151	VDD_1P2_SYS	PI	1.2 V I/O supply for SWR and charger I/Os
97	VDD_PDPHY	PI	3.075 V supply for PDPHY
134	VDD_3V_eUSB	PI	3.075 V supply for eUSB repeater
135	VDD_1P8_eUSB	PI	1.8 V supply for eUSB repeater
136	VDD_1P2_eUSB	PI	1.2 V supply for eUSB repeater
147	VREG_1P6_eUSB	PO	1.6 V LDO output for eUSB repeater

[a] See Table 2-1 for pin voltage and type definitions

Table 2-9 Pin descriptions — ground pads

Pin #	Pin name and/or function	Pin type [a]	Functional description
Common grounds			
62, 66, 77	GND_CHG	GNDC	Ground for ESD cell
90	GND_PSUB_CHG	GNDC	Ground for charger substrate
113, 114, 125, 126, 127	CMN_GND	GNDC	Common ground
154	GND_HBST	GNDC	Ground for haptics boost controller
146, 157	GND_EUSB	GNDC	Ground for eUSB repeater
115	TEST_EN_VPP	GNDC	Pin must be grounded externally
Special grounds			
148	GND_MBG	GNDP	Ground for MBG
65	REF_GND_CHG	GNDC	Quiet reference ground
98	GND_ADC	GNDP	ADC ground pin

Table 2-9 Pin descriptions — ground pads (cont.)

Pin #	Pin name and/or function	Pin type [a]	Functional description
92, 93, 94, 95, 96	PGND_CHG	GNDP	Charger Buck/Boost power ground
152	PGND_HAP	GNDP	Haptics driver power ground connecting to H-Bridge
139	GND_HAP	GNDC	Ground connecting to internal circuitries
143, 144	PGND_HBST	GNDP	Power ground for haptics boost

[a] See Table 2-1 for pin voltage and type definitions

Table 2-10 Pin descriptions — no connection pins

Pin #	Pin name and/or function	Functional description
120, 131, 132	NC	No connect; not connected externally

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Terminal voltage range				
USB_SNS	USB OVP input voltage remove sense	-0.3	30	V
WLS_SNS	WLS input voltage remote sense	-0.3	30	V
USB_SNS	10 µs pulse transient for USB OVP input voltage remote sense	–	45	V
USB_DRV	USB OVP FET gate drive	-0.3	33	V
WLS_DRV	WLS blocking FET gate drive	-0.3	33	V
USB_IN	USB power input of the charger	-0.3	25	V
WLS_IN	Wireless (DC) power input of the charger	-0.3	25	V
MID_CHG [a]	Mid joint point of QUSB, QWLS, and charger buck input	-0.3	25	V
VSW_CHG to VPH_PWR	QBYP off	-0.3	16	V
CFH	Flying capacitor high side node	-0.3	25	V
VSW_CHG	Charger buck/boost switch node	-0.3	20	V
CFL	Flying capacitor low side node	-0.3	14	V
CBAL	Balance node for flying capacitor	-0.3	18	V
VDRV_H	Bootstrap capacitor high-side connection Converter not switching	-0.3	18	V
	Bootstrap capacitor high-side connection Converter switching	-0.3	27	V
VDRV_L	Bootstrap capacitor low-side connection Converter not switching	-0.3	18	V
	Bootstrap capacitor low-side connection Converter switching	-0.3	22	V
VARB	10 µs pulse on power source arbitration circuit output.	-0.3	7.5	V
QBYP2_DRV_VSW	3LBk/Div2 external bypass FET gate drive 1, near VSW_CHG side	-0.3	28	V
QBYP2_DRV_VOUT	3LBk/Div2 external bypass FET gate drive 2, near VOUT_CHG side	-0.3	18	V
QPH2_DRV	External QPH2 FET gate drive	-0.3	20	V
VPH1_PWR VBAT1_PWR	System power input/output node (applies to both 1S and 2S application) Battery power input/output node (applies to both 1S and 2S application)			
	DC	-0.3	6	V
	10 ms transient	-0.3	7	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Units
VBAT2_PWR	Powers VARB node			
VOUT_CHG	–			
	DC	-0.3	+12	V
	10 ms transient	-0.3	+14	V
CC1, CC2, SBU1, SBU2 [a]	USB Type-C CC1/CC2/SBU1/SBU2 pins	-0.3	22	V
CC_OUT		-0.3	2	V
USB_DP	USB D+ signal line for BC1.2 detection and USB2.0 positive I/O	-0.5	5.5	V
USB_DM	USB D- signal line for BC1.2 detection and USB2.0 negative I/O	-0.5	5.5	V
EDP	eUSB2 positive I/O	-0.5	2.2	V
EDM	eUSB2 negative I/O	-0.5	2.2	V
All other pins		-0.3	Vxx [b]	V
Temperature ratings				
T_s	Storage temperature [c] [d]	-65	+150	°C

[a] The device needs to be powered/biased via USB_IN, WLS_IN or > 2.5 V (1S) and > 5.5 V (2S) VBATT_PWR before applying voltage on any of the other output I/Os
[b] Vxx is the lower of +6 V and (USB_IN, WLS_IN or VBATT_PWR) + 0.5 V
[c] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
[d] For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage and thermal conditions (Table 3-2). The device meets all performance specifications listed in DC power consumption through Haptics, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter	Description	Min	Typ	Max	Units
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +125	°C
Power pads					
USB_IN	USB power input of the charger	3.7	–	21.5	V
WLS_IN	Wireless (DC) power input of the charger	3.7	–	21.5	V
MID_CHG	Mid joint point of QUSB, QWLS, and charger buck input	3.7	–	21.5	V
VSW_CHG	Charger buck/boost switch node	0	–	12.5	V
VBAT1_PWR	Battery power input/output node (applies to both 1S and 2S application)	2.5	–	5.0	V
VPH1_PWR	System power input/output node (applies to both 1S and 2S application)				
	Steady state (DC)	2.5	–	5.0	V

Table 3-2 Operating conditions (cont.)

Parameter	Description	Min	Typ	Max	Units
	Short duration VPH excursions beyond normal operating voltage range (< 1 ms)	2.1	–	5.25	V
VDD_3V_EUSB	USB2.0 analog voltage	3	3.075	3.3	V
VDD_1P2_EUSB	eUSB2 supply voltage	1.08	1.2	1.32	V
VDD_1P8_EUSB	Supply to feed 1.6 V LDO	TBD	1.8	TBD	V

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default settings.

Table 3-3 DC power supply currents

Parameter	Symbol	Min	Typ	Max	Units
Battery supply current, active mode (1S and 2S application) [a]	IDD_{ACTIVE_BAT}	–	565	848	mA
Charger supply current, active mode (1S and 2S application) [b]	IDD_{ACTIVE_CHG}	–	3965	5948	µA
Battery supply current, sleep mode (1S and 2S application) [c]	IDD_{SLEEP}	–	179	268	µA
Battery supply current, off mode [d]	IDD_{OFF}				
1S application		–	28	42	µA
2S application		–	31	46	µA
Battery supply current, ship mode [e]	IDD_{SHIP}				
1S application		–	13	19	µA
2S application		–	15	23	µA
PM8550BHS + SMB1399 battery supply current, off mode [f]	$IDD_{OFF\_COMBINED}$				
2S application		–	112	190	µA
PM8550BHS + SMB1399 battery supply current, off mode [g]	$IDD_{OFF\_COMBINED}$				
2S application		–	70	130	µA

[a] IDD_{ACTIVE_BAT} is the total supply current from a main battery with PM8550B/PM8550BH/PM8550BHS/PM8550BHP on, Qualcomm battery gauge in active state, charger in standby and OLED, haptics modules are off. XBL has been loaded.

[b] IDD_{ACTIVE_CHG} is the total supply current running off the charger with PM8550B/PM8550BH/PM8550BHS/PM8550BHP on, Qualcomm battery gauge in active state, and OLED, haptics modules are off. XBL has been loaded.

[c] IDD_{SLEEP} is the total supply current from a main battery with PM8550B/PM8550BH/PM8550BHS/PM8550BHP on, Qualcomm battery gauge in low power mode, charger in standby, sleep_b = 1 and OLED, haptics modules are off. XBL is loaded and the MPM sleep sequence is executed.

[d] IDD_{OFF} is the total supply current from a main battery with PM8550B/PM8550BH/PM8550BHS/PM8550BHP off. This only applies when the temperature is between -30°C and 60°C and the system has powered on after battery attach, prior to powering off.

[e] IDD_{SHIP} is the total supply current from a main battery with PM8550B/PM8550BH/PM8550BHS/PM8550BHP off and in ship mode. BATFET is open. This only applies when the temperature is between -30°C and 60°C.

[f] $IDD_{OFF\_COMBINED}$ is the total supply current from a main battery for total off current with PM8550BHS + SMB1399. This only applies when the temperature is between -30°C and 60°C and the system has powered on after battery attach, prior to powering off. Applicable to PM8550BHS v2.0

[g] $IDD_{OFF\_COMBINED}$ is the total supply current from a main battery for total off current with PM8550BHS + SMB1399. This only applies when the temperature is between -30°C and 60°C and the system has powered on after battery attach, prior to powering off. Applicable to PM8550BHS v2.1.

3.4 Digital logic characteristics

The charger has unique digital signaling characteristics as listed within Charger; all other PM8550B/PM8550BH/PM8550BHS/PM8550BHP digital I/O characteristics are specified in Table 3-4.

Table 3-4 Digital I/O specifications

Parameter	Symbol	Condition	LLimit	ULimit	Units
Input voltage, logic high [a]	V_{IH}	–	0.65 × V_{IO}	V_{IO}+ 0.3	V
Input voltage, logic low [a]	V_{IL}	–	-0.3	0.35 × V_{IO}	V
Output voltage, logic high [a]	V_{OH}	I_{OUT} = I_{OH}	V_{IO} - 0.45	V_{IO}	V
Output voltage, logic low	V_{OL}	I_{OUT} = I_{OL}	0.0	0.45	V
Schmitt trigger hysteresis	V_{HYST}	–	15	–	mV
Output current, logic high [b]	I_{OH}	–	3	–	mA
Output current, logic low [b]	I_{OL}	–	–	-3	mA
Input leakage current, digital input [c]	I_L	–	-200	+200	nA
Input capacitance, digital input or I/O	C_{IN-D}	–	–	5	pF

[a] VIO = VDD_1P8_SYS, unless otherwise noted
[b] The output current specification applies to all digital outputs unless otherwise specified. It is superseded by specifications on specific pins.
[c] GPIOs comply with the input leakage specification when configured either as a digital input or in tri-state mode.

Table 3-5 GPIO output impedance

Driver strength setting	V_{IO}	Driver output impedance			Unit
		Min	Typ	Max	
Low strength driver	1.8 V	10	40	80	Ω
	1.2 V	10	48	80	
Medium strength driver	1.8 V	10	28	80	
	1.2 V	10	31	80	
High strength driver	1.8 V	10	22	80	
	1.2 V	10	23	80	

3.5 Charger

T_A = -30°C to +85°C, V_{USB_IN} = +5.0 V, +9.0 V, +12.0 V, +15.0 V, +20 V, V_{WLS_IN} = +5.0 V, +9.0 V, +12.0 V, +15.0 V, +20 V, V_{FLT} = +4.4 V, V_{BATT} = +3.9 V, F_{SW} = 0.533 MHz, unless otherwise noted. All voltages are relative to GND.

3.5.1 Input power specifications

Table 3-6 Input power source control and protection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
USB OVP FET and WLS blocking FET control						
$V_{USB\_OVP\_THD}$	USB/WLS_SNS OVP threshold	V_{USB/WLS_SNS} rising	6.6	6.9	7.2	V
$V_{WLS\_OVP\_THD}$			13.2	13.5	13.8	V

Table 3-6 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
			16	16.4	16.8	V
			19	19.4	19.8	V
			19.8	20.2	20.6	V
			20.6	21	21.4	V
			21.5	22	22.5	V
			22.5	23	23.5	V
	Hysteresis	V_{USB/WLS_SNS} falling; % of V_{USB/WLS_OVP_THD}	1	–	2	%
t_{USB_OVP}	USB OVP response time	From V_{USB/WLS_SNS} > V_{USB/WLS_OVP_THD} to V_{USB/WLS_DRV} drops to V_{USB/WLS_IN} + 0.2 V (QOVP off); V_{USB/WLS_SNS} rising slew rate >10 V/µs	–	100	200	ns
$V_{USB\_SNS\_UVLO\_F}$ $V_{WLS\_SNS\_UVLO\_F}$	USB/WLS_SNS UVLO	V_{USB/WLS_SNS} falling	3.25	3.4	3.55	V
	Hysteresis	V_{USB/WLS_SNS} rising	–	0.8	–	V
$V_{USB\_SNS\_UVOK\_R}$ $V_{WLS\_SNS\_UVOK\_R}$	USB/WLS_SNS UVOK	V_{USB/WLS_SNS} rising	4.05	4.2	4.35	V
$V_{USB\_DRV\_ON}$ $V_{WLS\_DRV\_ON}$	USB/WLS_DRV ON voltage (V_{USB_DRV} – V_{USB_IN}) (V_{WLS_DRV} – V_{WLS_IN})	V_{USB/WLS_SNS_UVLO} < V_{USB/WLS_SNS} < V_{USB/WLS_OVP_THD}, V_{ARB} > 3.6 V; Up to 1 µA gate leakage (QOVP IGSS and PCB)	9	9.5	13.5	V
I_{PU_USB/WLS_DRV}	USB/WLS_DRV pull-up current	–	10	15	20	µA
$V_{USB\_DRV\_OFF}$ $V_{WLS\_DRV\_OFF}$	USB/WLS_DRV OFF voltage (V_{USB_DRV} – V_{USB_IN}) (V_{WLS_DRV} – V_{WLS_IN})	V_{USB/WLS_SNS} > V_{USB/WLS_OVP_THD} or V_{USB/WLS_SNS} < V_{USB/WLS_SNS_UVLO}	-2	-1.6	0	V
	USB_DRV OFF voltage (V_{USB_DRV} – V_{GND})	V_{USB_SNS} > $V_{USB\_OVP\_THD}$ or V_{USB_SNS} < $V_{USB\_SNS\_UVLO}$	0	V_{USB_IN} -1.6	V_{USB_IN}	V
	WLS_DRV OFF voltage (V_{USB_DRV} – V_{GND})	V_{WLS_SNS} > $V_{WLS\_OVP\_THD}$ or V_{WLS_SNS} < $V_{WLS\_SNS\_UVLO}$	0	V_{WLS_IN} -1.6	V_{WLS_IN}	V
$t_{OVP\_FET\_en}$	USB/WLS OVP enable deglitch time	From V_{USB/WLS_SNS_UVLO} < V_{USB/WLS_SNS} < V_{USB/WLS_OVP_THD} to V_{USB/WLS_DRV} rises to VUSB/WLS_SNS + 2.5 V (QOVP on)	–	5	–	ms
$t_{OVP\_FET\_SS}$	USB/WLS OVP soft-start	V_{USB/WLS_DRV} rise from 10% to 90% with QOVP CISS = 1~4 nF	0.5	–	5	ms
Input voltage monitoring						
V_{COARSE_DET}/ V_{LT_VT}	USB/WLS input coarse detection threshold	V_{USB_IN}/V_{WLS_IN} rising and falling	0.6	1.0	1.3	V
	Deglitch filter time for USB/WLS_IN I_{PD}	V_{USB_IN}/V_{WLS_IN} falling, extending USB/WLS_IN I_{PD}	–	25	–	ms
	Deglitch filter time for ship mode exit	V_{USB_IN}/V_{WLS_IN} rising	–	25	–	ms

Table 3-6 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Deglitch filter time for USB/WLS_LT_VT INT	V_{USB_IN}/V_{WLS_IN} rising and falling	–	1	–	ms
V_{UVLO}	USB/WLS input undervoltage lockout (UVLO) threshold	V_{IN} [a] falling; for LV options	3.5	3.6	3.7	V
		V_{IN} [a] falling; for MV options	6.6	6.9	7.2	V
		V_{IN} [a] falling; for HV options	9.3	9.6	9.9	V
	Hysteresis	V_{IN} [a] rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} and V_{WLS_IN} [a] rising and falling	–	20	–	ms
V_{OVLO}	USB/WLS input overvoltage lockout (OVLO) threshold	V_{IN} [a] rising, for LV option	6.2	6.4	6.6	V
		V_{IN} [a] rising, for MV option	16.8	17.2	17.6	V
		V_{IN} [a] rising, for HV option	21.5	22	22.5	V
	Hysteresis	V_{IN} [a] falling	–	200	–	mV
	Response time [b]	V_{IN} [a] rising at 5 V/µs, HV threshold	–	–	2	µs
		V_{IN} [a] rising at 5 V/µs, LV or MV threshold	–	10	–	ms
	Deglitch filter time	V_{IN} [a] falling	–	100	–	ms
V_{ASHDN}	USB/WLS input auto-shutdown threshold	V_{IN} [a] –V_{SYS}, V_{IN} [a] falling	50	130	190	mV
	Hysteresis	V_{IN} [a] rising	–	80	–	mV
	Deglitch filter time	V_{IN} [a] rising and falling	–	20	–	ms
V_{REVI}	USB/WLS input reverse-current threshold	V_{IN} [a] –V_{SYS}, V_{IN} [a] falling	-220	-130	-70	mV
	Hysteresis	V_{IN} [a] rising	–	80	–	mV
	Deglitch filter time	V_{IN} [a] falling	–	100	–	µs
		V_{IN} [a] rising	–	1	–	ms
Input current limit						
I_{SUSP_USB}	USB_IN suspend mode current	USB_IN path in suspend mode, V_{USB_IN} = 5 V, V_{BAT} = 4.5 V	–	1	1.2	mA
		USB_IN path in suspend mode, V_{USB_IN} = 5V, VBAT = 3.6 V	–	2.5	3.0	mA
I_{SUSP_WLS}	WLS suspend mode current	WLS_IN path in suspend mode, V_{WLS_IN} = 5 V, V_{BAT} = 4.4 V	–	1.0	1.2	mA
		WLS_IN path in suspend mode, V_{WLS_IN} = 5 V, V_{BAT} = 3.6 V	–	2.5	3.0	mA
I_{LIM_USB}	USB path maximum input current limit	USB 2.0 option: 100 mA mode, T= 0°C to +70°C, USB_IN = 5 V	70	85	100	mA
		USB 3.0 option: 150 mA mode, T= 0°C to +70°C, USB_IN = 5 V	115	–	150	mA

Table 3-6 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		USB 2.0 option: 500 mA mode, T= 0°C to +70°C, USB_IN = 5 V	450	475	500	mA
		USB 3.0 option: 900 mA mode, T= 0°C to +70°C, USB_IN = 5 V	810	855	900	mA
		Type-C 1.5 A mode, T = 0°C to +70°C, USB_IN = 5 V	1350	1425	1500	mA
		Type-C 3.0 A mode, T = 0°C to +70°C, USB_IN = 5 V	2700	2850	3000	mA
		USB high-current mode (0 A–50 mA–5.0 A programmable), VUSB_IN =5 V to 20 V, 0.5 A ≤ ILIM_USB ≤5 A, T = 0°C to +70°C	0.9 × I_{LIM_USB}	0.95 × I_{LIM_USB}	I_{LIM_USB}	mA
I_{LIM_WLS}	WLS path maximum input current limit	[0 A:50 mA:3 A] programmable	0	–	3	A
	Accuracy	V_{WLS_IN} = 5 V to 20 V, 0.5 A ≤ I_{LIM_WLS} ≤ 3 A, T=0°C to +70°C	0.9 × I_{LIM_WLS}	0.95 × I_{LIM_WLS}	I_{LIM_WLS}	mA
Automatic input current limiting (AICL)						
V_{AICL_CLPS}	LV AICL voltage collapse threshold	Programmable range (8 settings in 100 mV steps); V_{USB_IN} falling	4.1	–	4.8	V
	MV AICL voltage collapse threshold	Programmable range (8 settings in 200 mV steps); V_{USB_IN} falling	7.2	–	8.6	V
	HV AICL voltage collapse threshold	Programmable range (8 settings in 200 mV steps); V_{USB_IN} falling	10.2	–	11.6	V
	AICL voltage collapse threshold – continuous mode	Programmable range ■ 4.1 V: 100 mV: 4.8 V ■ 5.0 V: 200 mV: 12.8 V ■ 13.2 V: 400 mV: 19.2 V V_{USB/WLS_IN} falling	4.1	–	19.2	V
	Accuracy	V_{USB/WLS_IN} falling	-3.5	–	3.5	%
	Hysteresis	V_{USB/WLS_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB/WLS_IN} rising and falling; Programmable in 0.2, 0.5, 1, 2 ms	0.2	1	2	ms
	Deglitch filter time accuracy	–	-8	–	25	%
t_{AICL_step}	AICL step up time	Programmable in 2, 5, 10, 20 ms	2	10	20	ms
	AICL step down time 1	Programmable in 0.5, 1, 2, 5 ms	0.5	2	5	ms
	AICL step down time 2	Programmable in 20, 50, 100, 200 µs	20	100	200	µs
	Accuracy	–	-1	–	15	%

Table 3-6 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AICL_rerun}	AICL rerun timer	Programmable in 3, 12, 45, 360 sec	3	45	360	s
	Accuracy	–	-5	–	20	%
Input missing poller						
I_{IN_LOW}	I_{IN_LOW} comparator threshold	–	100	130	200	mA
	Deglitch filter time	I_{IN} rising or falling	–	1	–	ms
$I_{PD\_USB\_IN}$	USB_IN pull-down current source	V_{USB_IN} OV or UV	5	10	15	mA
$I_{PD\_WLS\_IN}$	WLS_IN pull-down current source	V_{WLS_IN} OV or UV	5	10	15	mA
$I_{PD\_MID\_CHG}$	MID_CHG pull-down current source	V_{USB_IN} or V_{WLS_IN} UV	20	30	40	mA
t_{IMP}	Input missing poller active timing	Charger buck disabled, current sink enabled	–	10	–	ms
$t_{IMP\_ATTEMPT}$	Number of IMP attempts	IMP conditions = true	–	–	3	
t_{IMP_RETRY}	After three attempts, the time before the IMP attempts to re-enable	IMP conditions = true	–	1	–	s
V_{IMP}	Input missing detection voltage threshold	Input missing poller active, charger buck disabled, 20 mA current sink enabled	–	V_{REVI}	–	V
Surge protection						
USB_IN surge protection	IEC61000-4-5 1.2/50 µs voltage surge waveform, ext. TVS diode [c]	–	-350	–	350	V
Maximum QUSB/ QWLS VDS during surge	IEC61000-4-5 1.2/50 µs voltage surge waveform, ext. TVS diode [c]	–	–	–	25	V
Maximum V_{USB_SNS} during surge	IEC61000-4-5 1.2/50 µs voltage surge waveform, ext. TVS diode [c]	–	–	–	45	V

[a] For the PM8550B charger, V_{IN} is V_{USB_IN} for the USB path or V_{WLS_IN} for wireless input path.
[b] The OVP response time is defined as from V_{IN} rises above V_{OVLO}, to switcher stops switching.
[c] External TVS diode: WillSemi ESD56161D24 25V reverse breakdown voltage, 30 V maximum clamping voltage at 150 A.

Table 3-7 USB Type-C and BC1.2 specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
APSD for BC1.2						
	D+/D- isolation resistors		350	500	650	Ω
V_{DP_SRC}	D+ source voltage	Load ≤ 250 µA	0.5	0.65	0.7	V
V_{DM_SRC}	D- source voltage	Load ≤ 250 µA	0.5	0.65	0.7	V
V_{DAT_REF}	Data detect voltage		0.3	0.35	0.4	V

Table 3-7 USB Type-C and BC1.2 specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DP_UP}	D+ pull-up voltage		3	3.3	3.6	V
I_{DM_SINK}	D- sink current		25	50	75	µA
I_{DP_SINK}	D+ sink current		25	50	75	µA
I_{DP_SRC}	Data contact detect current source		3.5	5.5	7.5	µA
R_{DM_DWN}	D- pull-down resistance		14.25	19.5	24.8	kΩ
$t_{DCD\_TIMEOUT}$	DCD timeout	Option 1	321	328	335	ms
		Option 2	642	656	670	ms
$t_{DP\_SRC\_ON}$	D+ source on time		100	–	–	ms
$t_{ENUM\_TIMEOUT}$	SDP enumeration timeout		–	–	2	min
t_{DPSRC_HICRNT}	D+ source off to high current		40	–	–	ms
t_{DPSRC_CON}	D+ source off to connect		40	–	–	ms
USB Type-C						
CC_{CAP}	Maximum CC pin capacitance		200	–	600	pF
Z_{OPEN}	Sink minimum open-circuit CC impedance to ground	In Disabled or Error Recovery state	126	420	–	kΩ
$V_{CC\_CLAMP\_SNK}$	Sink CC clamp voltage	As Rd during shutdown	0.88	1.1	1.32	V
R_{PD_SNK}	Sink crude sensor pull-down resistor	Before source attach	150 [a]	200	250	kΩ
R_{PU_SRC}	Sink crude sensor pull-up resistor	Before sink attach	75 [b]	100	125	kΩ
Rd	Sink Rd pull-down resistor		4.59	5.1	5.61	kΩ
I_{RP_SRC}	Source Rp current source – default USB		64	80	96	µA
	Source Rp current source – 1.5 A		166	180	194	µA
	Source Rp current source – 3.0 A		304	330	356	µA
vSafe0V			0	–	0.8	V
vSafe5V			4.75	–	5.5	V
$V_{BUS\_RMV\_5V}$	Sink VBUS removal detection threshold if = 5 V (vSinkDisconnect)	V_{USB_IN} falling; for determining exit from Attached.SNK state	0.8	2.5	3.67	V
	Hysteresis	V_{USB_IN} rising	–	500	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{BUS\_RMV\_9V}$	Sink VBUS removal detection threshold if = 9 V	V_{USB_IN} falling; for determining exit from Attached.SNK state	6.6	6.9	7.2	V
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{BUS\_RMV\_12V}$	Sink VBUS removal detection threshold if = 12 V	V_{USB_IN} falling; for determining exit from Attached.SNK state	9.3	9.6	9.9	V
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{SNK\_RMV\_PPS}$	Sink VBUS removal detection threshold if > 5 V through PD (vSinkDisconnectPD)	[3.7 V:0.1 V:5.2 V], 16 steps	3.7	–	5.2	V
		[5.4 V:0.2 V:11.6 V], 32 steps	5.4	–	11.6	V
		[12 V:0.4 V:18 V], 16 steps	12	–	18	V

Table 3-7 USB Type-C and BC1.2 specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy	V_{USB_IN} falling	-3.5	–	3.5	%
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$t_{CCDebounce}$	Time a port shall wait before it can determine it is attached	Transitioning between the AttachWait.SNK/SRC state and the Attached.SNK/SRC state; programmable range (103, 125, 150, 175)	100	150	200	ms
$t_{PDDebounce}$	Time a port shall wait before it can determine it is either detached or there has been a change in the Type-C current advertisement	Programmable in 12, 14, 16, 18 ms	10	14	20	ms
V_{CONN} switch						
V_{CONN}	V_{CONN} voltage range	V_{CONN} enabled, 3.2 V≤ VPH_PWR ≤ 4.5 V	3.0	–	4.5	V
	V_{CONN} load	V_{CONN} enabled, VPH_PWR ≥ 3.2 V	1.5	–	–	W
R_{VCONN}	V_{CONN} switch resistance	V_{CONN} enabled, VPH_PWR ≥ 3.2 V T = 0°C to +70°C	–	–	400	mΩ
I_{OCP_VCONN}	V_{CONN} overcurrent protection threshold	V_{CONN} enabled, VPH_PWR ≥ 3.2 V T = 0°C to +70°C, 100 mA option	10	100	200	mA
		200 mA option	100	200	350	mA
		300 mA option	200	300	450	mA
		400 mA option	300	400	600	mA
		500 mA option	450	500	750	mA
$V_{DIP\_VCONN\_SS}$	VPH_PWR dip when V_{CONN} soft-start	10 µF V_{CONN} load; enable V_{CONN}	0	–	200	mV
t_{VCONN_ON}	V_{CONN} powering on time	From the source supplies VBUS (reaches vSafe5V) to VCONN reaches the minimum valid voltage.	–	–	2	ms
t_{VCONN_OFF}	V_{CONN} powering off time	From the time that a Sink is detached or as commanded until V_{CONN} supply is disabled and the bulk capacitance is removed	–	–	35	ms
SBU						
	SBU1/2 R_{PD}		1.0	1.5	2.0	MΩ
UFCS D+ (3.3 V input) to GPIO (1.8/1.2 V output) buffer						
	$V_{IH\_DpDm\_3p3}$	VDDA = 3.3 V	2.31	3.3	3.6	V
	$V_{IL\_DpDm\_3p3}$	VDDA = 3.3 V	-0.3	0.0	0.99	V
	$V_{OH\_GPIO\_1p8}$	VDDB = 1.8 V	1.44	–	1.8	V
	$V_{OL\_GPIO\_1p8}$	VDDB = 1.8 V	0	–	0.36	V
	$V_{OH\_GPIO\_1p2}$	VDDB = 1.2 V	0.96	–	1.2	V
	$V_{OL\_GPIO\_1p2}$	VDDB = 1.2 V	0	–	0.24	V
	t_{Rise} on GPIO	10% to 90%; 10 pF on GPIO3/4	–	1	–	µs
	t_{Fall} on GPIO	10% to 90%; 10 pF on GPIO3/4	–	1	–	µs
UFCS GPIO (1.8/1.2 V input) to D- (3.3 V output) buffer						

Table 3-7 USB Type-C and BC1.2 specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	$V_{IH\_GPIO\_1p8}$	VDDB = 1.8 V	1.17	–	1.8	V
	$V_{IL\_GPIO\_1p8}$	VDDB = 1.8 V	0	–	0.63	V
	$V_{IH\_GPIO\_1p2}$	VDDB = 1.2 V	0.78	–	1.2	V
	$V_{IL\_GPIO\_1p2}$	VDDB = 1.2 V	0	–	0.42	V
	$V_{OH\_DpDm\_3p3}$	VDDA = 3.3 V, 0 mA ≤ IO ≤ 0.5 mA	1.44	3.3	3.6	V
	$V_{OL\_DpDm\_3p3}$	VDDA = 3.3 V, -0.5 mA ≤ IO ≤0 mA	0	–	0.6	V
	t_{Rise} on D-	10% to 90%; 0.2 nF on D+/D-	–	1	–	µs
	t_{Fall} on D-	90% to 10%; 0.2 nF on D+/D-	–	1	–	µs
	Output impedance	Buffer disabled, 3.3 V VDDA off	0.5			mΩ

[a] R_{PD_SNK} (min) must be higher than minimum zOPEN (126 kΩ) so the source does not treat R_{PD_SNK} as Rd.
[b] R_{PU_SRC} (min) must be higher than maximum Rp (56 kΩ) so the sink does not treat R_{PU_SRC} as Rp

3.5.2 Battery charger specifications

Table 3-8 1S battery charger specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{TRKL}	Trickle charge current	$V_{BATT} < V_{TRKL}$	25	50	75	mA
V_{TRKL}	Trickle charge to pre-charge threshold		2.0	2.1	2.2	V
I_{PRE_CHG}	Pre-charge current range	Programmable [100 mA:50 mA:250 mA] [300 mA:100 mA:600 mA]	100	–	600	mA
	Accuracy	T= 0°C to +70°C	± 10% of setting ± 10 mA			
V_{P2F}	Pre-charge to fast-charge voltage threshold		V_{SYS_MIN} [a]			V
V_{SYS_MIN}	Minimum VPH regulated output voltage range	Group 1: [2.8 V:0.2 V:3.4 V]	2.8	3.0	3.4	V
		Group 2: [4.0 V:0.2 V:4.6 V]	4.0	–	4.6	V
	Accuracy	500 mA load, $V_{BAT1} < V_{SYS\_MIN}$	-2	–	2	%
V_{SYS}	VPH_PWR (V_{SYS}) output voltage	V_{IN} present, during trickle/pre-charging, $V_{BAT1} < V_{SYS\_MIN} - V_{BAT\_TRACK}$	V_{SYS_MIN}			V
		V_{IN} present, during pre-charging, $V_{SYS\_MIN} - V_{BAT\_TRACK} < V_{BAT1} < V_{SYS\_MIN}$	$V_{BAT1} + V_{BAT\_TRACK}$			V
		V_{IN} present, during fast charging, $V_{BAT1} > V_{SYS\_MIN}$	$V_{BAT1} + I_{CHG} \times R_{DSON\_BF}$			V
		V_{IN} present, charging terminated or disabled	$V_{BAT1} + V_{BAT\_TRACK}$			V
V_{BAT_TRACK}	V_{BAT} tracking voltage during pre-charge	VPH = VBAT * (1 + X) X = 7%, 8%, 9%	–	9	–	%
			–	8	–	%
			–	7	–	%
	V_{BAT} tracking voltage after EoC	VPH = VBAT * (1 + X) X = 0%, 0.5%, 1%, 2%, 3%	–	3	–	%

Table 3-8 1S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
			–	2	–	%
			–	1	–	%
			–	0.5	–	%
			–	0	–	%
	Accuracy		-20		+20	mV
I_{FC}	Fast charge current (FCC) range	Programmable (200 settings in 60 mA steps with 4.22 kΩ R_{SUM_ICHG})	0	–	12	A
	Accuracy when using QBAT1 sensing	T= 0°C to +70°C, 0.5 A < I_{FC} < 3 A	-10	–	10	%
		T= 0°C to +70°C, $I_{FC} \geq$ 3.0 A	-5	–	5	%
		T= 25°C, 0.5 A < I_{FC} < 3 A	-5	–	5	%
		T= 25°C, $I_{FC} \geq$ 3.0 A	-2.5	–	2.5	%
	FCC soft-start slew rate	Programmable stepper: 60 mA every 25/50/100/200 µs	25	–	200	60 mA/ X µs
	FCC soft-stop slew rate	Programmable stepper: 60 mA every 25/50/100/200 µs	25	–	200	60 mA/ X µs
V_{FLT}	Float voltage range	Programmable (120 settings with 10 mV steps), T= 0°C to +70°C	3.6	–	4.79	V
	Accuracy	VFLT < 4.2 V, EN_BATT_DIFFSENSE = 1, T = 0°C to +70°C	-1	–	1	%
		VFLT $\geq$ 4.2 V, EN_BATT_DIFFSENSE = 1, T = 0°C to +70°C	-0.5	–	0.5	%
I_{TERM_ADC}	Charge termination current range	IADC range	50	200	750	mA
	Accuracy	IADC internal current sense, V_{BATT} = 4.2 V–4.55 V, I_{TERM} = 200 mA, T = 0°C to +70°C	-25	–	25	mA
	Deglitch filter time	Charger sniffs FG making IADC requests	100	–	4000	ms
V_{RECHG}	VBAT ADC based automatic recharge threshold	Programmable VBAT range	3.6	–	4.8	V
	Accuracy	T= 0°C to +70°C	-20	–	+20	mV
	Deglitch filter time	Charger make 1 VBAT ADC request (16 # of average) every 1 sec	8	–	4000	ms
SoC_{RECHG}	SoC-based automatic recharge threshold	Programmable SoC range	0	–	100	%
	Accuracy	T= 0°C to +70°C	-1	–	+1	%
	Deglitch filter time	FG update SoC every 1 sec	100	–	4000	ms
$V_{INHIBIT}$	VBAT ADC based charger inhibit threshold voltage range	Programmable VBAT range	3.6	–	4.8	mV
	Accuracy	T= 0°C to +70°C	-20	–	20	mV
	Hysteresis	VBATT falling,50/100/150/200 mV	50	100	200	mV

Table 3-8 1S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LOW_BATT}	VBAT ADC based low-battery voltage/SYSOK detection (triggers PMIC power-on) threshold range	Programmable VBAT range	2.4	2.8	3.2	V
	Accuracy	T= 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} rising, 50/100/150/200 mV	50	100	200	mV
V_{BATT_OV}	Battery overvoltage lockout	V_{BATT} rising, above V_{FLT}	30	40	50	mV
			50	60	70	mV
			70	80	90	mV
			90	100	110	mV
	Hysteresis	V_{BATT} falling	10	20	30	mV
	Deglitch filter time	V_{BATT} rising or falling; Programmable in 5/10/15/20 ms	5	–	20	ms
$V_{PH\_HV\_ALM}$	V_{SYS} high-voltage alarm	[4.3 V: 0.1 V: 5.0 V] programmable	4.3	4.8	5.0	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	50	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYS\_HV\_ALM}$, Programmable (10/100/1000 µs)	10	10	1000	µs
V_{PH_OV}	System overvoltage protection threshold	[4.5 V: 0.1 V: 5.2 V] programmable	4.5	5.0	5.2	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	75	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYSOV}$, Programmable (10/100/1000 µs)	10	100	1000	µs

[a] On PMIC5 chargers, the QBAT linear operation is removed, and pre-charge to fast-charge transition happens when V_{BAT} reaches V_{SYS_MIN} threshold.

Table 3-9 2S battery charger specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{TRKL}	Trickle charge current	At 1S battery level [a]	50	100	150	mA
		At 2S battery level [b]	25	50	75	mA
V_{TRKL}	Trickle charge to pre-charge threshold	At 2S battery level	4.0	4.2	4.4	V
I_{PRE_CHG}	Pre-charge current range	At 1S battery level: 8 settings [100 mA:50 mA:250 mA] [300 mA:100 mA:600 mA]	100	–	600	mA
		At 2S battery level: 8 settings	50	–	300	mA
	Accuracy	T= 0°C to +70°C	± 10% of setting ± 10 mA			
V_{P2F}	Pre-charge to fast-charge voltage threshold	At 1S battery level	V_{SYS_MIN} [c]			V
		At 2S battery level	2 × V_{SYS_MIN}			V
Charge current control when charging via QPH1 path						

Table 3-9 2S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{FC}	Fast charge current (FCC) range at 1S battery level	Programmable range (200 settings in 120 mA steps with 4.22 kΩ R_{SUM_ICHG})	0	–	24 [d]	A
	Fast charge current (FCC) range at 2S battery level	Programmable range (200 settings in 60 mA steps with 4.22 kΩ R_{SUM_ICHG})	0	–	12	A
	Accuracy when using QBAT1 sensing	T= 0°C to +70°C, 0.5 A < I_{FC} < 3 A	-10	–	10	%
		T= 0°C to +70°C, $I_{FC} \geq$ 3.0 A	-5	–	5	%
		T= 25°C, 0.5 A < I_{FC} < 3 A	-5	–	5	%
		T= 25°C, $I_{FC} \geq$ 3.0 A	-2.5	–	2.5	%
Charge current control when charging via QPH2 path						
I_{FC}	Fast charge current (FCC) range at 2S battery level	At 2S battery level: 200 settings in 60 mA steps with 4.22 kΩ R_{SUM_ICHG})	0	–	12	A
	Accuracy when using external 1 mΩ Rsns	T= 0°C to +70°C, 1 A < I_{FC} < 3 A	-10	–	10	%
		T= 0°C to +70°C, $I_{FC} \geq$ 3.0 A	-5	–	5	%
		T= 25°C, 1 A < I_{FC} < 3 A	-5	–	5	%
		T= 25°C, $I_{FC} \geq$ 3.0 A	-2.5	–	2.5	%
	Accuracy when using I_{BUCK_DC} sensing	T= 0°C to +70°C, 1 A < I_{FC} < 2 A	-15	–	15	%
		T= 0°C to +70°C, IFC $\geq$ 2.0 A	-7.5	–	7.5	%
		T= 25°C, 1 A < I_{FC} < 2 A	-7.5	–	7.5	%
		T= 25°C, $I_{FC} \geq$ 2.0 A	-5	–	5	%
	Accuracy when using I_{BAT2} = I_{BUCK_DC} + I_{QBAT1}/2	2 A $\leq$ I_{FC} $\leq$ 6.5 A, I_{BUCK_DC} = 2 A ~ 6.5 A, I_{QBAT1} = 0 A ~ 5 A; T = 25°C	-400	-	400	mA
		2 A $\leq$ I_{FC} $\leq$ 6.5 A, I_{BUCK_DC} = 2 A ~ 6.5 A, I_{QBAT1} = 0 A ~ 5 A; T = -20°C~70°C	-600	-	600	mA
V_{FLT}	Float voltage range	At 1S battery level: (120 settings with 10 mV steps)	3.6	–	4.79	V
		At 2S battery level: (120 settings with 20 mV steps)	7.2	–	9.58	V
	Accuracy	V_{FLT} < 8.4 V, EN_BATT_DIFFSENSE = 1, T = 0°C to +70°C	-1	–	1	%
		VFLT $\geq$ 8.4 V, EN_BATT_DIFFSENSE = 1, T = 0°C to +70°C	-0.5	–	0.5	%
I_{TERM_ADC}	Charge termination current range	IADC range	50	200	750	mA
	Accuracy	IADC internal current sense, V_{BATT} = 4.2 V–4.55 V, I_{TERM} = 200 mA, T = 0°C to +70°C	-25	–	25	mA
	Deglitch filter time	Charger sniffs FG making IADC requests	100	–	4000	ms
V_{RECHG}	VBAT ADC based automatic recharge threshold	At 1S battery level	3.6	–	4.8	V
		At 2S battery level	7.2	–	9.6	V
	Accuracy	T= 0°C to +70°C	-20	–	+20	mV
	Deglitch filter time	Charger make 1 VBAT ADC request (16 # of average) every 1 sec	8	–	4000	ms
SoC_{RECHG}	SoC-based automatic recharge threshold	Programmable SoC range	0	–	100	%

Table 3-9 2S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy	T= 0°C to +70°C	-1	–	+1	%
	Deglitch filter time	FG update SoC every 1 sec	100	–	4000	ms
$V_{INHIBIT}$	VBAT ADC based charger inhibit threshold voltage range	At 1S battery level	3.6	–	4.8	V
		At 2S battery level	7.2	–	9.6	V
	Accuracy	T= 0°C to +70°C	-20	–	20	mV
	Hysteresis	VBATT falling, 50/100/150/200 mV	50	100	200	mV
V_{LOW_BATT}	VBAT ADC based low-battery voltage/SYSOK detection (triggers PMIC power-on) threshold range	At 1S battery level	2.4	2.8	3.2	V
		At 2S battery level	4.8	–	6.4	V
	Accuracy	T= 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} rising, 50/100/150/200 mV	50	100	200	mV
V_{BATT_OV}	Battery overvoltage lockout	V_{BATT} (2S) rising,above V_{FLT}	60	80	100	mV
			100	120	140	mV
			140	160	180	mV
			180	200	220	mV
	Hysteresis	V_{BATT} (2S) falling	20	40	60	mV
	Deglitch filter time	V_{BATT} (2S) rising or falling; Programmable in 5/10/15/20 ms	5	–	20	ms
$V_{PH\_HV\_ALM}$	V_{SYS} high-voltage alarm	[4.3 V: 0.1 V: 5.0 V] programmable	4.3	4.8	5.0	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	50	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYS\_HV\_ALM}$, Programmable (10/100/1000 µs)	10	10	1000	µs
V_{PH_OV}	System overvoltage protection threshold	[4.5 V: 0.1 V: 5.2 V] programmable	4.5	5.0	5.2	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	75	–	mV
	Deglitch filtertime	$V_{SYS} > V_{SYSOV}$, Programmable (10/100/1000 µs)	10	100	1000	µs
QPH1/2 Automatic Charging Path Selection (ACPS)						
$V_{IN\_HI\_ACPS}$	V_{IN} high comparator for ACPS	$V_{USB/WLS\_IN} – V_{BAT2}$, V_{IN} falling, [50/100/150/200 mV] programmable	50	100	200	mV
	Accuracy		-30	–	30	mV
	Hysteresis	V_{IN} rising	40	60	80	mV
	Deglitch filter time	V_{IN} rising, [2.5/5/10/20 ms]	2.5	–	20	ms
		V_{IN} falling, [10/20/40/80 µs]	10	–	80	µs
V_{REVI2}		$V_{USB/WLS\_IN} – V_{BAT2}$, V_{IN} falling, [-300/-500/-700/-900 mV] programmable	-300	–	-900	mV
	Accuracy		-100	–	100	mV
	Hysteresis	V_{IN} rising	40	60	80	mV

Table 3-9 2S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{BAT\_HI\_ACPS}$	V_{BAT} high comparator for ACPS	V_{BAT1_PWR} rising	V_{SYS_MIN}			V
	Accuracy		-2	–	2	%
	Hysteresis	V_{BAT1_PWR} rising	75	100	125	mV
	Deglitch filter time	V_{BAT1_PWR} rising, [10/20/40/80 µs]	10	–	80	ms
		V_{BAT1_PWR} falling, [1/5/10/20 µs]	1	–	20	µs
$V_{PH1\_SPIKE\_ACPS}$	V_{PH1_PWR} voltage spike above V_{BAT1_PWR} upon ACPS	QPH2 path to QPH1 path switching; charging enabled, V_{BAT2_PWR} = 6 V ~ 9 V, V_{BAT1_PWR} = 3 V ~ 4.5 V; C_{OUT} = 10 µF, V_{PH1} = 20 µF, C_{BAT1} = 10 µF, C_{BAT2} = 10 µF	–	–	500	mV
$V_{PH1\_DIP\_ACPS}$	V_{PH1_PWR} voltage dip below V_{BAT1_PWR} upon ACPS	QPH1 path to QPH2 path switching; charging enabled, V_{BAT2_PWR} = 6 V ~ 9 V, V_{BAT1_PWR} = 3 V ~ 4.5 V; C_{OUT} = 10 µF, V_{PH1} = 20 µF, C_{BAT1} = 10 µF, C_{BAT2} = 10 µF	–	–	200	mV
QPH1						
R_{DSON_QPH1}	QPH1 on-resistance	T=0°C to +70°C	–	17	21	mΩ
QPH2_DRV						
$V_{QPH2\_DRV\_ON}$	QPH2 driver on voltage (V_{QPH2_DRV} – V_{BAT2_PWR})	QPH2_DRV enabled, V_{BAT2_PWR} = 6 V – 9 V; Up to 10 µA QPH2 gate to source leakage	9	10	10.5	V
$V_{QPH2\_DRV\_OFF}$	QPH2 driver off voltage (V_{QPH2_DRV} – GND)	QPH2_DRV disabled	–	0	–	V
$I_{PU\_QPH2\_DRV}$	QPH2_DRV pull-up current		20	30	40	µA
T_{QPH2_ON}	QPH2 turn-on time	QPH2 gate capacitance = 2 nF; from 0 V to 90% of $V_{QPH2\_DRV\_ON}$	1	–	5	ms
QBYP2_DRV_VSW						
$V_{ON\_QBYP2\_DRV1}$	QBYP2_DRV1 ON voltage (V_{QBYP2_DRV1} – V_{SW})	Up to 1 µA gate leakage (QBYP2 Gate 1 I_{GSS} and PCB)	5.0	5.4	6.0	V
$V_{OFF\_QBYP2\_DRV1}$	QBYP2_DRV1 OFF voltage (V_{QBYP2_DRV1} – V_{SW})		–	0	–	V
$R_{PU\_QBYP2\_DRV1}$	QBYP2_DRV1 pull up resistance		–	6.0	–	kΩ
$R_{PD\_QBYP2\_DRV1}$	QBYP2_DRV1 pull down resistance		0.2	1.2	2.2	Ω
QBYP2_DRV_VOUT						
$V_{ON\_QBYP2\_DRV2}$	QBYP2_DRV2 ON voltage (V_{QBYP2_DRV2} – V_{OUT})	Up to 1 µA gate leakage (QBYP2 Gate 2 IGSS and PCB)	5.0	5.4	6.0	V
$V_{OFF\_QBYP2\_DRV2}$	QBYP2_DRV2 OFF voltage (V_{QBYP2_DRV2} – V_{OUT})		–	0	–	V
$R_{PU\_QBYP2\_DRV2}$	Bypass_DRV pull up resistance		–	6.0	–	kΩ
$R_{PD\_QBYP2\_DRV2}$	Bypass_DRV pull down resistance		0.2	1.2	2.2	Ω

[a] For 2S battery charging, PM8550B charger has to work with SMB1399 voltage charger. This spec is defined at PM8550B charger output, that is 1S battery level, for PM8550B simulation and testing purpose

[b] This spec is defined at SMB1399 output, that is, 2S battery level, for system level application purpose.

[c] On PMIC5 chargers, the QBAT linear operation is removed, and pre-charge to fast-charge transition happens when V_{BAT} reaches V_{SYS_MIN} threshold

[d] PM8550B charger buck is designed to deliver 6 A max at 2S battery level. The 10 A/12 A setting is for PM8550B + 2x SMB1396 triple charging, with total ICHG sensed current summed at ICHG_FB pin, for PM8550B to regulate total ICHG at 10 A/12 A max.

3.5.3 Buck regulator specifications

Table 3-10 Buck regulator specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD_5V LDO						
V_{DD_5V}	VDD_5V LDO regulated output voltage	In 3LBk/D2CP mode, I_{OUT} = 20 mA, $V_{USB\_IN}/V_{WLS\_IN} \geq$ 5.0 V,	4.8	5	5.2	V
		In 3LBk/D2CP mode, 4.0 V $\leq V_{BAT1\_PWR}$ (as source) $\leq$ 4.5 V, I_{OUT} = 20 mA	3.9	–	4.5	V
		In boost mode, I_{OUT} = 20 mA, $V_{USB\_IN}/V_{WLS\_IN} \geq$ 5.0 V	4.6	4.8	5.0	V
		In boost mode, 4.0 V $\leq V_{BAT1\_PWR}$ (as source) $\leq$ 4.5 V, I_{OUT} = 20 mA	3.9	–	4.5	V
$V_{DD\_5V\_UVLO}$	VDD_5V LDO undervoltage lockout	V_{USB_IN}/V_{WLS_IN} rising	2.6	2.8	3.0	V
		V_{USB_IN}/V_{WLS_IN} falling	2.0	2.2	2.4	V
IDD_5V	VDD_5VLDO output current	$V_{USB\_IN}/V_{WLS\_IN} \geq$ 5.0 V	20	–	–	mA
PWM buck regulator						
I_{BUCK_DC}	Buck DC max output current	Eight programmable settings ([4 A: 500 mA: 7.5 A]) See Note 1 for Vin and Fsw , Vsys= 3.6 V-4.6 V	4.0	6	7.5	A
F_{SW_BUCK}	Buck switching frequency range	Eight programmable settings	342	–	800	kHz
	Accuracy	T= 0°C to +70°C	-6	–	6	%
DC_{BUCK}	Buck duty cycle		0	–	100	%
$V_{P-P\_BUCK\_PWM}$	Buck output ripple in PWM mode	Note 1, 2 A Load, V_{BATT} = 3.9 V, PWM mode, FSW = 530 kHz	–	25	50	mV
$V_{P-P\_BUCK\_PSM}$	Buck output ripple in Pulse Skipping mode	Note 1, No Load, V_{BATT} = 3.0 V, Pulse Skip mode	–	50	100	mV
ΔVSYSLOAD	V_{SYS} output voltage load regulation	I_{SYS}= 0.1 A to 4 A, V_{BATT} = 3.9 V, PWM mode, charging disabled	–	5	–	mV/A
V_{DIP_BUCK}	Buck V_{OUT} (VPH) voltage dip due to positive load transient	V_{USB_IN}/V_{MID_CHG} = 5.0 V I_{LIM_USB} = 3 A, V_{BATT} = 0 V, $V_{PH} = V_{SYS\_MIN}$, I_{SYS_LOAD} 0.1 A to 2 A in 1 A/µs	-500	–	–	mV
V_{SPIKE_BUCK}	Buck V_{OUT} (VPH) voltage spike due to negative load transient	V_{USB_IN}/V_{MID_CHG} = 5/7/9/12 V, $V_{BATT} = V_{FLT}$ (charging done), I_{SYS_LOAD} 4.0 A to 0.1 A in 1 A/µs	–	–	500	mV
	Buck V_{OUT} (VPH) variation due to positive line transient	Charging disabled, V_{BAT} = 0 V/3.5 V/4.5 V, $V_{PH} = V_{SYS\_MIN}$ or V_{BAT_TRACK}, I_{SYS} = 2 A, V_{IN} = 5 V to 9 V, 9 V to 12 V, 12 V to 15 V, 15 V to 20 V in 0.1 V/µs	-100	–	100	mV

Table 3-10 Buck regulator specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Buck V_{OUT} (VPH) variation due to negative line transient	Charging disabled, V_{BAT} = 0 V/3.5 V/4.5 V, V_{PH} = V_{SYS_MIN} or V_{BAT_TRACK}, I_{SYS} = 2 A, V_{IN} = 20 V to 15 V, 15 V to 12 V, 12 V to 9 V, 9 V to 5 V in -0.1 V/µs	-100	–	100	mV
I_{DD_BUCK}	Buck active supply current	Switcher enabled, no load, V_{IN} = 5/9/12/15/20 V, V_{SYS} = 3.5/4/4.5 V, pulse skip mode	–	2	5	mA
		Switcher enabled, no load, V_{IN} = 5/9/12/15/20 V, V_{SYS} = 3.5/4/4.5 V, PWM mode	–	30	–	mA
R_{DSON_QUSB}	QUSB (16 V) $R_{DS(ON)}$	T= 0°C to +70°C	–	10	15	mΩ
R_{DSON_QWLS}	QWLS (16 V) $R_{DS(ON)}$	T= 0°C to +70°C	–	20	30	mΩ
R_{DSON_Q1}	Q1 (16 V) on-resistance	T= 0°C to +70°C	–	12	16	mΩ
R_{DSON_Q2}	Q2 (12 V) on-resistance	T= 0°C to +70°C	–	8	12	mΩ
R_{DSON_Q3}	Q3 (12 V) on-resistance	T= 0°C to +70°C	–	8	12	mΩ
R_{DSON_Q4}	Q4 (12 V) on-resistance	T= 0°C to +70°C	–	8	12	mΩ
R_{DSON_QBYP}	QBYP on-resistance	T= 0°C to +70°C	–	15	20	mΩ
η	QPH1 charging path efficiency	5 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	94.9	–	%
		5 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	93.7	–	%
		5 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	92.4	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	94.8	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	93.5	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	92.2	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	93.8	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	92.7	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	91.6	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	92.7	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	91.8	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	90.6	–	%
		20 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 1 A	–	–	–	%
		20 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 2 A	–	–	–	%
		20 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	–	–	%
	QPH2 charging path efficiency	10 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 3 A	–	96.7	–	%
		10 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 4 A	–	96.3	–	%
		10 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 5 A	–	95.6	–	%
		12 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 3 A	–	96.2	–	%
		12 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 4 A	–	95.7	–	%
		12 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 5 A	–	94.9	–	%
		15 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 3 A	–	96.0	–	%
		15 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 4 A	–	95.4	–	%
		15 V V_{USB_IN},8.8 V V_{BAT}, I_{CHG} = 5 A	–	94.7	–	%
		20 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 3 A	–	96.0	–	%

Table 3-10 Buck regulator specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		20 V V_{USB_IN},8.8 V V_{BAT}, I_{CHG} = 4 A	–	95.2	–	%
		20 V V_{USB_IN}, 8.8 V V_{BAT}, I_{CHG} = 5 A	–	94.4	–	%

3.5.4 Div2 charge pump specifications

Table 3-11 Div2 charge pump specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3LBk ↔ D2CP mode transition						
$V_{CMB\_WIN\_HI}$	Combo WIN_HIGH comparator (V_{MID}/2 vs. V_{PH})	Programable threshold: V_{MID}/2 - V_{PH} =	250	300	350	mV
			300	350	400	mV
			350	400	450	mV
			400	450	500	mV
		Hysteresis	–	50	–	mV
		Deglitch, V_{MID}/2 - V_{PH} > $V_{CMB\_WIN\_HI}$	–	100	–	µs
			–	200	–	µs
			–	400	–	µs
			–	800	–	µs
		Deglitch, V_{MID}/2 - V_{PH} < $V_{CMB\_WIN\_HI}$ - V_{HYST}	–	0.1	–	ms
			–	0.5	–	ms
			–	1	–	ms
			–	10	–	ms
$V_{CMB\_WIN\_LO}$	Combo WIN_LOW comparator (V_{MID}/2 - V_{PH})	Programable threshold: V_{MID}/2 - V_{PH} =	–	-100	–	mV
			–	-50	–	mV
			–	30	–	mV
			–	60	–	mV
		Accuracy	-25		+25	mV
		Hysteresis	–	15	–	mV
		Deglitch, V_{MID}/2 - V_{PH} < $V_{CMB\_WIN\_LO}$	–	100	–	µs
			–	200	–	µs
			–	400	–	µs
			–	800	–	µs
		Deglitch, V_{MID}/2 - V_{PH} > $V_{CMB\_WIN\_LO}$ + V_{HYST}	–	0.1	–	ms
			–	0.5	–	ms
			–	1	–	ms
			–	10	–	ms
Div2 operation						
DC_{D2CP}	Div2 CP Duty Cycle		–	50	–	%
	QPH1 2:1 charging efficiency	IOUT = 2 A	–	95.7	–	%
		IOUT = 3 A	–	95.0	–	%

Table 3-11 Div2 charge pump specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	V_{USB_IN} = ~9 V, 4.4 V V_{BAT}, 800 kHz F_{sw}, 3 × 22 µF CFLY, VARB and VDD5 favor VBAT1	IOUT = 4 A	–	94.0	–	%
		IOUT = 5 A	–	93.0	–	%
	QPH2 4:2 charging efficiency V_{USB_IN} = ~18 V, 8.8 V V_{BAT2}, 800 kHz F_{sw}, 3 × 22 µF CFLY, VARB and VDD5 favor VBAT1	IOUT = 2 A	–	96.7	–	%
		IOUT = 3 A	–	96.6	–	%
		IOUT = 4 A	–	96.2	–	%
		IOUT = 5 A	–	95.6	–	%

3.5.5 Reverse boost specifications

Table 3-12 Reverse boost regulator specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PWM boost regulator						
$V_{OUT\_BST\_USB}$	Boost regulator output voltage	Range 1: [4.8 V:100 mV:5.2 V] Range 2: [5.25 V:50 mV:5.5 V]	4.8	5.0	5.5	V
	Accuracy	All settings	-2	–	2	%
$V_{OUT\_BST\_WLS}$	Boost regulator output voltage	Range 1: [4.8 V:100 mV:5.2 V] Range 2: [5.25 V:50 mV:10 V] Range 3: [10.1 V:100 mV:12 V]	4.8	5.0	12	V
	Accuracy	All settings	-2	–	2	%
I_{OUT_BST}	Boost output current rating	V_{PH1} > 2.5 V, V_{OUT_BST} = 5 V	2	–	–	A
		V_{PH1} > 3.0 V, V_{OUT_BST} = 5 V	2.5	–	–	A
		V_{PH1} > 3.6 V, V_{OUT_BST} = 5 V	3	–	–	A
		V_{PH1} > 3.0 V, V_{OUT_BST} = 7.5 V	1.6	–	–	A
		V_{PH1} > 3.8 V, V_{OUT_BST} = 12 V	1	–	–	A
		V_{BAT2} > 6.0 V, V_{OUT_BST} = 12 V	1	–	–	A
Reverse boost soft-start						
	USB reverse boost soft-start current level	V_{USB_IN} < LT_VT	130	250	390	mA
		1 V < V_{USB_IN} < 3.6 V	370	500	750	mA
		3.6 V < V_{USB_IN} < 4.9 V	500	750	1100	mA
	USB reverse boost start-up overshoot	V_{USB_IN} above V_{OUT_BST} setting	–	–	+500	mV
	WLS reverse boost soft-start rate	V_{WLS_IN} < 5.5 V	–	–	1/300	V/µs
		V_{WLS_IN} > 5.5 V	–	–	1/300	V/µs
	WLS reverse boost start-up overshoot	V_{WLS_IN} above V_{OUT_BST} setting	–	–	+250	mV
Reverse boost OCP						
$I_{OUT\_BST\_OCP}$	Steady-state boost output current limit	Programmable ranges: ■ [1.0 A: 250 mA: 2.0 A] ■ [2.5 A: 500 mA: 3.5 A]	1.0	1.125	1.25	A
			1.25	1.375	1.5	A
			1.5	1.625	1.75	A
			1.75	1.875	2.0	A

Table 3-12 Reverse boost regulator specifications (cont.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
			2.0	2.25	2.5	A
			2.5	2.75	3.0	A
			3.0	3.25	3.5	A
			3.5	3.75	4.0	A
$T_{BOOST\_OCP\_RETRY}$	Number of boost restart attempts	$I_{BOOST} > I_{BOOST\_LIM}$	–	–	3	–
F_{SW_BOOST}	Boost switching frequency range	Eight programmable settings	480	–	1600	kHz
	Boost switching frequency accuracy	T = 0°C to +70°C	-6	–	6	%
$V_{P-P\_BOOST\_PWM}$	PWM boost output ripple	Note 1, 1 A load, V_{BAT1} = 4.0 V, PWM mode, F_{SW} = 0.8 MHz	–	50	100	mV
$V_{P-P\_BOOST\_PSM}$	PSM boost output ripple	Note 1, no load, V_{BAT1} = 4.0 V, pulse skip mode; deep skip mode enabled	–	50	100	mV
$V_{DIP\_BST\_USB}$	$V_{OUT\_BST\_USB}$ dip due to positive load transient	Note 1, V_{BATT} = 4.0 V, V_{USB_IN} = 5.0 V, F_{SW} = 0.8 MHz, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 0.1 A to 1.5 A in 0.3 A/us	-500	–	–	mV
		Note 1, V_{BATT} = 4.0 V, V_{USB_IN} = 5.0 V, F_{SW} = 0.8 MHz, I_{BOOST_LIM} = 3.0 A, I_{LOAD} 3.0 A to 0.1 A in 0.3 A/us	-600	–	–	mV
$V_{SPIKE\_BST\_USB}$	$V_{OUT\_BST\_USB}$ dip due to negative load transient	Note 1, V_{BATT} = 4.0 V, V_{USB_IN} = 5.0 V, F_{SW} = 0.8 MHz, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 1.5 A to 0.1 A in 0.3 A/us	–	–	+500	mV
		Note 1, V_{BATT} = 4.0 V, V_{USB_IN} = 5.0 V, F_{SW} = 0.8 MHz, I_{BOOST_LIM} = 3.0 A, I_{LOAD} 3.0 A to 0.1 A in 0.3 A/us	–	–	+600	mV
$V_{DIP\_BST\_WLS}$	$V_{OUT\_BST\_WLS}$ dip due to positive load transient	Note 1, V_{BATT} = 4.0 V, V_{WLS_IN} = 7.5 V, F_{SW} = 0.8 MHz, C_{WLS_SNS} = 25 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 0.1 A to 1 A in 100 µs	-200	–	–	mV
		I_{LOAD} 0.1 A to 1 A in 10 µs	-500	–	–	mV
		Note 1, V_{BATT} = 4.0 V, V_{WLS_IN} = 10 V, F_{SW} = 1.2 MHz, C_{WLS_SNS} = 25 µF, C_{MID_CHG} = 10 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 0.1 A to 1 A in 100 µs	-200	–	–	mV
		I_{LOAD} 0.1 A to 1 A in 10 µs	-700	–	–	mV
$V_{SPIKE\_BST\_WLS}$	$V_{OUT\_BST\_WLS}$ spike due to negative load transient	Note 1, V_{BATT} = 4.0 V, V_{WLS_IN} = 7.5 V, F_{SW} = 0.8 MHz, C_{WLS_SNS} = 25 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 1 A to 0.1 A in 100 µs	–	–	+200	mV
		I_{LOAD} 1 A to 0.1 A in 10 µs	–	–	+500	mV
		Note 1, V_{BATT} = 4.0 V, V_{WLS_IN} = 10 V, F_{SW} = 1.2 MHz, C_{WLS_SNS} = 25 µF, C_{MID_CHG} = 10 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 1 A to 0.1 A in 100 µs	–	–	+200	mV
		I_{LOAD} 1 A to 0.1 A in 10 µs	–	–	+700	mV

Table 3-12 Reverse boost regulator specifications (cont.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Boost V_{OUT} (V_{USB/WLS_IN}) variation due to positive line transient	V_{USB_IN} = 5.0 V or V_{WLS_IN} = 7.5/10/12 V, $I_{USB/WLS}$ = 1 A, V_{BAT_CELL} = 3.5 V/4.0/4.5 V, battery ESR = 100 mΩ, I_{SYS} = 4 A → 0 A in 1 A/us,	–	–	250	mV
	Boost V_{OUT} (V_{USB/WLS_IN}) variation due to negative line transient	V_{USB_IN} = 5.0 V or V_{WLS_IN} = 7.5/10/12 V, $I_{USB/WLS}$ = 1 A, V_{BAT_CELL} = 3.5 V/4.0/4.5 V, battery ESR = 100 mΩ, I_{SYS} = 0 A → 4 A in 1 A/us	-250	–	–	mV
I_{DD_BOOST}	Boost supply current	V_{BATT} = 4.0 V, V_{BOOST} = 5.0 V, PFM, OTG Mode, No load, Type-C disabled, VARB and VDD5 favor V_{BAT1}	–	2.0	2.5	mA
		V_{BATT} = 4.0 V, V_{BOOST} = 5.0 V, PFM, Type-C source mode, Rp-1.5 A pull-up (180 µA) enabled	–	2.2	2.7	mA
		V_{BATT} = 4.0 V, V_{BOOST} = 5.0 V, PFM, Type-C source mode, Rp-3 A pull-up (330 µA) enabled	–	2.4	2.9	mA
$E_{ff\_BOOST\_PWM}$	Boost efficiency in PWM mode	V_{BAT1} = 4.0 V, V_{USB_IN} = 5.0 V, PWM mode, F_{SW} = 0.8 MHz, 1.0 A load	–	94.9	–	%
		2.0 A load	–	94.3	–	%
		3.0 A load	–	92.8	–	%
		V_{BAT1} = 4.0 V, V_{WLS_IN} = 7.5 V, PWM mode, F_{SW} = 1.2 MHz, 1.0 A load	–	90.0	–	%
		V_{BAT1} = 4.0 V, V_{WLS_IN} = 10 V, PWM mode, F_{SW} = 1.2 MHz, 1.0 A load	–	89.5	–	%
		From V_{BAT2} = 8.0 V, V_{WLS_IN} = 10 V, PWM mode, FSW = 0.8 MHz, 1.0 A load	–	87.3	–	%
		From V_{BAT2} = 8.0 V, V_{WLS_IN} = 12 V, PWM mode, F_{SW} = 0.8 MHz, 1.0 A load	–	92.4	–	%
$E_{ff\_BOOST\_PFM}$	Boost efficiency in PFM mode	Note 1, V_{BATT} = 4.0 V, V_{USB_IN} = 5.0 V, PFM mode, 10 mA load	–	82	–	%

3.5.6 Full-Duty charge specifications

Table 3-13 Full-Duty charge specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-Duty Charge (FDC) via QPH1 path						
$R_{PATH\_FDC\_QPH1}$	FDC path impedance	From USB OVP to V_{BAT1_PWR}	–	63	–	mΩ
DC_{FDC_QPH1}	Buck duty cycle during FDC	V_{USB_IN} = 3.5 V ~ 4.5 V, V_{BAT1_PWR} = 3.5 V ~ 4.5 V;	–	–	100	%
Full-Duty Charge (FDC) via QPH2 path						
$R_{PATH\_FDC\_QPH2}$	FDC path impedance	From USB OVP to V_{BAT2_PWR}	–	50	–	mΩ

Table 3-13 Full-Duty charge specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC_{FDC_QPH2}	Buck duty cycle during FDC	V_{USB_IN} = 7 V ~ 9 V, V_{BAT2_PWR} = 7 V ~ 9 V;	–	–	100	%
Factory VBUS-to-VPH Pass-Through Normal Power Mode (FVPT NPM)						
$I_{DD\_FVPT\_NPM}$	Charger I_{USB} during USB-to-VPH pass-through mode in NPM	3.0 V < VBAT < 4.5 V, VBAT ≤ VBUS < VBAT+0.8 V, VBUS < 4.8 V, T = 25°C	–	4.5	5.0	mA
		T = 0°C to +70°C	–	–	–	–
		3.0 V < VBAT < 3.8 V, VBAT+1 V ≤ VBUS < 4.8 V, T = 25°C	–	5.5	6.0	mA
		T = 0°C to +70°C	–	–	–	–
Factory VPT Low Power Mode (FVPT LPM)						
R_{ON_QFVPT}	Factory VPT FET (Q_{FVPT}) from USB_SNS to VPH1_PWR	3.0 V < VBAT_PWR < 4.5 V 3.0 V < VUSB_SNS < 4.5 V Pin-to-pin; T = 15°C to 35°C	–	80	100	Ω
$I_{DD\_FVPT\_LPM}$	Charger I_{USB} during USB-to-VPH pass-through mode in LPM	3.0 V < VBAT < 4.5 V, VBAT ≤ VBUS < VBAT + 0.8 V, T = 25°C	–	30	60	µA

3.5.7 Battery interface specifications

Table 3-14 Battery interface specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QBAT						
R_{DSON_QBAT}	QBAT on-resistance	Battery FET (5 V) from VPH_PWR to VBAT_PWR ball-to-ball resistance	–	5.0	6.6	mΩ
I_{BF_DC}	Maximum continuous DC QBAT current	Battery discharging	–	–	12	A
I_{BF_PEAK}	Peak QBAT current	Battery discharging, max 10 ms	–	–	14	A
$I_{LKG\_VBAT\_SNS\_P}$	Leakage current into VBAT_SNS_P	PMIC off, VBAT_SNS_P = 2.5 V, VBAT_SNS_M = 0 V	–	–	1	mA
		PMIC on, VBAT_SNS_P = 2.5 V–4.5V, VBAT_SNS_M = 0 V	–	–	2	mA
		PMIC on, VBAT_SNS_P = 5.0 V–9.0 V, VBAT_SNS_M = 0 V	–	–	4	mA
QBAT soft-start						
$R_{DSON\_QBAT\_SS}$	Soft-start QBAT on-resistance	–	–	5	–	Ω
t_{QBAT_SS}	VPH rise time upon VBAT insertion	100 µF ~ 500 F VPH_PWR capacitance; VBAT - VPH < 1 V; VBAT = 2.5 V – 4.5 V	0.25	–	10	ms
I_{QBAT_SS}	IBAT during QBAT soft-start	100 µF ~ 500 µF VPH_PWR capacitance; measured from VBAT insertion + 50 µs to VPH = VBAT; VBAT = 2.5 V – 4.5 V	–	–	1.5	A
$V_{QBAT\_SS\_DONE}$	VPH1_PWR high comparator	Detects $V_{PH1\_PWR} > V_{BAT1\_PWR} – 1$ V; V_{BAT1_PWR} = 2.5 V – 4.5 V	–	1	–	V

Table 3-14 Battery interface specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QBAT fast-on						
$T_{QBAT\_FAST\_ON}$	Charger to battery switch-over time	From V_{IN} drop below V_{UVLO} to QBAT starts to conduct, 2 A I_{SYS}	–	–	10	ms
$V_{PH\_DIP\_FAST\_ON}$	V_{PH_PWR} voltage dip below V_{BAT_PWR} upon input removal	V_{USB_IN} = 5 V, I_{LIM_USB} = 3 A, V_{PH_PWR} = 3.6 V, V_{BATT} = 3.5 V, charging disabled; 2 A I_{SYS}; C_{BAT} = 10 µF, C_{SYS} = 22 µF	–	–	200	mV
R_{PD_VPH}	VPH pull-down load		–	100	–	Ω
Battery supplemental mode (BSM)						
V_{BSM_DET}	BSM detection comparator threshold	V_{PH1_PWR} – V_{BAT1_PWR} 50/100/150/200/ 300/400/500/ 600 mV programmable	-600	-50	-50	mV
		Accuracy	- (10% + 10 mV)	–	+ (10% + 10 mV)	
t_{BSM_ENTRY}	BSM activation time	From V_{PH_PWR} drop below V_{BSM_DET} to QBAT starts to conduct	–	–	5	ms
$V_{PH\_DIP\_BSM}$	V_{PH_PWR} voltage dip below V_{BAT_PWR} upon BSM	V_{USB_IN} = 5 V, I_{LIM_USB} = 500 mA, V_{PH_PWR} = 3.6 V, V_{BATT} = 3.5 V, charging disabled; V_{BSM_DET} = -50 mV; I_{SYS} rises from 100 mA to 3 A in 20 µs; C_{BAT} = 10 µF, C_{SYS} = 22 µF	–	–	200	mV
$I_{BSM\_TERM\_ANA}$	Analog BSM termination comparator range	Programmable range: 8 settings in 50 mA steps with 4.99 kΩ R_{SUM_ICHG}	100	200	450	mA
		Programmable range: 8 settings in 60 mA steps w/ 422 kΩ R_{SUM_ICHG}	120	240	540	mA
	IBSM_TERM_ANA comparator accuracy	T = 0°C to +70°C	± 10% of setting ± 50 mA			
$t_{BSM\_EXIT\_ANA}$	Analog BSM termination time	From IBAT across IBSM_TERM_ANA to QBAT stops conducting	–	–	5	ms
$I_{BSM\_TERM\_DIG}$	Digital BSM termination IADC samples	Programmable consecutive samples to determine IBAT (into the battery) exceeding 0 mA	1	–	4	mA
$t_{BSM\_EXIT\_DIG}$	Digital BSM termination time	From IBAT (into the battery) exceeding 0 mA to QBAT stops conducting	–	–	50	ms
Battery missing detection						
$t_{BAT\_GONE\_CHG}$	BAT_GONE debounce time for charging	Rising (battery removed)	38.8	40	46.4	ms
		Falling (battery present)	1.19	1.2	1.35	s
$t_{BAT\_GONE\_X2D2}$	BAT_GONE debounce time for X2D2_EN	Rising (battery removed)	38.8	40	46.4	us
		Falling: 1/5/10/20 ms programmable	1	5	20	ms

3.5.8 Miscellaneous specifications

Table 3-15 Miscellaneous specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VARB generation						
V_{ARB}	V_{ARB} voltage range	V_{USB/WLS_SNS}/V_{USB/WLS_IN} (as source) = 3.5 V to 25 V	3.0	–	5.5	V

Table 3-15 Miscellaneous specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{BAT1_PWR} (as source) = 4.0 V ~ 4.5 V	3.9	–	4.4	V
Thermal control and protection						
T_{CHG_TEMP}	Charger temperature sensor accuracy	T_{CHG_TEMP} = 40°C to 80°C, V_{USB_IN}/ $V_{WLS\_IN} \geq$ 5 V	-2.0	–	+2.0	°C
		T_{CHG_TEMP} = 0°C to 150°C, V_{USB_IN}/ $V_{WLS\_IN} \geq$ 5 V	-3.0	–	+3.0	°C
T_{SHDN}	Charger overtemperature shutdown threshold	T_{DIE} rising, Programmable range in 5°C steps	145	155	160	°C
		Accuracy	-3	–	+3	°C
		Hysteresis, T_{DIE} falling	15	20	25	°C
T_{TEMP_RST}	Charger hot reset threshold	T_{DIE} rising, Programmable range in 10°C steps	100	120	130	°C
		Accuracy	-3	–	+3	°C
		Hysteresis, T_{DIE} falling	4	–	6	°C
$T_{DIE\_REG\_H}$	Charger die temperature regulation window lower threshold	T_{DIE} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-3	–	+3	°C
$T_{DIE\_REG\_L}$	Charger die temperature regulation window lower threshold	T_{DIE} falling, ADC-based digital comparator	40	–	100	°C
		Accuracy	-3	–	+3	°C
$T_{USB\_REG\_H}$	USB connector temperature regulation window upper threshold	T_{CONN} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2	–	+2	°C
$T_{USB\_REG\_L}$	USB connector temperature regulation window lower threshold	T_{CONN} falling, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2	–	+2	°C
$T_{WLS\_REG\_H}$	WLS/SKIN temperature regulation window upper threshold	$T_{WLS/SKIN}$ rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2	–	+2	°C
$T_{WLS\_REG\_L}$	WLS/SKIN temperature regulation window lower threshold	$T_{WLS/SKIN}$ falling, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2	–	+2	°C
Watchdog and safety timers						
t_{CTOPC}	Pre-charge safety timer	Programmable (48 min-191 min)	-6	–	6	%
t_{CTOFC}	Complete charge safety timer	Programmable (382 min-1527 min)	-6	–	6	%
t_{CHG_HO}	Charger startup holdoff timer	Eight programmable settings	50	300	700	ms
		Accuracy	-1	–	15	%
t_{WD_SNARL}	Watchdog snarl timer	Programmable (1/16, 0.125, 0.25, 0.5, 1, 2, 4, 8) sec	1/16	–	8	s
		Accuracy	-6	–	6	%
t_{WD_BARK}	Watchdog bark timer	Programmable 16/32/64/128 sec	16	–	128	s
		Accuracy	-6	–	6	%
t_{WD_BITE}	Watchdog bite timer	Programmable 1/2/4/8 sec	1	–	8	s

Table 3-15 Miscellaneous specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Accuracy	-6	–	6	%
Logic inputs/outputs						
V_{IH}	Input logic-high threshold	KPD_PWR_N	1.4	–	–	V
V_{IL}	Input logic-low threshold	KPD_PWR_N	–	–	0.6	V
V_{OH}	Digital output high level	WLS_nEN, SYS_OK configured as CMOS push-pull output	1.5	1.8	–	V
V_{OL}	Digital output low level	WLS_nEN, SYS_OK configured as CMOS push-pull output, or SYS_OK configured as NMOS open-drain output	–	0.1	0.3	V
$V_{OH\_CC\_OUT}$	CC_OUT output high level	CCOUT_VIO_SEL = 1 (1.8 V)	1.44	1.8	–	V
		CCOUT_VIO_SEL = 0 (1.2 V)	0.96	1.2	–	V
$V_{OL\_CC\_OUT}$	CC_OUT output low level	CCOUT_VIO_SEL = 1 (1.8 V)	–	0	0.36	V
		CCOUT_VIO_SEL = 0 (1.2 V)	–	0	0.24	V
R_{PULL}	Push-pull output pull-up resistance	Output configured as push-pull, VDD = 1.8 V	–	1.27	–	kΩ
I_{LEAK}	Leakage current on digital input (KPD_PWR_N) or open-drain output (SYS_OK)	KPD_PWR_N = 1.8 V SYS_OK = 1.8 V	–	–	1	mA

3.6 eUSB2 repeater

The eUSB2 repeater has to be in complete compliance with the *Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification* (latest revision), in particular with regards to the AC/DC characteristics of the high-speed transceiver.

PM8550B/PM8550BH/PM8550BHS/PM8550BHP eUSB2 characteristics are specified in Table 3-16.

Table 3-16 eUSB2 electrical specifications

Parameter	Description	Min	Typ	Max	Units
P_{SLEEP}	Total sleep power	–	–	3.2	µW
P_{DET}	Detach power	–	–	100	µW
P_{L2S}	L2 suspend power	–	–	150	µW
PL1S	L1 sleep power	–	–	5	mW
PLSA	Low speed active power	–	–	20	mW
PFSA	Full speed active power	–	–	20	mW
P_{HSA}	High speed active power	–	–	88	mW

3.7 Qualcomm battery gauge

The Qualcomm battery gauge hardware is basically an ADC scheduler that collects battery voltage, current, and temperature data.

Table 3-17 Qualcomm battery gauge performance specifications

Parameter	Min	Typ	Max	Units
Supported Qualcomm battery range I_{batt} range (A)	- 20	–	+20	A
Typical Qualcomm battery gauge accuracy at 25°C, +1 A/-1 A battery current	–	± 1	–	%

3.8 ADC

This module contains all of the multiplexer circuitry for the PM8550B/PM8550BH/PM8550BHS/PM8550BHP device, as well as two analog-to-digital converters (ADCs); one for voltage signals known as the VADC, and the other for current signals known as the IADC. This module is standalone from the other modules and takes care of all analog-to-digital needs on the PM8550B/PM8550BH/PM8550BHS/PM8550BHP device for the charger module, battery interface module, the Qualcomm battery gauge module, GPIOs, and battery current limiting (BCL). The below tables are valid for the temperature range of -20°C to 70°C.

Table 3-18 Analog multiplexer and scaling functions

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
0	0	GND_REF	Pin: GND_MBG	1/1	Open	0 to 1.875
1	1	1P25VREF	Pin: REF_BYP	1/1	Open	0 to 1.875
2	2	VREF_VADC	Internal: VREF_VADC	1/1	Open	0 to 1.875
3	3	DIE_TEMP	Internal: DIE_TEMP	1/1	Open	0 to 1.875
4	4	AMUX_THM1	Pin: BATT_THERM	1/1	Open	0 to 1.875
5	5	AMUX_THM2	Pin: BATT_ID	1/1	Open	0 to 1.875
6	6	AMUX_THM3	Pin: SMB_TEMP	1/1	Open	0 to 1.875
7	7	AMUX_THM4	Pin: USB_THERM	1/1	Open	0 to 1.875
8	8	AMUX_THM5	Pin: OPTION	1/1	Open	0 to 1.875
9	9	AMUX_THM6	Pin: GPIO_10	1/1	Open	0 to 1.875
A	10	AMUX1_GPIO	Pin: GPIO_01	1/1	Open	0 to 1.875
B	11	AMUX2_GPIO	Pin: GPIO_05	1/1	Open	0 to 1.875
C	12	AMUX3_GPIO	Pin: GPIO_06	1/1	Open	0 to 1.875
D	13	AMUX4_GPIO	Pin: GPIO_12	1/1	Open	0 to 1.875
8E	142	VPH_PWR	Pin: VPH_PWR_1	1/3	Open	0 to 5
8F	143	VBAT_SNS_QBG	Pin: VBATT_SNS_P (with QBG GND)	1/3 for 1S 1/6 for 2S	Open	1S: 0 to 5 2S: 0 to 9.6
10	16	CHG_TEMP	Pin: CHG_TEMP	1/1	Open	0 to 1.875
11	17	USB_SNS_V/16	Pin: USB_IN	1/16	Open	0 to 25
12	18	VIN_DIV16_MUX	Pin: WLS_IN	1/16	Open	0 to 25
13	19	USBC_MUX	Pin: CC1_ID, CC2, SBU1, SBU2	1/1	Open	0 to 1.875

Table 3-18 Analog multiplexer and scaling functions (cont.)

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
94	148	VBAT_SNS_CHGR	Pin: VBATT_SNS_P (with CHGR GND)	1/3 for 1S 1/6 for 2S	Open	1S: 0 to 5 2S: 0 to 9.6
15	21	VREF_BAT_THERM	Internal: ADC 1.875V pull up referenced to BATT_THERM GND	1/1	Open	0 to 1.875
96	150	VBAT_2S_MID_QBG	Pin: VBAT_2S_MID	1/3	Open	0 to 5
17	23	IIN_FB	Pin: IIN_FB	1/1	Open	0 to 1.875
24	36	AMUX_THM1	Pin: BATT_THERM	1/1	30K	0 to 1.875
25	37	AMUX_THM2	Pin: BATT_ID	1/1	30K	0 to 1.875
26	38	AMUX_THM3	Pin: SMB_TEMP	1/1	30K	0 to 1.875
27	39	AMUX_THM4	Pin: USB_THERM	1/1	30K	0 to 1.875
28	40	AMUX_THM5	Pin: OPTION	1/1	30K	0 to 1.875
29	41	AMUX_THM6	Pin: GPIO_10	1/1	30K	0 to 1.875
2A	42	AMUX1_GPIO	Pin: GPIO_01	1/1	30K	0 to 1.875
2B	43	AMUX2_GPIO	Pin: GPIO_05	1/1	30K	0 to 1.875
2C	44	AMUX3_GPIO	Pin: GPIO_06	1/1	30K	0 to 1.875
2D	45	AMUX4_GPIO	Pin: GPIO_12	1/1	30K	0 to 1.875
33	51	USBC_MUX	Pin: CC1_ID, CC2, SBU1, SBU2	1/1	30K	0 to 1.875
44	68	AMUX_THM1	Pin: BATT_THERM	1/1	100K	0 to 1.875
45	69	AMUX_THM2	Pin: BATT_ID	1/1	100K	0 to 1.875
46	70	AMUX_THM3	Pin: SMB_TEMP	1/1	100K	0 to 1.875
47	71	AMUX_THM4	Pin: USB_THERM	1/1	100K	0 to 1.875
48	72	AMUX_THM5	Pin: OPTION	1/1	100K	0 to 1.875
49	73	AMUX_THM6	Pin: GPIO_10	1/1	100K	0 to 1.875
4A	74	AMUX1_GPIO	Pin: GPIO_01	1/1	100K	0 to 1.875
4B	75	AMUX2_GPIO	Pin: GPIO_05	1/1	100K	0 to 1.875
4C	76	AMUX3_GPIO	Pin: GPIO_06	1/1	100K	0 to 1.875
4D	77	AMUX4_GPIO	Pin: GPIO_12	1/1	100K	0 to 1.875
53	83	USBC_MUX	Pin: CC1_ID, CC2, SBU1, SBU2	1/1	100K	0 to 1.875
64	100	AMUX_THM1	Pin: BATT_THERM	1/1	400K	0 to 1.875
65	101	AMUX_THM2	Pin: BATT_ID	1/1	400K	0 to 1.875
66	102	AMUX_THM3	Pin: SMB_TEMP	1/1	400K	0 to 1.875
67	103	AMUX_THM4	Pin: USB_THERM	1/1	400K	0 to 1.875
68	104	AMUX_THM5	Pin: OPTION	1/1	400K	0 to 1.875
69	105	AMUX_THM6	Pin: GPIO_10	1/1	400K	0 to 1.875
6A	106	AMUX1_GPIO	Pin: GPIO_01	1/1	400K	0 to 1.875
6B	107	AMUX2_GPIO	Pin: GPIO_05	1/1	400K	0 to 1.875

Table 3-18 Analog multiplexer and scaling functions (cont.)

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
6C	108	AMUX3_GPIO	Pin: GPIO_06	1/1	400K	0 to 1.875
6D	109	AMUX4_GPIO	Pin: GPIO_12	1/1	400K	0 to 1.875
73	115	USBC_MUX	Pin: CC1_ID, CC2, SBU1, SBU2	1/1	400K	0 to 1.875
8A	138	AMUX1_GPIO	Pin: GPIO_01	1/3	Open	0 to 5
8B	139	AMUX2_GPIO	Pin: GPIO_05	1/3	Open	0 to 5
8C	140	AMUX3_GPIO	Pin: GPIO_06	1/3	Open	0 to 5
8D	141	AMUX4_GPIO	Pin: GPIO_12	1/3	Open	0 to 5
8E	142	VPH_PWR	Pin: VPH_PWR_1	1/3	Open	0 to 5
8F	143	VBAT_SNS_QBG	Pin: VBATT_SNS_P (with QBG GND)	1/3 for 1S 1/6 for 2S	Open	1S: 0 to 5 2S: 0 to 9.6
94	148	VBAT_SNS_CHGR	Pin: VBATT_SNS_P (with CHGR GND)	1/3 for 1S 1/6 for 2S	Open	1S: 0 to 5 2S: 0 to 9.6
96	150	VBAT_2S_MID_QBG	Pin: VBATT_2S_MID (with QBG GND)	1/3	Open	0 to 5
9D	157	VBAT_2S_MID_CHGR	Pin: VBAT_2S_MID (with QBG GND)	1/3	Open	0 to 5

Table 3-19 ADC electrical specifications

Specification	Test condition	Lower limit	Typical value	Upper limit	Units
1/1 channel end-to-end gain error for absolute calibration	Absolute calibration data result, -40ºC to 85ºC, VBAT = 2.5 V to 5.25 V, input = 0.0 V to 1.8 V	-0.5	–	0.5	%
1/1 channel end-to-end offset error for absolute calibration	Absolute calibration data,-40ºC to 85ºC, VBAT = 2.5 V to 5.25 V, input = 0.0 V to 1.8 V	-2	+/-0.5	2	mV
1/1 channel end-to-end accuracy with internal pull-up and ratio-metric calibration	Ratio-metric calibration data result for ratio (reported ratio will be within specified tolerance of actual ratio, where ratio error % = measured ratio% - actual ratio %), -40 to 85ºC, VBAT = 2.5 V to 5.25 V	-0.6	0.3	0.6	%
1/3 channel end-to-end accuracy	Calibrated data result, -40ºC to 85ºC, VBAT = 2.5 V to 5.25 V, input = 0.5 V to 5.25 V	-0.45	–	0.45	%
1/3 channel end-to-end accuracy on VBAT_SNS to PACK_SNS Inputs	Calibrated data result, 25ºC, VBAT = 2.5 V to 5.25 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to the SYS_GND	-0.2	–	0.2	%
1/3 channel end-to-end accuracy on VBAT_SNS to PACK_SNS Inputs	Calibrated data result, -40ºC to 85ºC, VBAT = 2.5 V to 5.25 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to the SYS_GND	-0.3	–	0.3	%
1/6 channel end-to-end accuracy on VBAT_SNS to PACK_SNS Inputs	Calibrated data result, -40ºC to 85ºC, VBAT = 5 V to 10.5 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to the SYS_GND	-0.3	–	0.3	%

Table 3-19 ADC electrical specifications (cont.)

Specification	Test condition	Lower limit	Typical value	Upper limit	Units
ADC resolution (LSB) for absolute measurement	1/1 channel	–	64.879	–	µV
	Scaled to 1/3 channel	–	194.637	–	µV
	Scaled to 1/6 channel	–	389.274	–	µV
ADC resolution (LSB) for ratio measurement	1/1 channel, ratiometric calibration - result is a 14 bit ratio from 0% (0x0000) to 100% (0x4000)	–	0.006104	–	%
ADC LDO voltage		1.828	1.875	1.922	V
ADC sample clock		–	4.8	–	MHz
ADC conversion time	1K decimation ratio, 4.8 MHz sample clock, SINC2 conversion, clock dithering not enabled	–	654	700	µs
Current consumption – ADC only	VADC active – does not include other PMIC infrastructure	–	450	500	µA
Current consumption – ADC and required infrastructure hardware	VADC, MBG and ADC clock source active	–	1000	1500	µA
100K pull-up	Trimmed value	99.5	100	100.5	kΩ
400K pull-up	Trimmed value	398	400	402	kΩ
30K pull-up	Trimmed value	29.7	30	30.3	kΩ
Pull-up temperature coefficient		-150	–	150	ppm/ºC
Pull-up aging	Value change over time and temperature cycling	-0.5	–	0.5	%
1/1 channel AMUX input resistance		10	–	–	MΩ
1/3 and 1/6 channel AMUX input resistance		1	–	–	MΩ
Leakage current – All pins using internal pull-up resistors	With Vbatt and aVdd present, apply 1.8 V to pin and monitor current, -40ºC to 85ºC, VBAT = 2.5 V to 5.25 V	–	–	10	nA
Balancing FET resistance (only in ADC_BG AHM)	Rdson for both cell balancing FETs, -40ºC to 85ºC, VBAT = 6.8 V to 10 V, with mid-node at 3.4 V to 5 V	10	20	30	Ω

Table 3-20 Internal current sensing specifications

Parameter	Conditions	Min	Typical	Max	Unit
Battery current sensing range	VBAT = 2.5 V to 5.25 V	-12	–	12	A
	T = -40ºC to 85ºC				
Battery current sensing offset	VBAT = 2.5 V to 5.25 V	-15	–	+15	mA
	IBAT = 0 A to 8.5 A				
	T = -40ºC to 85ºC				
Battery current gain error	VBAT = 2.5 V to 5.25 V	-5	–	5%	%
	IBAT = -12 A to 12 A				
	T = -40ºC to 85ºC				
ADC LSB		–	366.22	–	µA

Table 3-20 Internal current sensing specifications (cont.)

Parameter	Conditions	Min	Typical	Max	Unit
Current sensing noise	VBAT = 2.5 V to 5.25 V	–	–	20	mA
	IBAT = -12 A to 12 A				
	T = -40ºC to 85ºC				

Table 3-21 External current sensing specifications

Parameter	Conditions	Min	Typical	Max	Unit
Battery current sensing range	VBAT = 2.5 V to 5.25 V	-12	–	12	A
	T = -40ºC to 85ºC				
Battery current sensing offset (5 mΩ sense resistor)	VBAT = 2.5 V to 5.25 V	-6	–	6	mA
	IBAT = -12 A to 12 A				
	T = -40ºC to 85ºC				
	Offset auto calibration enabled				
Battery current relative error (5 mΩ sense resistor)	VBAT = 2.5 V to 5.25 V	-1	–	1	%
	IBAT = -12 A to 12 A				
	T = -40ºC to 85ºC				
ADC LSB		–	366.22	–	µA
Sense resistor value [a]	Sensing range programmable	1	2	5	mΩ
Sense resistor accuracy	This is recommended accuracy. Sense resistor error in not included in the prior error specifications and will directly add to the stated numbers.	–	0.50	1	%
Current sensing noise	VBAT = 2.5 V to 5.25 V, IBAT = -12 A to 12 A, T = -40ºC to 85ºC	–	–	–	
	1 mΩ sense resistor	–	20	–	mA
	2 mΩ sense resistor	–	10	–	mA
	5 mΩ sense resistor	–	5	–	mA

[a] See Table 3-22

Table 3-22 Option pin (124) configuration

Pull down value	Configuration
OPEN	Internal sense
~432 kΩ	Internal sense with charger disabled
~221 kΩ	2 × 5 mΩ external sensing
~127 kΩ	2 × 2 mΩ external sensing
~78.7 kΩ	2 × 1 mΩ external sensing
~45.2 kΩ	1 × 5 mΩ external sensing
~23.2 kΩ	1 × 2 mΩ external sensing
GND	1 × 1 mΩ external sensing

Table 3-23 BAT_THERM range and accuracy

Parameter	Minimum value	Ideal value	Maximum value
Thermistor value	10 K B = 4250	100 K, B = 4250	100 K, B = 4250
Internal pull-up value	30 K	100 K	100 K
Maximum error	1.0ºC	0.9ºC	0.9ºC

Table 3-24 BAT_ID range and accuracy

Parameter	Minimum value	Ideal value	Maximum value
BAT_ID value	1 K	100 K	450 K
Internal pull-up value	100 K	100 K	100 K
Maximum error	9%	0.7%	0.5%

Table 3-25 Temperature measurement specifications

Specification	Test condition	Lower limit	Typical value	Upper limit	Units
Temperature reading error using 100 K, 1%, 4250 K beta thermistor, and 100 K pull-up	Ratiometric calibration data (0ºC to 50ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-1.0	–	1.0	°C
	Ratiometric calibration data (-20ºC to 70ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-1.5	–	1.5	°C
Temperature reading error using 10 K to 100 K, 1%, 4250 K beta thermistor, and 30 K pull-up (not available with ADC_TINY)	Ratiometric calibration data (0ºC to 50ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-2.0	–	2.0	°C
	Ratiometric calibration data (-20ºC to 70ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-3.0	–	3.0	°C
Temperature reading error using 10 K to 100 K, 1%, 4250 K beta thermistor, and 100 K pull-up	Ratiometric calibration data (0ºC to 50ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-3.0	–	3.0	°C
	Ratiometric calibration data (-20ºC to 70ºC), VBAT = 2.5 V to 5.25 V, IBAT = 0 A	-5.0	–	5.0	°C

3.9 Battery current limiting (BCL)

BCL is a feature that supports system-wide mitigation based on high battery current or low battery voltage conditions. BCL on the PM8550B/PM8550BH/PM8550BHS/PM8550BHP device uses the ADC module, dedicated hardware comparators, and signals from other hardware modules to trigger mitigation levels that are then relayed to the system to ensure mitigation is done when needed. This aids in preventing brownouts, UVLO, or OCP conditions that will cause abrupt hardware shutdowns.

Table 3-26 BCL specifications

Parameter	Min	Typ	Max	Unit
Comparator accuracy	-50	–	50	mV
Comparator hysteresis low1/2 comparators	–	1% of $V_{threshold}$	–	V

Table 3-26 BCL specifications (cont.)

Parameter	Min	Typ	Max	Unit
I (Vbat) (per AHM)				
Active	–	4	–	µA
Off	–	0.01	–	µA
I (aVdd) (per AHM)				
Active	–	10	–	µA
Off	–	0.01	–	µA
Current monitoring range	0.094	–	12	A
Current monitoring accuracy (ADC accuracy) VBAT = 3.0 V to 4.75 V IBAT = 5 A to 8.5 A T= 0 to 70°C	-5% (internal) -1% (external)	–	5%(internal) -1% (external)	% %

3.10 Haptics

Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics are used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as confirmation of touchscreen contact, or dynamic feedback to enhance gaming experiences. Electrical specifications are listed in Table 3-27.

Unless otherwise specified, test conditions assume that VHPWR = 3.8 V, T_A = -30°C to +85°C.

Table 3-27 Haptics driver electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_HPWR_DC	H-bridge driver input supply average DC voltage applied at HPWR		5.0	–	10.6	V
V_HPWR_TRAN	H-bridge driver input supply voltage applied at HVDD	Applied for < ms	2	–	13	V
VHOUT_AVG	Differential output drive voltage averaged over one PWM cycle.	VHPWR =10.6 V, No load	0	–	10.2	V
ILIM	Cycle-by-cycle output current limit	Programmable: 1, 1.5, 2 A	–	1.5	–	A
IHVDD	Module operating current	Switching, I_{HOUT} = 0, HPWR = 10.5 V	–	4	5	mA
		Switching, I_{HOUT} = 0, HPWR = 5 V	–	2.5	3	mA
IQ_SHD	Module shutdown current	TA ≤ 60°C, HPWR = VPH ≤ 4.8 V (boost disabled	–	1	–	µA
		TA ≤ 60°C, HPWR > VPH (boost enabled- retention mode)	–	2	–	µA
RDSON	ON resistance of high side switch	VHPWR > 5 V	–	225	–	mΩ
	ON resistance of low side switch		–	105	–	mΩ
FPWM	Internal PWM frequency	Programmable	150	–	1200	kHz
ΔFPWM	Internal PWM frequency inaccuracy		-6	–	6	%
TLRA	Open loop LRA drive programmable frequency	Programmable	75	–	1000	Hz

Table 3-28 PM8550B 5 V Haptics boost electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_dc	DC input voltage range at VPH_PWR	Full parametric compliance	2.5	–	5.0	V
		Reduced specifications (See Iout)	2.15	–	–	V
VIN_trans	Transient input voltage range at VPH_PWR	Bounded by UVLO and max battery voltage. Transient < 1 ms	2	–	5.25	V
Vout			–	5	–	V
Iout	Output current (continuous), 2.2 µH inductor, 3 A current limit	Vout = 5 V, VPH > 4.2 V	–	–	1650	mA
		Vout = 5 V, 3.8 V < VPH < 4.2 V	–	–	1450	mA
		Vout = 5 V, 3.4 V < VPH < 3.8 V	–	–	1250	mA
		Vout = 5 V, 3.0 V < VPH < 3.4 V	–	–	1100	mA
		Vout = 5 V, 2.5 V < VPH < 3.0 V	–	–	850	mA
	Extend operational output current range	Vout = 5 V, 2.15 V < Vin < 2.5 V, T = 25°C	–	750	–	mA
Ipk_limit	Peak inductor current limit		–	3	–	A
Fsw	Switching frequency		–	0.8	–	MHz
L	Inductor value	Derated at DC bias current at Isat	1.54	–	–	µH
Cout_min	Output capacitance (derated)	Derated for temp, voltage, aging. Typical BOM = 6 × 4.7 µF 0402	7.5	–	–	µF
Vout_acc	VOUTDC accuracy	Across temp and voltage	-2	–	2	%
R_dson, p	High side PFET Rds, on		–	110	–	mΩ
R_dson, n	Low side NFET Rds, on		–	60	–	mΩ
Iout	Output current (continuous) 2.2 µH inductor, 3 A current limit	Vout = 5 V, VPH > 4.2 V			1650	mA
IQ_SHD	Module shutdown current	VPH = 2.5 V to 4.8 V	–	0.4	–	µA
IQ_stby	No load ground current	VPH = 3.8 V, no load, low power retention mode	–	–	7.5	µA
		VPH = 3.8 V, no load, fast recovery retention	–	–	30	µA
IQ_BST	Module operating current	VPH = 3.8 V, switching, no load, active pulse skip enabled, VOUT = 5 V	–	–	1.8	mA
T_startup	Start up time	Soft start. VPH = 3.8 V to VREG_BST = 5 V			190	µs
Vout ripple	Steady state ripple	Not in PSM. Load is within Iout_max limits	–	–	150	mV_pk pk
	Steady state ripple in PSM operation	PSM operation. VIN= 5 V, Vout = 5 V	–	–	400	mV_pk pk

Table 3-29 PM8550BH/BHS/BHP 10 V Haptics boost electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_dc	DC input voltage range at VPH_PWR	Full parametric compliance	2.5	–	5.0	V
		Reduced specifications (See Iout)	2.15	–	–	V
VIN_trans	Transient input voltage range at VPH_PWR	Bounded by UVLO and max battery voltage. Transient < 1 ms	2	–	5.25	V

Table 3-29 PM8550BH/BHS/BHP 10 V Haptics boost electrical specifications (cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Vout_prgm	Programmable output voltage range	Programmable with 50 mV steps	5	–	10	V
Iout (VOUT = 10 V)	Output current (continuous), 1 µH inductor, 4.4 A current limit	Vout = 10 V, VPH > 4.2 V	–	–	1050	mA
		Vout = 10 V, 3.8 V < VPH < 4.2 V	–	–	950	mA
		Vout = 10 V, 3.4 V < VPH < 3.8 V	–	–	800	mA
		Vout = 10 V, 3.0 V < VPH < 3.4 V	–	–	650	mA
		Vout = 10 V, 2.5 V < VPH < 3.0 V	–	–	450	mA
	Extend operational output current range	Vout = 10 V, 2.15 V < VPH < 2.5 V, T = 25°C	–	300	–	mA
Iout (VOUT = 5 V)	Output current (continuous), 1 µH inductor, 4.4 A current limit	Vout = 5 V, VPH > 4.2 V	–	–	2400	mA
		Vout = 5 V, 3.8 V < VPH < 4.2 V	–	–	2100	mA
		Vout = 5 V, 3.4 V < VPH < 3.8 V	–	–	1700	mA
		Vout = 5 V, 3.0 V < VPH < 3.4 V	–	–	1550	mA
		Vout = 5 V, 2.5 V < VPH < 3.0 V	–	–	1150	mA
	Extend operational output current range	Vout = 5 V, 2.15 V < VPH < 2.5 V, T = 25°C	–	850	–	mA
Iout (VOUT = 5 V, OTG mode settings)	Output current (continuous), 1 µH inductor, 4.4 A current limit	Vout = 5 V, VPH > 4.2 V	–	–	2200	mA
		Vout = 5 V, 3.8 V < VPH < 4.2 V	–	–	1800	mA
		Vout = 5 V, 3.4 V < VPH < 3.8 V	–	–	1600	mA
		Vout = 5 V, 3.0 V < VPH < 3.4 V	–	–	1500	mA
		Vout = 5 V, 2.5 V < VPH < 3.0 V	–	–	1150	mA
	Extend operational output current range	Vout = 5 V, 2.15 V < VPH < 2.5 V, T = 25°C	–	1000	–	mA
Ipk_limit	Peak inductor current limit		–	4.4	–	A
	Ipk_limit_acc		-10	–	10	%
Fsw	Switching frequency		–	3.2	–	MHz
L	Inductor value	Derated at DC bias current at Isat	0.7	–	–	µH
Cout_min	Output capacitance (derated)	Derated for temp, voltage, aging. Vout = 10 V. Typical BOM = 6 × 4.7 µF 0402	3	–	–	µF
Vout_acc	VOUT DC accuracy	Across temp and voltage	-2	–	2	%
R_dson, p	High side PFET Rds, on		–	100	–	mΩ
R_dson, n	Low side NFET Rds, on		–	50	–	mΩ
IQ_SHD	Module shutdown current	VPH = 3.8 V, T = 25°C	–	0.4	–	µA
IQ_stby	No load ground current	VPH = 3.8 V, no load, low power retention mode, RM_VSET = 7.5 V	–	–	10	µA
		VPH = 3.8 V, no load, fast recovery retention, RM_VSET = 7.5 V	–	–	40	µA
IQ_BST	Module operating current	VPH = 3.8 V, switching, no load, active pulse skip enabled, VOUT = 10 V	–	3	4.5	mA
T_startup	Start up time	Fast recovery retention mode voltage = 7.5 V transition to 10 V, Active Mode vreg_ready	–	220	–	µs

Table 3-29 PM8550BH/BHS/BHP 10 V Haptics boost electrical specifications (cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		LPRM retention mode voltage = 7.5 V transition to 10 V, Active Mode vreg_ready	–	250	–	µs
		Soft start. VPH = 3.8 V to VREG_BST = 10 V	–	250	–	µs
Vout ripple	Steady state ripple	Load is within Iout_max limits. Vout = 10 V	–	–	120	mV_pk pk
	Steady state ripple in PSM operation	VIN= 5 V, Vout = 10 V	–	–	200	mV_pk pk

4 Mechanical information

4.1 Device physical dimensions

The PM8550B/PM8550BH/PM8550BHS/PM8550BHP is available in the 168-pin fan-out wafer-level nanoscale package that includes ground pins for improved grounding, mechanical strength, and thermal continuity. The FOWNSP168 has a 5.79 mm × 4.85 mm body with a maximum height of 0.57 mm. Pin 1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below. A simplified version of the FOWNSP168 outline drawing is shown in Figure 4-1.

NOTE Click the following link to download *Package Outline Drawing, FOWNSP168, 5.79 × 4.85 × 0.57 mm, M328* (NT90-16787-1) from the Qualcomm® CreatePoint website

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-16787-1

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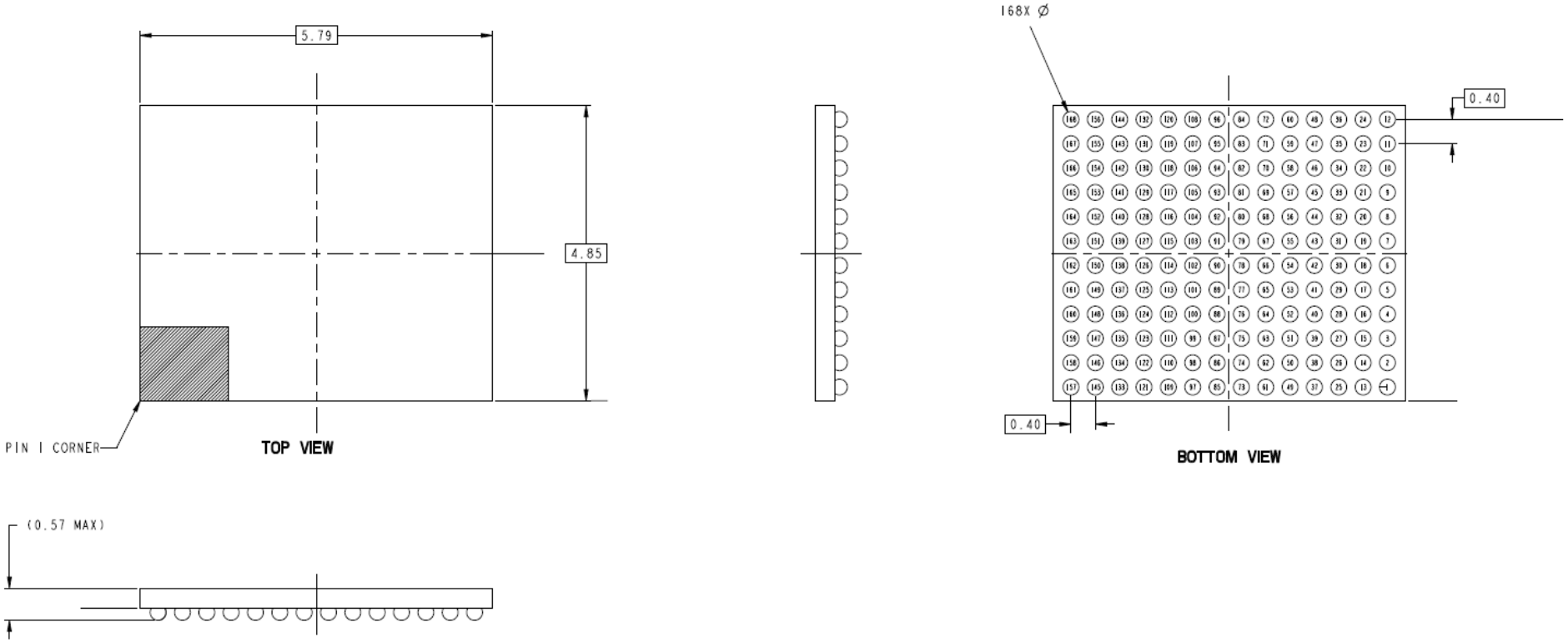

Figure 4-1 FOWNSP168 outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

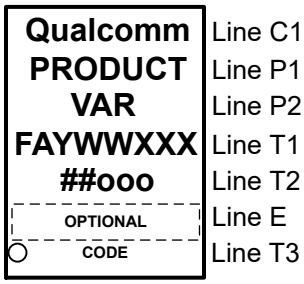

Figure 4-2 PM8550B/PM8550BH/PM8550BHS/PM8550BHP device marking (top view, not to scale)

Table 4-1 PM8550B/PM8550BH/PM8550BHS/PM8550BHP device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ PM8550B ■ PM8550BH ■ PM8550BHS ■ PM8550BHP
P2	VAR	Variant value (PRR-BB)
T1	FAYWWXXX	F = foundry company code ■ F = F for TSMC ■ F = P for SMIC A = assembly site (ball drop) code ■ A = E for ASE, Taiwan ■ A = 4 for NEPES, Korea Y = single/last digit of year WW = two-digit work week of current year XXX = segmented serial number portion of lot ID
T2	## ooo	## = Two digit wafer number Optional engineering information
E	OPTIONAL	Optional trace information
T3	**o** CODE	Pin1 or pin A1 indicator Indicates triangle code

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-2.

Table 4-2 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example 1	PM-8550B	-0	-FOWNSP	168			-MT	-00	-0	
Example 2	PM-8550BH	-0	-FOWNSP	168			-MT	-00	-0	
Example 3	PM-8550BHS	-0	-FOWNSP	168			-MT	-00	-0	
Example 4	PM-8550BHP	-0	-FOWNSP	168			-MT	-00	-0	

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: PM-8550B-0-FOWNSP168-MT-00-0
- Example 2: PM-8550BH-0-FOWNSP168-MT-00-0
- Example 3: PM-8550BHS-0-FOWNSP168-MT-00-0
- Example 4: PM-8550BHP-0-FOWNSP168-MT-00-0

Table 4-2 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification details

Device	Sample type	Product configuration code (P)	Product revision code (RR)	Feature code (BB) [a]	Hardware version	Source configuration code (S) [b]	Sample date
PM8550B	ES1	0	00	–	v1.0	0	02/24/2022
PM8550BH	ES1	0	00	–	v1.0	0	02/24/2022
PM8550BHS	ES1	0	00	–	v1.0	0	02/24/2022
PM8550BHP	ES1	0	00	–	v1.0	0	02/24/2022
PM8550B	ES2	0	01	–	v2.0	0	07/08/2022
PM8550BH	ES2	0	01	–	v2.0	0	07/08/2022
PM8550BHS	ES2	0	01	–	v2.0	0	07/08/2022
PM8550BHP	ES2	0	01	–	v2.0	0	07/08/2022

Table 4-3 Device identification details (cont.)

Device	Sample type	Product configuration code (P)	Product revision code (RR)	Feature code (BB) [a]	Hardware version	Source configuration code (S) [b]	Sample date
PM8550B	CS1 [c]	0	01	–	v2.0	0	08/26/2022
PM8550BH	CS1 [d]	0	01	–	v2.0	0	08/26/2022
PM8550BHS	CS1 [e]	0	01	–	v2.0	0	08/26/2022
PM8550BHP	CS1 [f]	0	01	–	v2.0	0	08/26/2022
PM8550B	CS2	0	02	–	v2.1	0	4/21/2023
PM8550BH	CS2	0	02	–	v2.1	0	4/21/2023
PM8550BHS	CS2	0	02	–	v2.1	0	4/21/2023
PM8550BHP	CS2	0	02	–	v2.1	0	4/21/2023

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants.
[b] S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped.
[c] PM8550B ES2 and CS1 parts have the same PRR code. All devices with date code YWW ≥ 234 or from the following lots are of CS1 quality.
[d] PM8550BH ES2 and CS1 parts have the same PRR code. All devices with date code YWW ≥ 234 or from the following lots are of CS1 quality.
[e] PM8550BHS ES2 and CS1 parts have the same PRR code. All devices with date code YWW ≥ 234 or from the following lots are of CS1 quality.
[f] PM8550BHP ES2 and CS1 parts have the same PRR code. All devices with date code YWW ≥ 234 or from the following lots are of CS1 quality.

PM8550B	PM8550BH	PM8550BHS	PM8550BHP
000FE217XT6.0E003	000FE217XT6.0E054	000FE217XT6.0E052	000FE217XTX.0E051
000FE217XT6.0E056	000FE217XT6.0E002	000FE217XT6.0E001	000FE217XTX.0E001
000PE218YZS.0E056	000FE217XT6.0E055	000F421879G.4N016	000FE217XTX.0E052
000PE218YZS.0E003	000PE218YZS.0E051	000F421879G.4N015	000PE218YZS.0E057
000PE218YZS.0E007	000PE218YZS.0E052	000F421879G.4N014	000PE218YZS.0E053
000PE218YZS.0E062	000PE218YZS.0E001	000P421879S.4N019	000PE218YZS.0E054
000F421879G.4N003	000F421879G.4N011	000P421879S.4N020	000PE218YZS.0E002
000F421879G.4N004	000F421879G.4N009	000P421879S.4N021	000PE218YZS.0E058
000F421879G.4N002	000F421879G.4N010	000P421879S.4N017	000PE218YZS.0E005
000P421879Q.4N008	000F421879G.4N008	000PE218YZS.0E060	000F421879G.4N024
000P421879Q.4N009	000P421879S.4N013	000PE218YZS.0E006	000F421879G.4N022
000P421879Q.4N007	000P421879S.4N011	000PE218YZS.0E064	000P421879Q.4N014
000PE218Z6G.0E052	000P421879S.4N012	000PE218YZS.0E004	000P421879Q.4N015
000PE218Z6G.0E001	000P421879S.4N010	000FE217XRG.0E054	000P421879Q.4N012
	000PE218Z4F.0E001	000FE217XRG.0E056	000PE218Z6G.0E054
	000PE218Z4F.0E052	000FE217XRG.0E002	000PE218Z6G.0E002
	000FE217XRG.0E001	000FE217XRG.0E003	000PE218Z6G.0E057
	000FE217XRG.0E052		000PE218Z6G.0E003

Table 4-4 Source configuration code

S value	F value = P	F value = F	A value = E	A value = 4
0	SMIC	TSMC	ASE, Taiwan	NEPES, Korea

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-5.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH; *PM8550B/PM8550BH/PM8550BHS/PM8550BHP* rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hrs	≤ 30°C/60% RH
4	72 hrs	≤ 30°C/60% RH
5	48 hrs	≤ 30°C/60% RH
5a	24 hrs	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8550B/PM8550BH/PM8550BHS/PM8550BHP devices are classified as MSL1; the qualification temperature was 260°C +0°/-5°C***. This qualification temperature (260°C +0°/-5°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θJC and θJA, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following link to download the *PM8550B FOWNSP168 Package Thermal Model Icepak* (HS11-33267-5HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-33267-5HW

Click the following link to download the *PM8550B FOWNSP168 Package Thermal Model Flotherm* (HS11-33267-6HW) from the CreatePoint website.

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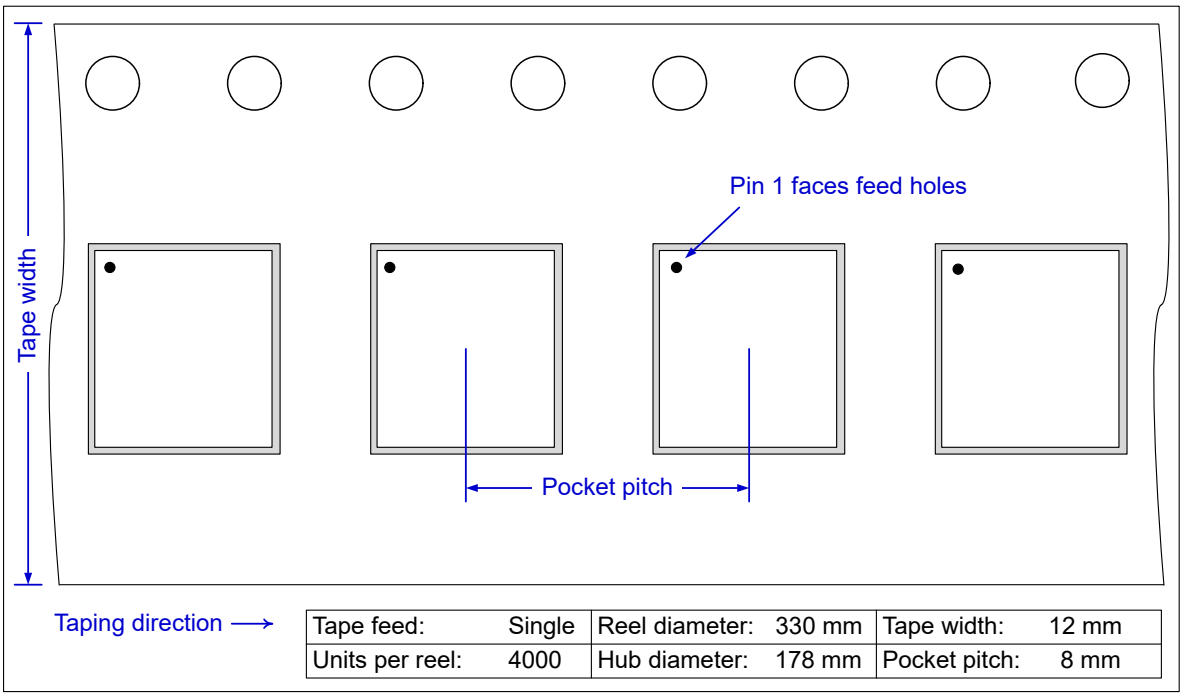
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM8550B/PM8550BH/PM8550BHS/PM8550BHP tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	12 mm
Units per reel:	4000	Hub diameter:	178 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

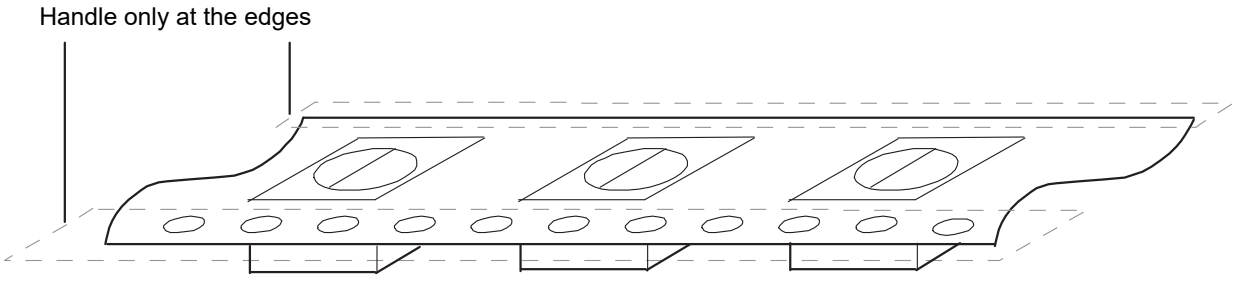


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8550B/PM8550BH/PM8550BHS/PM8550BHP devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the FOWNSP168 should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

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7 Part reliability

7.1 Reliability qualifications summary: SMIC and TSMC

Table 7-1 Silicon reliability results

Tests, standards, and conditions	SMIC Sample, number of lots	TSMC Sample, number of lots	Result
Early life failure rate (ELFR) in DPM (1 year life equivalent)HTOL: JESD22-A108-A in DPPM Note-1; Generic accumulated HTOL data from qualified 150 nm PMIC devices; >3 lots and >1000 samples per foundry (QBS to PMX65)	> 1000 > 3	> 1000 > 3	< 1000
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three fab lots per foundry)	231 (77 × 3 fab lots)	231 (77 × 3 fab lots)	< 50
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three fab lots)	231 (77 × 3 fab lots)	231 (77 × 3 fab lots)	> 20
ESD – human body model (HBM) rating JESD22-A114-F (Total samples from one wafer lot)	3 (1 fab lot)	3 (1 fab lot)	Pass 1750 V
ESD – charged device model (CDM) rating JESD22-C101-D (Total samples from one wafer lot)	3 (1 fab lot)	3 (1 fab lot)	Pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ± 100 mA; temperature: 85°C	3 (1 fab lot)	3 (1 fab lot)	Pass
Latch-up (Vsupply overvoltage):EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 85°C	3 (1 fab lot)	3 (1 fab lot)	Pass

Table 7-2 Package reliability results

Tests, standards, and conditions	ASE Sample size	NEPES Sample size	Result
Moisture resistance test (MRT) MSL1 ; J-STD-020-D 3× reflow cycles @ 255 +5/-0°C	693 (231 × 3 assembly lots per SAT)	693 (231 × 3 assembly lots per SAT)	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Minimum soak time at minimum/maximum temperature: 5 minutes Cycle rate: 2 cycles per hour (CPH) MSL1 preconditioning: JESD22-A113-F Reflow temperature: 255°C +5/-0°C (TC QBS to PM855A)	231 (77 × 3 assembly lots)	231 (77 × 3 assembly lots)	Pass
Unbiased highly accelerated stress test (UHAST): JESD22-A118 MSL1 preconditioning: JESD22-A113-F Reflow temperature: 255°C +5/-0°C	231 (77 × 3 assembly lots)	231 (77 × 3 assembly lots)	Pass
Biased highly accelerated stress test JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113 MSL1, reflow temperature: 260 +0/-5°C (BHAST QBS to PM8350)	231 (77 × 3 assembly lots)	231 (77 × 3 assembly lots)	Pass
High-temperature storage life: JESD22-A103-D Temperature 150°C, 1000 hours (HTS QBS to PM855A)	231 (77 × 3 assembly lots)	231 (77 × 3 assembly lots)	Pass
Physical dimensions: JESD22-B100-A	15 (1 assembly lot)	15 (1 assembly lot)	Pass
Solder ball shear JESD22-B117-B Total samples from three assembly lots at each SAT	45 (15 × 3 assembly lots)	45 (15 × 3 assembly lots)	Pass

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	PM8550B/PM8550BH/PM8550BHS/PM8550BHP
Package type	FOWNSP168
Package body size	5.79 mm × 4.85 mm × 0.57 mm
Solder ball composition	SAC405
Process	150 nm
Fab sites	■ TSMC ■ SMIC
Assembly sites	■ ASE, Taiwan ■ NEPES, Korea
Solder ball pitch	0.4 mm

8 Revision history

Revision	Date	Description
AA	October 2021	Initial release
AB	March 2022	■ Chapter 3 *Electrical specification*: Added this chapter ■ Section 4.2 *Part marking* : Added this section ■ Section 4.3 *Device identification*: Added this section ■ Section 4.4 *Device moisture-sensitivity level*: Added this section ■ Section 4.5 *Thermal characteristics*: Added this section ■ Chapter 5 *Carrier, storage, and handling information*: Added this chapter ■ Chapter 6 *PCB mounting guidelines*: Added this chapter
AC	April 2022	■ Section 4.4 *Device moisture-sensitivity level*: Updated the MSL rating ■ Option pin (124) configuration: Added this table
AD	July 2022	■ Table 2-7 *Pin descriptions — general-purpose input/output functions and other pins*: Updated the configurable function and functional description for GPIO_03 and GPIO_04 ■ Table 4-3 *Device identification details*: Updated the ES2 sample details and sample date information
AE	August 2022	■ Table 3-5 *GPIO output impedance*: Added this table ■ Table 3-6 *Input power source control and protection*: Updated the specification values ■ Table 3-7 *USB Type-C and BC1.2 specifications*: Updated the typical value of Z_{OPEN} ■ Table 3-9 *2S battery charger specifications*: Updated the specification values ■ Table 3-10 *Buck regulator specifications*: Updated the minimum value of F_{SW_BUCK} and typical values of QPH1 charging path efficiency ■ Table 3-11 *Div2 charge pump specifications*: Updated the specification values of Div2 operation ■ Table 3-12 *Reverse boost regulator specifications*: Updated the specification values ■ Table 3-13 *Full-Duty charge specifications*: Updated the specification values ■ Table 3-14 *Battery interface specifications*: Updated the specification values ■ Table 4-3 *Device identification details*: Added the CS sample details ■ Chapter 7 *Part reliability*: Added this chapter
AF	September 2022	Table 4-3 *Device identification details*: Added additional lots
AG	November 2022	Table 3-3 *DC power supply currents*: Added additional battery current specification
AH	April 2023	■ Table 3-1 *Absolute maximum ratings*: Updated the note ■ Table 3-3 *DC power supply currents*: Added additional specification for PM8550BHS + SMB1399 battery supply current, off mode ■ Section 4.2 *Part marking*: Updated the device marking drawing and definition ■ Table 4-3 *Device identification details*: Updated the device identification details for v2.1

For additional information or to submit technical questions, go to https://www.qualcomm.com/support

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.