Qualcomm Technologies, Inc.

SM8650/SM8650P

Data Sheet

80-40938-1 Rev. AJ

June 2, 2023

Device description

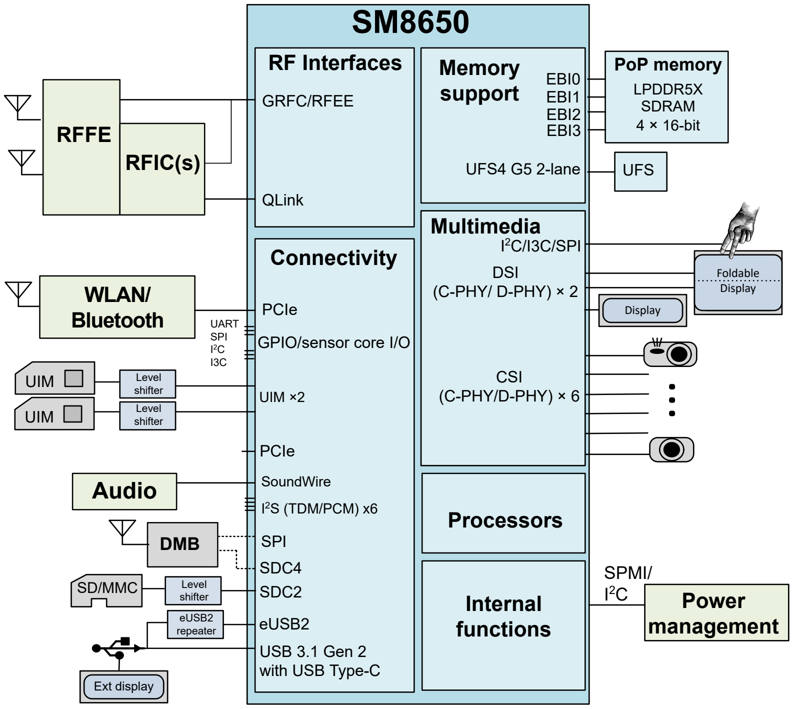
The SM8650/SM8650P device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with a 4 nm process, for superior performance and power efficiency. SM8650/SM8650P includes the following key components:

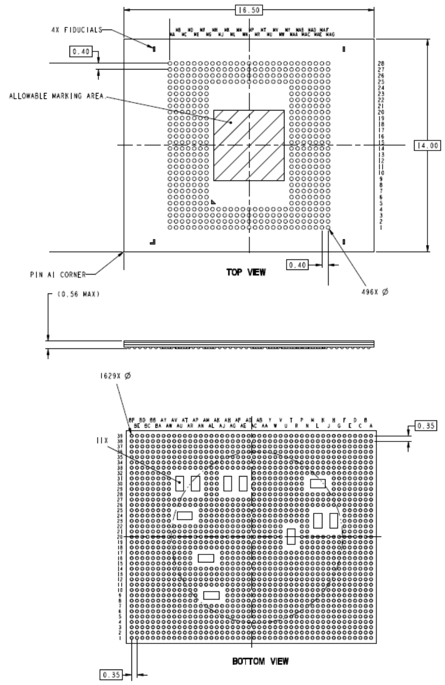
- Qualcomm® Kryo™ CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 750 GPU for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ Image Signal Processor for the ultimate photography and videography experiences
- Adreno VPU 8650 for high-quality, ultra HD video encode and decode
- Adreno DPU 1395 for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 bands (Rel 17 integrated modem)

Key features

- Low-Power AI (LPAI) subsystem with dedicated DSP and AI accelerator (eNPU) supporting always-on audio, sensors, contextual data streams, and always sensing camera (ASC)
- Qualcomm Aqstic™ Audio Technologies WCD9395 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Secure Processing Unit for advanced secure use cases
- Qualcomm® Hexagon™ Tensor Processor (HTP) with Hexagon Vector eXtensions (HVX) and Hexagon Matrix eXtensions (HMX)
- Qualcomm® FastConnect™ 7800 System with WCN785x, 802.11be, 2 × 2 MIMO, Bluetooth 5.3
- Quad-channel package-on-package (PoP) high-speed LPDDR5X SDRAM
- 16.5 × 14.0 × 0.56 mm MPSP1629 PoP

SM8650/SM8650P high-level block diagram and MPSP1629 outline drawing





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1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

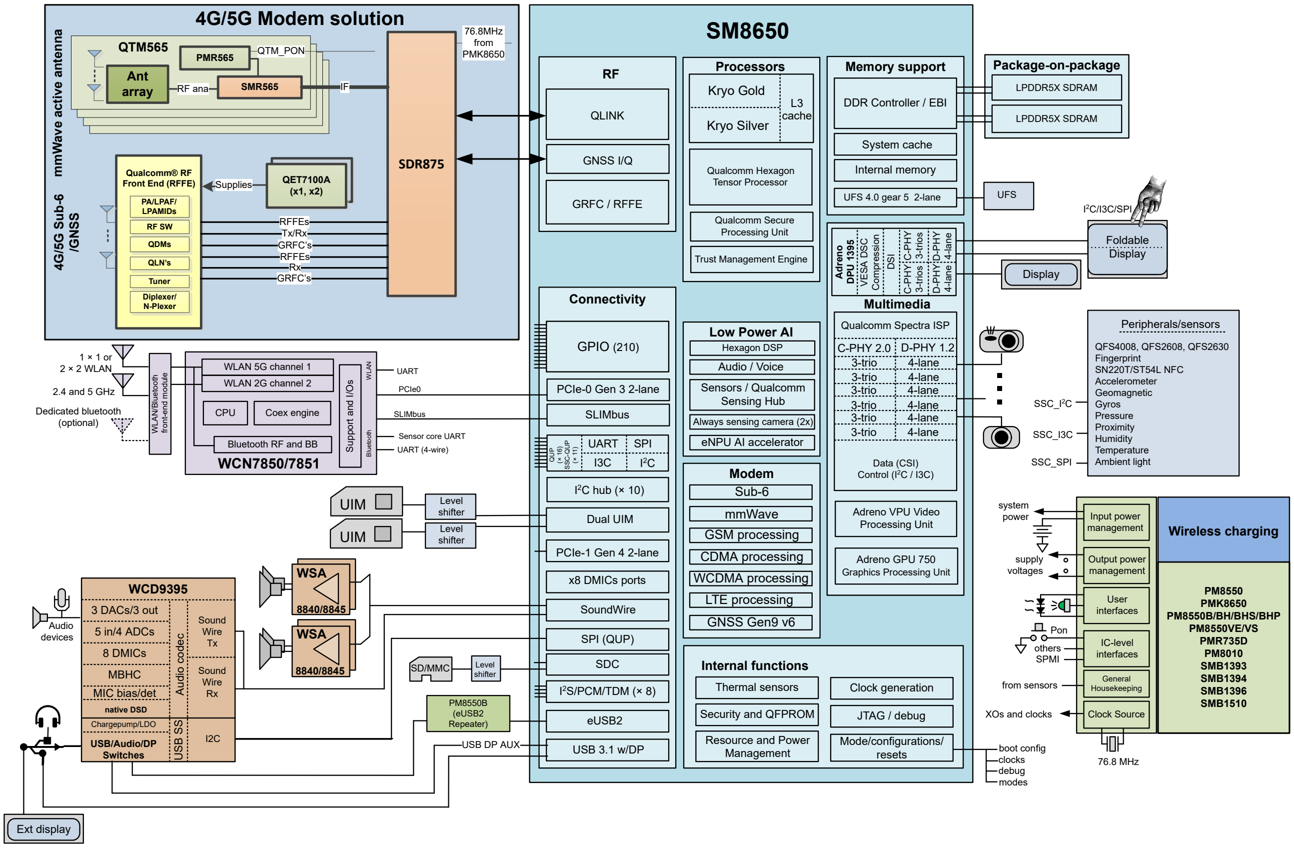

Figure 1-1 SM8650 + SDR875 (sub-6/mmW solution) functional block diagram and example application

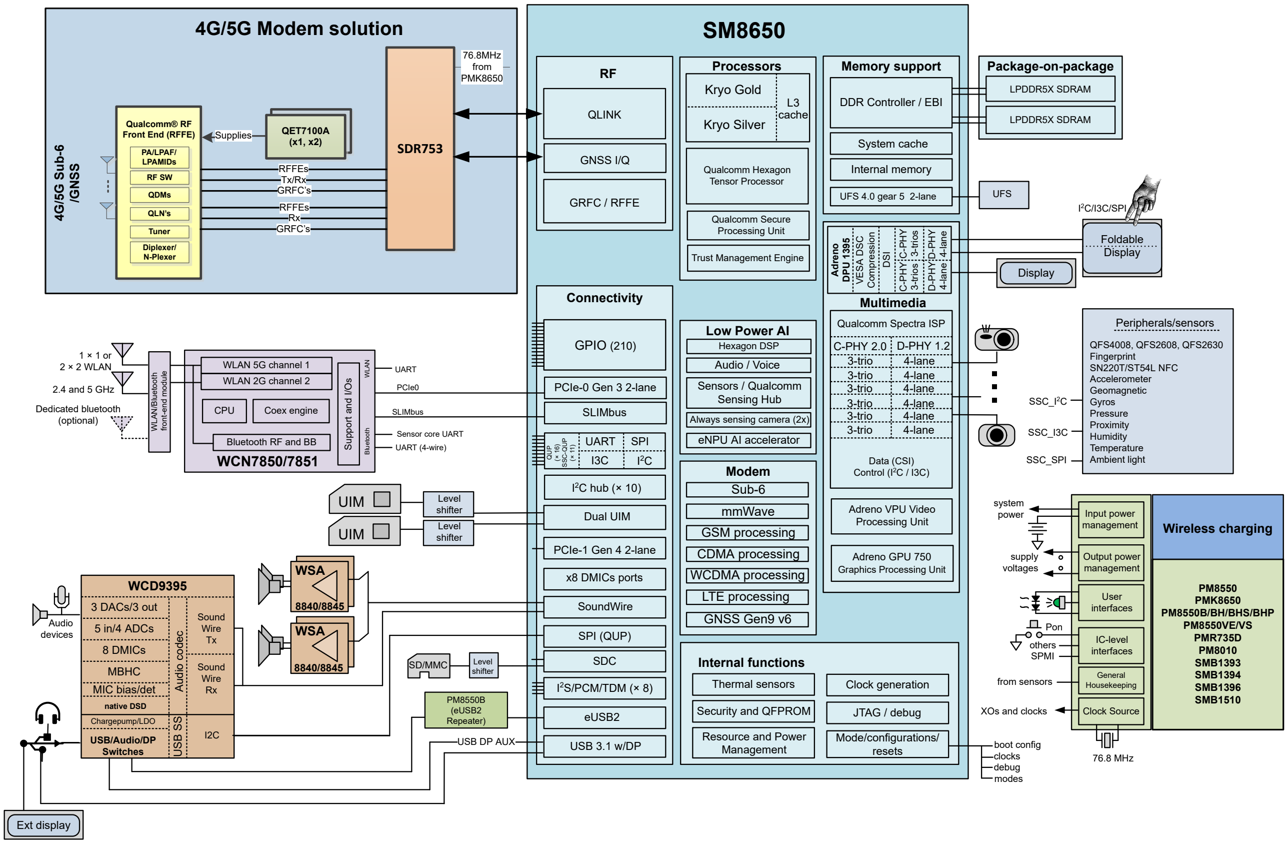

Figure 1-2 SM8650 + SDR753 (sub-6 solution) functional block diagram and example application

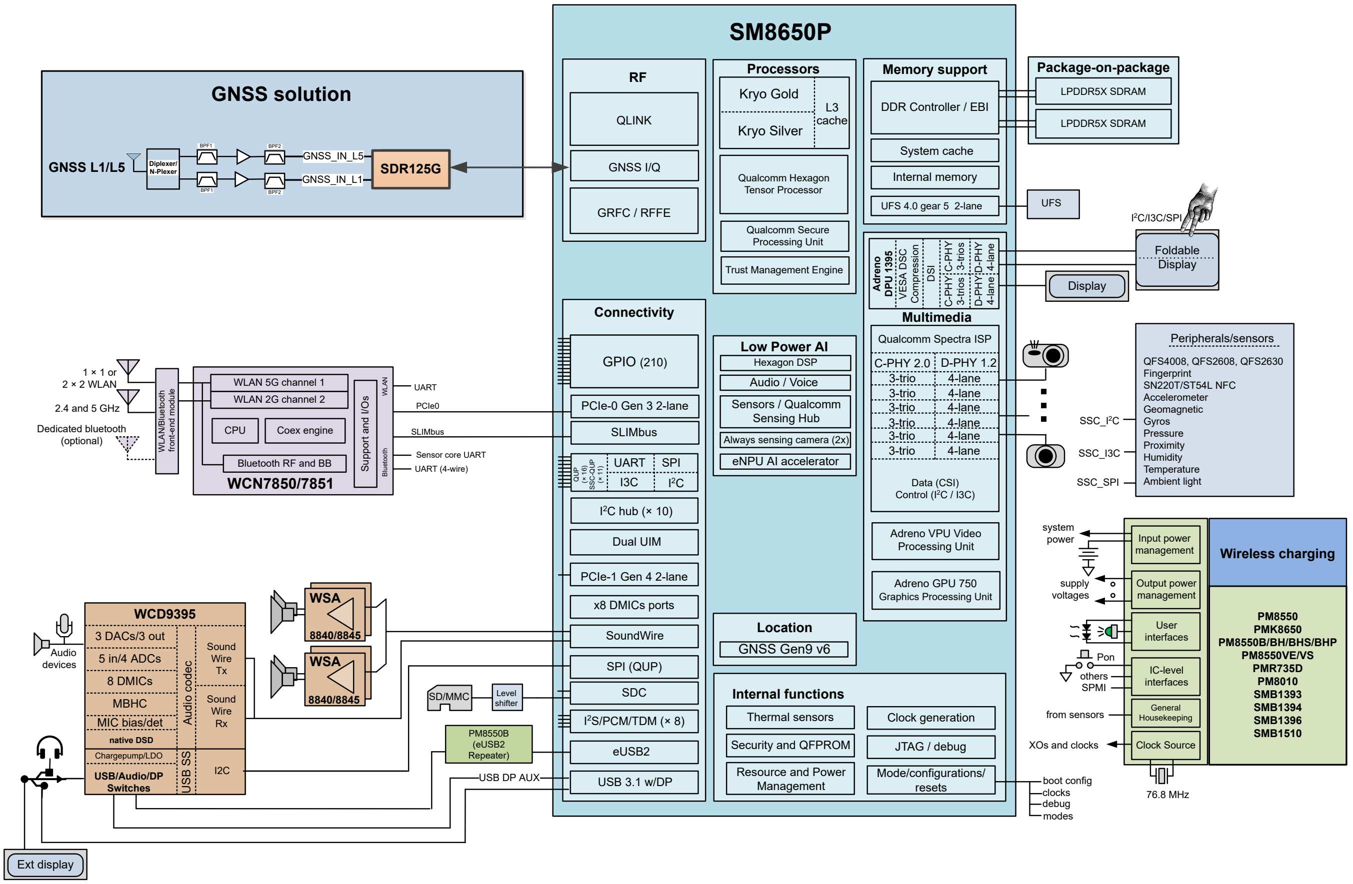

Figure 1-3 SM8650P functional block diagram and example application

1.2 SM8650/SM8650P features

NOTE Some of the hardware features integrated within the SM8650/SM8650P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8650/SM8650P features.

Table 1-1 SM8650/SM8650P features

Feature	SM8650/SM8650P capability
Processors	
Applications	Kryo CPU subsystem ■ Prime and high-performance cores for intensive tasks (1 + 5 + 2) ■ Power-efficient cores
Digital signal processing and artificial intelligence	■ Hexagon Tensor Processor □ V75 AI-optimized tensor processor □ Six scalar threads with enhanced micro architecture □ 4x HVX vector tightly couple coprocessors optimized for pixel processing □ 1x HMX matrix tightly couple coprocessor optimized for deep neural network processing, MAC arithmetic formats include INT8, A16W8, A8W4, and FP16 □ Large VTCM □ BW compression □ Improved power efficiency ■ AI use cases □ Noise reduction □ Super resolution □ ML ISP □ HDR □ Image enhancement □ Segmentation □ Depth estimation □ Classification/detection ■ For imaging, video, audio, and data-based NN use cases. ■ The hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the hexagon software algorithmic functions. ■ The audio/sensors hexagon DSP is dedicated to the low-power AI subsystem with support for always-on, low-power use cases. It incorporates a dedicated AI processor for offloading neural network use cases to improve the performance and minimize power consumption. ■ All hexagon DSP is cache-based processors with full access to DDR memory for large memory requirements.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Modem and location	
Modem	3G/4G/5G – mmWave and sub-6 bands (Rel 17) only for SM8650
Location	Gen9 v6 LocTech 23 SW GPS L1/L5/L2C, GLO G1, BDS B1I/B1C/B2A/B2B, GAL E1/E5A/E5B, QZSS L1/L5/L2C, NavIC L5 An analog GNSS interface to the transceiver IC

Table 1-1 SM8650/SM8650P features (cont.)

Feature	SM8650/SM8650P capability
Memory support	
System memory via EBI on PoP	Four-channel PoP high-speed memory – LPDDR5X SDRAM (4 × 16-bit) supports up to 4.2 GHz with system cache
Storage	UFS 4.0 gear 5 Rate B, 1x 2-lane
Via UFS	ICE with 4500 MB/s read and 4000 MB/s write
Via SDC	SD v3.0 4 bit for SD card
Multimedia	
Qualcomm® Adreno™ display processing unit (DPU)	DPU1395 ■ Maximum resolution for internal panel: Support up to 3360 × 1600 at 144 Hz, 2520 × 1200 at 240 Hz ■ Supports dual MIPI-DSI ports, with support for split-link for fold use case. ■ External panel support: DisplayPort v1.4 with MST (2x 4K60 10-bit or 1x 8K30 with DSC) ■ Compression support: 6x DSC v1.2 ■ Processing: HDR10/10+, HDR Vivid, Dolby Vision HDR, wide color gamut, scaling (improved quality on edge/corner/angle), SPR, and demura (improved quality) ■ Power-saving: Local tone mapping, QSync, variable refresh rate, panel self-refresh using LLC
Camera support	■ Qualcomm spectra image signal processor □ Qualcomm spectra ISP supports connectivity to multiple cameras due to six included C-PHY/D-PHY interfaces. Furthermore, up to 5 cameras may operate concurrently due to the Qualcomm spectra's 3 IFEs, 2 IFE-lites, and 3 SFEs ■ AI assisted camera with object-based pixel processing in single-camera and multicamera mode ■ Flicker correction improvements in HDR ■ 2 × always sensing camera support for simultaneous front and rear AOC with increased input resolution up to 1080p □ CSI4 and CSI2 with PM8010 SPMI interface, CAM_MCLK_4 (GPIO_104), and CAM_MCLK_2 (GPIO_102) □ QR code detection, rotation, and improved face detection accuracy ■ Hardware interface □ Triple 36 MP ISPs □ Six combo-PHYs with 4 lanes for D-PHY and 3 trios for C-PHY each – D-PHY v1.2: 2.5 Gbps/lane – C-PHY v2.0: 13.68 Gbps/trio □ Connect up to 12x/18x cameras, 5x concurrent ■ Throughput □ 108 MP at 30 fps ZSL with in-ISP pixel binning □ 64 MP at 30 fps ZSL with 2 IFEs combined, without in-ISP binning □ 200 MP non-ZSL snapshot capture □ 12 MP at 240 fps fast shutter sensor support - PHY and RAW dump ■ Key improvements □ Three concurrent 2 × 2/4 × 4/sHDR with motion improvement □ Seamless switch to fast readout and 108 MP capture □ Dynamic low voltage operation ■ ZSL example: □ (36 M + 36 M + 36 M) at 30 fps - triple camera □ (64 M + 36 M) at 30 fps - dual camera □ 108 M at 30 fps - single camera

Table 1-1 SM8650/SM8650P features (cont.)

Feature	SM8650/SM8650P capability
	■ MFHDR for snapshot, video, preview ■ Staggered HDR (overlap and nonoverlap) for snapshot, video, and preview
EVA	■ Hardware-based DL-FD 2.6 and DL-FL 2.0 ■ A depth processor for iTOF ■ Reprojection and grid inversion engine (RGE) ■ Dense motion map (SGM based OF, 1080p at 60 fps) ■ Depth from stereo (SGM-based DFS, 720p at 60 fps), concurrent with DMM
Adreno video processing unit (VPU)	Adreno VPU 8650 UHD 8K video processing unit Video decode up to 4K at 240 fps/8K at 60 fps and video encode up to 4K at 120 fps/8K at 30 fps Concurrent decode up to 4K at 60 fps and encode up to 4K at 60 fps for wireless display Max 24 concurrent stream support Native decode support for H.264, H.265, VP9, and AV1 formats Native encode support for H.264 and H.265 formats Slice-based encoder support for low-latency performance Max 8192 × 4320/Min 96 × 96 resolution of frame support Loss frame compression (UBWC) support
Adreno graphic processing unit (GPU)	Adreno GPU A750 OpenGL ES 3.2, Vulkan 1.3 OpenCL 3.0 full profile Adreno NN direct Ray tracing pipelines GMEM improvements for compute and graphics
Low power AI subsystem	Merged low-power island, for always-on audio/voice, sensors, sensing hub, and always sensing camera ■ Hexagon V73M 2 × cluster – 4 Thread DSP ■ 8.5 MB of LPI memory □ 3 MB TCM (DSP and LPAI) □ 5.5 MB of LPI LLC ■ Dual eNPU4 AI processor to accelerate neural networking use cases ■ Qualcomm Sensing Hub 4.0
Sensors hardware	■ Data acquisition engine (DAE) - buffer to enable batching of sensor data without waking up the DSP ■ Context change detector (CCD) 5.1 □ Hardware blocks to detect potential changes in context that are validated in software □ Wakes up DSP once context changes are detected
Sensors interfaces and supported sensors	■ Eleven dedicated buses □ 2 I3C/I^2C, 2 SPI, 2 I^2C, 2 UART □ 2 I3C/I^2C, 1 I^2C for ASC ■ 7 × I3C IBI for DAE and DSP ■ Sensors supported in QTI POR: □ 2 × Accelerometer/Gyroscope □ Magnetometer □ Ambient Light/Proximity □ Pressure □ Humidity/Temperature

Table 1-1 SM8650/SM8650P features (cont.)

Feature	SM8650/SM8650P capability
	□ SAR □ Hall □ Always sensing camera □ Plus others per customer inputs with I3C, I^{2}C, UART, SPI interface could be supported
Qualcomm Sensing Hub (QSH) supported technologies	■ QSH enables multiple data streams providing enhanced contextual data from: □ Sensors □ Always sensing camera □ Audio □ WWAN □ Location/Geofencing □ BLE □ Wi-Fi
Audio and voice hardware	■ Hardware linear echo cancellation accelerator ■ DSP-offload for audio playback (analog, Bluetooth audio, USB digital audio)
Audio interfaces	SLIMbus for WCN785x SoundWire ■ SoundWire interface (3 Tx and 2 Rx data lanes for codec) WCD9395, PMIC haptics ■ Two dedicated SoundWire interfaces to support up to 4 WSA884x for smart speaker amplifier DMICs ■ 4 DMIC ports support up to 8 DMICs ■ Up to 4 DMICs for low-power voice activation I^{2}S ■ 6 I^{2}S with 2x data lanes to support full duplex stereo, or up to 4 channel Tx/Rx application ■ 1 I^{2}S supports 4 data lanes for up to 8 channels Tx/Rx application TDM/PCM: Up to 32 channels at 48 kHz per individual interface (Qualcomm Technologies, Inc. (QTI) I^{2}S supports both TDM and PCM modes.)
Audio and voice algorithms	Voice UI ■ Snapdragon Voice Activation keyword detection ■ Echo cancellation and noise suppression (ECNS) Voice call ■ AI-based noise suppression ■ Far-end noise suppression Audio record ■ Ambient noise suppression ■ HDR record
Codec	Integrated within the WCD9395 high fidelity audio codec
Speaker amplifier	Integrated within the WSA8840/WSA8845/WSA8845H class-H, low noise smart amplifier
Connectivity	
I/Os	Dual voltage (1.2 V/1.8 V) support. For details, see Pin definitions.
Qualcomm universal peripheral (QUP) ports	Qualcomm universal peripheral (QUP) v3 support. 16 QUP serial engines + 11 SSC-QUP serial engines ■ UART ■ I^{2}C

Table 1-1 SM8650/SM8650P features (cont.)

Feature	SM8650/SM8650P capability
	■ I3C ■ SPI 10 I^{2}C hubs
USB	■ One USB 3.1 ports: Gen 2 10 Gbps (DisplayPort + data), support Type-C with DisplayPort v1.4, embedded USB (eUSB2)
UIM	Two 1.8 V/3 V SIM card using external level shifter
PCIe	2-lane Gen 3 2-lane Gen 4
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4) ■ SDC2: 1.2 V only; SD 3.0 ■ 1.8 V/3 V SD card operation using external level shifter ■ SDC4: dual-voltage, SDIO 3.0
Touchscreen support	■ Capacitive panels via ext IC (I^{2}C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display QFS4008, QFS2608, QFS2630
Configurable GPIOs	
Number of GPIOs	210 – GPIO_0 to GPIO_209
Security technologies	
Crypto	AES-GCM, HW ECC, RSA, SHA2 and SHA3, ICE crypto engine v5 (CE5), FIPS/CAVP 140-3 certified, PRNG compliant to NIST 800-90B
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sandboxing
Secure boot and tools	Secure boot/debug security with Sectools 2.0; easy to use tool set
Key management	Hardware key manager
User data encryption	File-based encryption (FBE)
Memory protection	DRAM memory protection for EEs (TEEs and VMs)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.x)
Hypervisor	Qualcomm® Type-1 hypervisor enables multiple trusted VMs (TVMs), Google AVF support
DSP security	DSP secure domain
HLOS kernel security	Qualcomm® runtime kernel security (QRKS)
Cellular connection security	Qualcomm® cellular connection security
QTEE and TVM services	DRM Widevine V18 L1, HDCP v2.3, Qualcomm® content protection, IP protection framework, camera security framework, trusted UI framework, trusted location, trusted time, QC WES device attestation service, QC WES secure provisioning service, QC WES third-party feature licensing service
SPU	SPU for SoC independent TCB, Android Strong box security
Internal functions	
Boot	See *SM8650 Boot and CoreBSP Architecture Overview* (80-TBD-11) for the details of boot sequence. Emergency boot over USB 3.1

Table 1-1 SM8650/SM8650P features (cont.)

Feature	SM8650/SM8650P capability
PLLs and clocks	■ 76.8 MHz X'tal ■ Multiple clock regimes; watchdog and sleep timers ■ Input: 38.4 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD)
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	SPMI; also I^{2}C as needed
Wireless connectivity	
WLAN	PCIe interface
Bluetooth	SLIMbus/UART interface
Fabrication technology, package, and major companion ICs	
Digital die	4 nm process
Package	1629 MPSP
PoP– small, thermally efficient package	16.5 × 14.0 × 0.56 mm
WLAN/Bluetooth	WCN7850, WCN7851
RF	SDR875 (4G/Sub-6/mmW/GNSS), SDR753 (4G/Sub-6/GNSS) QTM565 (mmW)
PMIC	PM8550, PMK8650, PM8550B/BH/BHS, PM8550VE/VS, PM8010 × 2, PMR735D
Audio	WCD9395, WSA8840/WSA8845/WSA8845H

2 Pin definitions

The SM8650/SM8650P is the lower device within a PoP system, as shown and explained in the figure below.

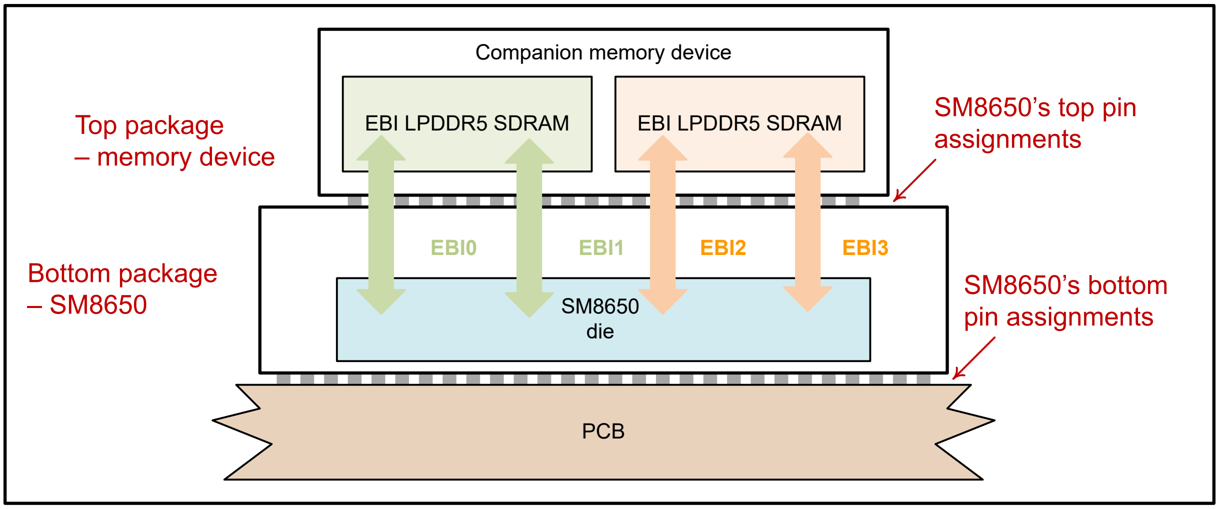

Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8650 bottom pins (Pin assignments: MSM bottom)
- SM8650 top pins (Pin assignments: MSM top)

2.1 I/O parameter definitions

Table 2-1 I/O description (pin type) parameters

Symbol	Description
Pin attribute	
AI	Analog input (does not include pin circuitry)
AO	Analog output (does not include pin circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pin pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pin voltage groupings for baseband circuits	
PX0	Pin group 0 (SPMI0, SPMI1, RESIN_N); 1.2 V
PX10	Pin group 10 (UFS0_REFCLK, UFS0_RESET_N); 1.2 V
PX11	Pin group 11 (CXO); 1.2 V
PX13	Pin group 13 (SP_ARI_POWER_ALARM); 1.85 V
PX14	Pin group 14 (SDC2, JTAG, UIM0, PS_HOLD, SLEEP_CLK, MODE, Modem, Audio SWR); 1.2 V
PX701	Pad group 701 (I/O pad); 1.8 V/1.2 V
PX702	Pad group 702 (I/O pad); 1.8 V/1.2 V
PX703	Pad group 703 (I/O pad); 1.8 V/1.2 V
PX704	Pad group 704 (I/O pad); 1.8 V/1.2 V
PX705	Pad group 705 (I/O pad); 1.8 V/1.2 V
PX706	Pad group 706 (I/O pad); 1.8 V/1.2 V
PX707	Pad group 707 (I/O pad); 1.8 V/1.2 V
PX708	Pad group 708 (I/O pad); 1.8 V/1.2 V
PX709	Pad group 709 (I/O pad); 1.8 V/1.2 V
PX710	Pad group 710 (I/O pad); 1.8 V/1.2 V
PX711	Pad group 711 (I/O pad); 1.8 V/1.2 V

Table 2-1 I/O description (pin type) parameters (cont.)

Symbol	Description
PX712	Pad group 712 (I/O pad); 1.8 V/1.2 V
PX713	Pad group 713 (I/O pad); 1.8 V/1.2 V
PX714	Pad group 714 (I/O pad); 1.8 V/1.2 V
PX715	Pad group 715 (I/O pad); 1.8 V/1.2 V

NOTE For detailed SM8650 pad group assignment, see the *SM8650/SM8650P Digital Baseband Design Guidelines/Training Slides* (80-40938-5).

2.2 Pin assignments: MSM bottom

2.2.1 Pin map: MSM bottom

The SM8650/SM8650P is available in the MPSP1629 package. Its bottom surface is equivalent to an MPSP1629 that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Mechanical information for package details and Pin assignments: MSM top for information about the top pin assignments.

A high-level view of the pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *SM8650/SM8650P Pin Assignment and GPIO Configuration Spreadsheet* (80-40938-1A). This Microsoft Excel spreadsheet lists all SM8650/SM8650P pin numbers (in alphanumeric order), pin names, pin voltages, pin types, and functional descriptions.

NOTE Click the following link to download the *SM8650/SM8650P Pin Assignment and GPIO Configuration Spreadsheet* (80-40938-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-40938-1A

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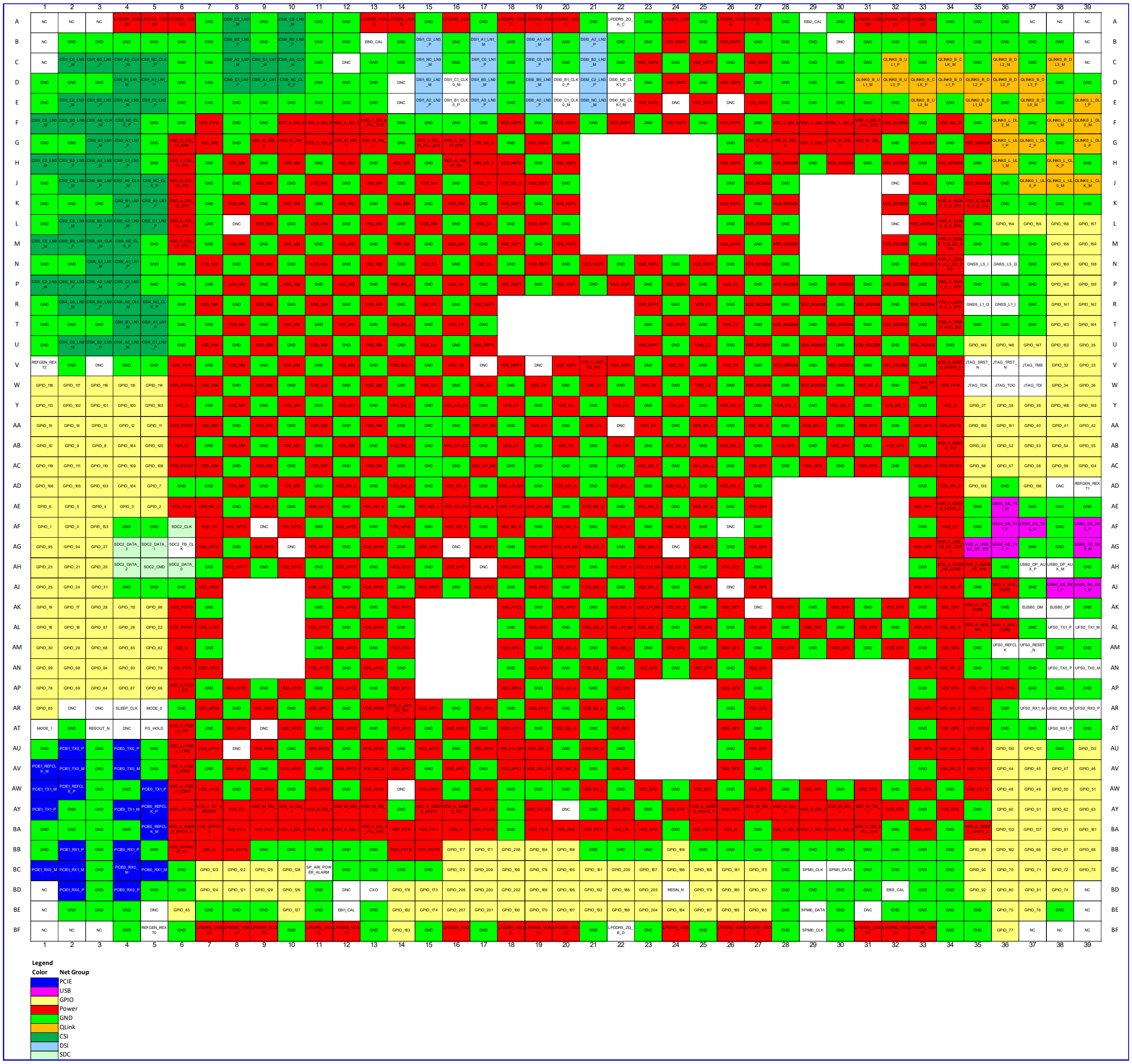


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
A	NC	NC	NC	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2H	GND	CSI0_C2_LN3_M	GND	CSI0_C0_LN0_M	GND	GND	LPDDR5_VDDQ	LPDDR5_VDDQ	GND	LPDDR5_VDD1	GND	LPDDR5_VDD2L	LPDDR5_VDD2L	LPDDR5_VDD2L	GND	LPDDR5_ZQ_A_C	GND	LPDDR5_VDD1	GND	LPDDR5_VDDQ	LPDDR5_VDDQ	GND	EBI2_CAL	GND	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2H	GND	GND	GND	NC	NC	NC
B	NC	GND	GND	GND	GND	GND	GND	CSI0_B2_LN3_P	GND	CSI0_B0_LN0_P	GND	GND	EBI0_CAL	GND	DSI1_C2_LN3_P	GND	DSI1_A1_LN1_M	GND	DSI0_A1_LN1_M	GND	DSI0_A2_LN2_P	GND	GND	VDD_NSP2	GND	VDD_NSP2	GND	GND	GND	DNC	GND	GND	GND	GND	GND	GND	GND	GND	NC
C	NC	CSI1_C0_LN0_M	CSI1_B0_LN0_P	CSI1_A0_CLK_M	CSI1_NC_CLK_P	GND	GND	CSI0_A2_LN2_M	CSI0_B1_LN1_M	CSI0_A0_CLK_M	GND	DNC	GND	GND	DSI1_NC_LN3_M	GND	DSI1_C0_LN1_P	GND	DSI0_C0_LN1_P	GND	DSI0_B2_LN2_M	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_NSP2	GND	GND	GND	GND	QLINK0_B_UL1_P	GND	QLINK0_B_CLK_M	GND	QLINK0_B_DL2_M	GND	QLINK0_B_DL3_M	NC
D	GND	GND	GND	CSI1_B1_LN1_M	CSI1_A1_LN1_P	GND	GND	CSI0_C1_LN2_P	CSI0_A1_LN1_P	CSI0_NC_CLK_P	GND	GND	GND	DNC	DSI1_B2_LN2_M	DSI1_C1_CLK0_M	DSI1_B0_LN0_M	GND	DSI0_B0_LN0_M	DSI0_B1_CLK0_P	DSI0_C2_LN3_P	DSI0_NC_CLK1_P	GND	VDD_NSP2	GND	VDD_NSP2	GND	GND	GND	GND	QLINK0_B_UL1_M	QLINK0_B_UL0_P	QLINK0_B_CLK_P	QLINK0_B_DL1_P	QLINK0_B_DL2_P	QLINK0_B_DL0_P	QLINK0_B_DL3_P	GND	GND
E	GND	CSI1_C2_LN3_M	CSI1_B2_LN3_P	CSI1_A2_LN2_M	CSI1_C1_LN2_P	GND	GND	GND	GND	GND	GND	GND	GND	DNC	DSI1_A2_LN2_P	DSI1_B1_CLK0_P	DSI1_A0_LN0_P	GND	DSI0_A0_LN0_P	DSI0_C1_CLK0_M	DSI0_NC_LN3_M	DSI0_NC_CLK1_M	VDD_NSP2	DNC	VDD_NSP2	DNC	VDD_NSP2	GND	GND	GND	GND	GND	QLINK0_B_UL0_M	GND	QLINK0_B_DL1_M	GND	QLINK0_B_DL0_M	GND	QLINK0_L_DL1_P
F	CSI3_C0_LN0_M	CSI3_B0_LN0_P	CSI3_A0_CLK_M	CSI3_NC_CLK_P	GND	GND	VDD_PX14	GND	GND	VDD_A_EBI_0	VDD_A_EBI_0	VDD_A_EBI_0	VDD_A_EBI_0_PLL_0P9	GND	GND	GND	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_A_EBI_2	VDD_A_EBI_2	VDD_A_EBI_2	VDD_A_EBI_2_PLL_0P9	VDD_MODEM	GND	VDD_MX_C	GND	QLINK0_L_DL2_M	GND	QLINK0_L_DL1_M	QLINK0_L_DL0_M
G	GND	GND	CSI3_B1_LN1_M	CSI3_A1_LN1_P	GND	VDD_A_CSI_01_0P9	VDD_MM	GND	VDD_IO_EBI_0	VDD_IO_EBI_0	VDD_D_EBI_0	VDD_IO_EBI_0	VDD_IO_EBI_0	GND	VDD_A_DSI_01_PLL_0P9	VDD_A_DSI_01_0P9	VDD_MX_C	GND	VDD_NSP2	GND						GND	VDD_IO_EBI_2	VDD_IO_EBI_2	VDD_D_EBI_2	VDD_IO_EBI_2	VDD_IO_EBI_2	GND	VDD_MODEM	GND	VDD_MODEM	QLINK0_L_UL1_P	QLINK0_L_DL2_P	GND	QLINK0_L_DL0_P
H	CSI3_C2_LN3_M	CSI3_B2_LN3_P	CSI3_A2_LN2_M	CSI3_C1_LN2_P	GND	VDD_A_CSI_01_1P2	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_A_DSI_01_1P2	VDD_MX_C	VDD_NSP2	GND	VDD_NSP2						VDD_NSP2	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	QLINK0_L_UL1_M	GND	QLINK0_L_CLK_P	GND
J	GND	CSI2_C0_LN0_M	CSI2_B0_LN0_P	CSI2_A0_CLK_M	CSI2_NC_CLK_P	VDD_A_CSI_35_1P2	GND	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	VDD_MX_C	VDD_NSP1	GND						GND	VDD_MODEM	GND				DNC	VDD_MX_A	GND	VDD_MODEM	GND	QLINK0_L_UL0_P	QLINK0_L_UL0_M	QLINK0_L_CLK_M
K	GND	GND	GND	CSI2_B1_LN1_M	CSI2_A1_LN1_P	VDD_A_CSI_35_0P9	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_NSP1	GND	VDD_NSP2						VDD_NSP2	GND	VDD_MODEM				VDD_MODEM	GND	VDD_A_QLINK_0_B_0P9	VDD_A_QLINK_0_B_1P2	GND	GND	GND	GND
L	GND	CSI2_C2_LN3_M	CSI2_B2_LN3_P	CSI2_A2_LN2_M	CSI2_C1_LN2_P	VDD_A_CSI_24_1P2	GND	DNC	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	GND	VDD_NSP1	GND						GND	VDD_MODEM	GND				DNC	VDD_MODEM	VDD_A_QLINK_0_B_0P9	GND	GPIO_154	GPIO_155	GPIO_156	GPIO_157
M	CSI5_C0_LN0_M	CSI5_B0_LN0_P	CSI5_A0_CLK_M	CSI5_NC_CLK_P	GND	VDD_A_CSI_24_0P9	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_NSP1	GND	VDD_NSP2						VDD_NSP2	GND	VDD_MODEM				VDD_MODEM	GND	VDD_A_QLINK_0_B_CK_0P9	GND	GND	GND	GPIO_158	GPIO_159
N	GND	GND	CSI5_B1_LN1_M	CSI5_A1_LN1_P	GND	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	GND	VDD_CX	GND	VDD_NSP1	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_NSP2	GND	VDD_MODEM	GND				GND	VDD_MODEM	VDD_A_QLINK_0_L_CK_0P9	GNSS_L5_I	GNSS_L5_Q	GND	GPIO_160	GPIO_138
P	CSI5_C2_LN3_M	CSI5_B2_LN3_P	CSI5_A2_LN2_M	CSI5_C1_LN2_P	GND	GND	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_C	GND	VDD_CX	GND	VDD_NSP1	GND	VDD_NSP1	GND	VDD_NSP1	GND	VDD_NSP1	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_A_QLINK_0_L_0P9	GND	GND	GND	GPIO_140	GPIO_139
R	GND	CSI4_C0_LN0_M	CSI4_B0_LN0_P	CSI4_A0_CLK_M	CSI4_NC_CLK_P	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	GND	VDD_NSP1						VDD_NSP1	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	VDD_A_QLINK_0_L_0P9	GNSS_L1_Q	GNSS_L1_I	GND	GPIO_141	GPIO_142
T	GND	GND	GND	CSI4_B1_LN1_M	CSI4_A1_LN1_P	GND	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_C	GND	VDD_CX	GND						GND	VDD_NSP1	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_A_GNSS_ADC_1P2	GND	GND	GND	GPIO_143	GPIO_144
U	GND	CSI4_C2_LN3_M	CSI4_B2_LN3_P	CSI4_A2_LN2_M	CSI4_C1_LN2_P	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	GND	VDD_NSP1						VDD_NSP1	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	GPIO_145	GPIO_146	GPIO_147	GPIO_152	GPIO_35
V	REFGEN_REXT2	GND	DNC	GND	GND	VDD_PX14	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_C	GND	VDD_CX	DNC	VDD_NSP1	DNC	VDD_NSP1	VDD_A_NSP_CS_1P2	VDD_NSP1	GND	VDD_CX	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_A_QREFS_0P875_5	JTAG_SRST_N	JTAG_TRST_N	JTAG_TMS	GPIO_32	GPIO_33
W	GPIO_118	GPIO_117	GPIO_116	GPIO_115	GPIO_114	VDD_PX705	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_MODEM	GND	VDD_MODEM	GND	VDD_MX_C	GND	VDD_LPI_MX_NAV	VDD_PX14	JTAG_TCK	JTAG_TDO	JTAG_TDI	GPIO_34	GPIO_36
Y	GPIO_113	GPIO_102	GPIO_101	GPIO_100	GPIO_163	VDD_IX	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_C	GND	VDD_LPI_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_IX	GPIO_37	GPIO_38	GPIO_39	GPIO_148	GPIO_149
AA	GPIO_15	GPIO_14	GPIO_13	GPIO_12	GPIO_11	VDD_PX706	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	GND	GND	VDD_LPI_MX	GND	VDD_CX	GND	VDD_CX	DNC	VDD_CX	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	VDD_PX715	GPIO_150	GPIO_151	GPIO_40	GPIO_41	GPIO_42
AB	GPIO_10	GPIO_9	GPIO_8	GPIO_164	GPIO_120	VDD_IX	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_C	GND	VDD_LPI_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_CX	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_A_QREFS_1P2	GPIO_43	GPIO_52	GPIO_53	GPIO_54	GPIO_55
AC	GPIO_119	GPIO_111	GPIO_110	GPIO_109	GPIO_108	VDD_PX707	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	VDD_MM	GND	GND	GND	VDD_LPI_MX	GND	GND	GND	GND	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	VDD_PX709	GPIO_56	GPIO_57	GPIO_58	GPIO_59	GPIO_134
AD	GPIO_106	GPIO_105	GPIO_103	GPIO_104	GPIO_7	GND	GND	VDD_MM	GND	VDD_MM	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_LPI_MX	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_C	GND	VDD_MX_C	GND						GND	VDD_MX_C	GPIO_135	GND	GPIO_136	DNC	REFGEN_REXT1
AE	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	VDD_PX14	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	VDD_LPI_CX	VDD_MX_A	VDD_LPI_CX	VDD_LPI_MX	GND	VDD_MX_A	GND	VDD_MX_C	GND	VDD_MX_C	GND	VDD_GFX						VDD_GFX	VDD_A_QREFS_0P875_4	GND	USB0_SS_TX1_M	GND	GND	GND
AF	GPIO_1	GPIO_0	GPIO_153	GND	GND	SDC2_CLK	VDD_CX	VDD_APC2	DNC	VDD_APC2	GND	VDD_APC0	GND	VDD_APC0	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_A	GND	VDD_MX_C	GND	DNC	GND						GND	VDD_CX	GND	USB0_SS_TX1_P	USB0_SS_TX0_M	GND	USB0_SS_RX0_P
AG	GPIO_95	GPIO_94	GPIO_27	SDC2_DATA_3	SDC2_DATA_1	SDC2_FB_CLK	VDD_APC2	GND	VDD_APC2	DNC	VDD_APC2	GND	VDD_APC0	GND	VDD_APC1	DNC	VDD_APC1	GND	VDD_APC1	VDD_LPI_MX	VDD_MX_A	GND	VDD_MX_C	DNC	VDD_MX_C	GND	VDD_GFX						VDD_GFX	VDD_A_USB_SS_DP_CORE	VDD_A_USB_SS_DP_1P2	USB0_SS_TX0_P	GND	GND	USB0_SS_RX0_M
AH	GPIO_23	GPIO_21	GPIO_20	SDC2_DATA_2	SDC2_CMD	SDC2_DATA_0	GND	VDD_APC2	GND	VDD_APC2	GND	VDD_APC0	GND	VDD_APC1	GND	VDD_APC1	DNC	VDD_APC1	GND	VDD_APC1	GND	VDD_MX_A	VDD_LPI_MX	VDD_MX_C	GND	VDD_GFX	GND						GND	VDD_A_EUSB_HS_CORE	VDD_A_EUSB_HS_1P2	GND	USB0_DP_AUX_P	USB0_DP_AUX_M	GND
AJ	GPIO_25	GPIO_24	GPIO_31	GND	GND	GND	VDD_APC2				VDD_APC2	GND	VDD_APC0	GND	VDD_APC1	GND	VDD_APC1	GND	VDD_APC1	GND	VDD_MX_A	GND	VDD_MX_C	GND	VDD_GFX	DNC	VDD_GFX						VDD_GFX	VDD_MX_C	GND	VDD_A_UFS_CORE	GND	USB0_SS_RX1_P	USB0_SS_RX1_M
AK	GPIO_19	GPIO_17	GPIO_28	GPIO_112	GPIO_96	VDD_PX710	GND				GND	VDD_APC0	GND	VDD_APC1				VDD_APC1	GND	VDD_APC1	GND	VDD_MX_A	VDD_LPI_MX	VDD_MX_C	GND	VDD_GFX	DNC	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	VDD_A_UFS_CORE	GND	EUSB0_DM	EUSB0_DP	GND
AL	GPIO_16	GPIO_18	GPIO_97	GPIO_26	GPIO_22	VDD_PX704	VDD_APC2				VDD_APC2	GND	VDD_APC0	GND				GND	VDD_APC1	GND	VDD_MX_A	VDD_LPI_MX	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	VDD_MX_C	VDD_A_UFS_1P2	VDD_A_UFS_CORE	GND	UFS0_TX1_P	UFS0_TX1_M
AM	GPIO_30	GPIO_29	GPIO_68	GPIO_83	GPIO_82	VDD_IX	GND				GND	VDD_APC0	GND	VDD_APC1				VDD_APC1	GND	VDD_MX_A	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	UFS0_REFCLK	UFS0_RESET_N	GND	GND
AN	GPIO_99	GPIO_98	GPIO_84	GPIO_93	GPIO_79	VDD_PX14	VDD_APC2				VDD_APC2	GND	VDD_APC0	GND				GND	VDD_APC1	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX						VDD_GFX	VDD_MX_C	GND	GND	GND	UFS0_TX0_P	UFS0_TX0_M
AP	GPIO_78	GPIO_69	GPIO_64	GPIO_67	GPIO_66	VDD_A_PCIE_1_1P2	GND	VDD_APC2	GND	VDD_APC2	GND	VDD_APC0	GND	VDD_APC1				VDD_APC1	GND	VDD_MX_A	GND	VDD_GFX				VDD_GFX	GND						GND	VDD_GFX	VDD_PX14	VDD_PX10	GND	GND	GND
AR	GPIO_65	DNC	DNC	SLEEP_CLK	MODE_0	GND	VDD_APC2	GND	VDD_APC2	GND	VDD_APC2	GND	VDD_APC0	VDD_A_APC_CS_1P2	VDD_APC1	GND	VDD_APC1	GND	VDD_APC1	GND	VDD_MX_C	GND				GND	VDD_GFX						VDD_GFX	VDD_MX_C	VDD_IX	GND	UFS0_RX1_M	UFS0_RX0_M	UFS0_RX0_P
AT	MODE_1	GND	RESOUT_N	DNC	PS_HOLD	VDD_A_PCIE_0_1P2	GND	VDD_APC2	DNC	VDD_APC2	GND	VDD_APC0	GND	VDD_APC1	GND	VDD_APC1	GND	VDD_APC1	GND	VDD_MX_A	GND	VDD_GFX				VDD_GFX	GND						GND	VDD_GFX	VDD_PX708	GND	GND	UFS0_RX1_P	GND
AU	GND	PCIE1_TX0_P	GND	PCIE0_TX0_P	GND	VDD_A_PCIE_1_CORE	VDD_APC0	DNC	VDD_APC0	GND	VDD_APC0	GND	VDD_APC0	GND	VDD_APC1	GND	VDD_APC1	VDD_LPI_MX	VDD_MX_A	GND	VDD_MX_C	GND				GND	VDD_GFX						VDD_GFX	VDD_MX_C	VDD_IX	GPIO_130	GPIO_131	GND	GPIO_132
AV	PCIE1_REFCLK_M	PCIE1_TX0_M	GND	PCIE0_TX0_M	GND	VDD_A_PCIE_1_CORE	GND	VDD_APC0	GND	VDD_APC0	GND	VDD_APC0	VDD_MX_A	VDD_APC1	GND	VDD_APC1	GND	VDD_APC1	VDD_LPI_CX	VDD_MX_A	GND	VDD_GFX				VDD_GFX	GND						GND	VDD_MX_C	VDD_PX711	GPIO_44	GPIO_45	GPIO_47	GPIO_46
AW	PCIE1_TX1_M	PCIE1_REFCLK_P	GND	GND	PCIE0_TX1_P	VDD_A_PCIE_0_CORE	VDD_APC0	GND	VDD_APC0	GND	VDD_APC0	GND	VDD_APC0	DNC	VDD_APC1	GND	VDD_APC1	GND	GND	GND	VDD_MX_C	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_GFX	GND	VDD_PX712	GPIO_48	GPIO_49	GPIO_50	GPIO_51
AY	PCIE1_TX1_P	GND	GND	PCIE0_TX1_M	PCIE0_REFCLK_P	VDD_LPI_MX	VDD_A_SP_SENSOR	VDD_CX	VDD_IO_EBI_1	VDD_IO_EBI_1	VDD_D_EBI_1	VDD_IO_EBI_1	VDD_IO_EBI_1	GND	VDD_A_QREFS_0P875	VDD_A_QREFS_1P2	VDD_LPI_CX	GND	VDD_LPI_CX	DNC	GND	VDD_GFX	GND	VDD_GFX	VDD_A_QREFS_0P875_1	VDD_GFX	VDD_IO_EBI_3	VDD_IO_EBI_3	VDD_D_EBI_3	VDD_IO_EBI_3	VDD_IO_EBI_3	VDD_GFX	GND	VDD_GFX	GND	GPIO_60	GPIO_61	GPIO_62	GPIO_63
BA	GND	GND	GND	GND	PCIE0_REFCLK_M	VDD_A_QREFS_0P875_0	VDD_QFPROM	VDD_PX14	VDD_PX13	VDD_A_EBI_1	VDD_A_EBI_1	VDD_A_EBI_1	VDD_A_EBI_1_PLL_0P9	VDD_PX14	VDD_PX11	VDD_IX	VDD_PX703	GND	VDD_PX14	VDD_PX0	VDD_PX14	VDD_CX	VDD_GFX	GND	VDD_PX701	VDD_IX	GND	VDD_A_EBI_3	VDD_A_EBI_3	VDD_A_EBI_3	VDD_A_EBI_3_PLL_0P9	GND	VDD_GFX	GND	VDD_A_QREFS_0P875_2	GPIO_133	GPIO_137	GPIO_91	GPIO_161
BB	GND	PCIE1_RX1_P	GND	PCIE0_RX1_P	GND	VDD_QFPROM_SP	VDD_IX	VDD_PX714	GND	GND	GND	GND	GND	VDD_PX713	VDD_PX702	GPIO_177	GPIO_171	GPIO_208	GPIO_194	GPIO_198	GND	GND	GND	GPIO_169	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GPIO_89	GPIO_162	GPIO_86	GPIO_87	GPIO_88
BC	PCIE1_RX0_M	PCIE1_RX1_M	GND	PCIE0_RX0_M	PCIE0_RX1_M	GND	GPIO_123	GPIO_122	GPIO_125	GPIO_128	SP_ARI_POWER_ALARM	GND	GND	GND	GND	GPIO_172	GPIO_209	GPIO_199	GPIO_176	GPIO_195	GPIO_191	GPIO_205	GPIO_187	GPIO_186	GPIO_168	GPIO_181	GPIO_175	GND	SPMI1_CLK	SPMI1_DATA	GND	GND	GND	GND	GPIO_90	GPIO_70	GPIO_71	GPIO_72	GPIO_73
BD	NC	PCIE1_RX0_P	GND	PCIE0_RX0_P	GND	GND	GPIO_124	GPIO_121	GPIO_129	GPIO_126	GND	DNC	CXO	GPIO_178	GPIO_173	GPIO_206	GPIO_200	GPIO_202	GPIO_166	GPIO_196	GPIO_192	GPIO_188	GPIO_203	RESIN_N	GPIO_179	GPIO_180	GPIO_107	GND	GND	GND	GND	EBI3_CAL	GND	GND	GPIO_92	GPIO_80	GPIO_81	GPIO_74	NC
BE	NC	GND	GND	GND	DNC	GPIO_85	GND	GND	GND	GPIO_127	GND	EBI1_CAL	GND	GPIO_182	GPIO_174	GPIO_207	GPIO_201	GPIO_190	GPIO_170	GPIO_197	GPIO_193	GPIO_189	GPIO_204	GPIO_184	GPIO_167	GPIO_185	GPIO_165	GND	SPMI0_DATA	GND	DNC	GND	GND	GND	GND	GPIO_75	GPIO_76	GND	NC
BF	NC	NC	NC	GND	REFGEN_REXT0	GND	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2H	GND	LPDDR5_VDDQ	LPDDR5_VDDQ	GND	GPIO_183	GND	LPDDR5_VDD1	GND	LPDDR5_VDD2L	LPDDR5_VDD2L	LPDDR5_VDD2L	GND	LPDDR5_ZQ_B_D	GND	LPDDR5_VDD1	GND	LPDDR5_VDDQ	LPDDR5_VDDQ	GND	SPMI0_CLK	GND	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2H	GND	GND	GPIO_77	NC	NC	NC

Legend

Color	Net Group
🟦	PCIE
🟪	USB
🟨	GPIO
🟥	Power
🟩	GND
🟧	QLink
🟩	CSI
🟦	DSI
🟩	SDC

Figure 2-2 SM8650 bottom pin assignments (top view)

2.2.2 Pin descriptions: MSM bottom

The bottom pins are described in Table 2-2 through Table 2-6.

Table 2-2 MSM bottom pin descriptions – general pins

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
C10	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential clock - minus MIPI CSI0 (C-PHY), trio lane 0 – A
D9	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 1 - plus MIPI CSI0 (C-PHY), trio lane 1 – A
C8	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 2 - minus MIPI CSI0 (C-PHY), trio lane 2 – A
B10	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 0 - plus MIPI CSI0 (C-PHY), trio lane 0 – B
C9	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 1 - minus MIPI CSI0 (C-PHY), trio lane 1 – B
B8	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 3 - plus MIPI CSI0 (C-PHY), trio lane 2 – B
A10	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 0 - minus MIPI CSI0 (C-PHY), trio lane 0 – C
D8	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 2 - plus MIPI CSI0 (C-PHY), trio lane 1 – C
A8	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI0 (D-PHY), differential lane 3 - minus MIPI CSI0 (C-PHY), trio lane 2 – C
D10	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI0 (D-PHY), differential clock - plus MIPI CSI0 (C-PHY), no connect
C4	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential clock - minus MIPI CSI1 (C-PHY), trio lane 0 – A
D5	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 1 - plus MIPI CSI1 (C-PHY), trio lane 1 – A

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
E4	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 2 - minus MIPI CSI1 (C-PHY), trio lane 2 – A
C3	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 0 - plus MIPI CSI1 (C-PHY), trio lane 0 – B
D4	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 1 - minus MIPI CSI1 (C-PHY), trio lane 1 – B
E3	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 3 - plus MIPI CSI1 (C-PHY), trio lane 2 – B
C2	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 0 - minus MIPI CSI1 (C-PHY), trio lane 0 – C
E5	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 2 - plus MIPI CSI1 (C-PHY), trio lane 1 – C
E2	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI1 (D-PHY), differential lane 3 - minus MIPI CSI1 (C-PHY), trio lane 2 – C
C5	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI1 (D-PHY), differential clock - plus MIPI CSI1 (C-PHY), no connect
J4	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential clock - minus MIPI CSI2 (C-PHY), trio lane 0 – A
K5	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 1 - plus MIPI CSI2 (C-PHY), trio lane 1 – A
L4	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 2 - minus MIPI CSI2 (C-PHY), trio lane 2 – A
J3	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 0 - plus MIPI CSI2 (C-PHY), trio lane 0 – B
K4	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 1 - minus MIPI CSI2 (C-PHY), trio lane 1 – B
L3	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 3 - plus MIPI CSI2 (C-PHY), trio lane 2 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
J2	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 0 - minus MIPI CSI2 (C-PHY), trio lane 0 – C
L5	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 2 - plus MIPI CSI2 (C-PHY), trio lane 1 – C
L2	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI2 (D-PHY), differential lane 3 - minus MIPI CSI2 (C-PHY), trio lane 2 – C
J5	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI2 (D-PHY), differential clock - plus MIPI CSI2 (C-PHY), no connect
F3	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential clock - minus MIPI CSI3 (C-PHY), trio lane 0 – A
G4	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 1 - plus MIPI CSI3 (C-PHY), trio lane 1 – A
H3	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 2 - minus MIPI CSI3 (C-PHY), trio lane 2 – A
F2	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 0 - plus MIPI CSI3 (C-PHY), trio lane 0 – B
G3	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 1 - minus MIPI CSI3 (C-PHY), trio lane 1 – B
H2	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 3 - plus MIPI CSI3 (C-PHY), trio lane 2 – B
F1	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 0 - minus MIPI CSI3 (C-PHY), trio lane 0 – C
H4	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 2 - plus MIPI CSI3 (C-PHY), trio lane 1 – C
H1	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI3 (D-PHY), differential lane 3 - minus MIPI CSI3 (C-PHY), trio lane 2 – C
F4	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI3 (D-PHY), differential clock - plus MIPI CSI3 (C-PHY), no connect

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
R4	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential clock - minus MIPI CSI4 (C-PHY), trio lane 0 – A
T5	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 1 - plus MIPI CSI4 (C-PHY), trio lane 1 – A
U4	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 2 - minus MIPI CSI4 (C-PHY), trio lane 2 – A
R3	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 0 - plus MIPI CSI4 (C-PHY), trio lane 0 – B
T4	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 1 - minus MIPI CSI4 (C-PHY), trio lane 1 – B
U3	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 3 - plus MIPI CSI4 (C-PHY), trio lane 2 – B
R2	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 0 - minus MIPI CSI4 (C-PHY), trio lane 0 – C
U5	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 2 - plus MIPI CSI4 (C-PHY), trio lane 1 – C
U2	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI4 (D-PHY), differential lane 3 - minus MIPI CSI4 (C-PHY), trio lane 2 – C
R5	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI4 (D-PHY), differential clock - plus MIPI CSI4 (C-PHY), no connect
M3	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential clock - minus MIPI CSI5 (C-PHY), trio lane 0 – A
N4	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 1 - plus MIPI CSI5 (C-PHY), trio lane 1 – A
P3	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 2 - minus MIPI CSI5 (C-PHY), trio lane 2 – A
M2	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 0 - plus MIPI CSI5 (C-PHY), trio lane 0 – B

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
N3	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 1 - minus MIPI CSI5 (C-PHY), trio lane 1 – B
P2	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 3 - plus MIPI CSI5 (C-PHY), trio lane 2 – B
M1	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 0 - minus MIPI CSI5 (C-PHY), trio lane 0 – C
P4	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 2 - plus MIPI CSI5 (C-PHY), trio lane 1 – C
P1	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI5 (D-PHY), differential lane 3 - minus MIPI CSI5 (C-PHY), trio lane 2 – C
M4	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI5 (D-PHY), differential clock - plus MIPI CSI5 (C-PHY), no connect
BD13	CXO	PX_11	DIS	Core crystal oscillator (digital 19.2 MHz system clock)
E19	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 0 - plus MIPI DSI0 (C-PHY), trio lane 0 – A
B19	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 1 - minus MIPI DSI0 (C-PHY), trio lane 1 – A
B21	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 2 - plus MIPI DSI0 (C-PHY), trio lane 2 – A
D19	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 0 - minus MIPI DSI0 (C-PHY), trio lane 0 – B
D20	DSI0_B1_CLK0_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 0 - plus MIPI DSI0 (C-PHY), trio lane 1 – B
C21	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 2 - minus MIPI DSI0 (C-PHY), trio lane 2 – B
C19	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 1 - plus MIPI DSI0 (C-PHY), trio lane 0 – C

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
E20	DSI0_C1_CLK0_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 0 - minus MIPI DSI0 (C-PHY), trio lane 1 – C
D21	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 3 - plus MIPI DSI0 (C-PHY), trio lane 2 – C
E22	DSI0_NC_CLK1_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 1 - minus MIPI DSI0 (C-PHY), no connect
D22	DSI0_NC_CLK1_P	DSI	AI, AO	MIPI DSI0 (D-PHY), differential clock 1 - plus MIPI DSI0 (C-PHY), no connect
E21	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI0 (D-PHY), differential lane 3 - minus MIPI DSI0 (C-PHY), no connect
E17	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 0 - plus MIPI DSI1 (C-PHY), trio lane 0 – A
B17	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 1 - minus MIPI DSI1 (C-PHY), trio lane 1 – A
E15	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 2 - plus MIPI DSI1 (C-PHY), trio lane 2 – A
D17	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 0 - minus MIPI DSI1 (C-PHY), trio lane 0 – B
E16	DSI1_B1_CLK0_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 0 - plus MIPI DSI1 (C-PHY), trio lane 1 – B
D15	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 2 - minus MIPI DSI1 (C-PHY), trio lane 2 – B
C17	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 1 - plus MIPI DSI1 (C-PHY), trio lane 0 – C
D16	DSI1_C1_CLK0_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential clock 0 - minus MIPI DSI1 (C-PHY), trio lane 1 – C
B15	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 3 - plus MIPI DSI1 (C-PHY), trio lane 2 – C

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
C15	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI1 (D-PHY), differential lane 3 - minus MIPI DSI1 (C-PHY), no connect
B13	EBI0_CAL	LPDDR5-VDDQ	AI	EBI0 calibration resistor
BE12	EBI1_CAL	LPDDR5-VDDQ	AI	EBI1 calibration resistor
A29	EBI2_CAL	LPDDR5-VDDQ	AI	EBI2 calibration resistor
BD32	EBI3_CAL	LPDDR5-VDDQ	AI	EBI3 calibration resistor
AK37	EUSB0_DM	-	AI, AO	Embedded USB0 high-speed data - minus
AK38	EUSB0_DP	-	AI, AO	Embedded USB0 high-speed data - plus
R36	GNSS_L1_I	-	AI	GNSS lane 1 - I
R35	GNSS_L1_Q	-	AI	GNSS lane 1 - Q
N35	GNSS_L5_I	-	AI	GNSS lane 5 - I
N36	GNSS_L5_Q	-	AI	GNSS lane 5 - Q
V35	JTAG_SRST_N	PX_14	DIS-PU	JTAG reset for debug
W35	JTAG_TCK	PX_14	DIS-PU	JTAG clock input
W37	JTAG_TDI	PX_14	DIS-PU:nppdkp	JTAG data input
W36	JTAG_TDO	PX_14	DO-Z	JTAG data output
V37	JTAG_TMS	PX_14	DI-PU:nppdkp	JTAG mode select input
V36	JTAG_TRST_N	PX_14	DI-PD:nppukp	JTAG reset
A22	LPDDR5_ZQ_A_C	LPDDR5-VDDQ	AI	ZQ calibration reference
BF22	LPDDR5_ZQ_B_D	LPDDR5-VDDQ	AI	ZQ calibration reference
AR5	MODE_0	PX_14	DIS	Mode control bit 0 – unconnected for native mode
AT1	MODE_1	PX_14	DIS	Mode control bit 1 – unconnected for native mode
BA5	PCIE0_REFCLK_M	-	AO	PCIe 0 Gen 3 reference clock - minus
AY5	PCIE0_REFCLK_P	-	AO	PCIe 0 Gen 3 reference clock - plus
BC4	PCIE0_RX0_M	-	AI	PCIe 0 Gen 3 receive 0 - minus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
BD4	PCIE0_RX0_P	-	AI	PCIe 0 Gen 3 receive 0 - plus
BC5	PCIE0_RX1_M	-	AI	PCIe 0 Gen 3 receive 1 - minus
BB4	PCIE0_RX1_P	-	AI	PCIe 0 Gen 3 receive 1 - plus
AV4	PCIE0_TX0_M	-	AO	PCIe 0 Gen 3 transmit 0 - minus
AU4	PCIE0_TX0_P	-	AO	PCIe 0 Gen 3 transmit 0 - plus
AY4	PCIE0_TX1_M	-	AO	PCIe 0 Gen 3 transmit 1 - minus
AW5	PCIE0_TX1_P	-	AO	PCIe 0 Gen 3 transmit 1 - plus
AV1	PCIE1_REFCLK_M	-	AO	PCIe 1 Gen 3 reference clock - minus
AW2	PCIE1_REFCLK_P	-	AO	PCIe 1 Gen 3 reference clock - plus
BC1	PCIE1_RX0_M	-	AI	PCIe 1 Gen 3 receive 0 - minus
BD2	PCIE1_RX0_P	-	AI	PCIe 1 Gen 3 receive 0 - plus
BC2	PCIE1_RX1_M	-	AI	PCIe 1 Gen 3 receive 1 - minus
BB2	PCIE1_RX1_P	-	AI	PCIe 1 Gen 3 receive 1 - plus
AV2	PCIE1_TX0_M	-	AO	PCIe 1 Gen 3 transmit 0 - minus
AU2	PCIE1_TX0_P	-	AO	PCIe 1 Gen 3 transmit 0 - plus
AW1	PCIE1_TX1_M	-	AO	PCIe 1 Gen 3 transmit 1 - minus
AY1	PCIE1_TX1_P	-	AO	PCIe 1 Gen 3 transmit 1 - plus
AT5	PS_HOLD	PX_14	Z	Power-supply hold signal to PMIC
J39	QLINK0_L_CLK_M	-	AO	QLink0 Port L clock minus
H38	QLINK0_L_CLK_P	-	AO	QLink0 Port L clock plus
F39	QLINK0_L_DL0_M	-	AI	QLink0 Port L lane D0 minus
G39	QLINK0_L_DL0_P	-	AI	QLink0 Port L lane D0 plus
F38	QLINK0_L_DL1_M	-	AI	QLink0 Port L lane D1 minus
E39	QLINK0_L_DL1_P	-	AI	QLink0 Port L lane D1 plus
F36	QLINK0_L_DL2_M	-	AI	QLink0 Port L lane D2 minus
G37	QLINK0_L_DL2_P	-	AI	QLink0 Port L lane D2 plus
J38	QLINK0_L_UL0_M	-	AO	QLink0 Port L lane U0 minus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
J37	QLINK0_L_UL0_P	-	AO	QLink0 Port L lane U0 plus
H36	QLINK0_L_UL1_M	-	AO	QLink0 Port L lane U1 minus
G36	QLINK0_L_UL1_P	-	AO	QLink0 Port L lane U1 plus
C34	QLINK0_B_CLK_M	-	AO	QLink0 Port B clock minus
D33	QLINK0_B_CLK_P	-	AO	QLink0 Port B clock plus
E37	QLINK0_B_DL0_M	-	AI	QLink0 Port B lane D0 minus
D36	QLINK0_B_DL0_P	-	AI	QLink0 Port B lane D0 plus
E35	QLINK0_B_DL1_M	-	AI	QLink0 Port B lane D1 minus
D34	QLINK0_B_DL1_P	-	AI	QLink0 Port B lane D1 plus
C36	QLINK0_B_DL2_M	-	AI	QLink0 Port B lane D2 minus
D35	QLINK0_B_DL2_P	-	AI	QLink0 Port B lane D2 plus
C38	QLINK0_B_DL3_M	-	AI	QLink0 Port B lane D3 minus
D37	QLINK0_B_DL3_P	-	AI	QLink0 Port B lane D3 plus
E33	QLINK0_B_UL0_M	-	AO	QLink0 Port B lane U1 plus
D32	QLINK0_B_UL0_P	-	AO	QLink0 Port B lane U1 plus
D31	QLINK0_B_UL1_M	-	AO	QLink0 Port B lane U1 plus
C32	QLINK0_B_UL1_P	-	AO	QLink0 Port B lane U1 plus
BF5	REFGEN_REXT0	-	AI	Reference voltage bias
AD39	REFGEN_REXT1	-	AI	Reference voltage bias
V1	REFGEN_REXT2	-	AI	Reference voltage bias
BD24	RESIN_N	PX_0	DI	Reset input
AT3	RESOUT_N	PX_14	DO	Reset output
AF6	SDC2_CLK	PX_14	DO	Secure digital controller 2 clock
AH5	SDC2_CMD	PX_14	B	Secure digital controller 2 command
AH6	SDC2_DATA_0	PX_14	B	Secure digital controller 2 data bit 0
AG5	SDC2_DATA_1	PX_14	B	Secure digital controller 2 data bit 1
AH4	SDC2_DATA_2	PX_14	B	Secure digital controller 2 data bit 2

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
AG4	SDC2_DATA_3	PX_14	B	Secure digital controller 2 data bit 3
AG6	SDC2_FB_CLK	PX_14	DI	Secure digital controller 2 feedback clock
AR4	SLEEP_CLK	PX_14	DIS	Sleep clock
BF29	SPMI0_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
BE29	SPMI0_DATA	PX_0	BS-PD:nppukp	Slave and PBUS interface for PMICs – data
BC29	SPMI1_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
BC30	SPMI1_DATA	PX_0	BS-PD:nppukp	Slave and PBUS interface for PMICs – data
BC11	SP_ARI_POWER_ALARM	PX_13	DI	Power alarm
AM36	UFS0_REFCLK	PX_10	DO	UFS0 reference clock
AM37	UFS0_RESET_N	PX_10	DO	UFS0 reset
AR38	UFS0_RX0_M	-	AI	UFS0 receive 0 - minus
AR39	UFS0_RX0_P	-	AI	UFS0 receive 0 - plus
AR37	UFS0_RX1_M	-	AI	UFS0 receive 1 - minus
AT38	UFS0_RX1_P	-	AI	UFS0 receive 1 - plus
AN39	UFS0_TX0_M	-	AO	UFS0 transmit 0 - minus
AN38	UFS0_TX0_P	-	AO	UFS0 transmit 0 - plus
AL39	UFS0_TX1_M	-	AO	UFS0 transmit 1 - minus
AL38	UFS0_TX1_P	-	AO	UFS0 transmit 1 - plus
AH38	USB0_DP_AUX_M	-	AI, AO	USB0 DisplayPort aux – minus
AH37	USB0_DP_AUX_P	-	AI, AO	USB0 DisplayPort aux – plus
AG39	USB0_SS_RX0_M	-	AI	USB0 SuperSpeed receive - minus
AF39	USB0_SS_RX0_P	-	AI	USB0 SuperSpeed receive - plus
AJ39	USB0_SS_RX1_M	-	AI	USB0 SuperSpeed receive - minus
AJ38	USB0_SS_RX1_P	-	AI	USB0 super-speed receive - plus
AF37	USB0_SS_TX0_M	-	AO	USB0 SuperSpeed transmit - minus

Table 2-2 MSM bottom pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
AG36	USB0_SS_TX0_P	-	AO	USB0 SuperSpeed transmit - plus
AE36	USB0_SS_TX1_M	-	AO	USB0 SuperSpeed transmit - minus
AF36	USB0_SS_TX1_P	-	AO	USB0 SuperSpeed transmit - plus

[a] See Table 2-1 for parameter and acronym definitions

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application’s requirements and map each GPIO to its function - carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull up or pull down
- External connections
  - Unused inputs
  - Connections to high impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM8650/SM8650P GPIOs (in numeric order), pin numbers, pin voltages, pull states, and available configurations.

NOTE Click the following link to download the *SM8650/SM8650P Pin Assignment and GPIO Configuration Spreadsheet* (80-40938-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-40938-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	**Type**		
AF2	GPIO_0		PX707	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L0			QUP 2 SE 0 lane 0	
		IBI_I3C_QUP2_SE0_SDA			QUP2 in-band interrupt I3C SE clock 2	
		SSC_20			EGPIO - SSC I/O 20	
		SSC_20:SSC_QUPV3_SE8_0				
AF1	GPIO_1		PX707	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L1			QUP 2 SE 0 lane 1	
		IBI_I3C_QUP2_SE0_SCL			QUP2 in-band interrupt I3C SE data 2	
		SSC_21			EGPIO - SSC I/O 21	
		SSC_21:SSC_QUPV3_SE8_1				
AE5	GPIO_2		PX707	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L2			QUP 2 SE 0 lane 2	
		SSC_27			EGPIO - SSC I/O 27	
		SSC_27:ASC_CAM2_STANDBY				
AE4	GPIO_3		PX707	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L3			QUP 2 SE 0 lane 3	
		SSC_26			EGPIO - SSC I/O 26	
		SSC_26:ASC_CAM2_RESET				
AE3	GPIO_4		PX707	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L0			QUP 2 SE 1 lane 0	
		IBI_I3C_QUP2_SE1_SDA			QUP2 in-band interrupt I3C SE clock 2	
		SSC_22			EGPIO - SSC I/O 22	
		SSC_22:SSC_QUPV3_SE9_0				
AE2	GPIO_5		PX707	PD:nppukp	Configurable I/O	N
		QUP2_SE1_L1			QUP 2 SE 1 lane 1	
		IBI_I3C_QUP2_SE1_SCL			QUP2 in-band interrupt I3C SE data 2	
		SSC_23			EGPIO - SSC I/O 23	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_23:SSC_QUPV3_SE9_1				
AE1	GPIO_6		PX707	PD:nppukp	Configurable I/O	N
		QUP2_SE1_L2			QUP 2 SE 1 lane 2	
		SSC_29			EGPIO - SSC I/O 29	
		SSC_29:ASC_CAM4_STANDBY				
AD5	GPIO_7		PX707	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L3			QUP 2 SE 1 lane 3	
		SSC_28			EGPIO - SSC I/O 28	
		SSC_28:ASC_CAM4_RESET				
AB3	GPIO_8		PX705	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L0			QUP 2 SE 2 lane 0	
		IBI_I3C_QUP2_SE2_SDA			QUP2 in-band interrupt I3C SE clock 2	
AB2	GPIO_9		PX705	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L1			QUP 2 SE 2 lane 1	
		IBI_I3C_QUP2_SE2_SCL			QUP2 in-band interrupt I3C SE data 2	
AB1	GPIO_10		PX705	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L2			QUP 2 SE 2 lane 2	
		CCI_TIMER2			Camera control interface timer 2	
AA5	GPIO_11		PX705	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L3			QUP 2 SE 2 Lane 3	
		CCI_TIMER3			Camera control interface timer 3	
AA4	GPIO_12		PX705	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L0			QUP 2 SE 3 lane 0	
		CCI_I2C_SDA3			Camera I^{2}C data 3	
		IBI_I3C_QUP2_SE3_SDA			QUP2 in-band interrupt I3C SE clock 2	
		QUP2_SE2_L6			QUP 2 SE 2 lane 6	
AA3	GPIO_13		PX705	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	**Type**		
		QUP2_SE3_L1			QUP 2 SE 3 lane 1	
		CCI_I2C_SCL3			Camera I^{2}C clock 3	
		IBI_I3C_QUP2_SE3_SCL			QUP2 in-band interrupt I3C SE data 2	
		QUP2_SE2_L4			QUP 2 SE 2 lane 4	
AA2	GPIO_14		PX705	PD:nppukp	Configurable I/O	N
		QUP2_SE3_L2			QUP 2 SE 3 lane 2	
AA1	GPIO_15		PX705	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L3			QUP 2 SE 3 lane 3	
		CCI_ASYNC_IN0			Camera control interface async 0	
		QUP2_SE2_L5			QUP 2 SE 2 lane 5	
AL1	GPIO_16		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE4_L0			QUP 2 SE 4 lane 0	
AK2	GPIO_17		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE4_L1			QUP 2 SE 4 lane 1	
AL2	GPIO_18		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L2			QUP 2 SE 4 lane 2	
AK1	GPIO_19		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L3			QUP 2 SE 4 lane 3	
AH3	GPIO_20		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L0			QUP 2 SE 5 lane 0	
AH2	GPIO_21		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE5_L1			QUP 2 SE 5 lane 1	
AL5	GPIO_22		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE5_L2			QUP 2 SE 5 lane 2	
AH1	GPIO_23		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L3			QUP 2 SE 5 lane 3	
		QUP2_SE5_L6			QUP 2 SE 5 lane 6	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AJ2	GPIO_24		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE6_L0			QUP 2 SE 6 lane 0	
AJ1	GPIO_25		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE6_L1			QUP 2 SE 6 lane 1	
AL4	GPIO_26		PX14	PD:nppukp	Configurable I/O	N
		QUP2_SE6_L2			QUP 2 SE 6 lane 2	
AG3	GPIO_27		PX14	PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L3			QUP 2 SE 6 lane 3	
AK3	GPIO_28		PX710	PD:nppukp	Configurable I/O	N
		QUP2_SE7_L0			QUP 2 SE 7 lane 0	
AM2	GPIO_29		PX710	PD:nppukp	Configurable I/O	Y
		QUP2_SE7_L1			QUP 2 SE 7 lane 1	
		USB_PHY_PS_MIRB			USB PHY port select	
AM1	GPIO_30		PX710	PD:nppukp	Configurable I/O	N
		QUP2_SE7_L2			QUP 2 SE 7 lane 2	
AJ3	GPIO_31		PX710	PD:nppukp	Configurable I/O	Y
		QUP2_SE7_L3			QUP 2 SE 7 lane 3	
V38	GPIO_32		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L0			QUP 1 SE 0 lane 0	
		IBI_I3C_QUP1_SE0_SDA			QUP1 in-band interrupt I3C SE clock 1	
V39	GPIO_33		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE0_L1			QUP 1 SE 0 lane 1	
		IBI_I3C_QUP1_SE0_SCL			QUP1 in-band interrupt I3C SE data 1	
W38	GPIO_34	NFC_RESET_N	PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE0_L2			QUP 1 SE 0 lane 2	
U39	GPIO_35		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L3			QUP 1 SE 0 lane 3	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
W39	GPIO_36		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L0			QUP 1 SE 1 lane 0	
		IBI_I3C_QUP1_SE1_SDA			QUP1 in-band interrupt I3C SE clock 1	
Y35	GPIO_37		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE1_L1			QUP 1 SE 1 lane 1	
		IBI_I3C_QUP1_SE1_SCL			QUP1 in-band interrupt I3C SE data 1	
Y36	GPIO_38		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE1_L2			QUP 1 SE 1 lane 2	
Y37	GPIO_39		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L3			QUP 1 SE 1 lane 3	
AA37	GPIO_40		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L0			QUP 1 SE 2 lane 0	
AA38	GPIO_41		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L1			QUP 1 SE 2 lane 1	
AA39	GPIO_42		PX715	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L2			QUP 1 SE 2 lane 2	
AB35	GPIO_43	FP_SPI_CS	PX715	PD:nppukp	Configurable I/O	Y
		QUP1_SE2_L3			QUP 1 SE 2 lane 3	
AV36	GPIO_44		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE3_L0			QUP 1 SE 3 lane 0	
		QUP1_SE2_L4			QUP 1 SE 2 lane 4	
AV37	GPIO_45		PX14	PD:nppukp	Configurable I/O	N
		QUP1_SE3_L1			QUP 1 SE 3 lane 1	
		QUP1_SE2_L5			QUP 1 SE 2 lane 5	
AV39	GPIO_46		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L2			QUP 1 SE 3 lane 2	
		QUP1_SE2_L6			QUP 1 SE 2 lane 6	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AV38	GPIO_47		PX14	PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L3			QUP 1 SE 3 lane 3	
		UIM0_PRESENT			UIM0 presence detection	
		DP_HOT_PLUG_DETECT			DisplayPort hot plug detect	
AW36	GPIO_48		PX708	PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L0			QUP 1 SE 4 lane 0	
		IBI_I3C_QUP1_SE4_SDA			QUP1 in-band interrupt I3C SE clock 1	
AW37	GPIO_49		PX708	PD:nppukp	Configurable I/O	N
		QUP1_SE4_L1			QUP 1 SE 4 lane 1	
		IBI_I3C_QUP1_SE4_SCL			QUP1 in-band interrupt I3C SE data 1	
AW38	GPIO_50		PX708	PD:nppukp	Configurable I/O	N
		QUP1_SE4_L2			QUP 1 SE 4 lane 2	
AW39	GPIO_51		PX708	PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L3			QUP 1 SE 4 lane 3	
AB36	GPIO_52		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L0			QUP 1 SE 5 lane 0	
AB37	GPIO_53		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L1			QUP 1 SE 5 lane 1	
		GP_MN			General-purpose M/N:D counter output	
AB38	GPIO_54		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L2			QUP 1 SE 5 lane 2	
		USB_PHY_PS_MIRA			USB PHY port select	
AB39	GPIO_55		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L3			QUP 1 SE 5 lane 3	
AC35	GPIO_56		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L0			QUP 1 SE 6 lane 0	
		IBI_I3C_QUP1_SE6_SDA			QUP1 in-band interrupt I3C SE clock 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QSPI_DATA[2]			Quad-SPI data	
		SDC4_DATA[2]			Secure digital controller data	
AC36	GPIO_57		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L1			QUP 1 SE 6 lane 1	
		IBI_I3C_QUP1_SE6_SCL			QUP1 in-band interrupt I3C SE data 1	
		QSPI_DATA[3]			Quad-SPI data	
		SDC4_DATA[3]			Secure digital controller data	
AC37	GPIO_58		PX709	PD:nppukp	Configurable I/O	N
		QUP1_SE6_L2			QUP 1 SE 6 lane 2	
		QSPI_CS_N_0			Quad-SPI chip select 0	
AC38	GPIO_59		PX709	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L3			QUP 1 SE 6 lane 3	
		QSPI_CS_N_1			Quad-SPI chip select 1	
		SDC4_CMD			Secure digital controller 4 command	
AY36	GPIO_60		PX708	PD:nppukp	Configurable I/O	N
		QUP1_SE7_L0			QUP 1 SE 7 lane 0	
AY37	GPIO_61		PX708	PD:nppukp	Configurable I/O	N
		QUP1_SE7_L1			QUP 1 SE 7 lane 1	
AY38	GPIO_62		PX708	PD:nppukp	Configurable I/O	N
		QUP1_SE7_L2			QUP 1 SE 7 lane 2	
AY39	GPIO_63		PX708	PD:nppukp	Configurable I/O	Y
		QUP1_SE7_L3			QUP 1 SE 7 lane 3	
AP3	GPIO_64		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L0			I^{2}C Hub 0 SE 0 lane 0	
AR1	GPIO_65		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE0_L1			I^{2}C hub 0 SE 0 lane 1	
AP5	GPIO_66		PX704	PD:nppukp	Configurable I/O	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		I2CHUB0_SE1_L0			I^2C hub 0 SE 1 lane 0	
AP4	GPIO_67		PX704	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE1_L1			I^2C hub 0 SE 1 lane 1	
AM3	GPIO_68		PX710	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE2_L0			I^2C hub 0 SE 2 lane 0	
AP2	GPIO_69		PX710	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE2_L1			I^2C hub 0 SE 2 lane 1	
BC36	GPIO_70		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L0			I^2C hub 0 SE 3 lane 0	
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
BC37	GPIO_71		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE3_L1			I^2C hub 0 SE 3 lane 1	
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
BC38	GPIO_72		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L0			I^2C hub 0 SE 4 lane 0	
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	
BC39	GPIO_73		PX711	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE4_L1			I^2C hub 0 SE 4 lane 1	
BD38	GPIO_74		PX14	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE5_L0			I^2C hub 0 SE 5 lane 0	
BE36	GPIO_75		PX14	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE5_L1			I^2C hub 0 SE 5 lane 1	
BE37	GPIO_76		PX14	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE6_L0			I^2C hub 0 SE 6 lane 0	
		UIM1_PRESENT			UIM1 presence detection	
BF36	GPIO_77	WPC_INT_N	PX14	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE6_L1			I^2C hub 0 SE 6 lane 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AP1	GPIO_78		PX710	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE7_L0			I^2C hub 0 SE 7 lane 0	
AN5	GPIO_79		PX710	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE7_L1			I^2C hub 0 SE 7 lane 1	
BD36	GPIO_80		PX711	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE9_L0			I^2C hub 0 SE 9 lane 0	
BD37	GPIO_81		PX711	PD:nppukp	Configurable I/O	Y
		I2CHUB0_SE9_L1			I^2C hub 0 SE 9 lane 1	
AM5	GPIO_82	PM8010_1_RESET_N	PX710	PD:nppukp	Configurable I/O	N
AM4	GPIO_83	PM8010_2_RESET_N	PX710	PD:nppukp	Configurable I/O	N
		FORCED_USB_BOOT			Forced USB boot	
AN3	GPIO_84		PX704	PD:nppukp	Configurable I/O	Y
BE6	GPIO_85		PX714	PD:nppukp	Configurable I/O	Y
BB37	GPIO_86		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA			MDP vertical sync – primary A	
		MDP_VSYNC0_OUT			MDP vertical sync 0 output	
		MDP_VSYNC1_OUT			MDP vertical sync 1 Output	
		GCC_GP1_CLK_MIRB			General-purpose clock 1 B	
BB38	GPIO_87		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA			MDP vertical sync – secondary A	
		MDP_VSYNC2_OUT			MDP vertical sync 2 output	
		MDP_VSYNC3_OUT			MDP vertical sync 3 output	
		GCC_GP2_CLK_MIRB			General-purpose clock 2 B	
BB39	GPIO_88		PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_E			MDP vertical sync – external	
		GCC_GP3_CLK_MIRB			General-purpose clock 3 B	
BB35	GPIO_89		PX712	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BC35	GPIO_90		PX712	PD:nppukp	Configurable I/O	Y
BA38	GPIO_91		PX708	PD:nppukp	Configurable I/O	N
BD35	GPIO_92		PX712	PD:nppukp	Configurable I/O	Y
AN4	GPIO_93		PX710	PD:nppukp	Configurable I/O	N
		SD_WRITE_PROTECT			Secure digital card write protection	
AG2	GPIO_94	PCIE0_RST_N	PX14	PD:nppukp	Configurable I/O	N
AG1	GPIO_95		PX14	PU:nppdkp	Configurable I/O	Y
		PCIE0_CLK_REQ_N			PCIe0 clock request	
AK5	GPIO_96	PCIE0_WAKE_N	PX14	PD:nppukp	Configurable I/O	Y
AL3	GPIO_97	PCIE1_RST_N	PX710	PD:nppukp	Configurable I/O	N
AN2	GPIO_98		PX710	PU:nppdkp	Configurable I/O	Y
		PCIE1_CLK_REQ_N			PCIe1 clock request	
AN1	GPIO_99	PCIE1_WAKE_N	PX710	PD:nppukp	Configurable I/O	Y
Y4	GPIO_100		PX705	PD:nppukp	Configurable I/O	N
		CAM_MCLK0			Camera 0 MCLK	
Y3	GPIO_101		PX705	PD:nppukp	Configurable I/O	N
		CAM_MCLK1			Camera 1 MCLK	
Y2	GPIO_102		PX705	PD:nppukp	Configurable I/O	N
		CAM_ASC_MCLK2			ASC camera 2 MCLK	
AD3	GPIO_103		PX706	PD:nppukp	Configurable I/O	N
		CAM_MCLK3			Camera 3 MCLK	
AD4	GPIO_104		PX707	PD:nppukp	Configurable I/O	N
		CAM_ASC_MCLK4			ASC camera 4 MCLK	
AD2	GPIO_105		PX706	PD:nppukp	Configurable I/O	N
		CAM_MCLK5			Camera 5 MCLK	
AD1	GPIO_106		PX706	PD:nppukp	Configurable I/O	N
		CAM_MCLK7			Camera 7 MCLK	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BD27	GPIO_107	WCD_RESET_N	PX14	PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[6]			Boot configuration bit 6	
AC5	GPIO_108		PX706	PD:nppukp	Configurable I/O	N
		CAM_MCLK6			Camera 6 MCLK	
AC4	GPIO_109		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera control interface timer 0	
AC3	GPIO_110		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera control interface timer 1	
AC2	GPIO_111		PX706	PD:nppukp	Configurable I/O	N
		CCI_TIMER4			Camera control interface timer 4	
AK4	GPIO_112		PX707	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SDA4			Camera I^2C data 4	
Y1	GPIO_113		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Camera I^2C data 0	
W5	GPIO_114		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Camera I^2C clock 0	
W4	GPIO_115		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Camera I^2C data 1	
W3	GPIO_116		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Camera I^2C clock 1	
W2	GPIO_117		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Camera I^2C data 2	
W1	GPIO_118		PX705	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Camera I^2C clock 2	
AC1	GPIO_119		PX706	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA5			Camera I^2C data 5	
AB5	GPIO_120		PX706	PD:nppukp	Configurable I/O	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		CCI_I2C_SCL5			Camera I^2C clock 5	
BD8	GPIO_121		PX714	PD:nppukp	Configurable I/O	N
		I2S1_SCK			I^2S 1 clock	
BC8	GPIO_122		PX714	PD:nppukp	Configurable I/O	N
		I2S1_DATA0			I^2S 1 serial data channel 0	
BC7	GPIO_123		PX714	PD:nppukp	Configurable I/O	N
		I2S1_WS			I^2S 1 serial data word select	
BD7	GPIO_124		PX714	PD:nppukp	Configurable I/O	N
		I2S1_DATA1			I^2S 1 serial data channel 1	
		AUDIO_REF_CLK			Audio reference clock	
BC9	GPIO_125		PX714	PD:nppukp	Configurable I/O	N
		AUDIO_EXT_MCLK0			Audio external MCLK 0	
BD10	GPIO_126		PX714	PD:nppukp	Configurable I/O	N
		I2S0_SCK			I^2S 0 clock	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
BE10	GPIO_127		PX714	PD:nppukp	Configurable I/O	N
		I2S0_DATA0			I^2S 0 serial data channel 0	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
BC10	GPIO_128		PX714	PD:nppukp	Configurable I/O	N
		I2S0_DATA1			I^2S 0 serial data channel 1	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
BD9	GPIO_129		PX714	PD:nppukp	Configurable I/O	N
		I2S0_WS			I^2S 0 serial data word select	
AU36	GPIO_130		PX14	PD:nppukp	Configurable I/O	N
		UIM0_DATA			UIM0 data	
AU37	GPIO_131		PX14	PD:nppukp	Configurable I/O	N
		UIM0_CLK			UIM0 clock	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AU39	GPIO_132		PX14	PD:nppukp	Configurable I/O	N
		UIM0_RESET			UIM0 reset	
BA36	GPIO_133	DISP0_RESET_N	PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRB			MDP vertical sync – secondary B	
AC39	GPIO_134		PX715	PD:nppukp	Configurable I/O	N
		UIM1_DATA			UIM1 data	
		QSPI_DATA[0]			Quad-SPI data	
		SDC4_DATA[0]			Secure digital Controller data	
		GCC_GP1_CLK_MIRA			General-purpose clock 1 A	
AD35	GPIO_135		PX715	PD:nppukp	Configurable I/O	N
		UIM1_CLK			UIM1 clock	
		QSPI_CLK			Quad SPI clock	
		SDC4_CLK			Secure digital controller clock	
		GCC_GP2_CLK_MIRA			General-purpose clock 2 A	
AD37	GPIO_136		PX715	PD:nppukp	Configurable I/O	Y
		UIM1_RESET			UIM1 reset	
		QSPI_DATA[1]			Quad-SPI data	
		SDC4_DATA[1]			Secure digital controller data	
		GCC_GP3_CLK_MIRA			General-purpose clock 3 A	
BA37	GPIO_137	DISP1_RESET_N	PX708	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRB			MDP vertical sync – primary B	
N39	GPIO_138		PX14	PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front end 0 interface clock	
		GRFC0			Generic RF controller bit 0	
P39	GPIO_139		PX14	PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front end 0 interface data	
		GRFC1			Generic RF controller bit 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		BOOT_CONFIG[10]			Boot configuration bit 10	
P38	GPIO_140		PX14	PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front end 1 interface clock	
		GRFC2			Generic RF controller bit 2	
R38	GPIO_141		PX14	PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front end 1 interface data	
		GRFC3			Generic RF controller bit 3	
		BOOT_CONFIG[9]			Boot configuration bit 9	
R39	GPIO_142		PX14	PD:nppukp	Configurable I/O	N
		RFFE2_CLK			RF front end 2 interface clock	
		GRFC4			Generic RF controller bit 4	
T38	GPIO_143		PX14	PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front end 2 interface data	
		GRFC5			Generic RF controller bit 5	
		BOOT_CONFIG[8]			Boot configuration bit 8	
T39	GPIO_144		PX14	PD:nppukp	Configurable I/O	N
		GRFC6			Generic RF controller bit 6	
		BOOT_CONFIG[1]			Boot configuration bit 1	
U35	GPIO_145		PX14	PD:nppukp	Configurable I/O	N
		GRFC7			Generic RF controller bit 7	
		BOOT_CONFIG[2]			Boot configuration bit 2	
U36	GPIO_146		PX14	PD:nppukp	Configurable I/O	N
		GRFC8			Generic RF controller bit 8	
		BOOT_CONFIG[3]			Boot configuration bit 3	
U37	GPIO_147		PX14	PD:nppukp	Configurable I/O	N
		GRFC9			Generic RF controller bit 9	
		BOOT_CONFIG[4]			Boot configuration bit 4	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
Y38	GPIO_148		PX14	PD:nppukp	Configurable I/O	Y
		COEX_UART1_RX			Interface between WCN and MSM 1	
Y39	GPIO_149		PX14	PD:nppukp	Configurable I/O	N
		COEX_UART1_TX			Interface between WCN and MSM 1	
AA35	GPIO_150	GNSS_ELNA_EN0	PX14	PD:nppukp	Configurable I/O	Y
		GRFC10			Generic RF controller bit 10	
		COEX_UART2_RX			Interface between WCN and MSM 2	
AA36	GPIO_151	GNSS_ELNA_EN1	PX14	PD:nppukp	Configurable I/O	N
		GRFC11			Generic RF controller bit 11	
		COEX_UART2_TX			Interface between WCN and MSM 2	
U38	GPIO_152		PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO2			GNSS control signal 2	
		GRFC12			Generic RF controller bit 12	
		BOOT_CONFIG[7]			Boot configuration bit 7	
AF3	GPIO_153	CAM_DRI_IRQ_1	PX707	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SCL4			Camera I^{2}C clock 4	
L36	GPIO_154	GNSS_TIMING_PULSE	PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO0			GNSS control signal 0	
		NAV_GPIO3			GNSS control signal 3	
		BOOT_CONFIG[5]			Boot configuration bit 5	
L37	GPIO_155		PX14	PD:nppukp	Configurable I/O	Y
		NAV_GPIO1			GNSS control signal 1	
		BOOT_CONFIG[11]			Boot configuration bit 11	
L38	GPIO_156		PX14	PD:nppukp	Configurable I/O	Y
		QLINK0_L_REQUEST			SDR QLINK0 port L request	
L39	GPIO_157		PX14	PD:nppukp	Configurable I/O	N
		QLINK0_L_ENABLE			SDR QLINK0 Port L Enable	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
M38	GPIO_158		PX14	PD:nppukp	Configurable I/O	N
		QLINK0_WMSS_RESET_N			SDR Modem Subsystem Reset Output	
		BOOT_CONFIG[0]			Boot Configuration bit 0	
M39	GPIO_159		PX14	PD:nppukp	Configurable I/O	Y
		QLINK0_B_REQUEST			SDR QLINK0 port B request	
		QDSS_CTI_TRIG1_IN_MIRA			QDSS trigger input 1 A	
N38	GPIO_160		PX14	PD:nppukp	Configurable I/O	N
		QLINK0_B_ENABLE			SDR QLINK0 port B enable	
BA39	GPIO_161		PX708	PD:nppukp	Configurable I/O	N
BB36	GPIO_162		PX708	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG0_IN_MIRA			QDSS trigger input 0 A	
Y5	GPIO_163		PX705	PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN1			Camera control interface async 1	
AB4	GPIO_164		PX706	PD:nppukp	Configurable I/O	N
		CCI_ASYNC_IN2			Camera control interface async 2	
BE27	GPIO_165		PX14	PD:nppukp	Configurable I/O	N
		LPASS_0			EGPIO - LPASS I/O 0	
		LPASS_0:SWR_TX_CLK			SoundWire transmit clock	
		LPASS_0:LPI_I2S0_SCK			LPI I2S 0 clock	
BD19	GPIO_166		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_1			EGPIO - LPASS I/O 1	
		LPASS_1:SWR_TX_DATA0			SoundWire transmit data 0	
		LPASS_1:LPI_I2S0_WS			LPI I2S 0 serial data word select	
BE25	GPIO_167		PX14	PD:nppukp	Configurable I/O	N
		LPASS_2			EGPIO - LPASS I/O 2	
		LPASS_2:SWR_TX_DATA1			SoundWire transmit data 1	
		LPASS_2:LPI_I2S0_DATA0			LPI I2S 0 serial data channel 0	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
BC25	GPIO_168		PX14	PD:nppukp	Configurable I/O	N
		LPASS_3			EGPIO - LPASS I/O 3	
		LPASS_3:SWR_RX_CLK			SoundWire receive clock	
		LPASS_3:LPI_I2S0_DATA1			LPI I2S 0 serial data channel 1	
BB24	GPIO_169		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_4			EGPIO - LPASS I/O 4	
		LPASS_4:SWR_RX_DATA0			SoundWire receive data 0	
		LPASS_4:LPI_I2S0_DATA2			LPI I2S 0 serial data channel 2	
BE19	GPIO_170		PX14	PD:nppukp	Configurable I/O	N
		LPASS_5			EGPIO - LPASS I/O 5	
		LPASS_5:SWR_RX_DATA1			SoundWire receive data 1	
		LPASS_5: EXT_MCLK1_C			External MCLK1 C	
		LPASS_5:LPI_I2S0_DATA3			LPI I2S 0 serial data channel 3	
BB17	GPIO_171		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_6			EGPIO - LPASS I/O 6	
		LPASS_6:LPI_DMIC1_CLK			DMIC 1 clock	
		LPASS_6:LPI_I2S1_CLK			LPI I2S 1 clock	
BC16	GPIO_172		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_7			EGPIO - LPASS I/O 7	
		LPASS_7:LPI_DMIC1_DATA			DMIC 1 data	
		LPASS_7:LPI_I2S1_WS			LPI I2S 1 serial data word select	
BD15	GPIO_173		PX702	PD:nppukp	Configurable I/O	N
		LPASS_8			EGPIO - LPASS I/O 8	
		LPASS_8:LPI_DMIC2_CLK			DMIC 2 clock	
		LPASS_8:LPI_I2S1_DATA0			LPI I2S 0 serial data channel 0	
BE15	GPIO_174		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_9			EGPIO - LPASS I/O 9	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_9:LPI_DMIC2_DATA			DMIC 2 data	
		LPASS_9:LPI_I2S1_DATA1			LPI I2S 0 serial data channel 1	
		LPASS_9: EXT_MCLK1_B			External MCLK1 B	
BC27	GPIO_175		PX701	PD:nppukp	Configurable I/O	N
		LPASS_10			EGPIO - LPASS I/O 10	
		LPASS_10:LPI_I2S2_CLK			LPI I2S 2 clock	
		LPASS_10:WSA_SWR_CLK			SoundWire clock for WSA	
BC19	GPIO_176		PX701	PD:nppukp	Configurable I/O	Y
		LPASS_11			EGPIO - LPASS I/O 11	
		LPASS_11:LPI_I2S2_WS			LPI I2S 2 serial data word select	
		LPASS_11:WSA_SWR_DATA			SoundWire data for WSA	
BB16	GPIO_177		PX702	PD:nppukp	Configurable I/O	Y
		LPASS_12			EGPIO - LPASS I/O 12	
		LPASS_12:LPI_DMIC3_CLK			DMIC 3 clock	
		LPASS_12:LPI_I2S3_CLK			LPI I2S 3 clock	
BD14	GPIO_178		PX702	PD:nppukp	Configurable I/O	N
		LPASS_13			EGPIO - LPASS I/O 13	
		LPASS_13:LPI_DMIC3_DATA			DMIC 3 data	
		LPASS_13:LPI_I2S3_WS			LPI I2S 3 serial data word select	
		LPASS_13: EXT_MCLK1_A			External MCLK1 A	
BD25	GPIO_179		PX14	PD:nppukp	Configurable I/O	N
		LPASS_14			EGPIO - LPASS I/O 14	
		LPASS_14:SWR_TX_DATA2			SoundWire transmit data 2	
		LPASS_14: EXT_MCLK1_D			External MCLK1 D	
BD26	GPIO_180		PX701	PD:nppukp	Configurable I/O	N
		LPASS_15			EGPIO - LPASS I/O 15	
		LPASS_15:LPI_I2S2_DATA0			LPI I2S 2 serial data channel 0	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_15:WSA2_SWR_CLK			SoundWire clock for WSA	
BC26	GPIO_181		PX701	PD:nppukp	Configurable I/O	Y
		LPASS_16			EGPIO - LPASS I/O 16	
		LPASS_16:LPI_I2S2_DATA1			LPI I2S 2 serial data channel 1	
		LPASS_16:WSA2_SWR_DATA			SoundWire data for WSA	
BE14	GPIO_182	WSA0_EN	PX702	PD:nppukp	Configurable I/O	Y
		LPASS_17			EGPIO - LPASS I/O 17	
		LPASS_17:LPI_DMIC4_CLK			DMIC 4 clock	
		LPASS_17:LPI_I2S3_DATA0			LPI I2S 3 serial data channel 0	
BF14	GPIO_183	WSA2_EN	PX702	PD:nppukp	Configurable I/O	N
		LPASS_18			EGPIO - LPASS I/O 18	
		LPASS_18:LPI_DMIC4_DATA			DMIC 4 data	
		LPASS_18:LPI_I2S3_DATA1			LPI I2S 3 serial data channel 1	
BE24	GPIO_184		PX14	PD:nppukp	Configurable I/O	N
		LPASS_19			EGPIO - LPASS I/O 19	
		LPASS_19:LPI_I2S4_CLK			LPI I2S 4 clock	
		LPASS_19:SLIMBUS_CLK			SLIMbus clock	
BE26	GPIO_185		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_20			EGPIO - LPASS I/O 20	
		LPASS_20:LPI_I2S4_WS			LPI I2S 4 serial data word select	
		LPASS_20:SLIMBUS_DATA			SLIMbus data	
BC24	GPIO_186		PX14	PD:nppukp	Configurable I/O	N
		LPASS_21			EGPIO - LPASS I/O 21	
		LPASS_21:LPI_I2S4_DATA0			LPI I2S 4 serial data channel 0	
BC23	GPIO_187		PX14	PD:nppukp	Configurable I/O	Y
		LPASS_22			EGPIO - LPASS I/O 22	
		LPASS_22:LPI_I2S4_DATA1			LPI I2S 4 serial data channel 1	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPASS_22: EXT_MCLK1_E			External MCLK1 E	
BD22	GPIO_188		PX703	PD:nppukp	Configurable I/O	Y
		SSC_0			EGPIO - SSC I/O 0	
BE22	GPIO_189		PX703	PD:nppukp	Configurable I/O	N
		SSC_1			EGPIO - SSC I/O 1	
BE18	GPIO_190		PX703	PD:nppukp	Configurable I/O	Y
		SSC_2			EGPIO - SSC I/O 2	
BC21	GPIO_191		PX703	PD:nppukp	Configurable I/O	Y
		SSC_3			EGPIO - SSC I/O 3	
BD21	GPIO_192		PX703	PD:nppukp	Configurable I/O	Y
		SSC_4			EGPIO - SSC I/O 4	
BE21	GPIO_193		PX703	PD:nppukp	Configurable I/O	Y
		SSC_5			EGPIO - SSC I/O 5	
BB19	GPIO_194		PX703	PD:nppukp	Configurable I/O	N
		SSC_6			EGPIO - SSC I/O 6	
		SSC_6:SSC_QUPV3_SE2_2				
		SSC_6:SSC_QUPV3_SE4_4				
		SSC_6:SSC_GPIO_6_CLK				
BC20	GPIO_195		PX703	PD:nppukp	Configurable I/O	Y
		SSC_7			EGPIO - SSC I/O 7	
		SSC_7:SSC_QUPV3_SE2_3				
		SSC_7:SSC_QUPV3_SE4_5				
		SSC_7:SSC_GPIO_7_CLK				
BD20	GPIO_196		PX703	PD:nppukp	Configurable I/O	Y
		SSC_8			EGPIO - SSC I/O 8	
		SSC_8:SSC_QUPV3_SE3_0				
		SSC_8:SSC_QUPV3_SE2_4				

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	**Type**		
BE20	GPIO_197		PX703	PD:nppukp	Configurable I/O	Y
		SSC_9			EGPIO - SSC I/O 9	
		SSC_9:SSC_QUPV3_SE3_1				
		SSC_9:SSC_QUPV3_SE2_5				
BB20	GPIO_198		PX703	PD:nppukp	Configurable I/O	Y
		SSC_10			EGPIO - SSC I/O 10	
		SSC_10:SSC_QUPV3_SE4_0				
		SSC_10:SSC_GPIO_10_CLK				
BC18	GPIO_199		PX703	PD:nppukp	Configurable I/O	Y
		SSC_11			EGPIO - SSC I/O 11	
		SSC_11:SSC_QUPV3_SE4_1				
		SSC_11:SSC_GPIO_11_CLK				
BD17	GPIO_200		PX703	PD:nppukp	Configurable I/O	Y
		SSC_12			EGPIO - SSC I/O 12	
		SSC_12:SSC_QUPV3_SE4_2				
		SSC_12:SSC_GPIO_12_CLK				
BE17	GPIO_201		PX703	PD:nppukp	Configurable I/O	Y
		SSC_13			EGPIO - SSC I/O 13	
		SSC_13:SSC_QUPV3_SE4_3				
		SSC_13:SSC_GPIO_13_CLK				
BD18	GPIO_202		PX14	PD:nppukp	Configurable I/O	Y
		SSC_14			EGPIO - SSC I/O 14	
		SSC_14:SSC_QUPV3_SE5_2				
		SSC_14:SSC_QUPV3_SE5_0				
		SSC_14:SSC_GPIO_14_CLK				
BD23	GPIO_203		PX14	PD:nppukp	Configurable I/O	Y
		SSC_15			EGPIO - SSC I/O 15	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_15:SSC_QUPV3_SE5_3				
		SSC_15:SSC_QUPV3_SE5_1				
		SSC_15:SSC_GPIO_15_CLK				
BE23	GPIO_204		PX14	PD:nppukp	Configurable I/O	Y
		SSC_16			EGPIO - SSC I/O 16	
		SSC_16:SSC_QUPV3_SE6_2				
		SSC_16:SSC_QUPV3_SE6_0				
		SSC_16:SSC_QUPV3_SE10_2				
		SSC_16:SSC_GPIO_16_CLK				
BC22	GPIO_205		PX14	PD:nppukp	Configurable I/O	Y
		SSC_17			EGPIO - SSC I/O 17	
		SSC_17:SSC_QUPV3_SE6_3				
		SSC_17:SSC_QUPV3_SE6_1				
		SSC_17:SSC_QUPV3_SE10_3				
		SSC_17:SSC_GPIO_17_CLK				
BD16	GPIO_206		PX713	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE8_L0			I^2C hub 0 SE 8 lane 0	
		SSC_18			EGPIO - SSC I/O 18	
		SSC_18:SSC_QUPV3_SE7_0				
		SSC_18:SSC_GPIO_18_CLK				
BE16	GPIO_207		PX713	PD:nppukp	Configurable I/O	N
		I2CHUB0_SE8_L1			I^2C hub 0 SE 8 lane 1	
		SSC_19			EGPIO - SSC I/O 19	
		SSC_19:SSC_QUPV3_SE7_1				
		SSC_19:SSC_GPIO_19_CLK				
BB18	GPIO_208		PX703	PD:nppukp	Configurable I/O	N
		SSC_24			EGPIO - SSC I/O 24	

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pin number	Pin name	Configurable functions	Pin characteristics [a]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		SSC_24:SSC_QUPV3_SE10_0				
		SSC_24:SSC_GPIO_24_CLK				
BC17	GPIO_209		PX703	PD:nppukp	Configurable I/O	N
		SSC_25			EGPIO - SSC I/O 25	
		SSC_25:SSC_QUPV3_SE10_1				
		SSC_25:SSC_GPIO_25_CLK				

[a] See Table 2-1 for parameter and acronym definitions.

Table 2-4 MSM bottom pin descriptions: Power-supply pins

Pin number	Pin name	Functional description
A16, A24, BF16, BF24	LPDDR5_VDD1	Power for PoP LPDDR5 memory core
A4, A5, A6, A31, A32, A33, BF7, BF8, BF9, BF31, BF32, BF33	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core
A18, A19, A20, BF18, BF19, BF20	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core
A13, A14, A26, A27, BF11, BF12, BF26, BF27	LPDDR5_VDDQ	Power for PoP LPDDR5 memory core
AF12, AF14, AG13, AH12, AJ13, AK12, AL13, AM12, AN13, AP12, AR13, AT12, AU7, AU9, AU11, AU13, AV8, AV10, AV12, AW7, AW9, AW11, AW13	VDD_APC0	Power for the Kryo application processor
AG15, AG17, AG19, AH14, AH16, AH18, AH20, AJ15, AJ17, AJ19, AK14, AK18, AK20, AL19, AM14, AM18, AN19, AP14, AP18, AR15, AR17, AR19, AT14, AT16, AT18, AU15, AU17, AV14, AV16, AV18, AW15, AW17	VDD_APC1	Power for the Kryo application processor
AF8, AF10, AG7, AG9, AG11, AH8, AH10, AJ7, AJ11, AL7, AL11, AN7, AN11, AP8, AP10, AR7, AR9, AR11, AT8, AT10	VDD_APC2	Power for the Kryo application processor
AR14	VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits
G6	VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits
H6	VDD_A_CSI_01_1P2	Power for MIPI CSI01 1.2 V analog circuits
M6	VDD_A_CSI_24_0P9	Power for MIPI CSI24 0.9 V analog circuits
L6	VDD_A_CSI_24_1P2	Power for MIPI CSI24 1.2 V analog circuits
K6	VDD_A_CSI_35_0P9	Power for MIPI CSI35 0.9 V analog circuits
J6	VDD_A_CSI_35_1P2	Power for MIPI CSI35 1.2 V analog circuits
G16	VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits
H16	VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits
G15	VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V
F10, F11, F12	VDD_A_EBI_0	Power for EBI0 PHY
F13	VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits
BA10, BA11, BA12	VDD_A_EBI_1	Power for EBI1 PHY
BA13	VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits
F28, F29, F30	VDD_A_EBI_2	Power for EBI2 PHY
F31	VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits
BA28, BA29, BA30	VDD_A_EBI_3	Power for EBI3 PHY
BA31	VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits
AH35	VDD_A_EUSB_HS_1P2	Power for eUSB 1.2 V analog circuits
AH34	VDD_A_EUSB_HS_CORE	Power for eUSB core analog circuits
T34	VDD_A_GNSS_ADC_1P2	Power for GNSS ADC analog circuits
V21	VDD_A_NSP_CS_1P2	Power for NSP current sensor
AT6	VDD_A_PCIE_0_1P2	Power for PCIe0 1.2 V circuit
AW6	VDD_A_PCIE_0_CORE	Power for PCIe0 core

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
AP6	VDD_A_PCIE_1_1P2	Power for PCIe1 1.2 V circuit
AU6, AV6	VDD_A_PCIE_1_CORE	Power for PCIe1 core
P34, R34	VDD_A_QLINK_0_L_0P9	Power for QLink0 Port L (0.9 V)
N34	VDD_A_QLINK_0_L_CK_0P9	Power for QLink0 Port L clock circuit
K34, L34	VDD_A_QLINK_0_B_0P9	Power for QLink0 Port B (0.9 V)
K35	VDD_A_QLINK_0_B_1P2	Power for QLink0 Port B (1.2 V)
M34	VDD_A_QLINK_0_B_CK_0P9	Power for QLink0 Port B clock circuit
AY15	VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits
BA6	VDD_A_QREFS_0P875_0	Reference voltage for QREFS 0.875 V analog circuits
AY25	VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875 V analog circuits
BA35	VDD_A_QREFS_0P875_2	Reference voltage for QREFS 0.875 V analog circuits
AE34	VDD_A_QREFS_0P875_4	Reference voltage for QREFS 0.875 V analog circuits
V34	VDD_A_QREFS_0P875_5	Reference voltage for QREFS 0.875 V analog circuits
AB34, AY16	VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V analog circuits
AY7	VDD_A_SP_SENSOR	
AL35	VDD_A_UFS_1P2	Power for UFS 1.2 V circuits
AJ36, AK35, AL36	VDD_A_UFS_CORE	Power for UFS core circuits
AG35	VDD_A_USB_SS_DP_1P2	Power for the USB super-speed and DisplayPort high-speed 1.2 V analog circuits
AG34	VDD_A_USB_SS_DP_CORE	Power for the USB super-speed and DisplayPort high-speed core analog circuits
AA19, AA21, AA23, AB18, AB20, AB22, AF7, AF34, AY8, BA22, J17, L17, N15, N17, P16, P26, R15, R25, T16, T26, U15, U25, V16, V24, V26, W15, W17, W19, W21, W23, W25, Y18, Y20, Y22, Y24	VDD_CX	Power for digital core circuits
G11	VDD_D_EBI_0	Power for EBI0 digital circuits
AY11	VDD_D_EBI_1	Power for EBI1 digital circuits
G29	VDD_D_EBI_2	Power for EBI2 digital circuits
AY29	VDD_D_EBI_3	Power for EBI3 digital circuits
AA31, AA33, AB28, AB30, AB32, AC27, AC29, AC31, AC33, AE27, AE33, AG27, AG33, AH26, AJ25, AJ27, AJ33, AK26, AK28, AK30, AK32, AK34, AL25, AL27, AL29, AL31, AL33, AM24, AM26, AM28, AM30, AM32, AM34, AN23, AN25, AN27, AN33, AP22, AP26, AP34, AR27, AR33, AT22, AT26, AT34, AU27, AU33, AV22, AV26, AW23, AW25, AW27, AW29, AW31, AW33, AY22, AY24, AY26, AY32, AY34, BA23, BA33	VDD_GFX	Power for graphics

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
G9, G10, G12, G13	VDD_IO_EBI_0	Power for the EBI_0 I/O circuits
AY9, AY10, AY12, AY13	VDD_IO_EBI_1	Power for the EBI_1 I/O circuits
G27, G28, G30, G31	VDD_IO_EBI_2	Power for the EBI_2 I/O circuits
AY27, AY28, AY30, AY31	VDD_IO_EBI_3	Power for the EBI_3 I/O circuits
AB6, AM6, AR35, AU35, BA16, BA26, BB7, Y6, Y34	VDD_IX	Power for dual voltage pins (0.9 V)
AB16, AE16, AE18, AV19, AY17, AY19, Y16	VDD_LPI_CX	Power for LPI digital core circuits
AA17, AC17, AD18, AE19, AG20, AH23, AK23, AL22, AU18, AY6	VDD_LPI_MX	Power for low-power island memory circuits
W33	VDD_LPI_MX_NAV	Power for low-power island on chip memory-NAV
AA7, AA9, AA11, AA13, AB8, AB10, AB12, AC7, AC9, AC11, AC13, AD8, AD10, G7, H8, H10, H12, H14, J9, J11, J13, J15, K8, K10, K12, K14, K16, L9, L11, L13, L15, M8, M10, M12, M14, M16, N7, N9, N11, N13, P8, P10, P12, R7, R9, R11, R13, T8, T10, T12, U7, U9, U11, U13, V8, V10, V12, W7, W9, W11, W13, Y8, Y10, Y12	VDD_MM	Power for multimedia subsystem circuits
F32, G33, G35, H28, H30, H32, H34, J27, J35, K28, K32, L27, L33, M28, M32, N27, N33, P28, P30, P32, R27, R29, R31, R33, T28, T30, T32, U27, U29, U31, U33, V28, V30, V32, W27, W29	VDD_MODEM	Power for modem circuits
AD12, AD14, AD16, AD20, AD22, AE7, AE9, AE11, AE13, AE15, AE17, AE21, AF16, AF18, AF20, AF22, AG21, AH22, AJ21, AK22, AL21, AM20, AP20, AT20, AU19, AV13, AV20, J33	VDD_MX_A	Power for memory circuits
AA25, AA27, AA29, AB14, AB24, AB26, AC23, AC25, AD24, AD26, AD34, AE23, AE25, AF24, AG23, AG25, AH24, AJ23, AJ34, AK24, AL23, AL34, AM22, AN21, AN34, AR21, AR34, AU21, AU34, AV34, AW21, F34, G17, H17, J18, P14, T14, V14, W31, Y14, Y26, Y28, Y30, Y32	VDD_MX_C	Power for memory circuits
J19, K18, L19, M18, N19, P18, P20, P22, P24, R17, R23, T24, U17, U23, V18, V20, V22	VDD_NSP1	Power for NSP circuits
B24, B26, C23, C25, C27, D24, D26, E23, E25, E27, F18, F20, F22, F24, F26, G19, H18, H20, H26, K20, K26, M20, M26, N21, N23, N25	VDD_NSP2	Power for NSP circuits
BA20	VDD_PX0	Power for pin group 0
AP36	VDD_PX10	Power for pin group 10
BA15	VDD_PX11	Power for pin group 11
BA9	VDD_PX13	Power for pin group 13
AE6, AN6, AP35, BA8, BA14, BA19, BA21, F7, V6, W34	VDD_PX14	Power for pin group 14

Table 2-4 MSM bottom pin descriptions: Power-supply pins (cont.)

Pin number	Pin name	Functional description
BA25	VDD_PX701	Power for pin group 701
BB15	VDD_PX702	Power for pin group 702
BA17	VDD_PX703	Power for pin group 703
AL6	VDD_PX704	Power for pin group 704
W6	VDD_PX705	Power for pin group 705
AA6	VDD_PX706	Power for pin group 706
AC6	VDD_PX707	Power for pin group 707
AT35	VDD_PX708	Power for pin group 708
AC34	VDD_PX709	Power for pin group 709
AK6	VDD_PX710	Power for pin group 710
AV35	VDD_PX711	Power for pin group 711
AW35	VDD_PX712	Power for pin group 712
BB14	VDD_PX713	Power for pin group 713
BB8	VDD_PX714	Power for pin group 714
AA34	VDD_PX715	Power for pin group 715
BA7	VDD_QFPROM	Power for programming the QFPROM
BB6	VDD_QFPROM_SP	Power for programming the QFPROM for secure Processor Unit

Table 2-5 MSM bottom pin descriptions: Ground pins

Pin number	Pin name	Functional description
A7, A9, A11, A12, A15, A17, A21, A23, A25, A28, A30, A34, A35, A36, AA8, AA10, AA12, AA14, AA15, AA16, AA18, AA20, AA24, AA26, AA28, AA30, AA32, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AB25, AB27, AB29, AB31, AB33, AC8, AC10, AC12, AC14, AC15, AC16, AC18, AC19, AC20, AC21, AC22, AC24, AC26, AC28, AC30, AC32, AD6, AD7, AD9, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD25, AD27, AD33, AD36, AE8, AE10, AE12, AE14, AE20, AE22, AE24, AE26, AE35, AE37, AE38, AE39, AF4, AF5, AF11, AF13, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AF33, AF35, AF38, AG8, AG12, AG14, AG18, AG22, AG26, AG37, AG38, AH7, AH9, AH11, AH13, AH15, AH19, AH21, AH25, AH27, AH33, AH36, AH39, AJ4, AJ5, AJ6, AJ12, AJ14, AJ16, AJ18, AJ20, AJ22, AJ24, AJ35, AJ37, AK7, AK11, AK13, AK19, AK21, AK25, AK29, AK31, AK33, AK36, AK39, AL12, AL14, AL18, AL20, AL24, AL26, AL28, AL30, AL32, AL37, AM7, AM11, AM13, AM19, AM21, AM23, AM25, AM27, AM29, AM31, AM33, AM35, AM38, AM39, AN12, AN14, AN18, AN20, AN22, AN24, AN26, AN35, AN36, AN37, AP7, AP9, AP11, AP13, AP19, AP21, AP27, AP33, AP37, AP38, AP39, AR6, AR8, AR10, AR12, AR16, AR18, AR20, AR22, AR26, AR36, AT2, AT7, AT11, AT13, AT15, AT17, AT19, AT21, AT27, AT33, AT36, AT37, AT39, AU1, AU3, AU5, AU10, AU12, AU14, AU16, AU20, AU22, AU26, AU38, AV3, AV5, AV7, AV9, AV11, AV15, AV17, AV21, AV27, AV33, AW3, AW4, AW8, AW10, AW12, AW16, AW18, AW19, AW20, AW22, AW24, AW26, AW28, AW30, AW32, AW34, AY2, AY3, AY14, AY18, AY21, AY23, AY33, AY35, B2, B3, B4, B5, B6, B7, B9, B11, B12, B14, B16, B18, B20, B22, B23, B25, B27, B28, B29, B31, B32, B33, B34, B35, B36, B37, B38, BA1, BA2, BA3, BA4, BA18, BA24, BA27, BA32, BA34, BB1, BB3, BB5, BB9, BB10, BB11, BB12, BB13, BB21, BB22, BB23, BB25, BB26, BB27, BB28, BB29, BB30, BB31, BB32, BB33, BB34, BC3, BC6, BC12, BC13, BC14, BC15, BC28, BC31, BC32, BC33, BC34, BD3, BD5, BD6, BD11, BD28, BD29, BD30, BD31, BD33, BD34, BE2, BE3, BE4, BE7, BE8, BE9, BE11, BE13, BE28, BE30, BE32, BE33, BE34, BE35, BE38, BF4, BF6, BF10, BF13, BF15, BF17, BF21, BF23, BF25, BF28, BF30, BF34, BF35, C6, C7, C11, C13, C14, C16, C18, C20, C22, C24, C26, C28, C29, C30, C31, C33, C35, C37, D1, D2, D3, D6, D7, D11, D12, D13, D18, D23, D25, D27, D28, D29, D30, D38, D39, E1, E6, E7, E8, E9, E10, E11, E12, E13, E18, E28, E29, E30, E31, E32, E34, E36, E38, F5, F6, F8, F9, F14, F15, F16, F17, F19, F21, F23, F25, F27, F33, F35, F37, G1, G2, G5, G8, G14, G18, G20, G26, G32, G34, G38, H5, H7, H9, H11, H13, H15, H19, H27, H29, H31, H33, H35, H37, H39, J1, J7, J8, J10, J12, J14, J16, J20, J26, J28, J34, J36, K1, K2, K3, K7, K9, K11, K13, K15, K17, K19, K27, K33, K36, K37, K38, K39, L1, L7, L10, L12, L14, L16, L18, L20, L26, L28, L35, M5, M7, M9, M11, M13, M15, M17, M19, M27, M33, M35, M36, M37, N1, N2, N5, N6, N8, N10, N12, N14, N16, N18, N20, N22, N24, N26, N28, N32, N37, P5, P6, P7, P9, P11, P13, P15, P17, P19, P21, P23, P25, P27, P29, P31, P33, P35, P36, P37, R1, R6, R8, R10, R12, R14, R16, R24, R26, R28, R30, R32, R37, T1, T2, T3, T6, T7, T9, T11, T13, T15, T17, T23, T25, T27, T29, T31, T33, T35, T36, T37, U1, U6, U8, U10, U12, U14, U16, U24, U26, U28, U30, U32, U34, V2, V4, V5, V7, V9, V11, V13, V15, V23, V25, V27, V29, V31, V33, W8, W10, W12, W14, W16, W18, W20, W22, W24, W26, W28, W30, W32, Y7, Y9, Y11, Y13, Y15, Y17, Y19, Y21, Y23, Y25, Y27, Y29, Y31, Y33	GND	Ground

Table 2-6 MSM bottom pin descriptions: Not connected pins

Pin number	Pin name	Functional description
AR3, AR2, AU8, AG16, AG10, AK27, L32, V17, E26, C12, BD12, B30, BE31, AT4, BE5, AD38, V3, AT9, AH17, AF9, AA22, AJ26, AG24, L8, J32, AW14, AF26, V19, E24, AY20, E14, D14	DNC	Do not connect; connected internally, do not connect externally.
A1, A2, A3, A37, A38, A39, B1, B39, BD1, BD39, BE1, BE39, BF1, BF2, BF3, BF37, BF38, BF39, C1, C39	NC	Do not connect; connected internally, do not connect externally.

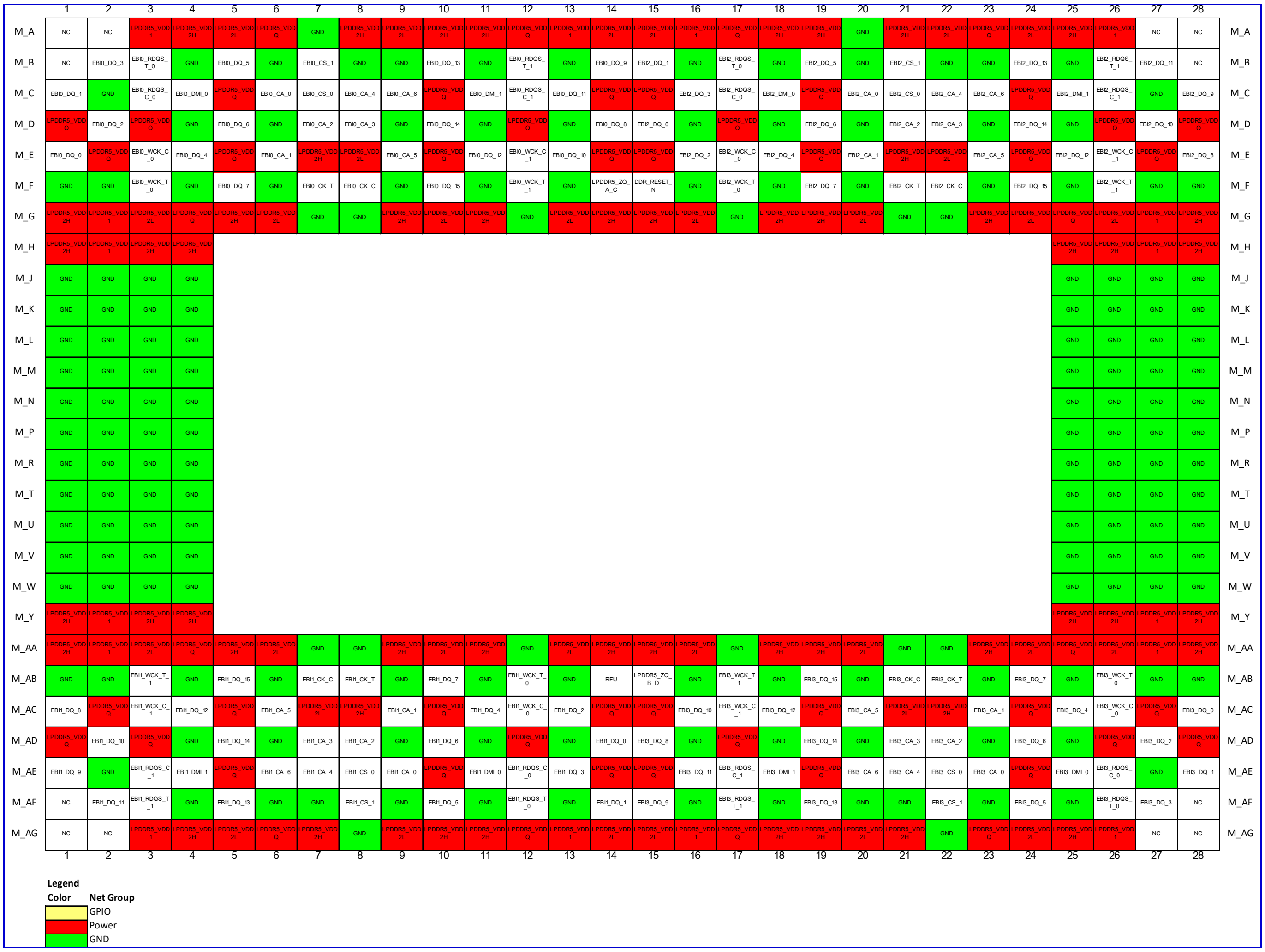
2.3 Pin assignments: MSM top

2.3.1 Pin map: MSM top

The SM8650/SM8650P is available in the MPSP1629. See Mechanical information for package details and Pin assignments: MSM bottom for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in below.

The text within the below image is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in Pin map: MSM bottom.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
M_A	NC	NC	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2L	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2H	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD1	NC	NC	M_A
M_B	NC	EBI0_DQ_3	EBI0_RDQS_T_0	GND	EBI0_DQ_5	GND	EBI0_CS_1	GND	GND	EBI0_DQ_13	GND	EBI0_RDQS_T_1	GND	EBI0_DQ_9	EBI2_DQ_1	GND	EBI2_RDQS_T_0	GND	EBI2_DQ_5	GND	EBI2_CS_1	GND	GND	EBI2_DQ_13	GND	EBI2_RDQS_T_1	EBI2_DQ_11	NC	M_B
M_C	EBI0_DQ_1	GND	EBI0_RDQS_C_0	EBI0_DMI_0	LPDDR5_VDDQ	EBI0_CA_0	EBI0_CS_0	EBI0_CA_4	EBI0_CA_6	LPDDR5_VDDQ	EBI0_DMI_1	EBI0_RDQS_C_1	EBI0_DQ_11	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI2_DQ_3	EBI2_RDQS_C_0	EBI2_DMI_0	LPDDR5_VDDQ	EBI2_CA_0	EBI2_CS_0	EBI2_CA_4	EBI2_CA_6	LPDDR5_VDDQ	EBI2_DMI_1	EBI2_RDQS_C_1	GND	EBI2_DQ_9	M_C
M_D	LPDDR5_VDDQ	EBI0_DQ_2	LPDDR5_VDDQ	GND	EBI0_DQ_6	GND	EBI0_CA_2	EBI0_CA_3	GND	EBI0_DQ_14	GND	LPDDR5_VDDQ	GND	EBI0_DQ_8	EBI2_DQ_0	GND	LPDDR5_VDDQ	GND	EBI2_DQ_6	GND	EBI2_CA_2	EBI2_CA_3	GND	EBI2_DQ_14	GND	LPDDR5_VDDQ	EBI2_DQ_10	LPDDR5_VDDQ	M_D
M_E	EBI0_DQ_0	LPDDR5_VDDQ	EBI0_WCK_C_0	EBI0_DQ_4	LPDDR5_VDDQ	EBI0_CA_1	LPDDR5_VDD2H	LPDDR5_VDD2L	EBI0_CA_5	LPDDR5_VDDQ	EBI0_DQ_12	EBI0_WCK_C_1	EBI0_DQ_10	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI2_DQ_2	EBI2_WCK_C_0	EBI2_DQ_4	LPDDR5_VDDQ	EBI2_CA_1	LPDDR5_VDD2H	LPDDR5_VDD2L	EBI2_CA_5	LPDDR5_VDDQ	EBI2_DQ_12	EBI2_WCK_C_1	LPDDR5_VDDQ	EBI2_DQ_8	M_E
M_F	GND	GND	EBI0_WCK_T_0	GND	EBI0_DQ_7	GND	EBI0_CK_T	EBI0_CK_C	GND	EBI0_DQ_15	GND	EBI0_WCK_T_1	GND	LPDDR5_ZQ_A_C	DDR_RESET_N	GND	EBI2_WCK_T_0	GND	EBI2_DQ_7	GND	EBI2_CK_T	EBI2_CK_C	GND	EBI2_DQ_15	GND	EBI2_WCK_T_1	GND	GND	M_F
M_G	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD2H	GND	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_G
M_H	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2H																					LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2H	M_H
M_J	GND	GND	GND	GND																					GND	GND	GND	GND	M_J
M_K	GND	GND	GND	GND																					GND	GND	GND	GND	M_K
M_L	GND	GND	GND	GND																					GND	GND	GND	GND	M_L
M_M	GND	GND	GND	GND																					GND	GND	GND	GND	M_M
M_N	GND	GND	GND	GND																					GND	GND	GND	GND	M_N
M_P	GND	GND	GND	GND																					GND	GND	GND	GND	M_P
M_R	GND	GND	GND	GND																					GND	GND	GND	GND	M_R
M_T	GND	GND	GND	GND																					GND	GND	GND	GND	M_T
M_U	GND	GND	GND	GND																					GND	GND	GND	GND	M_U
M_V	GND	GND	GND	GND																					GND	GND	GND	GND	M_V
M_W	GND	GND	GND	GND																					GND	GND	GND	GND	M_W
M_Y	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2H																					LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2H	M_Y
M_AA	LPDDR5_VDD2H	LPDDR5_VDD1	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD2H	GND	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2L	GND	GND	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDD2H	M_AA
M_AB	GND	GND	EBI1_WCK_T_1	GND	EBI1_DQ_15	GND	EBI1_CK_C	EBI1_CK_T	GND	EBI1_DQ_7	GND	EBI1_WCK_T_0	GND	RFU	LPDDR5_ZQ_B_D	GND	EBI3_WCK_T_1	GND	EBI3_DQ_15	GND	EBI3_CK_C	EBI3_CK_T	GND	EBI3_DQ_7	GND	EBI3_WCK_T_0	GND	GND	M_AB
M_AC	EBI1_DQ_8	LPDDR5_VDDQ	EBI1_WCK_C_1	EBI1_DQ_12	LPDDR5_VDDQ	EBI1_CA_5	LPDDR5_VDD2L	LPDDR5_VDD2H	EBI1_CA_1	LPDDR5_VDDQ	EBI1_DQ_4	EBI1_WCK_C_0	EBI1_DQ_2	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI3_DQ_10	EBI3_WCK_C_1	EBI3_DQ_12	LPDDR5_VDDQ	EBI3_CA_5	LPDDR5_VDD2L	LPDDR5_VDD2H	EBI3_CA_1	LPDDR5_VDDQ	EBI3_DQ_4	EBI3_WCK_C_0	LPDDR5_VDDQ	EBI3_DQ_0	M_AC
M_AD	LPDDR5_VDDQ	EBI1_DQ_10	LPDDR5_VDDQ	GND	EBI1_DQ_14	GND	EBI1_CA_3	EBI1_CA_2	GND	EBI1_DQ_6	GND	LPDDR5_VDDQ	GND	EBI1_DQ_0	EBI3_DQ_8	GND	LPDDR5_VDDQ	GND	EBI3_DQ_14	GND	EBI3_CA_3	EBI3_CA_2	GND	EBI3_DQ_6	GND	LPDDR5_VDDQ	EBI3_DQ_2	LPDDR5_VDDQ	M_AD
M_AE	EBI1_DQ_9	GND	EBI1_RDQS_C_1	EBI1_DMI_1	LPDDR5_VDDQ	EBI1_CA_6	EBI1_CA_4	EBI1_CS_0	EBI1_CA_0	LPDDR5_VDDQ	EBI1_DMI_0	EBI1_RDQS_C_0	EBI1_DQ_3	LPDDR5_VDDQ	LPDDR5_VDDQ	EBI3_DQ_11	EBI3_RDQS_C_1	EBI3_DMI_1	LPDDR5_VDDQ	EBI3_CA_6	EBI3_CA_4	EBI3_CS_0	EBI3_CA_0	LPDDR5_VDDQ	EBI3_DMI_0	EBI3_RDQS_C_0	GND	EBI3_DQ_1	M_AE
M_AF	NC	EBI1_DQ_11	EBI1_RDQS_T_1	GND	EBI1_DQ_13	GND	GND	EBI1_CS_1	GND	EBI1_DQ_5	GND	EBI1_RDQS_T_0	GND	EBI1_DQ_1	EBI3_DQ_9	GND	EBI3_RDQS_T_1	GND	EBI3_DQ_13	GND	GND	EBI3_CS_1	GND	EBI3_DQ_5	GND	EBI3_RDQS_T_0	EBI3_DQ_3	NC	M_AF
M_AG	NC	NC	LPDDR5_VDD1	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDDQ	LPDDR5_VDD2H	GND	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDDQ	LPDDR5_VDD1	LPDDR5_VDD2L	LPDDR5_VDD2L	LPDDR5_VDD1	LPDDR5_VDDQ	LPDDR5_VDD2H	LPDDR5_VDD2H	LPDDR5_VDD2L	LPDDR5_VDD2H	GND	LPDDR5_VDDQ	LPDDR5_VDD2L	LPDDR5_VDD2H	LPDDR5_VDD1	NC	NC	M_AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Legend

Color	Net Group
🟨	GPIO
🟥	Power
🟩	GND

Figure 2-3 SM8650 top pin LPDDR5 assignments (top view)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in Table 2-7 through Table 2-11

Table 2-7 MSM top pin descriptions – general pins

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_F15	DDR_RESET_N	PX_1	DO	LPDDR5 reset
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock (C)
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock (T)
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9
M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 (C)
M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 (C)
M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 (T)
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 (T)
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (C)
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (C)
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (T)
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (T)
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0
M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 1
M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5 command/address bit 2
M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 3
M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 4
M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 5
M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock (C)
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock (T)
M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5 chip select 0
M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5 chip select 1
M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR4X (and LPDDR5) data mask for byte 0

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR4X (and LPDDR5) data mask for byte 1
M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0
M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1
M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10
M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11
M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12
M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13
M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14
M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15
M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2
M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3
M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4
M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5
M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6
M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7
M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8
M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9
M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 (C)
M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 (C)
M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 (T)
M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 (T)
M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (C)
M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (C)
M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (T)
M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (T)
M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5 command/address bit 0
M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5 command/address bit 1

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5 command/address bit 2
M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5 command/address bit 3
M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5 command/address bit 4
M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5 command/address bit 5
M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5 differential clock (C)
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5 differential clock (T)
M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5 chip select 0
M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5 chip select 1
M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR4X (and LPDDR5) data mask for byte 0
M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR4X (and LPDDR5) data mask for byte 1
M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5 data bit 0
M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5 data bit 1
M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5 data bit 10
M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5 data bit 11
M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5 data bit 12
M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5 data bit 13
M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5 data bit 14
M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5 data bit 15
M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5 data bit 2
M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5 data bit 3
M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5 data bit 4
M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5 data bit 5
M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5 data bit 6
M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5 data bit 7
M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5 data bit 8
M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5 data bit 9

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 (C)
M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 (C)
M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 (T)
M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 (T)
M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (C)
M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (C)
M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (T)
M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (T)
M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5 command/address bit 0
M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5 command/address bit 1
M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5 command/address bit 2
M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5 command/address bit 3
M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5 command/address bit 4
M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5 command/address bit 5
M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5 differential clock (C)
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5 differential clock (T)
M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5 chip select 0
M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5 chip select 1
M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR4X (and LPDDR5) data mask for byte 0
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR4X (and LPDDR5) data mask for byte 1
M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5 data bit 0
M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5 data bit 1
M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5 data bit 10
M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5 data bit 11
M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5 data bit 12
M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5 data bit 13

Table 2-7 MSM top pin descriptions – general pins (cont.)

Pin number	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5 data bit 14
M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5 data bit 15
M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5 data bit 2
M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5 data bit 3
M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5 data bit 4
M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5 data bit 5
M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5 data bit 6
M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5 data bit 7
M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5 data bit 8
M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5 data bit 9
M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 (C)
M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 (C)
M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 (T)
M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 (T)
M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (C)
M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (C)
M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (T)
M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (T)
M_F14	LPDDR5_ZQ_A_C	-	Reference	ZQ calibration reference (channels A and C)
M_AB15	LPDDR5_ZQ_B_D	-	Reference	ZQ calibration reference (channels B and D)

[a] See Table 2-1 for parameter and acronym definitions

Table 2-8 MSM top pin descriptions – power-supply pins

Pin number	Pin name	Functional description
M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16, M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27	LPDDR5_VDD1	Power for PoP LPDDR5 memory core
M_A4, M_A8, M_A10, M_A11, M_A18, M_A19, M_A21, M_A25, M_AA1, M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_E21, M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_Y25, M_Y26, M_Y28	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core
M_A5, M_A9, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10, M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_G20, M_G24, M_G26	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core
M_A6, M_A12, M_A17, M_A23, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10, M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_E27, M_G4, M_G25	LPDDR5_VDDQ	Power for PoP LPDDR5 memory core

Table 2-9 MSM top pin descriptions – ground pins

Pin number	Pin name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground

Table 2-10 MSM top pin descriptions – not connected pins

Pin number	Pin name	Functional description
M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally.

Table 2-11 MSM top pin descriptions – reserved pins

Pin number	Pin name	Functional description
M_AB14	RFU	Reserved pins

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo application processor	-0.3	TBD	V
VDD_APC1	Qualcomm Kryo application processor	-0.3	TBD	V
VDD_APC2	Qualcomm Kryo application processor	-0.3	TBD	V
VDD_GFX	Power for graphics	-0.3	TBD	V
VDD_CX	Power for digital core circuits	-0.3	TBD	V
VDD_D_EBI_0	Power for EBI0 digital circuits			
VDD_D_EBI_1	Power for EBI1 digital circuits			
VDD_D_EBI_2	Power for EBI2 digital circuits			
VDD_D_EBI_3	Power for EBI3 digital circuits			
VDD_LPI_CX	Power for LPI digital core circuits	-0.3	TBD	V
VDD_LPI_MX	Power for low-power island memory circuits	-0.3	TBD	V
VDD_LPI_MX_NAV	Power for low-power island on chip memory-NAV	-0.3	TBD	V
VDD_MM	Power for multimedia subsystem circuits	-0.3	TBD	V
VDD_MODEM	Power for modem circuits	-0.3	TBD	V
VDD_MX_A	Power for memory circuits	-0.3	TBD	V
VDD_MX_C				
VDD_NSP1	Power for NSP circuits	-0.3	TBD	V
VDD_NSP2	Power for NSP circuits	-0.3	TBD	V
VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits	-0.3	TBD	V
VDD_A_CSI_24_0P9	Power for MIPI CSI24 0.9 V analog circuits			
VDD_A_CSI_35_0P9	Power for MIPI CSI35 0.9 V analog circuits			
VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits			
VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V			
VDD_A_PCIE_0_CORE	Power for PCIe0 core			
VDD_A_EUSB_0_CORE	Power for eUSB2 core circuits			
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits	-0.3	TBD	V
VDD_A_PCIE_1_CORE	Power for PCIe1 core	-0.3	TBD	V
VDD_A_UFS_CORE	Power for UFS core circuits	-0.3	TBD	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_QLINK_0_L_0P9	Power for QLink0 Port L (0.9 V)	-0.3	TBD	V
VDD_A_QLINK_0_L_CK_0P9	Power for QLink0 Port L clock circuit			
VDD_A_QLINK_0_B_0P9	Power for QLink0 Port B (0.9 V)	-0.3	TBD	V
VDD_A_QLINK_0_B_CK_0P9	Power for QLink0 Port B clock circuit			
VDD_A_EBI_0	Power for EBI0 digital circuits	-0.3	TBD	V
VDD_A_EBI_1	Power for EBI1 digital circuits			
VDD_A_EBI_2	Power for EBI2 digital circuits			
VDD_A_EBI_3	Power for EBI3 digital circuits			
VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits			
VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits			
VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits			
VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits			
VDD_A_USB_SS_DP_CORE	Power for the USB SuperSpeed and DisplayPort high-speed core analog circuits	-0.3	TBD	V
VDD_A_CSI_01_1P2	Power for MIPI CSI01 1.2 V analog circuits	-0.3	TBD	V
VDD_A_CSI_24_1P2	Power for MIPI CSI24 1.2 V analog circuits			
VDD_A_CSI_35_1P2	Power for MIPI CSI35 1.2 V analog circuits			
VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits			
VDD_A_PCIE_0_1P2	Power for PCIe0 1.2 V circuit			
VDD_A_PCIE_1_1P2	Power for PCIe1 1.2 V circuit			
VDD_A_EUSB_0_1P2	Power for eUSB2 1.2 V analog circuits			
VDD_A_UFS_1P2	Power for UFS 1.2 V circuits			
VDD_A_USB_SS_DP_1P2	Power for the USB SS and DisplayPort1.2 V analog circuits			
VDD_A_QLINK_0_B_1P2	Power for QLink0 Port B (1.2 V)			
VDD_PX0	Power for pin group 0 - control signals	-0.3	TBD	V
VDD_PX10	Power for pin group 10 - UFS0_REFCLK, UFS_RESET- 1.2 V	-0.3	TBD	V
VDD_PX11	Power for pin group 11 - CXO; 1.2 V	-0.3	TBD	V
VDD_PX13	Power for pin group 13 - SP_ARI_POWER_ALARM; 1.85 V	-0.3	TBD	V
VDD_PX14	Power for pin group 14 - SDC2, JTAG, UIM0, PS_HOLD, sleep clock, mode, modem, audio SWR - 1.2 V	-0.3	TBD	V
VDD_IX	Power for dual voltage pins (0.9 V)	-0.3	TBD	V
VDD_PX701 - VDD_PX715	Power for digital pad circuits - dual voltage* (1.2 V/1.8 V) * Per pad group, intended power supply should be connected properly, either 1.2 V or 1.8 V	-0.3	TBD	V
VDD_QFPROM	Power for programming the QFPROM	-0.3	TBD	V
VDD_QFPROM_SP	Power for programming the QFPROM for secure processor unit	-0.3	TBD	V
VDD_A_GNSS_ADC_1P2	Power for GNSS ADC analog circuits	-0.3	TBD	V
VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V analog circuits	-0.3	TBD	V
VDD_A_NSP_CS_1P2	Power for NSP current sensor			
VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits			
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits	-0.3	TBD	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_IO_EBI_0 VDD_IO_EBI_1 VDD_IO_EBI_2 VDD_IO_EBI_3 LPDDR5_VDDQ	Power for EBI0 digital circuits Power for EBI1 digital circuits Power for EBI2 digital circuits Power for EBI3 digital circuits Power for PoP LPDDR5 memory core [a]	-0.3	TBD	V
LPDDR5_VDD1	Power for PoP LPDDR5 memory core [a]	-0.3	TBD	V
LPDDR5_VDD2H	Power for PoP LPDDR5 memory core [a]	–	–	V
LPDDR5_VDD2L	Power for PoP LPDDR5 memory core [a]	–	–	V
T_S	Storage temperature [b] [c]	-55	150	°C
ESD protection - see Part reliability				
Thermal conditions - see Thermal characteristics				

[a] See the LPDDR5 standard (JESD209-5B) and vendor's data sheets for the absolute maximum DC ratings for minimum and maximum voltages of VDDQ, VDD1, VDD2H and VDD2L.

[b] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[c] For devices shipped in tape and reel, the storage temperature range is [-35°C to +15°C] and relative humidity (RH) < 90%. QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [a]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo application processor	TBD	TBD	V
VDD_APC1	Qualcomm Kryo application processor	TBD	TBD	V
VDD_APC2	Qualcomm Kryo application processor	TBD	TBD	V
VDD_GFX	Power for graphics	TBD	TBD	V
VDD_CX VDD_D_EBI_0 VDD_D_EBI_1 VDD_D_EBI_2 VDD_D_EBI_3	Power for digital core circuits Power for EBI0 digital circuits Power for EBI1 digital circuits Power for EBI2 digital circuits Power for EBI3 digital circuits	TBD	TBD	V
	Retention	TBD	TBD	V
VDD_LPI_CX	Power for LPI digital core circuits	TBD	TBD	V
VDD_LPI_MX	Power for low-power island memory circuits	TBD	TBD	V
VDD_LPI_MX_NAV	Power for low-power island on chip memory-NAV	TBD	TBD	V
VDD_MM	Power for multimedia subsystem circuits	TBD	TBD	V
VDD_MODEM	Power for modem circuits	TBD	TBD	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [a]		Min	Max	Unit
VDD_MX_A VDD_MX_C	Power for memory circuits	TBD	TBD	V
VDD_NSP1	Power for NSP circuits	TBD	TBD	V
VDD_NSP2	Power for NSP circuits	TBD	TBD	V
VDD_A_EBI_0	Power for EBI0 digital circuits	TBD	TBD	V
VDD_A_EBI_1	Power for EBI1 digital circuits			
VDD_A_EBI_2	Power for EBI2 digital circuits			
VDD_A_EBI_3	Power for EBI3 digital circuits			
VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL 0.9 V analog circuits			
VDD_A_EBI_1_PLL_0P9	Power for EBI1 PLL 0.9 V analog circuits			
VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL 0.9 V analog circuits			
VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL 0.9 V analog circuits			

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-3 Operating conditions for non AVS voltage rails

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits	0.844	0.88	0.92	V
VDD_A_CSI_24_0P9	Power for MIPI CSI24 0.9 V analog circuits				
VDD_A_CSI_35_0P9	Power for MIPI CSI35 0.9 V analog circuits				
VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits				
VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V				
VDD_A_PCIE_0_CORE	Power for PCIe0 core				
VDD_A_EUSB_0_CORE	Power for eUSB2 core circuits				
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits	0.846	0.88	0.935	V
VDD_A_PCIE_1_CORE	Power for PCIe1 core	0.844	0.88	0.92	V
VDD_A_UFS_CORE	Power for UFS core circuits	0.879	0.912	0.958	V
VDD_A_QLINK_0_L_0P9 VDD_A_QLINK_0_L_CK_0P9	Power for QLink0 Port L (0.9 V) Power for QLink0 Port L clock circuit	0.844	0.88	0.92	V
VDD_A_QLINK_0_B_0P9 VDD_A_QLINK_0_B_CK_0P9	Power for QLink0 Port B (0.9 V) Power for QLink0 Port B clock circuit	0.879	0.912	0.958	V
VDD_A_USB_SS_DP_CORE	Power for the USB SuperSpeed and DisplayPort high-speed core analog circuits	0.844	0.88	0.92	V
VDD_A_CSI_01_1P2	Power for MIPI CSI01 1.2 V analog circuits	1.157	1.2	1.26	V
VDD_A_CSI_24_1P2	Power for MIPI CSI24 1.2 V analog circuits				
VDD_A_CSI_35_1P2	Power for MIPI CSI35 1.2 V analog circuits				
VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits				
VDD_A_PCIE_0_1P2	Power for PCIe0 1.2 V circuit				
VDD_A_PCIE_1_1P2	Power for PCIe1 1.2 V circuit				
VDD_A_EUSB_0_1P2	Power for eUSB2 1.2 V analog circuits				
VDD_A_UFS_1P2	Power for UFS 1.2 V circuits				

Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
VDD_A_USB_SS_DP_1P2 VDD_A_QLINK_0_B_1P2	Power for the USB SS and DisplayPort1.2 V analog circuits Power for QLink0 Port B (1.2 V)	1.157	1.2	1.26	V
VDD_PX0	Power for pin group 0 - control signals	1.1	1.2	1.3	V
VDD_PX10	Power for pin group 10 - UFS0_REFCLK, UFS_RESET- 1.2 V	1.157	1.2	1.26	V
VDD_PX11	Power for pin group 11 - CXO; 1.2 V	1.17	1.2	1.29	V
VDD_PX13	Power for pin group 13 - SP_ARI_POWER_ALARM; 1.85 V	1.7	1.856	1.95	V
VDD_PX14	Power for pin group 14 - SDC2, JTAG, UIM0, PS_HOLD, sleep clock, mode, modem, audio SWR - 1.2 V	1.157	1.2	1.26	V
VDD_IX	Power for dual voltage pins (0.9 V)	0.87	0.9	0.945	V
VDD_PX701 - VDD_PX715	Power for digital pad circuits - dual voltage* (1.2 V/1.8 V)	1.157	1.2	1.3	V
	* Per pad group, intended power supply should be connected properly - either 1.2 V or 1.8 V	1.74	1.8	1.9	
VDD_QFPROM VDD_QFPROM_SP	Power for programming the QFPROM Power for programming the QFPROM for secure processor unit	1.7	1.8	1.9	V
VDD_A_GNSS_ADC_1P2	Power for GNSS ADC analog circuits	1.157	1.2	1.26	V
VDD_A_QREFS_1P2 VDD_A_NSP_CS_1P2 VDD_A_APC_CS_1P2	Reference voltage for QREFS 1.2 V analog circuits Power for NSP current sensor Power for application processor current sensor 1.2 V analog circuits	1.157	1.2	1.26	V
VDD_IO_EBI_0 VDD_IO_EBI_1 VDD_IO_EBI_2 VDD_IO_EBI_3 LPDDR5_VDDQ	Power for EBI0 digital circuits Power for EBI1 digital circuits Power for EBI2 digital circuits Power for EBI3 digital circuits Power for PoP LPDDR memory core [c]				
	LPDDR5 spec range 1 [d]	0.47	0.5	0.57	V
	LPDDR5 spec range 2 [e]	0.27	0.3	0.37	V
LPDDR5_VDD1	Power for PoP LPDDR memory core [c]	–	–	–	V
LPDDR5_VDD2H	Power for PoP LPDDR memory core [c]	–	–	–	V
LPDDR5_VDD2L	Power for PoP LPDDR memory core [c]	–	–	–	V

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

[b] Typical voltages represent the recommended output settings of the companion PMIC device.

[c] See the LPDDR5 standard (JESD209-5B) and vendor's data sheets for the recommended DC operating conditions (min/typ/max voltages and PDN specification) of VDD1/VDD2H/VDD2L/VDDQ

[d] LPDDR5 spec range 1 is intended for I/O operation with both ODT enabled and disabled.

[e] LPDDR5 spec range 2 is intended for I/O operation with ODT disabled.

3.2.1 Thermal conditions

Table 3-4 Thermal conditions

Parameter	Description	Min	Typ	Max	Units
T_J	Device operating junction temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8650/SM8650P Chipset Power Delivery Network Specification* (80-40938-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8650 with SDR875/SDR753 Linux Android Current Consumption Data Application Note* (80-40938-7A/80-40938-7B).

3.5 Digital logic characteristics

A digital I/O’s performance specification depends on its pad type,its usage,and/or its supply voltage:

- Some are dedicated for interconnections between the SM8650 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-5 DC specification of 1.8 V GPIOs (VDD_PX701 to VDD_PX715)

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PXN [a]	VDD_PXN [a] + 0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3	0.35 × VDD_PXN [a]	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PXN [a]	VDD_PXN [a] + 0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3	0.3 × VDD_PXN [a]	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	250	–	mV
I_{IH}	Input high leakage current [b]	–	2	μA
I_{IL}	Input low leakage current [b]	-2	–	μA
R_{PD}	Pull-down resistance	10 K	50 K	Ω
R_{PU}	Pull-up resistance	10 K	50 K	Ω
R_{KP}	Bus keeper resistor	10 K	50 K	Ω
Rpu_I2C	Pull-up resistance for I^2C	–	2.2	kΩ
V_{OH}	High-level output voltage	VDD_PXN [a] - 0.45	VDD_PXN [a]	V
V_{OL}	Low-level output voltage	0.0	0.45	V

[a] PXN, where N defines:

PX701 to PX715 pad group 701 to 715 (GPIOs) when configured as 1.8 V

[b] I_{IH} and I_{IL} values are based on characterization of corner devices over temperature.

Table 3-6 UFS REFLK, reset DC specification (VDD_PX10)

Parameter	Description	Min	Max	Units
V_{OL}	Low-level output voltage	0	0.25 × VDD_PX10	V
V_{OH}	High-level output voltage	0.75 × VDD_PX10	VDD_PX10	V

Table 3-6 UFS REFLK, reset DC specification (VDD_PX10) (cont.)

Parameter	Description	Min	Max	Units
$R_{PULL\text{-}UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL\text{-}DOWN}$	Pull-down resistance	20	–	kΩ
I_{LEAK}	Stand by leakage	-10	10	µA

Table 3-7 1.2 V DC specification (VDD_PX14, VDD_PX701 to VDD_PX715)

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, (HIHYS_EN = LOW)	0.65 × VDD_PXN [a]	VDD_PXN [a] + 0.3	V
V_{IL}	Low-level input voltage (HIHYS_EN = LOW)	-0.3	0.35 × VDD_PXN [a]	V
V_{IH}	High-level input voltage, (HIHYS_EN = HIGH)	0.7 × VDD_PXN [a]	VDD_PXN [a] + 0.3	V
V_{IL}	Low-level input voltage (HIHYS_EN = HIGH)	-0.3	0.3 × VDD_PXN [a]	V
V_{SHYS}	Schmitt hysteresis (HIHYS_EN = LOW)	100	–	mV
V_{SHYS}	Schmitt hysteresis (HIHYS_EN = HIGH)	200	–	mV
I_{IH}	Input high leakage current [b]	–	2	µA
I_{IL}	Input low leakage current [b]	-2	–	µA
R_{PU}	Pull-up resistance	10 K	50 K	Ω
R_{PD}	Pull-down resistance	10 K	50 K	Ω
R_{KP}	Bus keeper resistor	10 K	50 K	Ω
Rpu_I2C	Pull-up resistance for I^2C	–	2.2	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_PXN [a]	VDD_PXN [a]	V
V_{OL}	Low-level output voltage	0	0.25 × VDD_PXN [a]	V

[a] PXN, where N defines:

PX14 pad group 14 (SDC2, JTAG, UIM0, PS_HOLD, SLEEP_CLK, MODE): 1.2 V

PX701 to PX715 pad group 701 to 715 (GPIOs) when configured as 1.2 V

[b] I_{IH} and I_{IL} values are based on characterization of corner devices over temperature.

NOTE Table 3-8 is applicable to SPMI0_CLK and SPMI0_DATA only.

Table 3-8 DC specification of 1.2 V SPMI (VDD_PX0)

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, (HIHYS_EN = LOW)	0.65 × VDD_PX0	VDD_PX0 + 0.3	V
V_{IL}	Low-level input voltage (HIHYS_EN = LOW)	-0.3	0.35 × VDD_PX0	V
V_{IH}	High-level input voltage, (HIHYS_EN = HIGH)	0.7 × VDD_PX0	VDD_PX0 + 0.3	V
V_{IL}	Low-level input voltage (HIHYS_EN = HIGH)	-0.3	0.3 × VDD_PX0	V
V_{SHYS}	Schmitt hysteresis (HIHYS_EN = LOW)	100	–	mV
V_{SHYS}	Schmitt hysteresis (HIHYS_EN = HIGH)	200	–	mV
I_{IH}	Input high leakage current [a]	–	5	µA
I_{IL}	Input low leakage current [a]	-5	–	µA
R_{PU}	Pull-up resistance	10 K	50 K	Ω
R_{PD}	Pull-down resistance	10 K	50 K	Ω
R_{KP}	Bus keeper resistor	10 K	50 K	Ω

Table 3-8 DC specification of 1.2 V SPMI (VDD_PX0) (cont.)

Parameter	Description	Min	Max	Units
V_{OH}	High-level output voltage	0.75 × VDD_PX0	VDD_PX0	V
V_{OL}	Low-level output voltage	0	0.25 × VDD_PX0	V

[a] I_{IH} and I_{IL} values are based on characterization of corner devices over temperature.

3.6 Timing characteristics

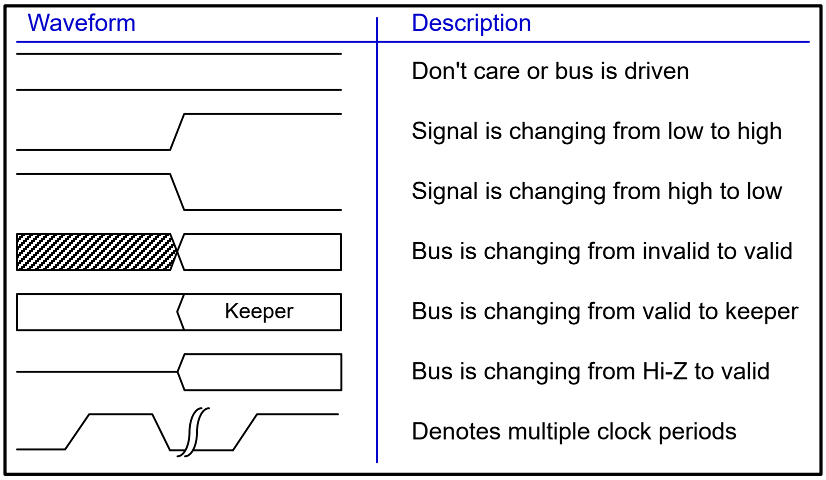
Specifications for the device timing characteristics are included (where appropriate) under each function’s section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM8650 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Rise and fall time specifications.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the figure below.

Figure 3-1 Timing diagram conventions



For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don’t care.

3.6.2 Rise and fall time specifications

The testers that characterize SM8650 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the figure below.

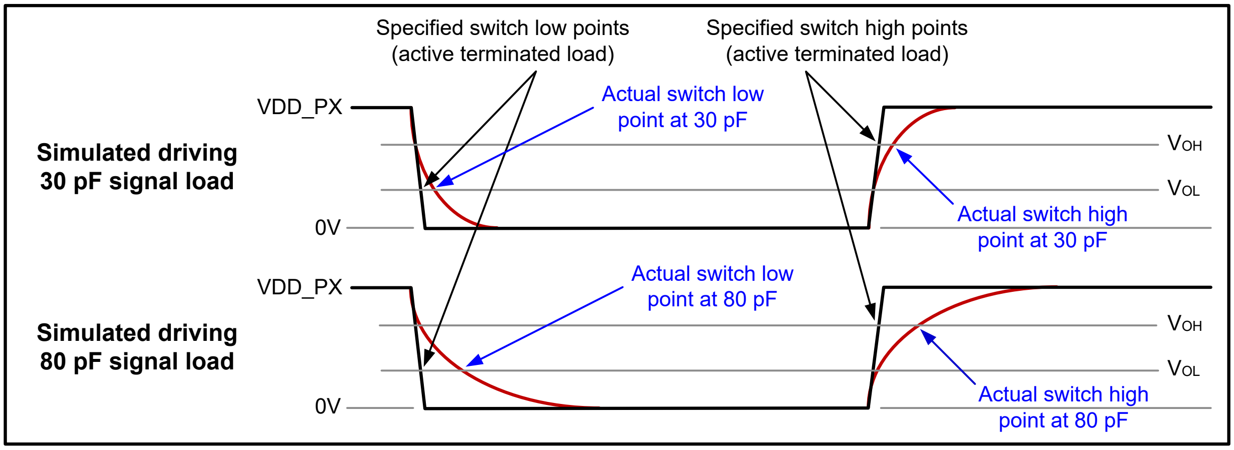


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8650 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SM8650 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated VDDPX_x supply (Figure 3-3). The input switch point for pure input-only pads is designed to be VDDPX_x/2 (or 50% of VDDPX_x). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of VDDPX_x for VIL and 65% of VDDPX_x for VIH.

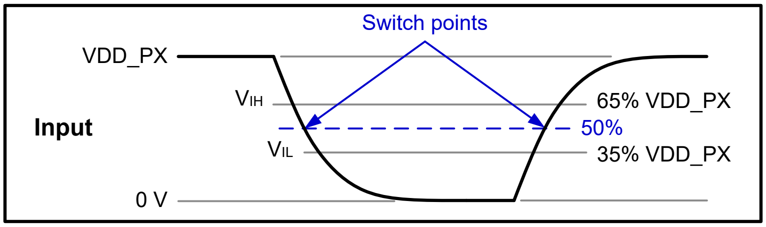


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL} (max) levels over worst-case process/voltage/ temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- VOH ~ VDDPX_x - 50 mV or more
- VOL ~ 50 mV or less

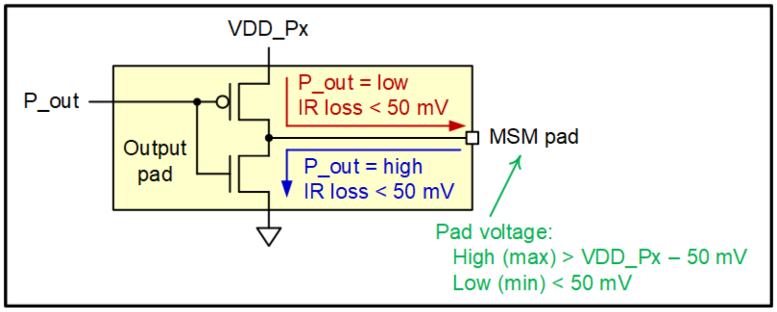


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and VDDPX_x - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [VDDPX_x - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (T_{RISE}) and fall time (T_{FALL}) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7 Memory support

The EBI0, EBI1, EBI2, and EBI3 ports are dedicated to the PoP LPDDR5X SDRAM memory that is attached to the top of the SM8650 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8650 Recommendations* (80-VP300-22).

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SM8650 device supports up to six D-PHY or C-PHY camera interfaces.

Table 3-9 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v3.0	Following features are not supported: ▪ Raw6/7 data formats ▪ All DPCM formats ▪ LRTE with EPD over D-PHY ▪ EoTp

Table 3-9 Supported MIPI_CSI standards and exceptions (cont.)

Applicable standard	Feature exceptions
	■ USL ■ sROI
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v2.0	Following features are not supported: ■ Bidirectional lanes ■ Alternate low power (ALP) mode

3.8.2 Audio support

The SM8650 supports the WCD9395 audio codec IC to provide the system's audio functions. SM8650 audio-related interface options with the WCD include:

- Digital microphone: Section 3.9.7
- SWR: SoundWire (SWR) interface
- I^{2}S: I^{2}S interfaces
- PCM/TDM: Section 3.9.11
- I^{2}C/I3C: Section 3.9.13
- SPI: Section 3.9.14

See the *Qualcomm Aqstic WCD9395 Data Sheet* (80-42519-1) for performance characteristics.

3.8.3 Display support

The SM8650 device supports up to two D-PHY or C-PHY displays.

Table 3-10 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface v1.3.1	Following features are not supported: ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission
MIPI Alliance Specification for Display Serial Interface 2 v2.0	Following features are not supported: ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission ■ Packed pixel stream, 20-bit YCbCr 4:2:2 format
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

3.9 Connectivity

The connectivity functions supported by the SM8650 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral component interconnect express (PCIe) interfaces
- Digital microphone PDM interface
- SoundWire (SWR) interface
- Serial low-power interchip media bus (SLIMbus) interface
- Inter-IC sound (I2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Touchscreen connections
- Through proper configuration of the QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Interintegrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - Improved interintegrated circuit (I3C) interfaces

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

Table 3-11 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical layer specification version 3.0	TBD
SDIO card specification version 3.0	TBD

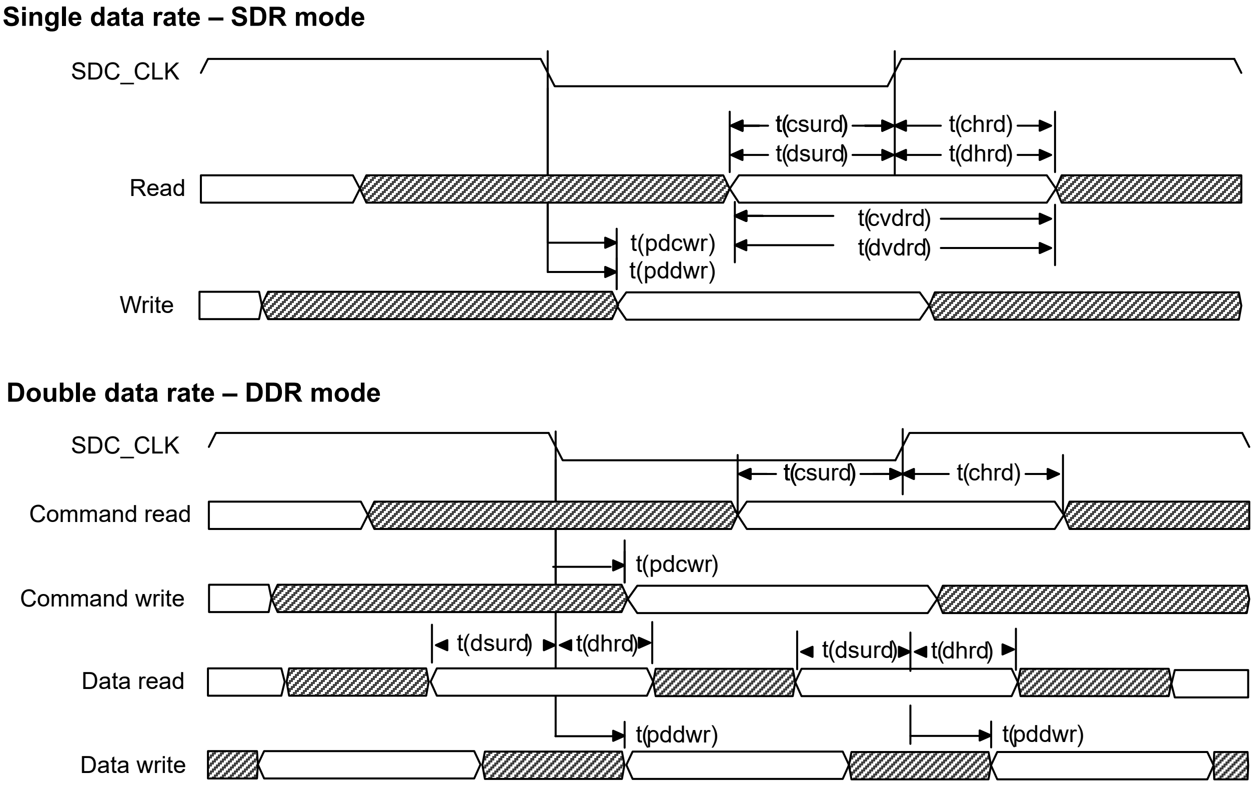


Figure 3-5 SD interface timing

NOTE SD interface timing parameters can be found at the standards mentioned above.

3.9.2 USB interfaces

Table 3-12 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	U1 and U2 stages are not enabled in USB3 Gen1 and Gen2 device mode due to interoperability concerns
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)
Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 1.1 Specification	None

3.9.3 DisplayPort

Table 3-13 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4a	None

3.9.4 PCIe interface

Table 3-14 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Base Specification Revision 3.0	None
PCI Express Base Specification Revision 4.0	None

3.9.5 UFS interface

Table 3-15 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None
Universal Flash Storage (UFS), Version 4.0	None

3.9.6 UIM interface

Table 3-16 Supported UIM standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.7 Digital microphone PDM interface

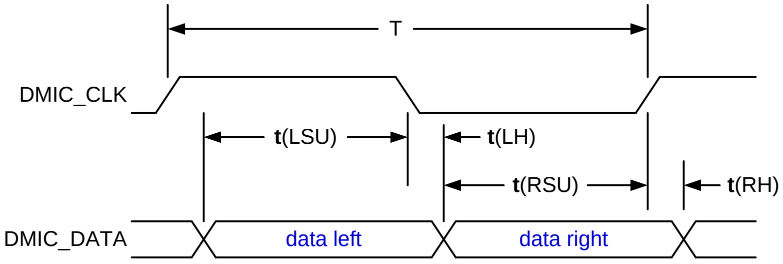


Figure 3-6 Digital microphone PDM interface timing

Table 3-17 Digital microphone timing

Parameter		Min	Typ	Max	Units
1/T	DMIC clock frequency	0.6	–	12.288	MHz
	DMIC clock duty cycle	45	–	55	%
t(LSU)	Data left setup time to clock falling edge	10	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	ns

3.9.8 SoundWire (SWR) interface

This information will be included in future revisions of this document.

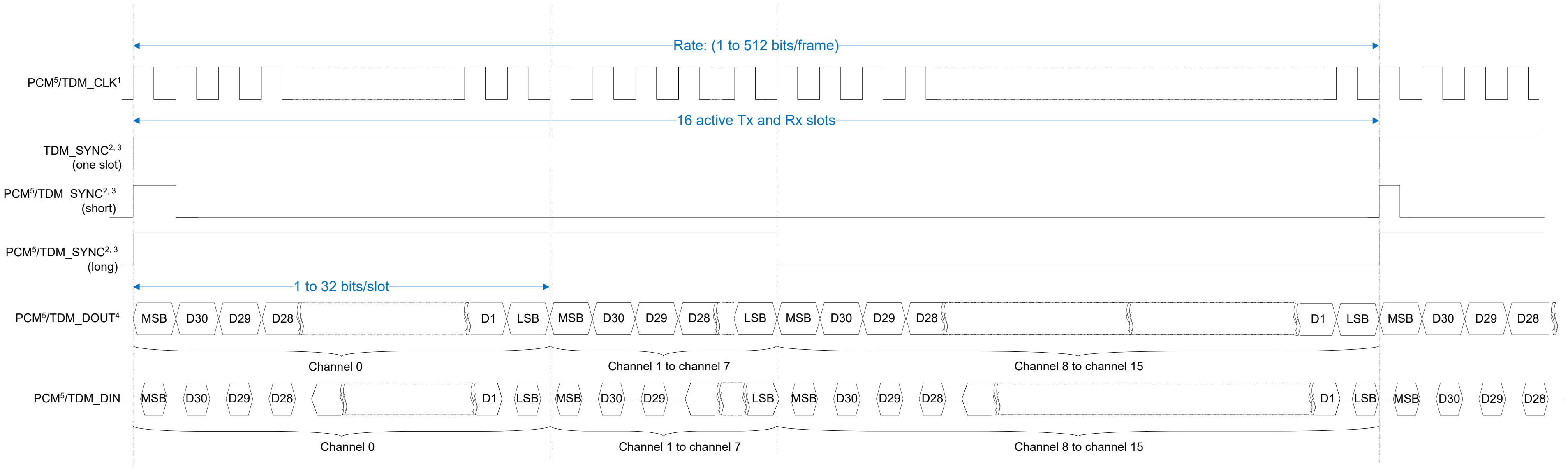
3.9.9 SLIMbus interface

This information will be included in future revisions of this document.

3.9.10 I^{2}S interfaces

This information will be included in future revisions of this document.

3.9.11 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-7 PCM/TDM audio format with different sync modes

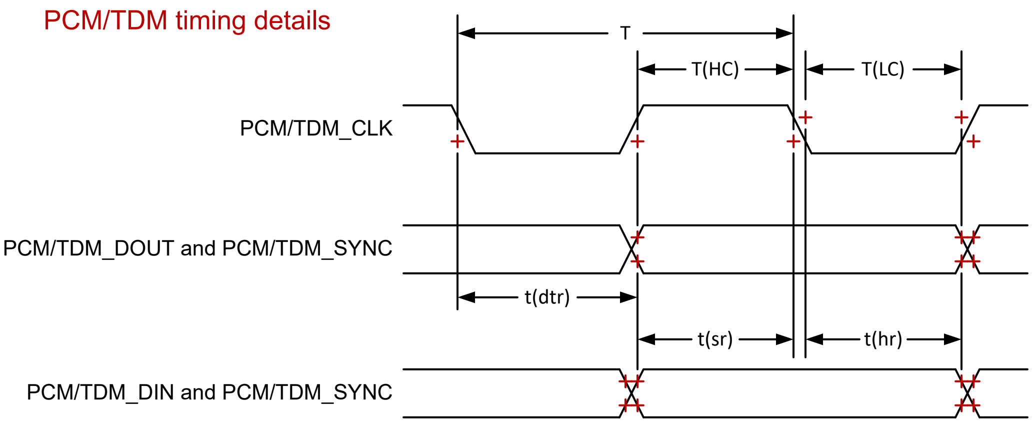


Figure 3-8 PCM/TDM timing diagram

Table 3-18 PCM/TDM interface timing parameters

Parameter		Comments [a]	Min	Max	Unit
Master mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns
Slave mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns

[a] Load capacitance is between 10 pF to 40 pF

3.9.12 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (I^{2}C/I3C interface) and GPIOs configured as discrete digital inputs (Digital logic characteristics). Additional specifications are not required.

3.9.13 I^2C/I3C interface

Table 3-19 Supported I^2C/I3C standards and exceptions

Applicable standard	Feature exceptions
I^2C specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.9.14 Serial peripheral interface

The SM8650 supports SPI as a master only. Any one of the QUP ports can be configured as an SPI master.

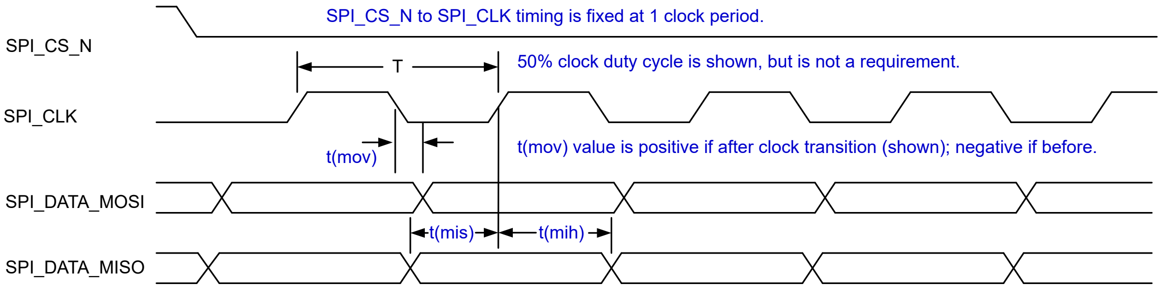


Figure 3-9 SPI master timing diagram

Table 3-20 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Units
T (SPI clock period) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 38.4 MHz CXO input

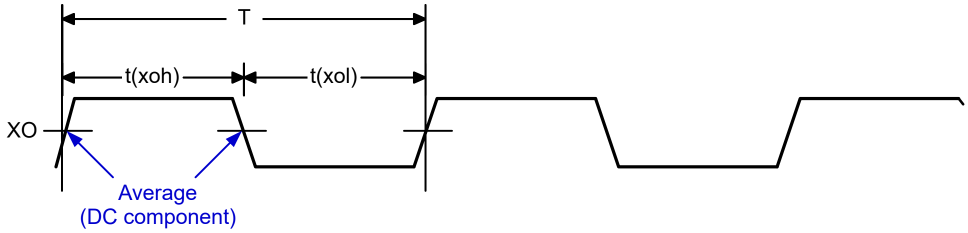


Figure 3-10 XO timing parameters

Table 3-21 CXO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	11.5	–	14.5	ns
t(xol)	XO logic low	–	11.5	–	14.5	ns
T	XO clock period	–	–	26.042	–	ns
1/T	Frequency	38.4 MHz must be used	–	38.4	–	MHz

[a] See Section 3.6.2 *76.8 MHz XO crystal requirements* of *PMK8550 Data Sheet* (80-33270-1) for more information.

3.10.1.2 Sleep clock

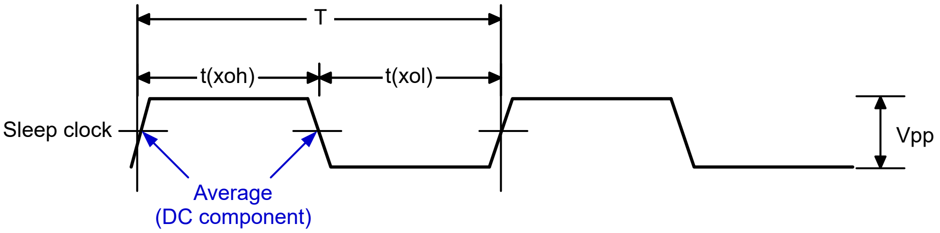


Figure 3-11 Sleep-clock timing parameters

Table 3-22 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	μs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	μs
T	Sleep-clock period	–	–	30.521	–	μs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Digital logic characteristics.

3.10.3 JTAG

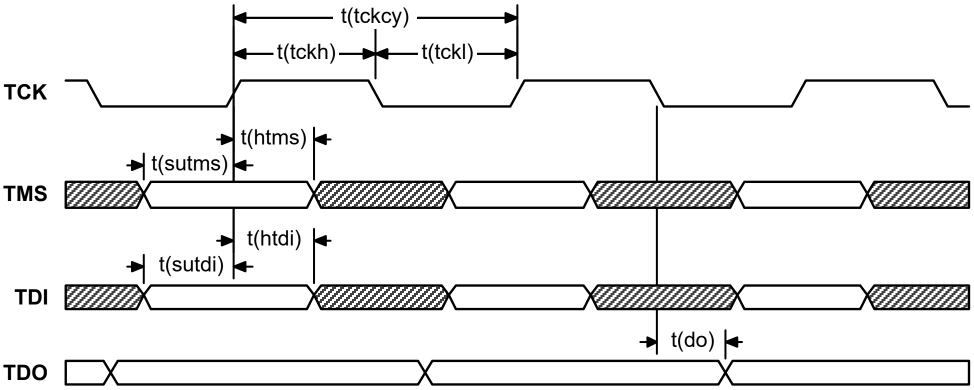


Figure 3-12 JTAG interface timing diagram

Table 3-23 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)ns	TDO data output delay	–	–	15	ns

3.10.4 SWD

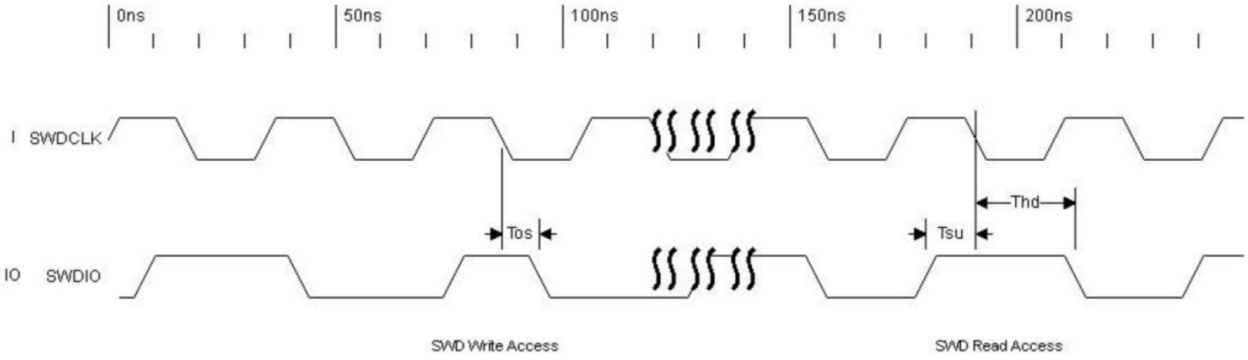


Figure 3-13 SWD write and read AC timing diagram

Table 3-24 SWD write and read AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T-7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	4	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	1	–	ns

NOTE SWDCLK runs at 20 MHz or lower.

3.11 Power management interface

The digital I/Os must meet the logic-level requirements specified in Digital logic characteristics.

3.11.1 System power management interface (SPMI)

Table 3-25 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM8650/SM8650P device is available in the MPSP1629 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1629 has a 16.5 mm by 14.0 mm body, with a maximum height of 0.56 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1629 outline drawing is shown in Figure 4-1.

NOTE Click the following link to download the *Package Outline Drawing, MPSP1629, 16.5 × 14.0 × 0.56 mm, ST94, M147, SB130, NSPPB 496, PL1, MEP* (NT90-16783-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-16783-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the Related Files line that is located directly underneath the PDF link.

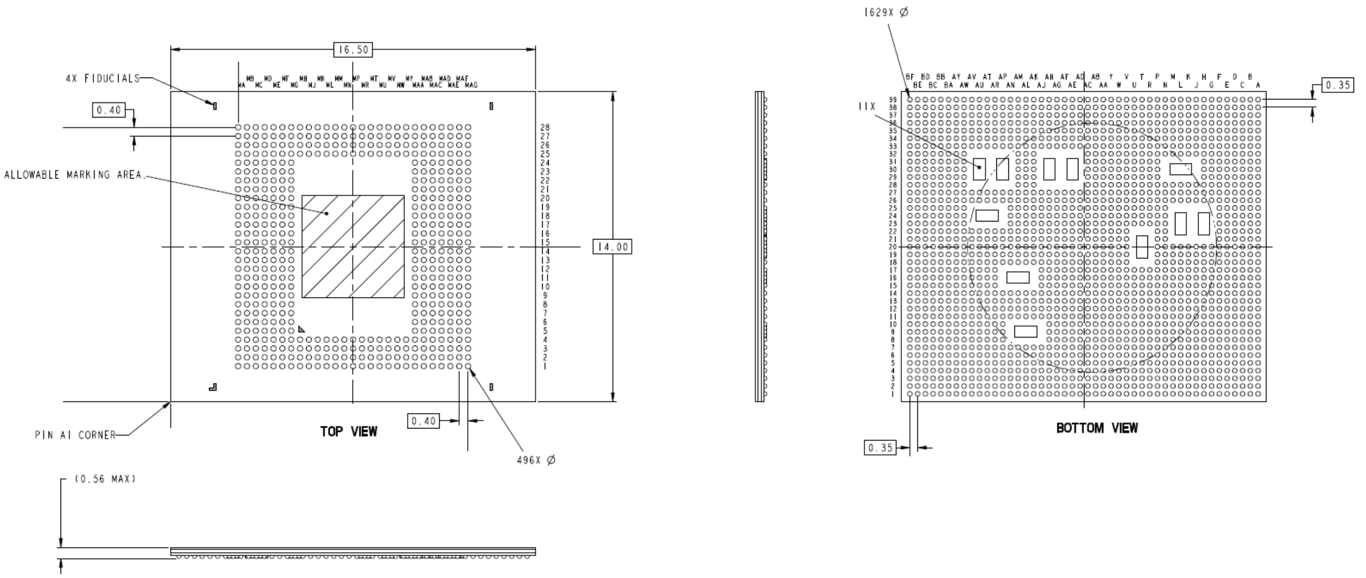


Figure 4-1 MPSP1629 outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

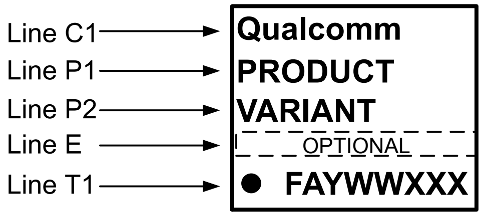


Figure 4-2 SM8650 device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ SM8650
P2	VARIANT	PRR-BB ■ See Table 4-4 for the assigned values.
E	Blank or random	Optional information
T1	FAYWWXXX	F = foundry company code ■ F = F for TSMC A = assembly site code ■ A = X (Amkor, Japan) ■ A = C (Amkor, Korea) Y = single/last digit of year WW = two-digit work week of current year XXX = lot serial number
	●	Ball A1 indicator

NOTE For complete marking definitions of all SM8650/SM8650P variants and revisions, see the *SM8650/SM8650P Device Revision Guide* (80-40938-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 Related register (0x221C2098)

Bit location	Name	Description
[bits [27:20]	FEATURE_ID	Feature ID is used for differentiating SKUs/variants
bits [19:0]	JTAG_ID	These bits map to [31:12] of the JTAG_ID register (0x221C8744). Fuse bit 0 maps to bit 12 of JTAG_ID

4.3 Device identification

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8650	-0	-MPSP	1629			-TR	-01	-0	-AB

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example

- Example 1: SM-8650-0-MPSP1629-MT-01-0-AB

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	**Sample type**	**Variant (PRR-BB)** **P = product configuration code** **RR = product revision code** **BB = feature code** [a]	**FEATURE_ID** [b]	**Hardware revision number**	**Source configuration code (S)** [c]	**Comments**	**Sample date**
SM8650	ES1	001-AB	0x2	0x0 0227 0E1	0	SM8650, MPSP1629, CPU, GPU, 4.2 GHz LPDDR5X, 2 × ASC, sub-6 and mmW, 0.57 mm height	3/31/2023
SM8650	ES2	002-AB	0x2	0x2 0227 0E1	0	SM8650, MPSP1629, CPU, GPU, 4.2 GHz LPDDR5X, 2 × ASC, sub-6 and mmW, 0.57 mm height	6/30/2023
SM8650P	ES	002-AB	0x0	0x2 0228 0E1	0	SM8650P, MPSP1629, CPU, GPU, 4.2 GHz LPDDR5X, 2 × ASC, sub-6 and mmW, 0.57 mm height	6/30/2023

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.

[b] See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.

[c] S is the source configuration code that identifies all the qualified die fabrication-source/assembly site combinations available when the particular sample type was shipped. S values are defined in Table 4-5.

Table 4-5 Source configuration codes

S value	**F value = F**	**A value = C**	**A value = X**
0	TSMC	Amkor, Korea	Amkor, Japan

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

For the daisy chain interconnect information, see *Daisy Chain Interconnect, MPSP1629, 16.5 × 14.0 mm* (DS90-16783-R1).

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-16783-R1

NOTE For LPDDR5X daisy chain ordering part number, contact the LPDDR manufacturer.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM8650/SM8650P rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8650/SM8650P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the

SM8650 LPDDR5X 12 GB Package Thermal Model Icepak (HS11-40938-5HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-40938-5HW

SM8650 LPDDR5X 12 GB Package Thermal Model Flowtherm (HS11-40938-6HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-40938-6HW

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

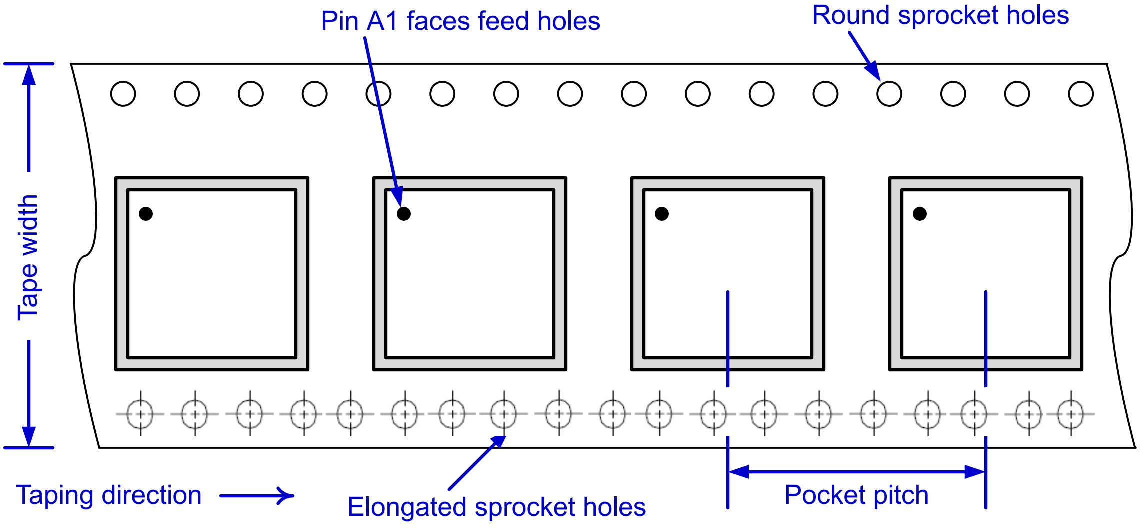
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8650/SM8650P tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Dual	Reel diameter:	330 mm	Tape width:	32 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

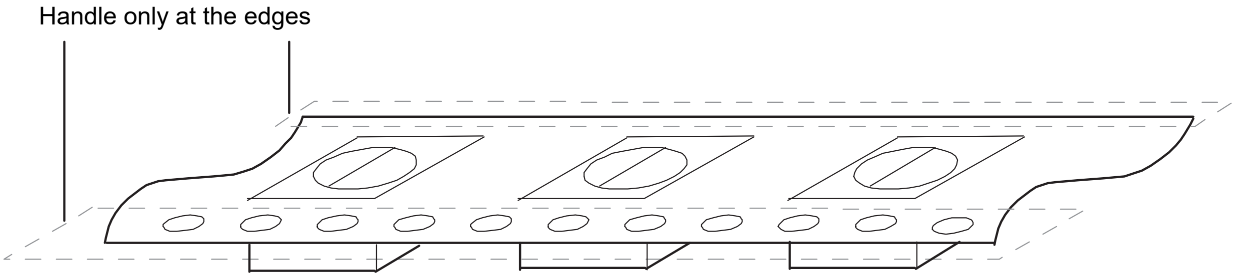


Figure 5-2 Tape handling

5.1.2 Matrix tray information - available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See Figure 5-3 for matrix-tray key attributes. See Table 5-1 for matrix-tray key dimensions.

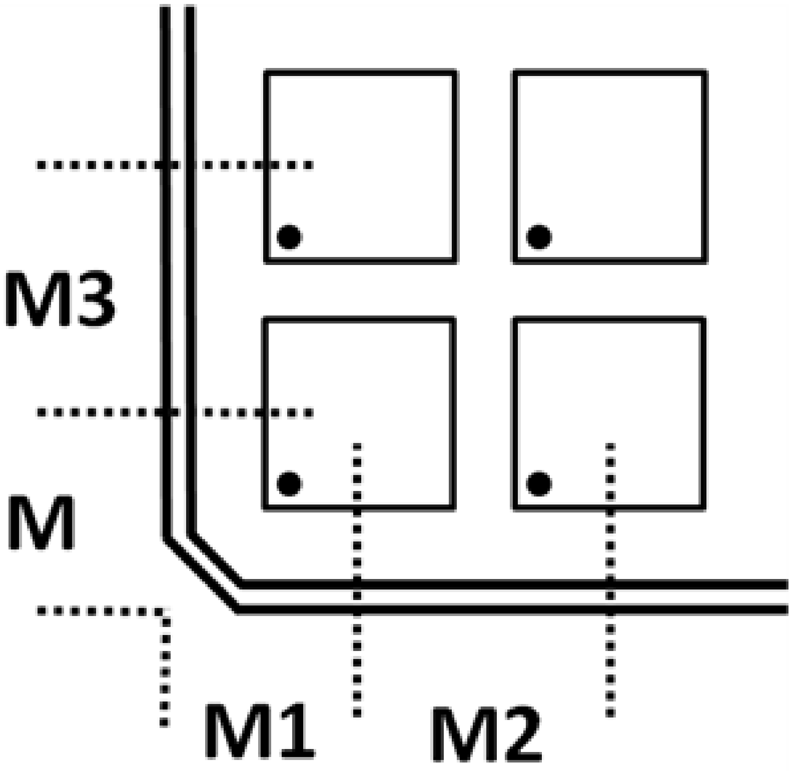


Figure 5-3 Matrix-tray key attributes

Table 5-1 Matrix-tray key dimensions

Key dimensions	
Array	6 × 15 (90)
M	15.45 mm
M1	14.00 mm
M2	20.50 mm
M3	21.00 mm

5.2 Storage

5.2.1 Bagged storage conditions

SM8650/SM8650P devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out of bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Device moisture sensitivity level.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is not necessary to bake the SM8650/SM8650P if the conditions specified in Bagged storage conditions and Out of bag duration have **not been exceeded.**

It is **necessary** to bake the SM8650/SM8650P if any condition specified in Bagged storage conditions or Out of bag duration has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	TBD	TBD
HTOL in FIT (ƛ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	TBD	TBD
Mean time to failure (MTTF) t = 1/ƛ in million hours (Total samples from three different wafer lots)	TBD	TBD
ESD – human body model (HBM) rating JS001-2017 (Total samples from one wafer lot)	TBD	TBD
ESD – charged device model (CDM) rating JS002-2018 (Total samples from one wafer lot)	TBD	TBD
Latch-up (I-test): EIA/JESD78E Trigger current: ± 100 mA; temperature: 95°C (Total samples from one wafer lot)	TBD	TBD
Latch-up (Vsupply overvoltage): EIA/JESD78E Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 95°C (Total samples from one wafer lot)	TBD	TBD

Table 7-2 Package reliability results

Tests, standards, and conditions	Sample size Amkor, Korea	Sample size Amkor, Japan	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260°C +0/-5°C (Total samples from three different assembly lots)	TBD	TBD	TBD
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260°C +0/-5°C (Total samples from three different assembly lots)	TBD	TBD	TBD
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260°C +0/-5°C (Total samples from three different assembly lots)	TBD	TBD	TBD
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260°C +0/-5°C (Total samples from three different assembly lots)	TBD	TBD	TBD
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (Total samples from three different assembly lots)	TBD	TBD	TBD
Flammability UL-STD-94 **Note**: Flammability test – not required Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	TBD	TBD	TBD
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	TBD	TBD	TBD
Die shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	TBD	TBD	TBD
Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	TBD	TBD	TBD
Internal/external visual (Total samples from three different assembly lots at each SAT)	TBD	TBD	TBD

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	SM8650/SM8650P
Package type	MPSP1629
Package body size	16.5 mm × 14.0 mm × 0.56 mm
Lead composition	SAC125/Ni
Fab process	4 nm
Fab sites	TSMC
Assembly sites	▪ Amkor, Japan ▪ Amkor, Korea
Solder ball pitch	0.35 mm

8 Revision history

Revision	Date	Description
AA	August 23, 2022	Initial release
AB	August 31, 2022	▪ Figure 1-1 *SM8650 + SDR875 (sub-6/mmW solution) functional block diagram and example application*: Updated the block diagram ▪ Figure 1-2 *SM8650 + SDR753 (sub-6 solution) functional block diagram and example application*: Updated the block diagram ▪ Table 1-1 *SM8650/SM8650P features*: Updated the location feature capability and QFS support ▪ Chapter 2 *Pin definitions*: Added this chapter
AC	September 11, 2022	▪ SM8650/SM8650P high-level block diagram and MPSP1629 outline drawing: Updated eUSB2 ▪ Figure 1-1 *SM8650 + SDR875 (sub-6/mmW solution) functional block diagram and example application*: Updated eUSB2 ▪ Figure 1-2 *SM8650 + SDR753 (sub-6 solution) functional block diagram and example application*: Updated eUSB2 ▪ Table 2-3 *MSM bottom pin descriptions – general-purpose input/output ports*: Updated GPIOs pad group naming to match the definition
AD	September 14, 2022	▪ Global: Updated WCD939x to WCD9395 across the document ▪ Figure 1-3 *SM8650P functional block diagram and example application*: Added the SM8650P block diagram ▪ Table 2-3 *MSM bottom pin descriptions – general-purpose input/output ports*: Added additional configurable functions for GPIO_125, GPIO_170, GPIO_174, GPIO_178, GPIO_179, and GPIO_187
AE	November 2022	▪ Figure 1-1 *SM8650 + SDR875 (sub-6/mmW solution) functional block diagram and example application*: Updated the block diagram ▪ Figure 1-2 *SM8650 + SDR753 (sub-6 solution) functional block diagram and example application*: Updated the block diagram ▪ Figure 1-3 *SM8650P functional block diagram and example application*: Updated the block diagram ▪ Table 1-1 *SM8650/SM8650P features*: Updated the SoundWire interface and USB features ▪ Table 2-1 *I/O description (pin type) parameters*: Updated the pin voltage groupings for baseband circuits ▪ Figure 2-2 *SM8650 bottom pin assignments (top view)*: Updated pins D14 and E14 to DNC ▪ Table 2-6 *MSM bottom pin descriptions: Not connected pins*: Added pins D14 and E14 to DNC
AF	December 2022	▪ Table 1-1 *SM8650/SM8650P features*: Updated the SoundWire interface feature ▪ Table 2-1 *I/O description (pin type) parameters*: Updated the I/O description for PX10 and PX14 ▪ Figure 2-2 *SM8650 bottom pin assignments (top view)*: Updated the pin name of pin T34 to VDD_A_GNSS_ADC_1P2 ▪ Table 2-4 *MSM bottom pin descriptions: Power-supply pins*: Updated the pin name of pin T34 to VDD_A_GNSS_ADC_1P2
AG	February 2023	▪ Figure 1-2 *SM8650 + SDR753 (sub-6 solution) functional block diagram and example application*: Corrected protocol naming from eUSB to eUSB2. ▪ Table 1-1 *SM8650/SM8650P features*: Updated Adreno graphic processing unit (GPU) feature

Revision	Date	Description
		■ Table 2-3 *MSM bottom pin descriptions – general-purpose input/output ports*: Added alternate functions information such as GP_CLK, GP_MN, AUDIO_REF, GP_PDM, and so on for GPIOs 53, 70, 71, 72, 86, 87, 88, 124, 126, 127, 128, 134, 135, and 136 ■ Section 4.2 *Part marking*: Added this section ■ Section 4.3 *Device identification*: Added this section ■ Section 4.4 *Device moisture sensitivity level*: Added this section ■ Section 4.5 *Thermal characteristics*: Added this section ■ Chapter 5 *Carrier, storage, and handling information*: Added this chapter ■ Chapter 6 *PCB mounting guidelines*: Added this chapter ■ Chapter 7 *Part reliability*: Added this chapter
AH	March 2023	■ Global: Replaced always on camera (AON) with always sensing camera (ASC) across the document ■ Table 1-1 *SM8650/SM8650P features*: Added Kryo CPU capability ■ Chapter 3 *Electrical specifications*: Added this chapter
Revision AI was omitted in accordance with QTI document conventions.		
AJ	May 2023	■ Global: Corrected the assembly site across the document. ■ Table 3-1 *Absolute maximum ratings*: Updated the following net names: □ VDD_A_UFS_0_CORE to VDD_A_UFS_CORE □ VDD_A_UFS_0_1P2 to VDD_A_UFS_1P2 ■ Table 3-3 *Operating conditions for non AVS voltage rails*: Added the specification values ■ Table 4-4 *Device identification details*: □ Added SM8650 AB SKU for ES2 samples □ Added SM8650P AB SKU for ES samples

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