Qualcomm Technologies, Inc.

Device description

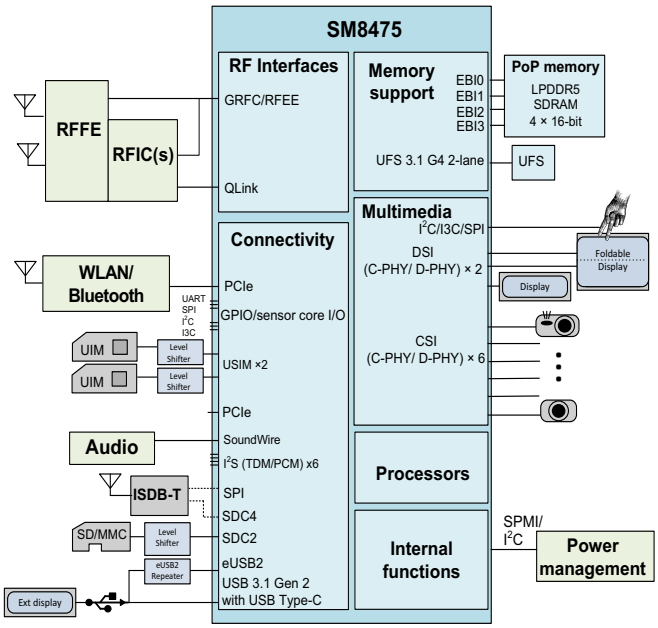
The SM8475 device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with a 4 nm process, for superior performance and power efficiency. SM8475 includes the following key components:

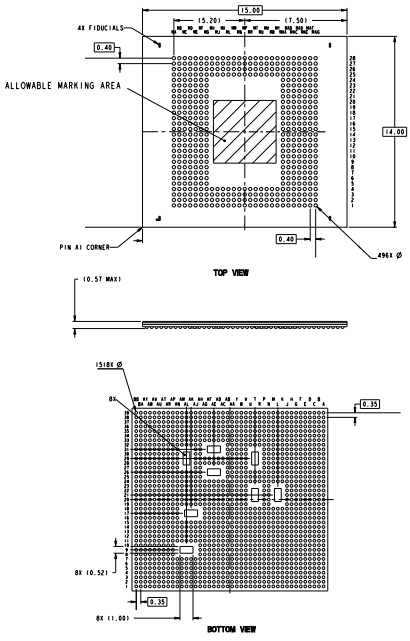
- Qualcomm® Kryo™ 780 CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 730 GPU for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ 680 Image Signal Processor for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 1195 DPU for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 GHz bands (Rel 16 integrated modem)

Key features (see Section 1.2 for details)

- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9380/WCD9385 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Snapdragon Sensors Core Technology for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU260) for advanced secure use cases
- Qualcomm® Hexagon™ Tensor Processor (HTP) with Hexagon Vector eXtensions (HVX) and Hexagon Matrix eXtensions (HMX)
- Qualcomm® FastConnect™ 6900 System with WCN685x, 802.11ax, 2 × 2 MIMO, Bluetooth 5.2
- Quad-channel package-on-package (PoP) high-speed LPDDR5 SDRAM
- 15.0 × 14.0 mm × 0.57 mm, MPSP1518B PoP

SM8475 high-level block diagram and MPSP1518B outline drawing





Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

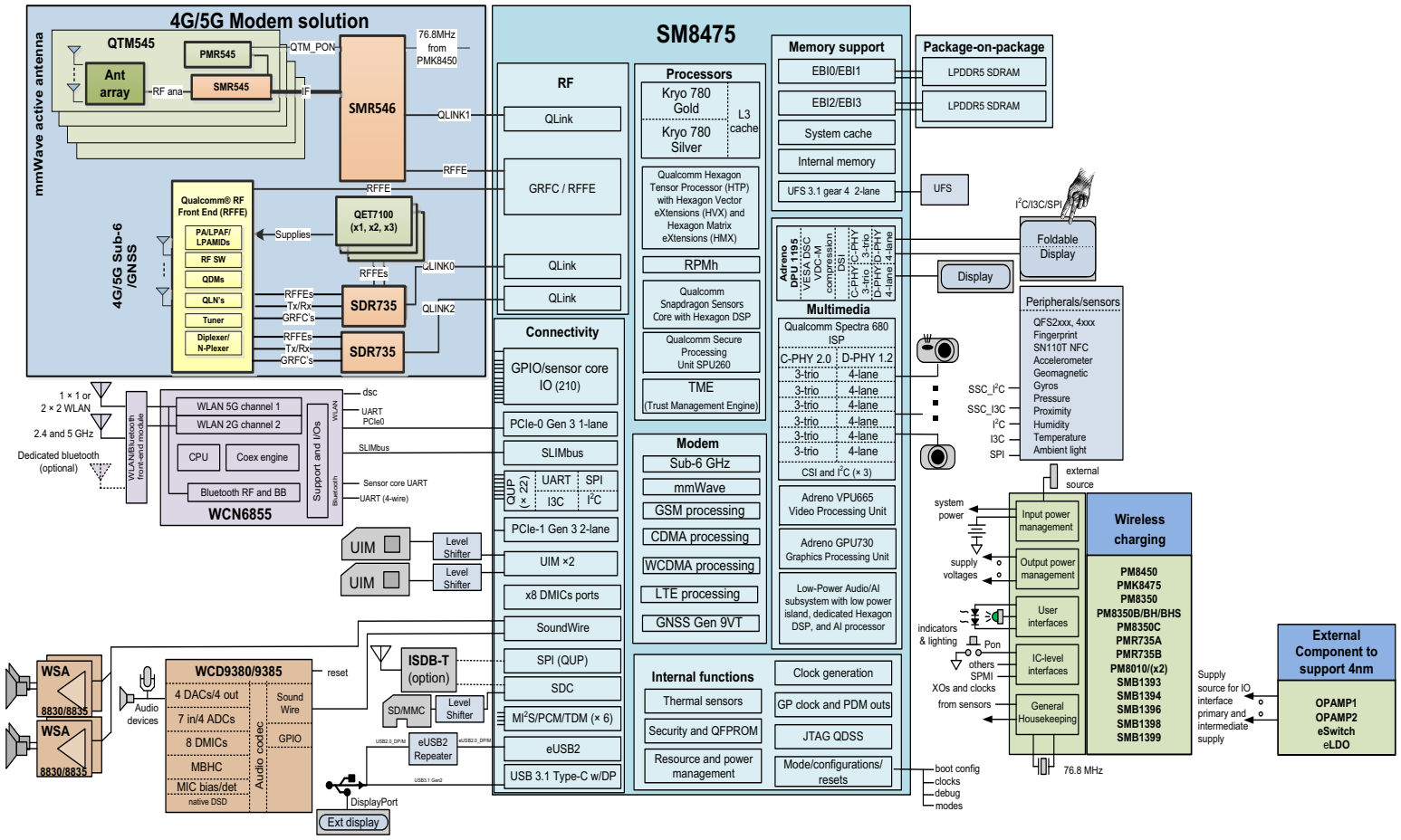


Figure 1-1 SM8475 functional block diagram and example application

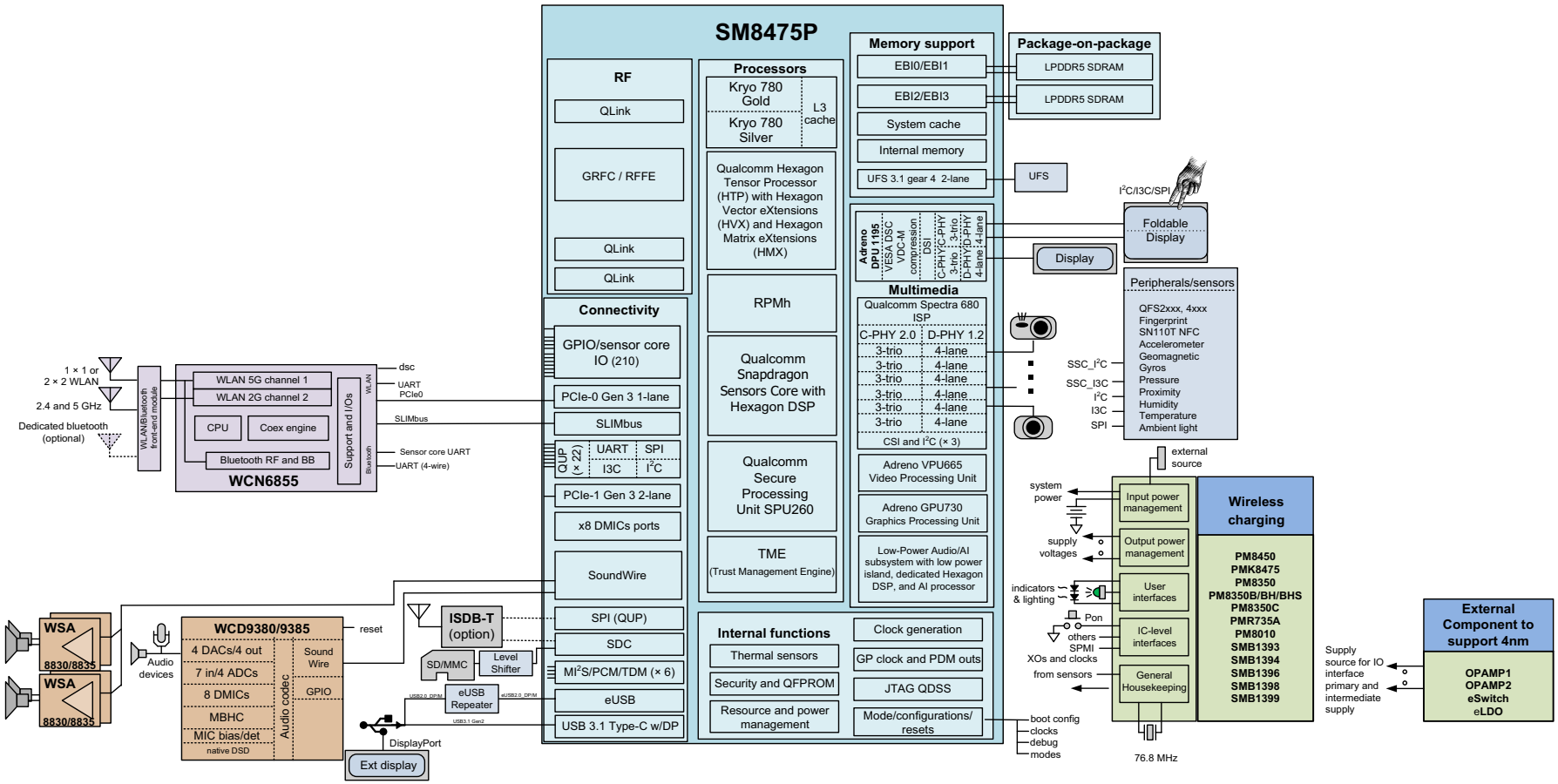


Figure 1-2 SM8475P functional block diagram and example application

1.2 SM8475/SM8475P features

NOTE: Some of the hardware features integrated within the SM8475/SM8475P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8475/SM8475P features.

Table 1-1 SM8475/SM8475P features

<table>
<tr><th>Feature</th><th>SM8475/SM8475P capability</th></tr>
<tr><td colspan="2">Processors</td></tr>
<tr><td>Applications</td><td>Kryo 780 CPU subsystem
■ Prime and high-performance cores for intensive tasks
■ Quad power-efficient cores

<table>
<tr><th>Cores</th><th>F_{max}</th><th>Cache per core</th></tr>
<tr><td>1 - Kryo Prime</td><td>3.2 GHz</td><td>1 MB L2</td></tr>
<tr><td>3 - Kryo Gold</td><td>2.75 GHz</td><td>512 KB L2</td></tr>
<tr><td>4 - Kryo Silver</td><td>2.0 GHz</td><td>128 KB L2</td></tr>
</table>
Note: Each two Kryo Silver cores share one 128 KB L2 cache.</td></tr>
</table>

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
Digital signal processing and artificial intelligence	■ Hexagon tensor processor: □ V69 AI-optimized Tensor Processor □ Six threads Scalar DSP + 4x HVX vector co-processors □ Vector tightly-couple co-processor optimized for pixel processing □ BW compression □ Higher peak and batch = 1 performance □ Improved power efficiency ■ Benefit/use cases: □ Noise reduction □ Super resolution □ ML ISP □ HDR □ Image enhancement □ Segmentation □ Depth estimation □ Classification/detection ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. ■ The audio Hexagon DSP is dedicated to the audio subsystem with support for always-on low-power use cases. It incorporates a dedicated AI processor for offloading neural network use cases to improve the performance and minimize power consumption. ■ The sensor Hexagon DSP in the Snapdragon Sensors Core Technology supports always-on, low-power use cases. ■ All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements. ■ Hexagon Tensor Processor dedicated neural processing unit for neural network (NN) use cases. It incorporates an NN matrix engine to ensure efficient execution of various neural networks and their parameters. ■ Hexagon Tensor Processor may be used for typical imaging, video, audio, and data-based NN use cases.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
Snapdragon Sensors Core LPI	Hexagon v66 DSP – 845 MHz normal; 1.5 GHz turbo/2.5 MB memory ■ Data acquisition engine (DAE) ■ Context change detector 4.0 (CCD) ■ Eight dedicated buses (One I3C, three I^2C, one SPI, two UART, and one API I^2C) ■ I3C IBI ■ Pedometer 3.0 ■ Activity recognition 1.0 ■ Qualcomm Sensing HUB 2.0 ■ Sensors supported: □ Accel/Gyro □ Magnetometer □ Ambient Light/Proximity □ Pressure □ Humidity/Temp □ SAR □ Hall □ Plus others per customer inputs
Modem * Location * (* NA for SM8475P)	3G/4G/5G – mmWave and sub-6 GHz bands (Rel 16) Gen 9 VT v5 LocTech 21 SW
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR5 SDRAM (4 × 16-bit) designed for a 3200 MHz (LPDDR5) 4 MB system cache
External memory Via UFS Via SDC	 UFS 3.1 gear 4 Rate B, 1x 2-lane ICE with 2000 MB/s read and 1600 MB/s Write Booster (**Note**: Write Booster performance depends on UFS) SD v3.0 4 bit for SD card
Multimedia	
Display	DPU 1195 ■ Maximum resolution for internal panel: Support up to UHD (3026 × 2160) at 120 Hz, 30 bpp ■ Supports dual MIPI DSI ports, with support for split-link for fold use case. ■ External panel support: DisplayPort v1.4 with MST (2x 4K60 10-bit or 1x 8K30 with DSC) ■ Compression support: VDC-M for internal panel and DSC v1.2 ■ Processing: rounded corner, Demura engine and SPR ■ Power-saving: panel self-refresh using LLC ■ FP16 support to improve rendering pipeline efficiency, reduce DDR traffic, reduce power consumption, offload tone-mapping process from GPU

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
Camera support	■ Qualcomm Spectra 680 Image Signal Processor: □ Qualcomm Spectra 680 ISP supports connectivity to multiple cameras due to six included C-PHY/D-PHY interfaces. Furthermore, up to five cameras may operate concurrently due to the Qualcomm Spectra 680's 3 IFEs and 2 IFE-lites ■ Always on Camera (AON Camera) support: □ CSI4 with PM8010 SPMI interface and 19.2 MHz CAM_MCLK_4 (GPIO_104) ■ HW interface: □ Triple 36 MP ISPs □ Six combo-PHYs with four lanes each □ D-PHY 1.2 and C-PHY 2.0 □ 19.2 MHz (x8) camera clock support GPIO [107:100] ■ 2x throughput: □ 108 MP @ 30 fps ZSL with in-ISP pixel binning □ 64 MP @ 30 fps ZSL with two IFEs combined, without in-ISP binning □ 200 MP non-ZSL snapshot capture - note: 113 MP with MFNR □ 12 MP @ 240 fps fast shutter sensor support - PHY and RAW dump ■ Key improvements: □ QCFA sensor support w/ HW remosaic, HDR and binning □ Fast sensor switching for smooth camera transition experience □ Major IQ improvements to deliver DSLR experience □ VBSE (Video Bokeh and Special Effect) □ LCAC for wide-angle chromatic aberration correction □ Highlight recovery white balance □ MMF (Massive Multi Frame) processing for extreme low light □ HDR10+ statistics □ GTM (Global Tone Mapping) for FD (Face Detection) □ Staggered HDR for snapshot, video, preview ■ ZSL example: □ (28 M + 28 M + 28 M) @ 30 fps - triple camera □ (64 M + 25 M) @ 30 fps - dual camera □ 108 M @ 30 fps - single camera (binned in the ISP) ■ MFHDR HW for snapshot, video, preview ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port ■ C-PHY v2.0: 6 Gbps/trio (41.14Gbps) on three trios per port □ Connect up to 12x/18x camera, 5x concurrent
Adreno video processing unit (VPU)	Adreno VPU 665 UHD video processing unit Video decode up to 4K240/8K60 Video encode up to 4K120/8K30 Concurrent 4K60 decode and 4K60 encode for wireless display Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, and MPEG-2 formats Native encode support for H.265 Main 10, H.265 Main, H.264 High formats

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
Adreno graphic processing unit (GPU)	Adreno GPU 730 – 4K 120 fps UI OpenGL ES 3.2, Vulkan 1.2 OpenCL 2.0 full profile Adreno NN direct GMEM as General Purpose Memory - GMEM write for compute Concurrent processing to improve efficiency - concurrent binning Workload Reduction - Image based Variable Rate Shading Full Virtualization support
Audio	
Low-power AI subsystem (LPASS)	Integrated low power island, for always-on audio ■ Hexagon V66M with 1 MB L2/1 MB TCM ■ AI Processor (eNPU) v2, to accelerate neural networking use cases ■ HW linear echo cancellation accelerator ■ DSP-offload for audio playback (analog, Bluetooth Audio, USB Digital Audio)
Codec	Integrated within the WCD9380/WCD9385 high fidelity audio codec
Speaker amplifier	Integrated within the WSA8830/WSA8835 class-H, low noise smart amplifier
Audio interfaces	SLIMbus for WCN685x Soundwire for WCD9380/WCD9385, WSA8830/WSA8835 ■ SoundWire interface (two Tx and two Rx data for codec) ■ Two dedicated SoundWire interfaces to support up to 4 WSA883x for smart speaker amplifier DMICs ■ Four DMIC ports support up to eight DMICs ■ Up to four DMICs for low-power voice activation Five I^2S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application One I^2S supports four data lanes for up to eight channels Tx/Rx application TDM/PCM: Up to 32 channels at 48 kHz per individual interface (Qualcomm Technologies, Inc. (QTI) I2S supports both TDM and PCM modes.)
Voice and audio algorithms	Voice UI ■ Snapdragon Voice Activation keyword detection ■ Echo Cancellation and Noise Suppression (ECNS) Voice call ■ AI-based noise suppression ■ Far-end noise suppression

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
Connectivity	
Qualcomm universal peripheral (QUP) ports	Qualcomm universal peripheral (QUP) v3 support. 22 QUP serial engine Seven lanes each for 4-QUPs and four lanes each for the 18-QUPs ■ UART ■ I^2C ■ I3C ■ SPI
USB	■ One USB 3.1 ports: gen2 10 Gbps (DP + data), eUSB2 repeater interface, support Type-C with DisplayPort v1.4 ■ eUSB2 requires external repeater over eD+/eD-
UIM	■ Two 1.8V/3V SIM card using external level shifter
PCIe	1-lane Gen 3 2-lane Gen 3
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4) ■ SDC2: 1.2 V only, SD 3.0 ■ SDC4:1.8 V only, SDIO 3.0 ■ 1.8V/3V SD card operation using external level shifter
Touchscreen support	Capacitive panels via ext IC (I^2C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display QFS2608, QFS2604, QFS2530, QFS4008
ISDBT/DMB support	Via external ISDBT/DMB device (SDC or SPI)
Configurable GPIOs	
Number of GPIO ports	210 – GPIO_0 to GPIO_209
Internal functions	
Security	
Crypto	AES-GCM, "HW ECC & RSA" (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP certifiable
QFPROM	Fuse bits available for OEM use
Access Control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure Boot with Sec Tools 2.0; easy to use tool set
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.3)
DRM	DRM Widevine V16 L1, HDCP v2.3
QTEE services	QTEE services ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
SPU	SPU260 for SoC Independent TCB

Table 1-1 SM8475/SM8475P features (cont.)

Feature	SM8475/SM8475P capability
TME	Introduce TME (Trust Management Engine) for SOC Root of Trust
Boot sequence	1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) rest of subsystems Emergency boot over USB 3.1
PLLs and clocks	■ 78.4 MHz X'tal ■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD)
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	2-channel 2-line SPMI; plus other lines, as needed, via GPIOs, I^2C, eBOM components to support 4nm technology
Wireless connectivity WLAN Bluetooth	 PCIe interface SLIMbus/UART interface
Fabrication technology and package	
Digital die	4 nm process
Package	MPSP1518B
PoP – small, thermally efficient package	15.0 × 14.0 × 0.57 mm
WLAN/BT/FM RF (SM8475P does not support the RF features listed here) PMIC (PMR735B is not applicable for SM8475P) Codec	WCN6855, WCN6856 SDR735 (4G/Sub-6/GNSS), SMR546/QTM545 (mmW) PM8010 × 2, PM8450, PMK8475, PM8350, PM8350B/BH/BHS, PM8350C, PMR735A, PMR735B WCD9380/WCD9385, WSA8830/WSA8835

2 Pin definitions

The SM8475/SM8475P is the lower device within a PoP system, as shown and explained in Figure 2-1.

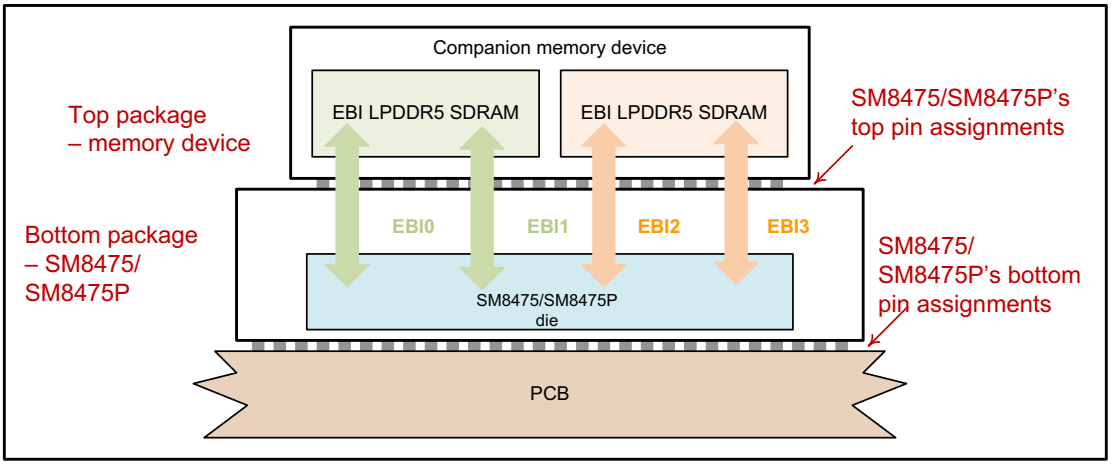


Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8475/SM8475P bottom pins (Section 2.2)
- SM8475/SM8475P top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
PX0	Pad group 0 (SPMI, RESIN); 1.8 V
PX5	Pad group 5 (UICC 0, UICC 1); 1.8 V
PX701	Pad group 701 (IO pad); 1.8 V
PX702	Pad group 702 (IO pad); 1.8 V
PX10	Pad group 10 (UFS IO); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
PX13	Pad group 13 (Secure processor); 1.85 V
PX14	Pad group 14 (SDC2 IO); 1.2 V
PX703	Pad group 703 (IO pad); 1.8 V
PX704	Pad group 704 (IO pad); 1.8 V
PX705	Pad group 705 (IO pad); 1.8 V
PX706	Pad group 706 (IO pad); 1.8 V
PX707	Pad group 707 (IO pad); 1.8 V
PX709	Pad group 709 (IO pad); 1.8 V

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
PX712	Pad group 712 (IO pad); 1.8 V
PX713	Pad group 713 (IO pad); 1.8 V
PX714	Pad group 714 (IO pad); 1.8 V
PX715	Pad group 715 (IO pad); 1.8 V
PX716	Pad group 716 (IO pad); 1.8 V
VDD_1P2_PX0	VDD 1.2 V for PX0 pads
VDD_IX	Intermediate supply; 0.9 V
VDD_IX_PX0	Intermediate supply for the PX0; 0.9 V

2.2 Pin assignments: MSM bottom

2.2.1 Pin map: MSM bottom

The SM8475/SM8475P is available in the MPSP1518B package. Its bottom surface is equivalent to an
MPSP1518B that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details and Section 2.3 for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in — the resolution is sufficient for comfortable reading.
- Download the SM8475/SM8475P *Pin Assignment and GPIO Configuration Spreadsheet* (80-27620-1A). This Microsoft Excel spreadsheet lists all SM8475/SM8475P pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-27620-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-27620-1A

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

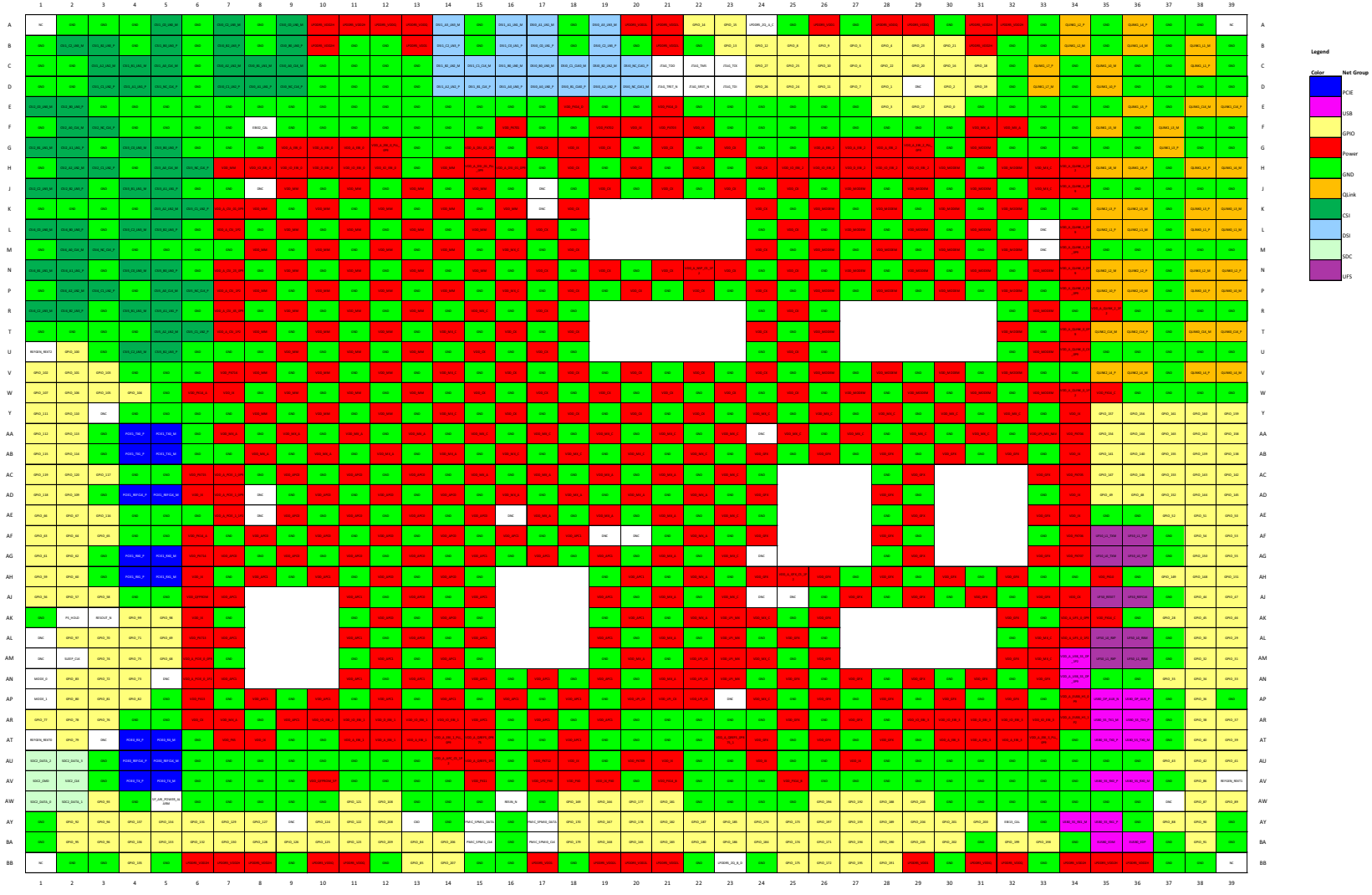


Figure 2-2 SM8475/SM8475P bottom pin assignments (top view)

2.2.2 Pin descriptions: MSM bottom

The bottom pins are described in Table 2.2 through Table 2-5.

Table 2-2 Pad descriptions

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
D9	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - plus MIPI CSI 0 (C-PHY), no connect
C9	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential clock - minus MIPI CSI 0 (C-PHY), trio lane 0 – A
B9	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - plus MIPI CSI 0 (C-PHY), trio lane 0 – B
A9	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 0 - minus MIPI CSI 0 (C-PHY), trio lane 0 – C
D8	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - plus MIPI CSI 0 (C-PHY), trio lane 1 – A
C8	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 1 - minus MIPI CSI 0 (C-PHY), trio lane 1 – B
D7	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - plus MIPI CSI 0 (C-PHY), trio lane 1 – C
C7	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 2 - minus MIPI CSI 0 (C-PHY), trio lane 2 – A
B7	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - plus MIPI CSI 0 (C-PHY), trio lane 2 – B
A7	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (D-PHY), differential lane 3 - minus MIPI CSI 0 (C-PHY), trio lane 2 – C
D5	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - plus MIPI CSI 1 (C-PHY), no connect
C5	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential clock - minus MIPI CSI 1 (C-PHY), trio lane 0 – A
B5	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - plus MIPI CSI 1 (C-PHY), trio lane 0 – B
A5	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 0 - minus MIPI CSI 1 (C-PHY), trio lane 0 – C
D4	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - plus MIPI CSI 1 (C-PHY), trio lane 1 – A
C4	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 1 - minus MIPI CSI 1 (C-PHY), trio lane 1 – B
D3	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - plus MIPI CSI 1 (C-PHY), trio lane 1 – C

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
C3	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 2 - minus MIPI CSI 1 (C-PHY), trio lane 2 – A
B3	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - plus MIPI CSI 1 (C-PHY), trio lane 2 – B
B2	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (D-PHY), differential lane 3 - minus MIPI CSI 1 (C-PHY), trio lane 2 – C
F3	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - plus MIPI CSI 2 (C-PHY), no connect
F2	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential clock - minus MIPI CSI 2 (C-PHY), trio lane 0 – A
E2	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - plus MIPI CSI 2 (C-PHY), trio lane 0 – B
E1	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 0 - minus MIPI CSI 2 (C-PHY), trio lane 0 – C
G2	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - plus MIPI CSI 2 (C-PHY), trio lane 1 – A
G1	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 1 - minus MIPI CSI 2 (C-PHY), trio lane 1 – B
H3	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - plus MIPI CSI 2 (C-PHY), trio lane 1 – C
H2	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 2 - minus MIPI CSI 2 (C-PHY), trio lane 2 – A
J2	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - plus MIPI CSI 2 (C-PHY), trio lane 2 – B
J1	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (D-PHY), differential lane 3 - minus MIPI CSI 2 (C-PHY), trio lane 2 – C
H6	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - plus MIPI CSI 3 (C-PHY), no connect
H5	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential clock - minus MIPI CSI 3 (C-PHY), trio lane 0 – A
G5	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - plus MIPI CSI 3 (C-PHY), trio lane 0 – B
G4	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 0 - minus MIPI CSI 3 (C-PHY), trio lane 0 – C
J5	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - plus MIPI CSI 3 (C-PHY), trio lane 1 – A
J4	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 1 - minus MIPI CSI 3 (C-PHY), trio lane 1 – B

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
K6	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - plus MIPI CSI 3 (C-PHY), trio lane 1 – C
K5	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 2 - minus MIPI CSI 3 (C-PHY), trio lane 2 – A
L5	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - plus MIPI CSI 3 (C-PHY), trio lane 2 – B
L4	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (D-PHY), differential lane 3 - minus MIPI CSI 3 (C-PHY), trio lane 2 – C
M3	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - plus MIPI CSI 4 (C-PHY), no connect
M2	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential clock - minus MIPI CSI 4 (C-PHY), trio lane 0 – A
L2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - plus MIPI CSI 4 (C-PHY), trio lane 0 – B
L1	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - minus MIPI CSI 4 (C-PHY), trio lane 0 – C
N2	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - plus MIPI CSI 4 (C-PHY), trio lane 1 – A
N1	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 1 - minus MIPI CSI 4 (C-PHY), trio lane 1 – B
P3	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 - plus MIPI CSI 4 (C-PHY), trio lane 1 – C
P2	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 2 - minus MIPI CSI 4 (C-PHY), trio lane 2 – A
R2	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - plus MIPI CSI 4 (C-PHY), trio lane 2 – B
R1	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 3 - minus MIPI CSI 4 (C-PHY), trio lane 2 – C
P6	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - plus MIPI CSI 5 (C-PHY), no connect
P5	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential clock - minus MIPI CSI 5 (C-PHY), trio lane 0 – A
N5	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - plus MIPI CSI 5 (C-PHY), trio lane 0 – B
N4	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 0 - minus MIPI CSI 5 (C-PHY), trio lane 0 – C
R5	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - plus MIPI CSI 5 (C-PHY), trio lane 1 – A

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
R4	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 1 - minus MIPI CSI 5 (C-PHY), trio lane 1 – B
T6	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - plus MIPI CSI 5 (C-PHY), trio lane 1 – C
T5	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 2 - minus MIPI CSI 5 (C-PHY), trio lane 2 – A
U5	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - plus MIPI CSI 5 (C-PHY), trio lane 2 – B
U4	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - minus MIPI CSI 5 (C-PHY), trio lane 2 – C
F8	EBI02_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI02_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
AY32	EBI13_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI13_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
A24	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	AI	ZQ calibration reference: The ZQ_A_C pin should be connected to VDDQ (S3H/PM8450) through a 240 Ω ±1% resistor. See LPDDR5 specification.
BB23	LPDDR5_ZQ_B_D	LPDDR5_VDDQ	AI	ZQ calibration reference: The ZQ_B_D pin should be connected to VDDQ (S3H/PM8450) through a 240 Ω ±1% resistor. See LPDDR5 specification.
D17	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - plus MIPI DSI 0 (C-PHY), trio lane 0 – A
C17	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 0 - minus MIPI DSI 0 (C-PHY), trio lane 0 – B
B17	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - plus MIPI DSI 0 (C-PHY), trio lane 0 – C
A17	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 1 - minus MIPI DSI 0 (C-PHY), trio lane 1 – A
D18	DSI0_B1_CLK0_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - plus MIPI DSI 0 (C-PHY), trio lane 1 – B
C18	DSI0_C1_CLK0_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 0 - minus MIPI DSI 0 (C-PHY), trio lane 1 – C
D19	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - plus MIPI DSI 0 (C-PHY), trio lane 2 – A

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
C19	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 2 - minus MIPI DSI 0 (C-PHY), trio lane 2 – B
B19	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - plus MIPI DSI 0 (C-PHY), trio lane 2 – C
A19	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential lane 3 - minus MIPI DSI 0 (C-PHY), NC
C20	DSI0_NC_CLK1_P	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - plus MIPI DSI 0 (C-PHY), NC
D20	DSI0_NC_CLK1_M	DSI	AI, AO	MIPI DSI 0 (D-PHY), differential clock 1 - minus MIPI DSI 0 (C-PHY), NC
D16	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - plus MIPI DSI 1 (C-PHY), trio lane 0 – A
C16	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 0 - minus MIPI DSI 1 (C-PHY), trio lane 0 – B
B16	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - plus MIPI DSI 1 (C-PHY), trio lane 0 – C
A16	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 1 - minus MIPI DSI 1 (C-PHY), trio lane 1 – A
D15	DSI1_B1_CLK0_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0 - plus MIPI DSI 1 (C-PHY), trio lane 1 – B
C15	DSI1_C1_CLK0_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential clock 0- minus MIPI DSI 1 (C-PHY), trio lane 1 – C
D14	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - plus MIPI DSI 1 (C-PHY), trio lane 2 – A
C14	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 2 - minus MIPI DSI 1 (C-PHY), trio lane 2 – B
B14	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - plus MIPI DSI 1 (C-PHY), trio lane 2 – C
A14	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (D-PHY), differential lane 3 - minus MIPI DSI 1 (C-PHY), NC
D22	JTAG_SRST_N	PX701	DIS-PU	JTAG reset for debug
C23	JTAG_TCK	PX701	DIS-PU	JTAG clock input
D23	JTAG_TDI	PX701	DIS-PU	JTAG data input
C21	JTAG_TDO	PX701	DO-Z	JTAG data output
C22	JTAG_TMS	PX701	DI-PU:nppdkp	JTAG mode select input
D21	JTAG_TRST_N	PX701	DI-PD:nppukp	JTAG reset

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
AU5	PCIE0_REFCLK_M	–	AO	PCIe 0 Gen 3 reference clock - minus
AU4	PCIE0_REFCLK_P	–	AO	PCIe 0 Gen 3 reference clock - plus
AT5	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive - minus
AT4	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive - plus
AV5	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit - minus
AV4	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit - plus
AD5	PCIE1_REFCLK_M	–	AO	PCIe 1 Gen 3 reference clock - minus
AD4	PCIE1_REFCLK_P	–	AO	PCIe 1 Gen 3 reference clock - plus
AG5	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive - minus
AG4	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive - plus
AH5	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive - minus
AH4	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive - plus
AA5	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit - minus
AA4	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit - plus
AB5	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit - minus
AB4	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit - plus
T38	QLINK0_CLK_M	–	AI, AO	QLink0 clock - minus
T39	QLINK0_CLK_P	–	AI, AO	QLink0 clock - plus
N38	QLINK0_L2_M	–	AI, AO	QLink0 lane 2 - minus
N39	QLINK0_L2_P	–	AI, AO	QLink0 lane 2 - plus
K39	QLINK0_L3_M	–	AI, AO	QLink0 lane 3 - minus
K38	QLINK0_L3_P	–	AI, AO	QLink0 lane 3 - plus
V39	QLINK0_L4_M	–	AI, AO	QLink0 lane 4 - minus
V38	QLINK0_L4_P	–	AI, AO	QLink0 lane 4 - plus
P39	QLINK0_L0_M	–	AI, AO	QLink0 lane 0 - minus
P38	QLINK0_L0_P	–	AI, AO	QLink0 lane 0 - plus
L39	QLINK0_L1_M	–	AI, AO	QLink0 lane 1 - minus
L38	QLINK0_L1_P	–	AI, AO	QLink0 lane 1 - plus
E38	QLINK1_CLK_M	–	AI, AO	QLink1 clock - minus
E39	QLINK1_CLK_P	–	AI, AO	QLink1 clock - plus
B36	QLINK1_L4_M	–	AI, AO	QLink1 lane 4 - minus
A36	QLINK1_L4_P	–	AI, AO	QLink1 lane 4 - plus
D33	QLINK1_L7_M	–	AI, AO	QLink1 lane 7 - minus
C33	QLINK1_L7_P	–	AI, AO	QLink1 lane 7 - plus

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
F35	QLINK1_L5_M	–	AI, AO	QLink1 lane 5 - minus
E36	QLINK1_L5_P	–	AI, AO	QLink1 lane 5 - plus
H39	QLINK1_L6_M	–	AI, AO	QLink1 lane 6 - minus
H38	QLINK1_L6_P	–	AI, AO	QLink1 lane 6 - plus
H35	QLINK1_L8_M	–	AI, AO	QLink1 lane 8 - minus
H36	QLINK1_L8_P	–	AI, AO	QLink1 lane 8 - plus
C35	QLINK1_L0_M	–	AI, AO	QLink1 lane 0 - minus
D35	QLINK1_L0_P	–	AI, AO	QLink1 lane 0 - plus
B34	QLINK1_L2_M	–	AI, AO	QLink1 lane 2 - minus
A34	QLINK1_L2_P	–	AI, AO	QLink1 lane 2 - plus
B38	QLINK1_L1_M	–	AI, AO	QLink1 lane 1 - minus
C38	QLINK1_L1_P	–	AI, AO	QLink1 lane 1 - plus
F37	QLINK1_L3_M	–	AI, AO	QLink1 lane 3 - minus
G37	QLINK1_L3_P	–	AI, AO	QLink1 lane 3 - plus
T35	QLINK2_CLK_M	–	AI, AO	QLink2 clock - minus
T36	QLINK2_CLK_P	–	AI, AO	QLink2 clock - plus
N35	QLINK2_L2_M	–	AI, AO	QLink2 lane 2 - minus
N36	QLINK2_L2_P	–	AI, AO	QLink2 lane 2 - plus
K36	QLINK2_L3_M	–	AI, AO	QLink2 lane 3 - minus
K35	QLINK2_L3_P	–	AI, AO	QLink2 lane 3 - plus
V36	QLINK2_L4_M	–	AI, AO	QLink2 lane 4 - minus
V35	QLINK2_L4_P	–	AI, AO	QLink2 lane 4 - plus
P36	QLINK2_L0_M	–	AI, AO	QLink2 lane 0 - minus
P35	QLINK2_L0_P	–	AI, AO	QLink2 lane 0 - plus
L36	QLINK2_L1_M	–	AI, AO	QLink2 lane 1 - minus
L35	QLINK2_L1_P	–	AI, AO	QLink2 lane 1 - plus
AV2	SDC2_CLK	PX14	DO	Secure digital controller 2 clock
AV1	SDC2_CMD	PX14	B	Secure digital controller 2 command
AW1	SDC2_DATA_0	PX14	B	Secure digital controller 2 data bit 0
AW2	SDC2_DATA_1	PX14	B	Secure digital controller 2 data bit 1
AU1	SDC2_DATA_2	PX14	B	Secure digital controller 2 data bit 2
AU2	SDC2_DATA_3	PX14	B	Secure digital controller 2 data bit 3
BA17	PMIC_SPMI0_CLK	PX0	DO	Slave and PBUS interface 0 for PMICs – clock
AY17	PMIC_SPMI0_DATA	PX0	B-PD	Slave and PBUS interface 0 for PMICs – data

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
BA15	PMIC_SPMI1_CLK	PX0	DO	Slave and PBUS interface 1 for PMICs – clock
AY15	PMIC_SPMI1_DATA	PX0	B-PD	Slave and PBUS interface 1 for PMICs – data
AY13	CXO	PX11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
AN1	MODE_0	PX713	DI-S PD	Mode control bit 0 – unconnected for native mode
AP1	MODE_1	PX713	DI-S PD	Mode control bit 1 – unconnected for native mode
AK2	PS_HOLD	PX713	DO	Power-supply hold signal to PMIC
AT1	REFGEN_REXT0	–	AI, AO	Reference voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
AV39	REFGEN_REXT1	–	AI, AO	Reference voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
U1	REFGEN_REXT2	–	AI, AO	Reference voltage bias circuit, pull down to GND by 100 Ω ± 1% resistor.
AW16	RESIN_N	PX0	DI	Reset input
AK3	RESOUT_N	PX713	DO	Reset output
AM2	SLEEP_CLK	PX713	DI	Sleep clock
AW5	SP_ARI_POWER_ ALARM	PX13	DI	Power alarm
AL36	UFS0_L0_RXM	–	AI	UFS 0 lane 0 receive - minus
AL35	UFS0_L0_RXP	–	AI	UFS 0 lane 0 receive - plus
AG35	UFS0_L0_TXM	–	AO	UFS 0 lane 0 transmit - minus
AG36	UFS0_L0_TXP	–	AO	UFS 0 lane 0 transmit - plus
AM36	UFS0_L1_RXM	–	AI	UFS 0 lane 1 receive - minus
AM35	UFS0_L1_RXP	–	AI	UFS 0 lane 1 receive - plus
AF35	UFS0_L1_TXM	–	AO	UFS 0 lane 1 transmit - minus
AF36	UFS0_L1_TXP	–	AO	UFS 0 lane 1 transmit - plus
AJ36	UFS0_REFCLK	PX10	DO	UFS 0 reference clock
AJ35	UFS0_RESET_N	PX10	DO	UFS 0 reset
AP35	USB0_DP_AUX_N	–	AI, AO	USB 0 DisplayPort aux minus
AP36	USB0_DP_AUX_P	–	AI, AO	USB 0 DisplayPort aux - plus
BA35	EUSB0_EDM	–	AI, AO	Extended USB2.0 high-speed data - minus
BA36	EUSB0_EDP	–	AI, AO	Extended USB2.0 high-speed data - plus
AV36	USB0_SS_RX0_M	–	AI	USB super-speed receive 0 - minus
AV35	USB0_SS_RX0_P	–	AI	USB super-speed receive 0 - plus

Table 2-2 Pad descriptions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
AY34	USB0_SS_RX1_M	–	AI	USB super-speed receive 0 - minus
AY35	USB0_SS_RX1_P	–	AI	USB super-speed receive 0 - plus
AT36	USB0_SS_TX0_M	–	AO	USB super-speed transmit 0 - minus
AT35	USB0_SS_TX0_P	–	AO	USB super-speed transmit 0 - plus
AR35	USB0_SS_TX1_M	–	AO	USB super-speed transmit 0 - minus
AR36	USB0_SS_TX1_P	–	AO	USB super-speed transmit 0 - plus

1. See Table 2-1 for parameter and acronym definitions.

GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

  To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that includes a worksheet for all SM8475/SM8475P GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the pin assignment spreadsheet (80-27620-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-27620-1A

After successfully logging in, the document is downloaded.

Make this document a favorite to be notified of any changes.

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
E30	GPIO_0	QUP_L0[0]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
D28	GPIO_1	QUP_L1[0]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
D30	GPIO_2	QUP_L2[0] QDSS_CTI_TRIG0_OUT_MIRB	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger output 0 B	Y
E28	GPIO_3	QUP_L3[0]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
B28	GPIO_4	QUP_L0[1]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
B27	GPIO_5	QUP_L1[1]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
C27	GPIO_6	QUP_L2[1]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
D27	GPIO_7	QUP_L3[1]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
B25	GPIO_8	QUP_L0[2]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
B26	GPIO_9	QUP_L1[2]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
C26	GPIO_10	QUP_L2[2]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
D26	GPIO_11	QUP_L3[2]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
B24	GPIO_12	QUP_L0[3]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
B23	GPIO_13	QUP_L1[3]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
A22	GPIO_14	QUP_L2[3]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
A23	GPIO_15	QUP_L3[3]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
C30	GPIO_16	QUP_L0[4]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
E29	GPIO_17	QUP_L1[4]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
C31	GPIO_18	QUP_L2[4]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
D31	GPIO_19	QUP_L3[4]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
C29	GPIO_20	QUP_L0[6] GP_PDM_MIRB[2]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 General-purpose PDM output 2 B	N
B30	GPIO_21	QUP_L1[6] GP_PDM_MIRB[1]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 General-purpose PDM output 1 B	Y
C28	GPIO_22	QUP_L2[6] GP_PDM_MIRB[0]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 General-purpose PDM output 0 B	N
B29	GPIO_23	QUP_L3[6]	PX703	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
D25	GPIO_24	QUP_L0[7] QUP_L4_6_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
C25	GPIO_25	QUP_L1[7] QUP_L5_6_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
D24	GPIO_26	QUP_L2[7] QUP_L6_6_CS	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
C24	GPIO_27	QUP_L3[7]	PX702	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AK37	GPIO_28	QUP_L0[8] IBI_I3C_QUP8_SDA	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP8 In-Band interrupt I3C SDA	Y
AL39	GPIO_29	QUP_L1[8] IBI_I3C_QUP8_SCL	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP8 In-Band interrupt I3C SCL	N
AL38	GPIO_30	QUP_L2[8]	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AM39	GPIO_31	QUP_L3[8]	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AM38	GPIO_32	QUP_L0[9] IBI_I3C_QUP9_SDA	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP9 In-Band interrupt I3C SDA	Y
AN39	GPIO_33	QUP_L1[9] IBI_I3C_QUP9_SCL	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP9 In-Band interrupt I3C SCL	N
AN38	GPIO_34	QUP_L2[9]	PX707	PD:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AN37	GPIO_35	QUP_L3[9]	PX707	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AP38	GPIO_36	QUP_L0[10]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AR39	GPIO_37	QUP_L1[10]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AR38	GPIO_38	QUP_L2[10]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AT39	GPIO_39	QUP_L3[10]	PX706	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AT38	GPIO_40	QUP_L0[11] QUP_L4_10_CS	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AU39	GPIO_41	QUP_L1[11] QUP_L5_10_CS	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AU38	GPIO_42	QUP_L2[11] QUP_L6_10_CS	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AU37	GPIO_43	QUP_L3[11]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AJ38	GPIO_44	QUP_L0[12]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AK38	GPIO_45	QUP_L1[12]	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AK39	GPIO_46	QUP_L2[12] MDP_VSYNC_S_MIRB	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 MDP vertical sync – secondary B	Y
AJ39	GPIO_47	QUP_L3[12] DP_HOT_PLUG_DETECT MDP_VSYNC_P_MIRB FORCED_USB_BOOT	PX706	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 DisplayPort hot plug detect MDP vertical sync – primary B Forced USB boot	Y
AD36	GPIO_48	QUP_L0[13] QSPI_DATA[2] SDC4_DATA[2]	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI data Secure digital controller 4 data bit [2]	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AD35	GPIO_49	QUP_L1[13] QSPI_DATA[3] SDC4_DATA[3]	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI data Secure digital controller 4 data bit [3]	N
AE39	GPIO_50	QUP_L2[13] QSPI_CLK SDC4_CLK	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad SPI clock Secure digital controller 4 clock	Y
AE38	GPIO_51	QUP_L3[13] QSPI_CS_N_1 SDC4_CMD	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI chip select 1 Secure digital controller 4 command	Y
AE37	GPIO_52	QUP_L0[14] QSPI_DATA[0] SDC4_DATA[0]	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI data Secure digital controller 4 data bit [0]	N
AF39	GPIO_53	QUP_L1[14] QSPI_DATA[1] SDC4_DATA[1] GP_MN	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI data Secure digital controller 4 data bit [1] General-purpose M/N:D counter output	N
AF38	GPIO_54	QUP_L2[14] QSPI_CS_N_0	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Quad-SPI chip select 0	N
AG39	GPIO_55	QUP_L3[14]	PX705	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AJ1	GPIO_56	QUP_L0[15] IBI_I3C_QUP15_SDA	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP15 In-Band interrupt I3C SDA	Y
AJ2	GPIO_57	QUP_L1[15] IBI_I3C_QUP15_SCL	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP15 In-Band interrupt I3C SCL	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AJ3	GPIO_58	QUP_L2[15] QUP_L4_18_CS	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AH1	GPIO_59	QUP_L3[15] QUP_L5_18_CS BOOT_CONFIG[4]	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Boot configuration bit 4	Y
AH2	GPIO_60	QUP_L0[16] IBI_I3C_QUP16_SDA	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP16 In-Band interrupt I3C SDA	Y
AG1	GPIO_61	QUP_L1[16] IBI_I3C_QUP16_SCL	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QUP16 In-Band interrupt I3C SCL	N
AG2	GPIO_62	QUP_L2[16] QUP_L6_18_CS	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AF1	GPIO_63	QUP_L3[16] QUP_L4_19_CS	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AF2	GPIO_64	QUP_L0[17]	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AF3	GPIO_65	QUP_L1[17]	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AE1	GPIO_66	QUP_L2[17] QUP_L5_19_CS	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AE2	GPIO_67	QUP_L3[17] QUP_L6_19_CS BOOT_CONFIG[1]	PX715	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 Boot configuration bit 1	Y
AM5	GPIO_68	QUP_L0[18]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AL5	GPIO_69	QUP_L1[18]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AL3	GPIO_70	QUP_L2[18]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AL4	GPIO_71	QUP_L3[18]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AN3	GPIO_72	QUP_L0[19]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AN4	GPIO_73	QUP_L1[19]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AM3	GPIO_74	QUP_L2[19]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AM4	GPIO_75	QUP_L3[19]	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AR3	GPIO_76	QUP_L0[20]	PX713	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AR1	GPIO_77	QUP_L1[20]	PX713	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AR2	GPIO_78	QUP_L2[20]	PX713	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	N
AT2	GPIO_79	QUP_L3[20]	PX713	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4	Y
AP2	GPIO_80	QUP_L0[21] QDSS_CTI_TRIG0_OUT_MIRA	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger output 0 A	Y
AP3	GPIO_81	QUP_L1[21] QDSS_CTI_TRIG1_OUT_MIRA	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger output 1 A	Y
AP4	GPIO_82	QUP_L2[21] QDSS_CTI_TRIG1_IN_MIRA	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger input 1 A	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AN2	GPIO_83	QUP_L3[21] QDSS_CTI_TRIG0_IN_MIRA	PX714	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger input 0 A	Y
BA13	GPIO_84	QUP_L2[5] QDSS_CTI_TRIG0_IN_MIRB	PX712	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger input 0 B	Y
BB13	GPIO_85	QUP_L3[5] QDSS_CTI_TRIG1_IN_MIRB	PX712	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 QDSS trigger input 1 B	Y
AV38	GPIO_86	MDP_VSYNC_P_MIRA GCC_GP1_CLK_MIRB	PX707	PD:nppukp	Configurable I/O MDP vertical sync – primary A General-purpose Clock 1 B	Y
AW38	GPIO_87	MDP_VSYNC_S_MIRA GCC_GP2_CLK_MIRB	PX707	PD:nppukp	Configurable I/O MDP vertical sync – secondary A General-purpose Clock 2 B	Y
AY37	GPIO_88	MDP_VSYNC_E GCC_GP3_CLK_MIRB	PX707	PD:nppukp	Configurable I/O MDP vertical sync – external General-purpose Clock 3 B	Y
AW39	GPIO_89		PX707	PD:nppukp	Configurable I/O	Y
AY38	GPIO_90		PX707	PD:nppukp	Configurable I/O	Y
BA38	GPIO_91	USB_PHY_PS	PX707	PD:nppukp	Configurable I/O USB PHY port select USB CC direction 1.8 V push-pull tri-state output indicating USB Type-C connector orientation (CC1 or CC2 connection)	Y
AY2	GPIO_92	SD_CARD_DET	PX713	PD:nppukp	Configurable I/O SD card detect	Y
AW3	GPIO_93	SD_WRITE_PROTECT QDSS_CTI_TRIG1_OUT_MIRB	PX713	PD:nppukp	Configurable I/O Secure digital card write protection QDSS trigger output 1 B	N
AY3	GPIO_94	PCIE0_RST_N	PX713	PD:nppukp	Configurable I/O PCIe reset	N
BA2	GPIO_95	PCIE0_CLKREQN	PX713	PU:nppdkp	Configurable I/O PCIE0 clock request	Y
BA3	GPIO_96	PCIE0_WAKE_N	PX713	PD:nppukp	Configurable I/O PCIe wake	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AL2	GPIO_97	PCIE1_RST_N	PX714	PD:nppukp	Configurable I/O PCIe reset	N
AK5	GPIO_98	PCIE1_CLKREQN	PX714	PU:nppdkp	Configurable I/O PCIE1 clock request	Y
AK4	GPIO_99	PCIE1_WAKE_N	PX714	PD:nppukp	Configurable I/O PCIe wake	Y
U2	GPIO_100	CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB[0]	PX716	PD:nppukp	Configurable I/O Camera 0 MCLK 19.2 MHz QDSS trace data 0 B	N
V2	GPIO_101	CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB[1]	PX716	PD:nppukp	Configurable I/O Camera 1 MCLK 19.2 MHz QDSS trace data 1 B	N
V1	GPIO_102	CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB[2]	PX716	PD:nppukp	Configurable I/O Camera 2 MCLK 19.2 MHz QDSS trace data 2 B	N
V3	GPIO_103	CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB[3]	PX716	PD:nppukp	Configurable I/O Camera 3 MCLK 19.2 MHz QDSS trace data 3 B	N
W4	GPIO_104	CAM_MCLK4 QDSS_GPIO_TRACEDATA_LOCB[4]	PX716	PD:nppukp	Configurable I/O Camera 4 MCLK 19.2 MHz QDSS trace data 4 B	N
W3	GPIO_105	CAM_MCLK5 QDSS_GPIO_TRACEDATA_LOCB[5]	PX716	PD:nppukp	Configurable I/O Camera 5 MCLK 19.2 MHz QDSS trace data 5 B	N
W2	GPIO_106	CAM_MCLK6 QDSS_GPIO_TRACEDATA_LOCB[11]	PX716	PD:nppukp	Configurable I/O Camera 6 MCLK 19.2 MHz QDSS trace data 11 B	N
W1	GPIO_107	CAM_MCLK7 QDSS_GPIO_TRACEDATA_LOCB[12]	PX716	PD:nppukp	Configurable I/O Camera 7 MCLK 19.2 MHz QDSS trace data 12 B	N
AW12	GPIO_108	AON_CAM_RESET	PX712	PD:nppukp	Configurable I/O AON camera reset	N
AD2	GPIO_109	CCI_ASYNC_IN0	PX715	PD:nppukp	Configurable I/O Camera control interface async 0	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
Y2	GPIO_110	CCI_I2C_SDA0 QDSS_GPIO_TRACEDATA_LOCB[7]	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 serial data QDSS trace data 7 B	N
Y1	GPIO_111	CCI_I2C_SCL0 QDSS_GPIO_TRACEDATA_LOCB[8]	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 clock QDSS trace data 8 B	N
AA1	GPIO_112	CCI_I2C_SDA1 QDSS_GPIO_TRACECLK_LOCB	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 serial data QDSS trace clock B	N
AA2	GPIO_113	CCI_I2C_SCL1 QDSS_GPIO_TRACECTL_LOCB	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 clock QDSS trace control B	N
AB2	GPIO_114	CCI_I2C_SDA2 QDSS_GPIO_TRACEDATA_LOCB[9]	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 2 serial data QDSS trace data 9 B	N
AB1	GPIO_115	CCI_I2C_SCL2 QDSS_GPIO_TRACEDATA_LOCB[10]	PX716	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 2 clock QDSS trace data 10 B	Y
AE3	GPIO_116	CCI_TIMER0	PX715	PD:nppukp	Configurable I/O Camera 0 control interface timer	Y
AC3	GPIO_117	CCI_TIMER1 QDSS_GPIO_TRACEDATA_LOCB[6]	PX716	PD:nppukp	Configurable I/O Camera 1 control interface timer QDSS trace data 6 B	Y
AD1	GPIO_118	CCI_TIMER2 QDSS_GPIO_TRACEDATA_LOCB[13]	PX715	PD:nppukp	Configurable I/O Camera 2 control interface timer QDSS trace data 13 B	Y
AC1	GPIO_119	CCI_TIMER3 CCI_ASYNC_IN1 QDSS_GPIO_TRACEDATA_LOCB[14]	PX716	PD:nppukp	Configurable I/O Camera 3 control interface timer Camera control interface async 1 QDSS trace data 14 B	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AC2	GPIO_120	CCI_TIMER4 CCI_ASYNC_IN2 QDSS_GPIO_TRACEDATA_LOCB[15]	PX716	PD:nppukp	Configurable I/O Camera 4 control interface timer Camera control interface async 2 QDSS trace data 15 B	N
AW11	GPIO_121	I2S2_SCK	PX712	PD:nppukp	Configurable I/O I2S 2 clock	N
AY11	GPIO_122	I2S2_DATA0	PX712	PD:nppukp	Configurable I/O I2S 2 serial data channel 0	N
BA11	GPIO_123	I2S2_WS	PX712	PD:nppukp	Configurable I/O I2S 2 serial data word select	N
AY10	GPIO_124	I2S2_DATA1 SEC_I2S_MCLK AUDIO_REF_CLK	PX712	PD:nppukp	Configurable I/O I2S 2 serial data channel 1 Secondary I2S master clock Audio reference clock	N
BA10	GPIO_125	PRI_I2S_MCLK	PX712	PD:nppukp	Configurable I/O Primary I2S master clock	N
BA9	GPIO_126	I2S0_SCK GP_PDM_MIRA[0]	PX712	PD:nppukp	Configurable I/O I2S 0 clock General-purpose PDM output 0 A	N
AY8	GPIO_127	I2S0_DATA0 GP_PDM_MIRA[1]	PX712	PD:nppukp	Configurable I/O I2S 0 serial data channel 0 General-purpose PDM output 1 A	N
BA8	GPIO_128	I2S0_DATA1 GP_PDM_MIRA[2]	PX712	PD:nppukp	Configurable I/O I2S 0 serial data channel 1 General-purpose PDM output 2 A	N
AY7	GPIO_129	I2S0_WS	PX712	PD:nppukp	Configurable I/O I2S 0 serial data word select	N
BA7	GPIO_130	UIM0_DATA	PX5	PD:nppukp	Configurable I/O UIM0 data	N
AY6	GPIO_131	UIM0_CLK	PX5	PD:nppukp	Configurable I/O UIM0 clock	N
BA6	GPIO_132	UIM0_RESET	PX5	PD:nppukp	Configurable I/O UIM0 reset	N
BA5	GPIO_133	UIM0_PRESENT	PX5	PD:nppukp	Configurable I/O UIM0 presence detection	Y
AY5	GPIO_134	UIM1_DATA GCC_GP1_CLK_MIRA	PX5	PD:nppukp	Configurable I/O UIM1 data General-purpose Clock 1 A	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BB4	GPIO_135	UIM1_CLK GCC_GP2_CLK_MIRA	PX5	PD:nppukp	Configurable I/O UIM1 clock General-purpose Clock 2 A	N
BA4	GPIO_136	UIM1_RESET GCC_GP3_CLK_MIRA	PX5	PD:nppukp	Configurable I/O UIM1 reset General-purpose Clock 3 A	N
AY4	GPIO_137	UIM1_PRESENT	PX5	PD:nppukp	Configurable I/O UIM1 presence detection	Y
AB39	GPIO_138	RFFE0_CLK GRFC0	PX704	PD:nppukp	Configurable I/O RF front end 0 interface clock Generic RF controller bit 0	N
AB38	GPIO_139	RFFE0_DATA GRFC1	PX704	PD:nppukp	Configurable I/O RF front end 0 interface data Generic RF controller bit 1	N
AB36	GPIO_140	RFFE1_CLK GRFC2	PX704	PD:nppukp	Configurable I/O RF front end 1 interface clock Generic RF controller bit 2	N
AB35	GPIO_141	RFFE1_DATA GRFC3	PX704	PD:nppukp	Configurable I/O RF front end 1 interface data Generic RF controller bit 3	N
AC39	GPIO_142	RFFE2_CLK GRFC4	PX705	PD:nppukp	Configurable I/O RF front end 2 interface clock Generic RF controller bit 4	N
AC38	GPIO_143	RFFE2_DATA GRFC5	PX705	PD:nppukp	Configurable I/O RF front end 2 interface data Generic RF controller bit 5	N
AD38	GPIO_144	RFFE3_CLK GRFC6	PX705	PD:nppukp	Configurable I/O RF front end 3 interface clock Generic RF controller bit 6	N
AD39	GPIO_145	RFFE3_DATA GRFC7	PX705	PD:nppukp	Configurable I/O RF front end 3 interface data Generic RF controller bit 7	N
AC36	GPIO_146	RFFE4_CLK GRFC8	PX705	PD:nppukp	Configurable I/O RF front end 4 interface clock Generic RF controller bit 8	N
AC35	GPIO_147	RFFE4_DATA GRFC9	PX705	PD:nppukp	Configurable I/O RF front end 4 interface data Generic RF controller bit 9	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AH38	GPIO_148	WLAN_COEX_UART1_RX	PX706	PD:nppukp	Configurable I/O Interface between WCN6855/6856 and SM8475	Y
AH37	GPIO_149	WLAN_COEX_UART1_TX BOOT_CONFIG[5]	PX706	PD:nppukp	Configurable I/O Interface between WCN6855/6856 and SM8475 Boot configuration bit 5	N
AG38	GPIO_150	GRFC10	PX706	PD:nppukp	Configurable I/O Generic RF controller bit 10	Y
AH39	GPIO_151	GRFC11	PX706	PD:nppukp	Configurable I/O Generic RF controller bit 11	N
AD37	GPIO_152	GRFC12	PX705	PD:nppukp	Configurable I/O Generic RF controller bit 12	N
AC37	GPIO_153	GRFC0_MIRA	PX705	PD:nppukp	Configurable I/O Generic RF controller bit	Y
AA35	GPIO_154		PX704	PD:nppukp	Configurable I/O	Y
AB37	GPIO_155		PX704	PD:nppukp	Configurable I/O	Y
Y36	GPIO_156	QLINK0_REQUEST	PX704	PD:nppukp	Configurable I/O QLINK 0 REQUEST for SDR735_0, SDR0_QLINK0_REQ	Y
Y35	GPIO_157	QLINK0_ENABLE	PX704	PD:nppukp	Configurable I/O QLINK 0 ENABLE 0 for SDR735_0, SDR0_QLINK0_EN	N
AA39	GPIO_158	QLINK0_WMSS_RESET_N BOOT_CONFIG[2]	PX704	PD:nppukp	Configurable I/O QLINK 0 modem subsystem reset output for SDR735_0, SDR0_QLINK0_WMSS_RESET_N Boot configuration bit 2	N
Y39	GPIO_159	QLINK1_REQUEST	PX704	PD:nppukp	Configurable I/O QLINK 1 REQUEST for SMR546, QLINK1_REQ	Y
Y38	GPIO_160	QLINK1_ENABLE	PX704	PD:nppukp	Configurable I/O QLINK 1 ENABLE for SMR546, QLINK1_EN	N
Y37	GPIO_161	QLINK1_WMSS_RESET_N BOOT_CONFIG[3]	PX704	PD:nppukp	Configurable I/O QLINK 1 modem subsystem reset output for SMR546 WMSS_RESETN pin, QLINK1_WMSS_RESET_N Boot configuration bit 3	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AA38	GPIO_162	QLINK2_REQUEST	PX704	PD:nppukp	Configurable I/O QLINK 2 REQUEST for SDR735_1, SDR1_QLINK2_REQ	Y
AA37	GPIO_163	QLINK2_ENABLE	PX704	PD:nppukp	Configurable I/O QLINK 2 ENABLE 2 for SDR735_1, SDR1_QLINK2_EN	N
AA36	GPIO_164	QLINK2_WMSS_RESET_N BOOT_CONFIG[0]	PX704	PD:nppukp	Configurable I/O QLINK 2 modem subsystem reset output for SDR735_1, SDR1_QLINK2_WMSS_RESET_N Boot configuration bit 0	N
BA20	GPIO_165	LPASS_0 LPASS_0:SWR_TX_CLK LPASS_0:LPI_QUA_MI2S_SCK	PX709	PD:nppukp	Configurable I/O LPASS I/O 0 SoundWire transmit clock LPI I2S clock	N
AW19	GPIO_166	LPASS_1 LPASS_1:SWR_TX_DATA0 LPASS_1:LPI_QUA_MI2S_WS	PX709	PD:nppukp	Configurable I/O LPASS I/O 1 SoundWire transmit data 0 LPI I2S serial data word select	Y
AY19	GPIO_167	LPASS_2 LPASS_2:SWR_TX_DATA1 LPASS_2:LPI_QUA_MI2S_ DATA0	PX709	PD:nppukp	Configurable I/O LPASS I/O 2 SoundWire transmit data 1 LPI I2S serial data channel 0	N
BA19	GPIO_168	LPASS_3 LPASS_3:SWR_RX_CLK LPASS_3:LPI_QUA_MI2S_ DATA1	PX709	PD:nppukp	Configurable I/O LPASS I/O 3 SoundWire receive clock LPI I2S serial data channel 1	N
AW18	GPIO_169	LPASS_4 LPASS_4:SWR_RX_DATA0 LPASS_4:LPI_QUA_MI2S_ DATA2	PX709	PD:nppukp	Configurable I/O LPASS I/O 4 SoundWire receive data 0 LPI I2S serial data channel 2	Y
AY18	GPIO_170	LPASS_5 LPASS_5:SWR_RX_DATA1 LPASS_5:EXT_MCLK1_C LPASS_5:LPI_QUA_MI2S_ DATA3	PX709	PD:nppukp	Configurable I/O LPASS I/O 5 SoundWire receive data 1 External MCLK 1C LPI I2S serial data channel 3	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BA26	GPIO_171	LPASS_6 LPASS_6:LPI_DMIC1_CLK LPASS_6:LPI_I2S1_CLK	PX709	PD:nppukp	Configurable I/O LPASS I/O 6 DMIC1 clock LPI I2S 1 clock	Y
BB26	GPIO_172	LPASS_7 LPASS_7:LPI_DMIC1_DATA LPASS_7:LPI_I2S1_WS	PX709	PD:nppukp	Configurable I/O LPASS I/O 7 DMIC1 data LPI I2S 1 serial data word select	Y
AY25	GPIO_173	LPASS_8 LPASS_8:LPI_DMIC2_CLK LPASS_8:LPI_I2S1_DATA0	PX709	PD:nppukp	Configurable I/O LPASS I/O 8 DMIC2 clock LPI I2S 1 serial data channel 0	N
BA25	GPIO_174	LPASS_9 LPASS_9:LPI_DMIC2_DATA LPASS_9:LPI_I2S1_DATA1 LPASS_9:EXT_MCLK1_B	PX709	PD:nppukp	Configurable I/O LPASS I/O 9 DMIC2 data LPI I2S 1 serial data channel 1 External MCLK 1 B	Y
BB25	GPIO_175	LPASS_10 LPASS_10:LPI_I2S2_CLK LPASS_10:WSA_SWR_CLK	PX709	PD:nppukp	Configurable I/O LPASS I/O 10 LPI I2S 2 clock SoundWire clock for WSA	N
AY24	GPIO_176	LPASS_11 LPASS_11:LPI_I2S2_WS LPASS_11:WSA_SWR_DATA	PX709	PD:nppukp	Configurable I/O LPASS I/O 11 LPI I2S 2 serial data serial data word select SoundWire data for WSA	Y
AW20	GPIO_177	LPASS_12 LPASS_12:LPI_DMIC3_CLK	PX709	PD:nppukp	Configurable I/O LPASS I/O 12 DMIC 3 clock	Y
AY20	GPIO_178	LPASS_13 LPASS_13:LPI_DMIC3_DATA LPASS_13:EXT_MCLK1_A	PX709	PD:nppukp	Configurable I/O LPASS I/O 13 DMIC3 data External MCLK 1 A	N
BA18	GPIO_179	LPASS_14 LPASS_14:SWR_TX_DATA2 LPASS_14:EXT_MCLK1_D	PX709	PD:nppukp	Configurable I/O LPASS I/O 14 SoundWire transmit data 2 External MCLK 1 D	N
BA22	GPIO_180	LPASS_15 LPASS_15:LPI_I2S2_DATA0 LPASS_15:WSA2_SWR_CLK	PX709	PD:nppukp	Configurable I/O LPASS I/O 15 LPI I2S 2 serial data channel 0 SoundWire clock for WSA2	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AW21	GPIO_181	LPASS_16 LPASS_16:LPI_I2S2_DATA1 LPASS_16:WSA2_SWR_DATA	PX709	PD:nppukp	Configurable I/O LPASS I/O 16 LPI I2S 2 serial data channel 1 SoundWire data for WSA2	Y
AY21	GPIO_182	LPASS_17 LPASS_17:LPI_DMIC4_CLK0	PX709	PD:nppukp	Configurable I/O LPASS I/O 17 DMIC 4 clock	Y
BA21	GPIO_183	LPASS_18 LPASS_18:LPI_DMIC4_DATA	PX709	PD:nppukp	Configurable I/O LPASS I/O 18 DMIC4 data	N
BA24	GPIO_184	LPASS_19 LPASS_19:LPI_I2S3_CLK LPASS_19:SLIMBUS_CLK	PX709	PD:nppukp	Configurable I/O LPASS I/O 19 LPI I2S 3 clock LPASS SLIMbus clock	N
AY23	GPIO_185	LPASS_20 LPASS_20:LPI_I2S3_WS LPASS_20:SLIMBUS_DATA	PX709	PD:nppukp	Configurable I/O LPASS I/O 20 LPI I2S 3 serial data serial data word select LPASS SLIMbus data	Y
BA23	GPIO_186	LPASS_21 LPASS_21:LPI_I2S3_DATA0	PX709	PD:nppukp	Configurable I/O LPASS I/O 21 LPI I2S 3 serial data channel 0	N
AY22	GPIO_187	LPASS_22 LPASS_22:LPI_I2S3_DATA1 LPASS_22:EXT_MCLK1_E	PX709	PD:nppukp	Configurable I/O LPASS I/O 22 LPI I2S 3 serial data channel 1 External MCLK 1 E	Y
AW28	GPIO_188	QDSS_GPIO_TRACEDATA_LOCA[0] SSC_0	PX709	PD:nppukp	Configurable I/O QDSS trace data 0 A SSC IO 0	Y
AY28	GPIO_189	QDSS_GPIO_TRACEDATA_LOCA[1] SSC_1	PX709	PD:nppukp	Configurable I/O QDSS trace data 1 A SSC_IO 1	N
BA28	GPIO_190	QDSS_GPIO_TRACEDATA_LOCA[2] SSC_2	PX709	PD:nppukp	Configurable I/O QDSS trace data 2 A SSC_IO 2	Y
BB28	GPIO_191	QDSS_GPIO_TRACEDATA_LOCA[3] SSC_3	PX709	PD:nppukp	Configurable I/O QDSS trace data 3 A SSC_IO 3	N

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
AW27	GPIO_192	QDSS_GPIO_TRACEDATA_LOCA[4] SSC_4	PX709	PD:nppukp	Configurable I/O QDSS trace data 4 A SSC_IO 4	Y
AY27	GPIO_193	QDSS_GPIO_TRACEDATA_LOCA[5] SSC_5	PX709	PD:nppukp	Configurable I/O QDSS trace data 5 A SSC_IO 5	N
BA27	GPIO_194	QDSS_GPIO_TRACEDATA_LOCA[6] SSC_6	PX709	PD:nppukp	Configurable I/O QDSS trace data 6 A SSC_IO 6	N
BB27	GPIO_195	QDSS_GPIO_TRACEDATA_LOCA[7] SSC_7	PX709	PD:nppukp	Configurable I/O QDSS trace data 7 A SSC_IO 7	Y
AW26	GPIO_196	QDSS_GPIO_TRACECTL_LOCA SSC_8	PX709	PD:nppukp	Configurable I/O QDSS trace control A SSC IO 8	N
AY26	GPIO_197	QDSS_GPIO_TRACECLK_LOCA SSC_9	PX709	PD:nppukp	Configurable I/O QDSS trace clock A SSC IO 9	N
BA33	GPIO_198	QDSS_GPIO_TRACEDATA_LOCA[8] SSC_10	PX709	PD:nppukp	Configurable I/O QDSS trace data 8 A SSC IO 10	N
BA32	GPIO_199	QDSS_GPIO_TRACEDATA_LOCA[9] SSC_11	PX709	PD:nppukp	Configurable I/O QDSS trace data 9 A SSC IO 11	N
AY31	GPIO_200	QDSS_GPIO_TRACEDATA_LOCA[10] SSC_12	PX709	PD:nppukp	Configurable I/O QDSS trace data 10 A SSC IO 12	N
AY30	GPIO_201	QDSS_GPIO_TRACEDATA_LOCA[11] SSC_13	PX709	PD:nppukp	Configurable I/O QDSS trace data 11 A SSC IO 13	Y

Table 2-3 MSM bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wakeup function? (yes/no)
			Voltage	Type		
BA30	GPIO_202	QDSS_GPIO_TRACEDATA_LOCA[12] SSC_14	PX709	PD:nppukp	Configurable I/O QDSS trace data 12 A SSC IO 14	N
AW29	GPIO_203	QDSS_GPIO_TRACEDATA_LOCA[13] SSC_15	PX709	PD:nppukp	Configurable I/O QDSS trace data 13 A SSC IO 15	Y
AY29	GPIO_204	QDSS_GPIO_TRACEDATA_LOCA[14] SSC_16	PX709	PD:nppukp	Configurable I/O QDSS trace data 14 A SSC IO 16	N
BA29	GPIO_205	QDSS_GPIO_TRACEDATA_LOCA[15] SSC_17	PX709	PD:nppukp	Configurable I/O QDSS trace data 15 A SSC IO 17	Y
BA14	GPIO_206	QUP_L0[5] SSC_18	PX712	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 SSC IO 18	N
BB14	GPIO_207	QUP_L1[5] SSC_19	PX712	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 SSC IO 19	N
AY12	GPIO_208	CCI_I2C_SDA3 SSC_20	PX712	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 3 serial data SSC IO 20	N
BA12	GPIO_209	CCI_I2C_SCL3 SSC_21	PX712	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 3 serial clock SSC IO 21	N

1. See Table 2-1 for the parameter and acronym definitions.

Table 2-4 QUP lane to GPIO mapping

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I2C	I3C	SPI [1]	UART	HS-UART
QUP[0]	L0	GPIO_0	SDA		MISO	CTS	
	L1	GPIO_1	SCL		MOSI	RFR	
	L2	GPIO_2			SCLK	TX	
	L3	GPIO_3			CS_0	RX	
QUP[1]	L0	GPIO_4	SDA		MISO	CTS	
	L1	GPIO_5	SCL		MOSI	RFR	
	L2	GPIO_6			SCLK	TX	
	L3	GPIO_7			CS_0	RX	
QUP[2]	L0	GPIO_8	SDA		MISO	CTS	
	L1	GPIO_9	SCL		MOSI	RFR	
	L2	GPIO_10			SCLK	TX	
	L3	GPIO_11			CS_0	RX	
QUP[3]	L0	GPIO_12	SDA		MISO	CTS	
	L1	GPIO_13	SCL		MOSI	RFR	
	L2	GPIO_14			SCLK	TX	
	L3	GPIO_15			CS_0	RX	
QUP[4]	L0	GPIO_16	SDA		MISO	CTS	
	L1	GPIO_17	SCL		MOSI	RFR	
	L2	GPIO_18			SCLK	TX	
	L3	GPIO_19			CS_0	RX	
QUP[5] [2]	L0	GPIO_206	SDA		MISO	CTS	
	L1	GPIO_207	SCL		MOSI	RFR	
	L2	GPIO_84			SCLK	TX	
	L3	GPIO_85			CS_0	RX	
QUP[6]	L0	GPIO_20	SDA		MISO	CTS	CTS
	L1	GPIO_21	SCL		MOSI	RFR	RFR
	L2	GPIO_22			SCLK	TX	TX
	L3	GPIO_23			CS_0	RX	RX
	L4	GPIO_24			CS_1		
	L5	GPIO_25			CS_2		
	L6	GPIO_26			CS_3		

Table 2-4 QUP lane to GPIO mapping (cont.)

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I^2C	I3C	SPI [1]	UART	HS-UART
QUP[7]	L0	GPIO_24	SDA		MISO	CTS	CTS
	L1	GPIO_25	SCL		MOSI	RFR	RFR
	L2	GPIO_26			SCLK	TX	TX
	L3	GPIO_27			CS_0	RX	RX
QUP[8]	L0	GPIO_28	SDA	SDA	MISO	CTS	
	L1	GPIO_29	SCL	SCL	MOSI	RFR	
	L2	GPIO_30			SCLK	TX	
	L3	GPIO_31			CS_0	RX	
QUP[9]	L0	GPIO_32	SDA	SDA	MISO	CTS	
	L1	GPIO_33	SCL	SCL	MOSI	RFR	
	L2	GPIO_34			SCLK	TX	
	L3	GPIO_35			CS_0	RX	
QUP[10]	L0	GPIO_36	SDA		MISO	CTS	
	L1	GPIO_37	SCL		MOSI	RFR	
	L2	GPIO_38			SCLK	TX	
	L3	GPIO_39			CS_0	RX	
	L4	GPIO_40			CS_1		
	L5	GPIO_41			CS_2		
	L6	GPIO_42			CS_3		
QUP[11]	L0	GPIO_40	SDA		MISO	CTS	
	L1	GPIO_41	SCL		MOSI	RFR	
	L2	GPIO_42			SCLK	TX	
	L3	GPIO_43			CS_0	RX	
QUP[12]	L0	GPIO_44	SDA		MISO	CTS	CTS
	L1	GPIO_45	SCL		MOSI	RFR	RFR
	L2	GPIO_46			SCLK	TX	TX
	L3	GPIO_47			CS_0	RX	RX
QUP[13]	L0	GPIO_48	SDA		MISO	CTS	CTS
	L1	GPIO_49	SCL		MOSI	RFR	RFR
	L2	GPIO_50			SCLK	TX	TX
	L3	GPIO_51			CS_0	RX	RX
QUP[14]	L0	GPIO_52	SDA		MISO	CTS	CTS
	L1	GPIO_53	SCL		MOSI	RFR	RFR
	L2	GPIO_54			SCLK	TX	TX
	L3	GPIO_55			CS_0	RX	RX

Table 2-4 QUP lane to GPIO mapping (cont.)

QUP	Lane	GPIO	TLMM QUP Lane to GPIO Mapping				
			I^2C	I3C	SPI [1]	UART	HS-UART
QUP[15]	L0	GPIO_56	SDA	SDA	MISO	CTS	
	L1	GPIO_57	SCL	SCL	MOSI	RFR	
	L2	GPIO_58			SCLK	TX	
	L3	GPIO_59			CS_0	RX	
QUP[16]	L0	GPIO_60	SDA	SDA	MISO	CTS	
	L1	GPIO_61	SCL	SCL	MOSI	RFR	
	L2	GPIO_62			SCLK	TX	
	L3	GPIO_63			CS_0	RX	
QUP[17]	L0	GPIO_64	SDA		MISO	CTS	
	L1	GPIO_65	SCL		MOSI	RFR	
	L2	GPIO_66			SCLK	TX	
	L3	GPIO_67			CS_0	RX	
QUP[18]	L0	GPIO_68	SDA		MISO	CTS	
	L1	GPIO_69	SCL		MOSI	RFR	
	L2	GPIO_70			SCLK	TX	
	L3	GPIO_71			CS_0	RX	
	L4	GPIO_58			CS_1		
	L5	GPIO_59			CS_2		
	L6	GPIO_62			CS_3		
QUP[19]	L0	GPIO_72	SDA		MISO	CTS	CTS
	L1	GPIO_73	SCL		MOSI	RFR	RFR
	L2	GPIO_74			SCLK	TX	TX
	L3	GPIO_75			CS_0	RX	RX
	L4	GPIO_63			CS_1		
	L5	GPIO_66			CS_2		
	L6	GPIO_67			CS_3		
QUP[20]	L0	GPIO_76	SDA		MISO	CTS	CTS
	L1	GPIO_77	SCL		MOSI	RFR	RFR
	L2	GPIO_78			SCLK	TX	TX
	L3	GPIO_79			CS_0	RX	RX
QUP[21]	L0	GPIO_80	SDA		MISO	CTS	CTS
	L1	GPIO_81	SCL		MOSI	RFR	RFR
	L2	GPIO_82			SCLK	TX	TX
	L3	GPIO_83			CS_0	RX	RX

1. SM8475/SM8475P QUP SPI interfaces are master only.

2. QUP[5] SPI interface supports speed up to 25 MHz. All other SPI interfaces support up to 50 MHz.

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins

Pad #	Pad name	Functional description
A1, A39, BB1, BB39	NC	No connect; not connected internally.
AL1, AM1, AE8, AF19, AJ24, M33, K17, D29, AY9, AN5, AT3, AW37, Y3, AD8, AF20, AG24, AJ25, AP23, J8, L33, AE16, AA24, J17	DNC	Do not connect; connected internally, do not connect externally.

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
A15, A18, A2, A25, A27, A3, A30, A33, A35, A37, A38, A4, A6, A8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA26, AA28, AA3, AA30, AA32, AA6, AA8, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AB25, AB27, AB29, AB3, AB31, AB33, AB6, AB7, AB9, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC24, AC28, AC4, AC5, AC8, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD29, AD3, AD33, AD9, AE6, AE10, AE12, AE14, AE18, AE20, AE22, AE24, AE28, AE35, AE36, AE4, AE5, AF11, AF13, AF15, AF17, AF21, AF23, AF29, AF33, AF37, AF4, AF5, AF7, AF9, AG10, AG12, AG14, AG16, AG18, AG20, AG22, AG28, AG3, AG37, AG8, AH11, AH13, AH15, AH19, AH21, AH23, AH27, AH29, AH3, AH31, AH33, AH34, AH36, AH7, AH9, AJ12, AJ14, AJ20, AJ22, AJ26, AJ28, AJ30, AJ32, AJ37, AJ4, AJ5, AK1, AK11, AK13, AK15, AK19, AK21, AK25, AK33, AK36, AK7, AL12, AL14, AL20, AL22, AL24, AL26, AL32, AL37, AM11, AM13, AM15, AM19, AM21, AM25, AM37, AM7, AN12, AN14, AN16, AN18, AN20, AN24, AN26, AN28, AN30, AN32, AN35, AN36, AP11, AP13, AP15, AP17, AP19, AP25, AP27, AP29, AP31, AP33, AP37, AP39, AP5, AP7, AP9, AR16, AR18, AR20, AR21, AR22, AR23, AR24, AR26, AR28, AR37, AR4, AR5, AR8, AT10, AT16, AT17, AT19, AT20, AT21, AT22, AT25, AT27, AT29, AT34, AT37, AT6, AT9, AU10, AU11, AU12, AU13, AU16, AU19, AU22, AU23, AU25, AU26, AU28, AU29, AU3, AU30, AU31, AU32, AU33, AU34, AU35, AU36, AU6, AU7, AU8, AU9, AV11, AV12, AV13, AV14, AV16, AV20, AV22, AV23, AV24, AV26, AV27, AV28, AV29, AV3, AV30, AV31, AV32, AV33, AV34, AV37, AV6, AV7, AV8, AV9, AW10, AW13, AW14, AW15, AW17, AW22, AW23, AW24, AW25, AW30, AW31, AW32, AW33, AW34, AW35, AW36, AW4, AW6, AW7, AW8, AW9, AY1, AY14, AY16, AY33, AY36, AY39, B1, B11, B12, B15, B18, B20, B22, B32, B33, B35, B37, B39, B4, B6, B8, BA1, BA16, BA31, BA34, BA37, BA39, BB12, BB15, BB16, BB18, BB2, BB22, BB24, BB3, BB30, BB33, BB37, BB38, BB5, BB9, C1, C10, C11, C12, C13, C2, C32, C34, C36, C37, C39, C6, D1, D10, D11, D12, D13, D2, D32, D34, D36, D37, D38, D39, D6, E10, E11, E12, E13, E14, E15, E16, E17, E19, E20, E22, E23, E24, E25, E26, E27, E3, E31, E32, E33, E34, E35, E37, E4, E5, E6, E7, E8, E9, F1, F10, F11, F12, F13, F14, F15, F17, F18, F23, F24, F25, F26, F27, F28, F29, F30, F33, F34, F36, F38, F39, F4, F5, F6, F7, F9, G13, G14, G16, G20, G22, G24, G25, G3, G30, G32, G33, G34, G35, G36, G38, G39, G6, G7, G8, H1, H13, H17, H19, H21, H23, H31, H37, H4, J10, J12, J14, J16, J18, J20, J22, J24, J26, J28, J3, J30, J32, J35, J36, J37, J38, J39, J6, J7, K1, K11, K13, K15, K2, K25, K27, K29, K3, K31, K33, K34, K37, K4, K9, L10, L12, L14, L16, L18, L24, L26, L28, L3, L30, L32, L37, L6, L8, M1, M11, M13, M15, M17, M25, M27, M29, M31, M35, M36, M37, M38, M39, M4, M5, M6, M7, M9, N10, N12, N14, N16, N18, N20, N24, N26, N28, N3, N30, N32, N37, N6, N8, P1, P11, P13, P15, P17, P19, P21, P23, P25, P27, P29, P31, P33, P37, P4, P9, R10, R12, R14, R16, R18, R24, R26, R3, R32, R34, R36, R37, R38, R39, R6, R8, T1, T11, T13, T15, T17, T2, T25, T3, T33, T37, T4, T9, U10, U12, U14, U16, U18, U24, U26, U3, U32, U35, U36, U37, U38, U39, U6, U7, U8, V11, V13, V15, V17, V19, V21, V23, V25, V27, V29, V31, V33, V34, V37, V4, V5, V6, V9, W10, W12, W14, W16, W18, W20, W22, W24, W26, W28, W30, W32, W36, W37, W38, W39, W5, W8, Y11, Y13, Y15, Y17, Y19, Y21, Y23, Y25, Y27, Y29, Y31, Y33, Y4, Y5, Y6, Y7, Y9	GND	Ground

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
A26, B13, BB17, BB29	LPDDR5_VDD1	Power for PoP DDR memory core – 1.8 V Nom (bottom LPDDR5_VDD1)
A10, A11, A31, A32, B10, B31, BB34, BB35, BB36, BB6, BB7, BB8	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core – 1.05 V Nom (bottom LPDDR5_VDD2H)
A20, A21, B21, BB19, BB20, BB21	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core – 0.9 V Nom (bottom LPDDR5_VDD2L)
A12, A13, A28, A29, BB10, BB11, BB31, BB32	LPDDR5_VDDQ	Power for PoP DDR pads 0.5 V Nom (bottom LPDDR5_VDDQ)
AV17	VDD_1P2_PX0	VDD 1.2 V for PX0 pads
AC11, AC13, AC9, AD10, AD12, AD14, AE11, AE13, AE15, AE9, AF10, AF12, AF14, AF8, AG11, AG13, AG7, AG9, AH12, AH14, AJ13, AK12, AK14, AL13	VDD_APC0	Power for the Kryo Silver application processor
AF16, AF18, AG15, AG17, AG19, AH10, AH20, AH8, AJ11, AJ15, AJ19, AJ7, AK20, AL11, AL15, AL19, AL7, AM12, AM14, AN11, AN13, AN15, AN17, AN19, AN7, AP10, AP12, AP14, AP16, AP18, AP8, AR15, AR17, AR19, AR9, AT18	VDD_APC1	Power for the Kryo Gold application processor
AU14	VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits
K7	VDD_A_CSI_01_0P9	Power for MIPI CSI01 0.9 V analog circuits
L7, P7, T7	VDD_A_CSI_1P2	Power for MIPI CSI 1.2 V analog circuits
N7	VDD_A_CSI_23_0P9	Power for MIPI CSI23 0.9 V analog circuits
R7	VDD_A_CSI_45_0P9	Power for MIPI CSI45 0.9 V analog circuits
H16	VDD_A_DSI_01_0P9	Power for MIPI DSI01 0.9 V analog circuits
G15	VDD_A_DSI_01_1P2	Power for MIPI DSI01 1.2 V analog circuits
H15	VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI01 PLL 0.9 V analog circuits
G10, G11, G9	VDD_A_EBI_0	Power for EBI0 PHY analog circuits
G12	VDD_A_EBI_0_PLL_0P9	Power for EBI0 PLL analog 0.9 V circuits
AT11, AT12, AT13	VDD_A_EBI_1	Power for EBI1 PHY analog circuits

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AT14	VDD_A_EBI_1_PLL_0P9	Power for EBI 1 PLL analog 0.9 V circuits
G26, G27, G28	VDD_A_EBI_2	Power for EBI2 PHY analog circuits
G29	VDD_A_EBI_2_PLL_0P9	Power for EBI2 PLL analog 0.9 V circuits
AT30, AT31, AT32	VDD_A_EBI_3	Power for EBI3 PHY analog circuits
AT33	VDD_A_EBI_3_PLL_0P9	Power for EBI3 PLL analog 0.9 V circuits
AP34	VDD_A_EUSB_HS_0P9	Power for the eUSB2 high-speed 0.9 V analog circuits
AR34	VDD_A_EUSB_HS_1P2	Power for the eUSB2 high-speed 1.2 V analog circuits
AH25	VDD_A_GFX_CS_1P2	Power for GFX Current Sensor 1.2 V analog circuits
N22	VDD_A_NSP_CS_1P2	Power for NSP Current Sensor 1.2 V analog circuits
AM6	VDD_A_PCIE_0_0P9	Power for PCIe0, 0.9 V analog circuits
AN6	VDD_A_PCIE_0_1P2	Power for PCIe0, 1.2 V analog circuits
AC7, AD7	VDD_A_PCIE_1_0P9	Power for PCIe1, 0.9 V analog circuits
AE7	VDD_A_PCIE_1_1P2	Power for PCIe1, 1.2 V analog circuits
T34	VDD_A_QLINK_0_0P9	Power for the QLink 0 0.9 V analog circuits
W34	VDD_A_QLINK_0_1P2	Power for the QLink 0 1.2 V analog circuits
U34	VDD_A_QLINK_0_CK_0P9	Power for Qlink 0 clock, 0.9 V analog circuits
J34, L34	VDD_A_QLINK_1_0P9	Power for the QLink 1 0.9 V analog circuits
H34	VDD_A_QLINK_1_1P2	Power for the QLink 1 1.2 V analog circuits
M34	VDD_A_QLINK_1_CK_0P9	Power for Qlink 1 clock, 0.9 V analog circuits
N34	VDD_A_QLINK_2_0P9	Power for the QLink 2 0.9 V analog circuits
R35	VDD_A_QLINK_2_1P2	Power for the QLink 2 1.2 V analog circuits
P34	VDD_A_QLINK_2_CK_0P9	Power for Qlink 2 clock, 0.9 V analog circuits

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AT15	VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V analog circuits
AT23	VDD_A_QREFS_0P875_1	Reference voltage for the QREFS 0.875 V analog circuit
AU15	VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V analog circuits
AK34	VDD_A_UFS_0_0P9	Power for the UFS0 0.9 V analog circuits
AL34	VDD_A_UFS_0_1P2	Power for the UFS0 1.2 V analog circuits
AN34	VDD_A_USB_SS_DP_0P9	Power for the USBSS and DisplayPort 0.9 V analog circuits
AM34	VDD_A_USB_SS_DP_1P2	Power for the USBSS and DisplayPort 1.2 V analog circuits
AJ34, AR6, G17, G19, G21, G23, H18, H20, H22, H24, J19, J21, J23, J25, K18, K24, L17, L25, M18, M24, N17, N19, N21, N23, N25, P18, P20, P22, P24, R17, R25, T16, T18, T24, U15, U17, U25, V16, V18, V20, V22, V24, W15, W17, W19, W21, W23, W25, Y16, Y18, Y20, Y22	VDD_CX	Power for digital core circuits
H10	VDD_D_EBI_0	Power for EBI_0 digital circuits
AR12	VDD_D_EBI_1	Power for EBI_1 digital circuits
H27	VDD_D_EBI_2	Power for EBI_2 digital circuits
AR31	VDD_D_EBI_3	Power for EBI_3 digital circuits
AB24, AB26, AB28, AB30, AB32, AC29, AC33, AD24, AD28, AE29, AE33, AF24, AF28, AG29, AG33, AH24, AH26, AH28, AH30, AH32, AJ27, AJ29, AJ31, AJ33, AK26, AK32, AL25, AM26, AM32, AN25, AN27, AN29, AN31, AN33, AP26, AP28, AP30, AP32, AR25, AR27, AT24, AT26, AT28	VDD_GFX	Power for graphics
H11, H12, H8, H9	VDD_IO_EBI_0	Power for the EBI_0 I/O circuits
AR10, AR11, AR13, AR14	VDD_IO_EBI_1	Power for the EBI_1 I/O circuits
H25, H26, H28, H29	VDD_IO_EBI_2	Power for the EBI_2 I/O circuits
AR29, AR30, AR32, AR33	VDD_IO_EBI_3	Power for the EBI_3 I/O circuits
AB34, AD34, AD6, AE34, AH6, AK6, AT8, AU18, AU21, AU24, AU27, F20, F22, G18, W7, Y34	VDD_IX	Intermediate supply; 0.9 V
AV19	VDD_IX_PX0	Intermediate supply for the PX0; 0.9 V
AM22, AN22, AP20, AP21, AP22	VDD_LPI_CX	Power for LPI digital core circuits
AK23, AL23, AM23, AN23	VDD_LPI_MX	Power for low-power island memory circuits
AA33	VDD_LPI_MX_NAV	Power for LPI on chip memory-NAV

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
H14, H7, J11, J13, J15, J9, K10, K12, K14, K16, K8, L11, L13, L15, L9, M10, M12, M14, M8, N11, N13, N15, N9, P10, P12, P14, P8, R11, R13, R9, T10, T12, T8, U11, U13, U9, V10, V12, V8, W11, W13, W9, Y10, Y12, Y8	VDD_MM	Power for multimedia subsystem circuits
G31, H30, H32, J27, J29, J31, K26, K28, K30, K32, L27, L29, L31, M26, M28, M30, M32, N27, N29, N31, N33, P26, P28, P30, P32, R33, T26, T32, U33, V26, V28, V30, V32, W27, W29, W31, W33	VDD_MODEM	Power for modem circuits
AA11, AA13, AA7, AA9, AB10, AB12, AB14, AB8, AC15, AC17, AC19, AC21, AD16, AD18, AD20, AD22, AE17, AE19, AE21, AF22, AG21, AH22, AJ21, AK22, AL21, AM20, AN21, AR7, F31, F32	VDD_MX_A	Power for on-chip memory
AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AB16, AB18, AB20, AB22, AC23, AE23, AG23, AJ23, AK24, AL33, AM24, AM33, AP24, H33, J33, M16, P16, R15, T14, V14, Y14, Y24, Y26, Y28, Y30, Y32	VDD_MX_C	Power for on-chip memory
AV18	VDD_PX0	Power for pad group 0
AH35	VDD_PX10	Power for pad group 10
AV15	VDD_PX11	Power for pad group 11
AP6	VDD_PX13	Power for pad group 13
AF6, W6	VDD_PX14_A	Power for pad group 14 A
AV21, AV25	VDD_PX14_B	Power for pad group 14 B
AK35, W35	VDD_PX14_C	Power for pad group 14 C
E18, E21	VDD_PX14_D	Power for pad group 14 D
AT7	VDD_PX5	Power for pad group 5
F16	VDD_PX701	Power for pad group 701
F19	VDD_PX702	Power for pad group 702
F21	VDD_PX703	Power for pad group 703
AA34	VDD_PX704	Power for pad group 704
AC34	VDD_PX705	Power for pad group 705
AF34	VDD_PX706	Power for pad group 706
AG34	VDD_PX707	Power for pad group 707
AU20	VDD_PX709	Power for pad group 709
AU17	VDD_PX712	Power for pad group 712
AL6	VDD_PX713	Power for pad group 713
AG6	VDD_PX714	Power for pad group 714
AC6	VDD_PX715	Power for pad group 715
V7	VDD_PX716	Power for pad group 716

Table 2-5 MSM bottom pin descriptions: DNC/NC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AJ6	VDD_QFPROM	Power for programming the QFPROM
AV10	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit

2.3 Pin assignments: MSM top

2.3.1 Pin map: MSM top

The SM8475/SM8475P is available in the MPSP1518B. See Chapter 4 for package details and Section 2.2 for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3.

The text within Figure 2-3 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in Section 2.2.1.

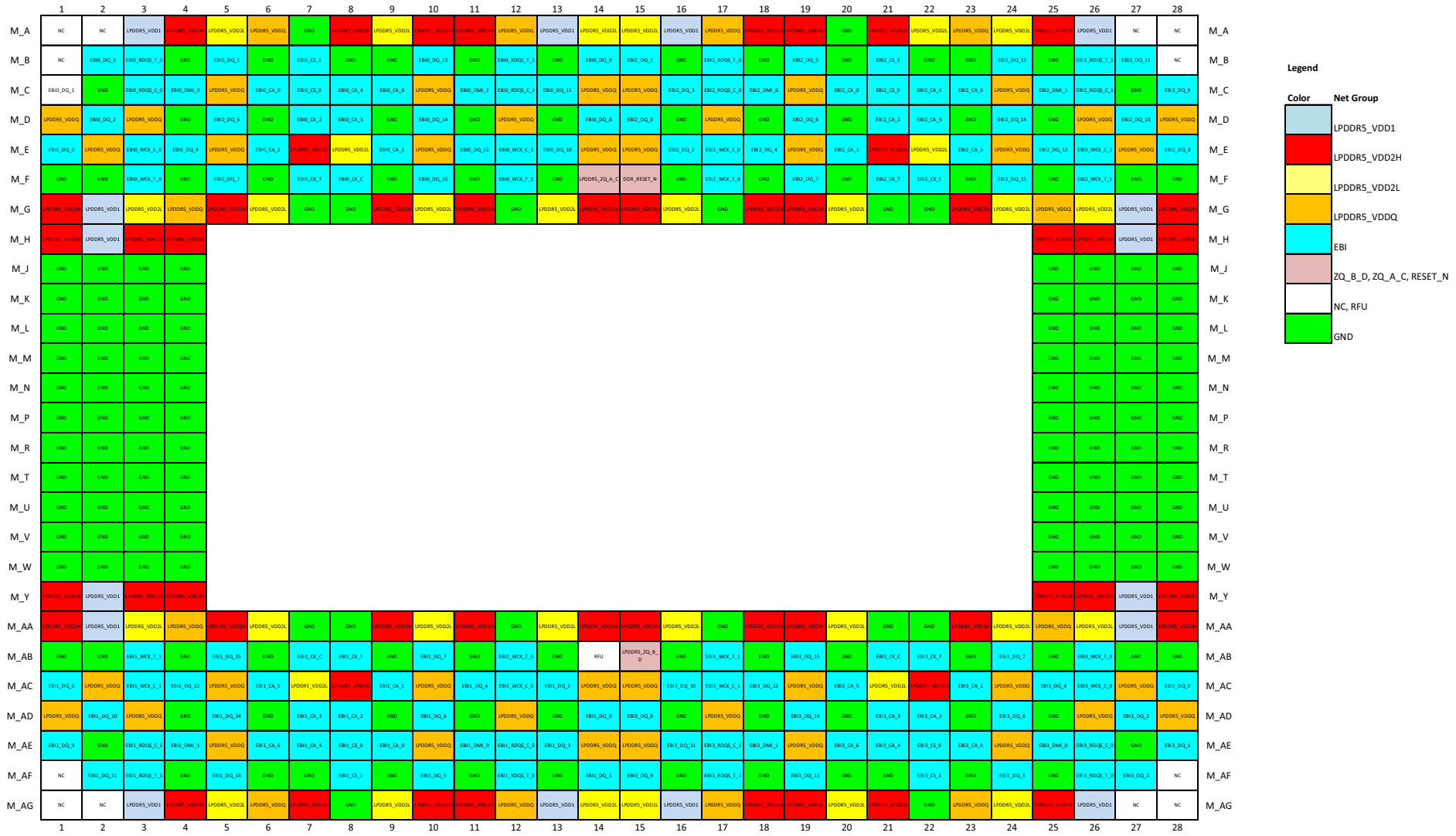


Figure 2-3 SM8475/SM8475P top pin LPDDR5 assignments (top view)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in Table 2-6 and Table 2-7.

Table 2-6 MSM top pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_F15	DDR_RESET_N	PX1	DO	LPDDR5 reset (shared by EBIs)
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock - negative
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock - positive
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9
M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 - positive

Table 2-6 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 - positive
M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 - negative
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 - negative
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - positive
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - positive
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - negative
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - negative
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0
M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 1
M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5 command/address bit 2
M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 3
M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 4
M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 5
M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock - negative
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock - positive
M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5 chip select 0
M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5 chip select 1
M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR5 data mask for byte 0
M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR5 data mask for byte 1
M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0
M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1
M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10
M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11
M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12
M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13
M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14
M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15
M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2
M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3

Table 2-6 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4
M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5
M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6
M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7
M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8
M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9
M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 - positive
M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 - positive
M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 - negative
M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 - negative
M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 - positive
M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 - positive
M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 - negative
M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 - negative
M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5 command/address bit 0
M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5 command/address bit 1
M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5 command/address bit 2
M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5 command/address bit 3
M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5 command/address bit 4
M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5 command/address bit 5
M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5 differential clock - negative
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5 differential clock - positive
M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5 chip select 0
M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5 chip select 1
M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR5 data mask for byte 0
M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR5 data mask for byte 1
M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5 data bit 0
M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5 data bit 1
M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5 data bit 10

Table 2-6 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5 data bit 11
M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5 data bit 12
M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5 data bit 13
M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5 data bit 14
M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5 data bit 15
M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5 data bit 2
M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5 data bit 3
M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5 data bit 4
M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5 data bit 5
M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5 data bit 6
M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5 data bit 7
M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5 data bit 8
M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5 data bit 9
M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 - positive
M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 - positive
M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 - negative
M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 - negative
M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 - positive
M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 - positive
M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 - negative
M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 - negative
M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5 command/address bit 0
M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5 command/address bit 1
M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5 command/address bit 2
M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5 command/address bit 3
M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5 command/address bit 4
M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5 command/address bit 5
M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5 differential clock - negative
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5 differential clock - positive

Table 2-6 MSM top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5 chip select 0
M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5 chip select 1
M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR5 data mask for byte 0
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR5 data mask for byte 1
M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5 data bit 0
M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5 data bit 1
M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5 data bit 10
M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5 data bit 11
M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5 data bit 12
M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5 data bit 13
M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5 data bit 14
M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5 data bit 15
M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5 data bit 2
M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5 data bit 3
M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5 data bit 4
M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5 data bit 5
M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5 data bit 6
M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5 data bit 7
M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5 data bit 8
M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5 data bit 9
M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 - positive
M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 - positive
M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 - negative
M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 - negative
M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 - positive
M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 - positive
M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 - negative
M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 - negative
M_F14	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	Reference	LPDDR5 ZQ calibration for channels A and C
M_AB15	LPDDR5_ZQ_B_D	LPDDR5_VDDQ	Reference	LPDDR5 ZQ calibration for channels B and D

1. See Table 2-1 for parameter and acronym definitions.

Table 2-7 MSM top pin descriptions – ground, NC, and power-supply pins

Pad #	Pad name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground
M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally
M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27, M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16	LPDDR5_VDD1	Power for PoP DDR memory core - 1.8 V Nom (top LPDDR5_VDD1)
M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_A4, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_A8, M_E21 , M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_A10, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_A11, M_Y25, M_Y26, M_Y28, M_A18, M_A19, M_A21, M_A25, M_AA1	LPDDR5_VDD2H	Power for PoP LPDDR5 memory core - 1.05 V Nom (top LPDDR5_VDD2H)
M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_A5, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_A9, M_G20, M_G24, M_G26, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10	LPDDR5_VDD2L	Power for PoP LPDDR5 memory core - 0.9 V Nom (top LPDDR5_VDD2L)

Table 2-7 MSM top pin descriptions – ground, NC, and power-supply pins (cont.)

Pad #	Pad name	Functional description
M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_A6, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_A12, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_A17, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_A23, M_E27, M_G4, M_G25, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10	LPDDR5_VDDQ	Power for PoP DDR pads 0.5 V Nom (top LPDDR5_VDDQ)
M_AB14	RFU	Reserved

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor	-0.3	1.2485	V
VDD_APC1	Qualcomm Kryo Gold application processor	-0.3	1.2485	V
VDD_A_EBI0 VDD_A_EBI1 VDD_A_EBI2 VDD_A_EBI3 VDD_A_PLL_EBI0 VDD_A_PLL_EBI1 VDD_A_PLL_EBI2 VDD_A_PLL_EBI3	EBI PHY and PLL circuits	-0.3	1.133	V
VDD_CX VDD_D_EBI_0 VDD_D_EBI_1 VDD_D_EBI_2 VDD_D_EBI_3	Digital core and EBI PHY digital circuits	-0.3	1.133	V
VDD_GFX	Graphics	-0.3	1.133	V
VDD_MM	Multimedia subsystem circuits	-0.3	1.133	V
VDD_MODEM	Modem subsystem	-0.3	1.133	V
VDD_MX_A VDD_MX_C	On-chip memory	-0.3	1.078	V
VDD_LPI_CX	Low power island core	-0.3	1.133	V
VDD_LPI_MX VDD_LPI_MX_NAV	Low power island memory	-0.3	1.078	V
VDD_A_CSI_01_0P9 VDD_A_CSI_23_0P9 VDD_A_CSI_45_0P9	Power for MIPI CSI 0.9V analog circuits	-0.3	1.012	V
VDD_A_CSI_1P2	Power for MIPI CSI 1.2V analog circuits	-0.3	1.386	V
VDD_A_DSI_01_0P9	Power for MIPI DSI 0.9V analog circuits	-0.3	1.012	V
VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI PLL 0.9V analog circuits	-0.3	1.012	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_DSI_01_1P2	Power for MIPI DSI 1.2V analog circuits	-0.3	1.386	V
VDD_A_PCIE_0_0P9	Power for PCIe0 0.9V analog circuits	-0.3	1.012	V
VDD_A_PCIE_1_0P9	Power for PCIe1 0.9V analog circuits	-0.3	1.012	V
VDD_A_PCIE_0_1P2 VDD_A_PCIE_1_1P2	Power for PCIe 1.2V circuits	-0.3	1.386	V
VDD_A_QLINK_0_0P9 VDD_A_QLINK_2_0P9	Power for QLINK0/2 0.9V analog circuits	-0.3	1.012	V
VDD_A_QLINK_0_CK_0P9 VDD_A_QLINK_2_CK_0P9	Power for QLINK0/2 clock 0.9V analog circuits			
VDD_A_QLINK_1_0P9	Power for QLINK1 0.9V analog circuits	-0.3	1.0538	V
VDD_A_QLINK_1_CK_0P9	Power for QLINK1 clock 0.9V analog circuits	-0.3	1.0538	V
VDD_A_QLINK_0_1P2 VDD_A_QLINK_1_1P2 VDD_A_QLINK_2_1P2	Power for QLINK0/1/2 1.2V analog circuits	-0.3	1.386	V
VDD_A_UFS_0_0P9	Power for UFS 0.9V analog circuits	-0.3	1.012	V
VDD_A_UFS_0_1P2	Power for UFS 1.2 V analog circuits	-0.3	1.386	V
VDD_A_EUSB_HS_0P9	Power for eUSB2 high-speed 0.9 V analog circuits	-0.3	1.012	V
VDD_A_EUSB_HS_1P2	Power for eUSB2 high-speed 1.2 V analog circuits	-0.3	1.386	V
VDD_A_USB_SS_DP_0P9	Power for USB super-speed and DisplayPort 0.9V analog circuits	-0.3	1.056	V
VDD_A_USB_SS_DP_1P2	Power for USB super-speed and DisplayPort 1.2V analog circuits	-0.3	1.386	V
VDD_A_QREFS_0P875 VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875V analog circuits	-0.3	1.012	V
VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2V analog circuits	-0.3	1.386	V
VDD_A_APC_CS_1P2	Power for Application Processor current sensor 1.2V analog circuits	-0.3	1.386	V
VDD_A_GFX_CS_1P2	Power for GFX current sensor 1.2V analog circuits	-0.3	1.386	V
VDD_A_NSP_CS_1P2	Power for NSP current sensor 1.2V analog circuits	-0.3	1.386	V
VDD_IO_EBI_0 VDD_IO_EBI_1 VDD_IO_EBI_2 VDD_IO_EBI_3	EBI I/O memory circuits	-0.3	0.627	V
VDD_PX0	Power for Pad Group 0 – control signals	-0.3	2.145	V
VDD_1P2_PX0	VDD 1.2 V for PX0 pads	-0.3	1.43	V
VDD_PX5	Power for Pad Group 5 – UIM pads	-0.3	2.09	V
VDD_PX10	Power for Pad Group 10 – UFS pads	-0.3	1.419	V
VDD_PX11	Power for Pad Group 11 – CXO pads	-0.3	1.419	V
VDD_PX13	Power for Pad Group 13 – Secure Processor Unit (SPU)	-0.3	2.09	V
VDD_PX14_A VDD_PX14_B VDD_PX14_C VDD_PX14_D	Power for Pad Group 14 – SDC2 pads	-0.3	1.43	V
VDD_PX701-707,709,712-716	Power for Pad Group 701 – I/O pads	-0.3	2.145	V
VDD_PX702	Power for Pad Group 702 – I/O pads	-0.3	2.145	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_QFPROM	Power for programming QFPROM	-0.3	2.09	V
VDD_QFPROM_SP	Power for programming QFPROM Secure Processor Unit	-0.3		V
VDD_IX	Intermediate supply; 0.9 V	-0.3	1.045	V
VDD_IX_PX0	Intermediate supply for the PX0; 0.9 V			
LPDDR5_VDDQ [1]	Power for PoP LPDDR5 memory IO pads	-0.3	0.627	V
LPDDR5_VDD1 [1]	Power for PoP LPDDR5 memory core	-0.3	2.145	V
LPDDR5_VDD2H [1]	Power for PoP LPDDR5 memory core	–	–	V
LPDDR5_VDD2L [1]	Power for PoP LPDDR5 memory core	–	–	V
T_S	Storage temperature [2] [3]	-55	150	°C
ESD protection – see Section 7.1.				
Thermal conditions – see Section 4.4.				

1. See the LPDDR5 data sheet for the absolute maximum DC ratings for minimum and maximum voltages of VDDQ, VDD1, VDD2H and VDD2L
2. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
3. For devices shipped in tape and reel, the storage temperature range is [-35°C to +15°C] and relative humidity (RH) < 90%. QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor Active	0.495	1.135	V
VDD_APC1	Qualcomm Kryo Gold application processor Active	0.512	1.135	V
VDD_A_EBI0 VDD_A_EBI1 VDD_A_EBI2 VDD_A_EBI3 VDD_A_PLL_EBI0 VDD_A_PLL_EBI1 VDD_A_PLL_EBI2 VDD_A_PLL_EBI3	EBI PHY and PLL circuits Active	0.64	1.03	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_CX VDD_D_EBI0 VDD_D_EBI1 VDD_D_EBI2 VDD_D_EBI3	Digital core and EBI PHY digital circuits Active Retention	 0.495 0.352	 1.03 0.48	 V V
VDD_GFX	Graphics Active	 0.485	 1.03	 V
VDD_MM	Multimedia subsystem circuits Active	 0.495	 1.03	 V
VDD_MODEM	Modem subsystem Active	 0.485	 1.03	 V
VDD_MX_A VDD_MX_C	On-chip memory Active Retention	 0.695 0.504	 0.98 0.68	 V V
VDD_LPI_CX	Low power island core Active Retention	 0.485 0.362	 1.03 0.48	 V V
VDD_LPI_MX VDD_LPI_MX_NAV	Low power island memory Active Retention	 0.695 0.504	 0.98 0.68	 V V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-3 Operating conditions for non AVS voltage rails

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A_CSI_01_0P9 VDD_A_CSI_23_0P9 VDD_A_CSI_45_0P9	Power for MIPI CSI 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_CSI_1P2	Power for MIPI CSI 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_DSI_01_0P9	Power for MIPI DSI 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_DSI_01_PLL_0P9	Power for MIPI DSI PLL 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_DSI_01_1P2	Power for MIPI DSI 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_PCIE_0_0P9	Power for PCIe0 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_PCIE_1_0P9	Power for PCIe1 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_PCIE_0_1P2 VDD_A_PCIE_1_1P2	Power for PCIe 1.2 V circuits	1.14	1.2	1.26	V
VDD_A_QLINK_0_0P9 VDD_A_QLINK_2_0P9	Power for QLINK0/2 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_QLINK_0_CK_0P9 VDD_A_QLINK_2_CK_0P9	Power for QLINK0/2 clock 0.9 V analog circuits				
VDD_A_QLINK_1_0P9	Power for QLINK1 0.9 V analog circuits	0.866	0.912	0.958	V
VDD_A_QLINK_1_CK_0P9	Power for QLINK1 clock 0.9 V analog circuits				
VDD_A_QLINK_0_1P2 VDD_A_QLINK_1_1P2 VDD_A_QLINK_2_1P2	Power for QLINK0/1/2 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_UFS_0_0P9	Power for UFS 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_UFS_0_1P2	Power for UFS 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_EUSB_HS_0P9	Power for eUSB2 high-speed 0.9 V analog circuits	0.83	0.88	0.92	V
VDD_A_EUSB_HS_1P2	Power for eUSB2 high-speed 1.2 V analog circuits	1.14	1.2	1.26	
VDD_A_USB_SS_DP_0P9	Power for USB super-speed and DisplayPort 0.9 V analog circuits	0.865	0.912	0.96	V
VDD_A_USB_SS_DP_1P2	Power for USB super-speed and DisplayPort 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_QREFS_0P875 VDD_A_QREFS_0P875_1	Reference voltage for QREFS 0.875 V analog circuits	0.83	0.88	0.92	V
VDD_A_QREFS_1P2	Reference voltage for QREFS 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_APC_CS_1P2	Power for Application Processor current sensor 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_A_GFX_CS_1P2	Power for GFX current sensor 1.2 V analog circuits	1.14	1.2	1.26	V

Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A_NSP_CS_1P2	Power for NSP current sensor 1.2 V analog circuits	1.14	1.2	1.26	V
VDD_IO_EBI	EBI I/O memory circuits				V
	LPDDR5 spec range 1 [3] [5]	0.47	0.504	0.57	
	LPDDR5 spec range 2 [4] [5]	0.27	0.3	0.37	
VDD_PX0	Power for Pad Group 0 – control signals	1.7	1.8	1.95	V
VDD_1P2_PX0	VDD 1.2 V for PX0 pads	1.1	1.2	1.3	V
VDD_PX5	Power for Pad Group 5 – UIM1 pads	1.7	1.8	1.9	V
VDD_PX10	Power for Pad Group 10 – UFS pads	1.12	1.2	1.29	V
VDD_PX11	Power for Pad Group 11 – CXO pads	1.17	1.2	1.29	V
VDD_PX13	Power for Pad Group 13 – Secure Processor Unit (SPU)	1.7	1.85	1.95	V
VDD_PX14_A VDD_PX14_B VDD_PX14_C VDD_PX14_D	Power for Pad Group 14 - SDC2 pads	1.1	1.2	1.3	V
VDD_PX701 to PX707, PX709, PX712 to PX716	Power for Pad Group 701 to 707, 709, 712 to 716 – I/O pads	1.7	1.8	1.95	V
VDD_QFPROM	Power for programming QFPROM	1.7	1.8	1.9	V
VDD_QFPROM_SP	Power for programming QFPROM Secure Processor Unit				
VDD_IX	Intermediate supply; 0.9 V	0.85	0.9	0.95	V
VDD_IX_PX0	Intermediate supply for the PX0; 0.9 V	0.85	0.9	0.95	V
LPDDR5_VDDQ	Power for PoP LPDDR5 memory IO pads				V
	LPDDR5 spec range 1 [3] [5]	0.47	0.504	0.57	
	LPDDR5 spec range 2 [4] [5]	0.27	0.3	0.37	
LPDDR5_VDD1	Power for PoP LPDDR5 memory core	1.7	1.8	1.95	V
LPDDR5_VDD2H	Power for PoP LPDDR5 memory core	_ [6]	_ [6]	_ [6]	V
LPDDR5_VDD2L	Power for PoP LPDDR5 memory core	_ [6]	_ [6]	_ [6]	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. LPDDR5 spec range 1 is intended for IO operation with both ODT enabled and disabled.
4. LPDDR5 spec range 1 is intended for IO operation with both ODT disabled
5. For more information, please check LPDDR5 PDN specification defined by JEDEC Solid State Technology Association (JESD209-5B)
6. See the LPDDR5 data sheets for the recommended DC operating conditions (min/typ/max voltages) of VDD2H/VDD2L/VDD1/VDDQ

3.2.1 Thermal conditions

Table 3-4 Thermal conditions

Parameter	Description	Min	Typ	Max	Units
Thermal conditions					
T_J	Device operating junction temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8475/SM8475P Chipset Power Delivery Network Specification* (80-27620-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8475 Linux Android Current Consumption Data Application Note* (80-27620-7).

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM8475/SM8475P device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-5 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PXN [1]	VDD_PXN [1] + 0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3	0.35 × VDD_PXN [1]	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PXN [1]	VDD_PXN [1]+ 0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3	0.3 × VDD_PXN [1]	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [2]	–	2	µA

Table 3-5 DC specification of 1.8 V GPIOs (cont.)

Parameter	Description	Min	Max	Units
I_{IL}	Input low leakage current [2]	-2	–	µA
R_{PD}	Pull-down resistance	10K	50K	Ω
R_{PU}	Pull-up resistance	10K	50K	Ω
R_{KP}	Bus keeper resistor	10K	50K	Ω
V_{OH}	High-level output voltage	VDD_PXN [1] - 0.45	VDD_PXN [1]	V
V_{OL}	Low-level output voltage	0.0	0.45	V

1. PXN, Where N defines;

   PX0 Pad group 0 (SPMI, RESIN); 1.8 V

   PX5 Pad group 5 (UICC 0, UICC 1); 1.8 V

   PX701 to PX707 Pad group 701 to 707 (IO pad); 1.8 V

   PX709 to PX716 Pad group 709 to 716 (IO pad); 1.8 V
2. I_{IH} and I_{IL} values are based on characterization of corner devices over temperature.

Table 3-6 UFS clock DC characteristics (VDD_PX10)

Parameter	Description	Min	Max	Units
V_{OL}	Low-level output voltage	0	0.25 × VDD_PX10	V
V_{OH}	High-level output voltage	0.75 × VDD_PX10	VDD_PX10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{LEAK}	Stand by leakage	-10	10	µA

Table 3-7 SDC2 1.2 V mode DC specifications (VDD_PX14)

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, (hihys_en = LOW)	0.65 × VDD_PX14	VDD_PX14 + 0.3	V
VIL	Low-level input voltage, (hihys_en = LOW)	-0.3	0.35 × VDD_PX14	V
VIH	High-level input voltage, (hihys_en = HIGH)	0.7 × VDD_PX14	VDD_PX14 + 0.3	V
VIL	Low-level input voltage, (hihys_en = HIGH)	-0.3	0.3 × VDD_PX14	V
VSHYS	Schmitt hysteresis, (hihys_en = LOW)	100	–	mV
VSHYS	Schmitt hysteresis, (hihys_en = HIGH)	200	–	mV
I_{IH}	Input high leakage current	–	2	µA
I_{IL}	Input low leakage current	-2	–	µA
RPD	Pull-down resistance	10K	50K	Ω
RPU	Pull-up resistance	10K	50K	Ω
R_{KP}	Bus keeper resistor	10K	50K	Ω
V_{OH}	High-level output voltage	0.75 × VDD_PX14	VDD_PX14	V
V_{OL}	Low-level output voltage	0	0.25 × VDD_PX14	V

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM8475/SM8475P devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-1.

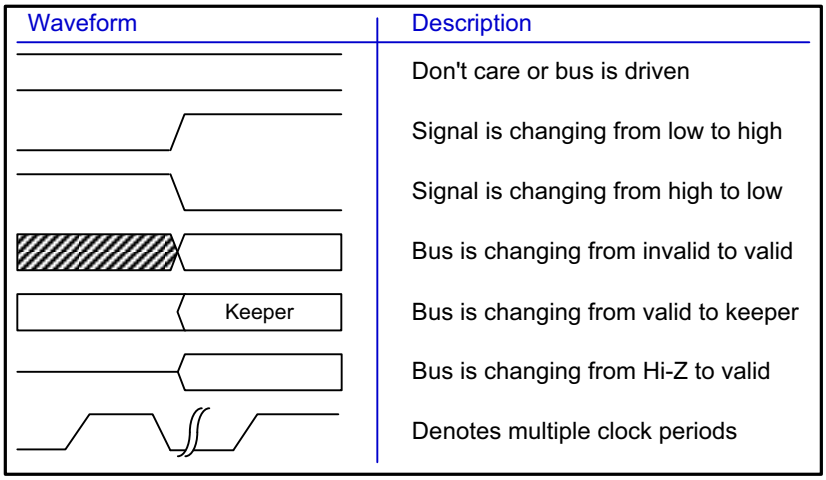


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SM8475/SM8475P devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-2.

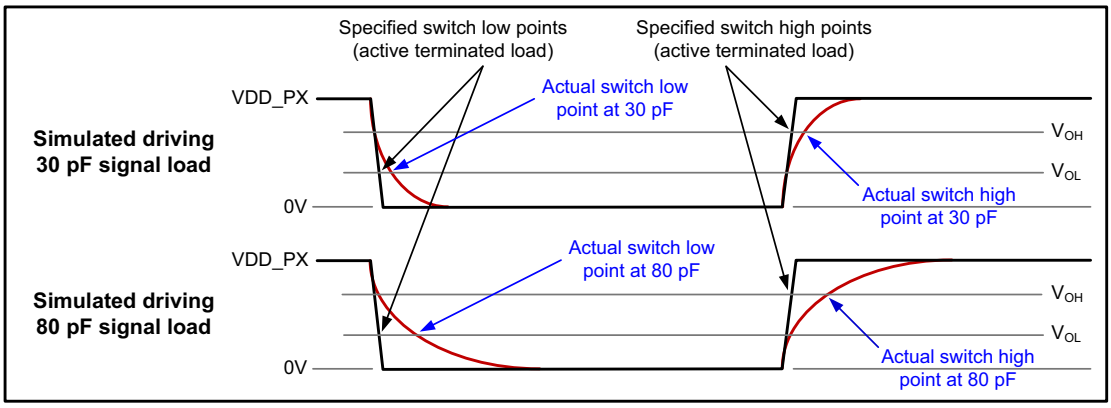


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8475/SM8475P device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SM8475/SM8475P device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

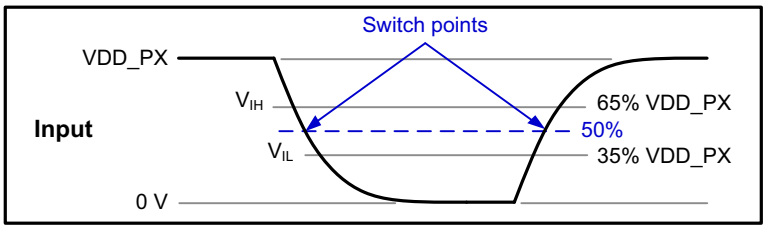


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX_x} - 50 mV or more
- V_{OL} ~ 50 mV or less

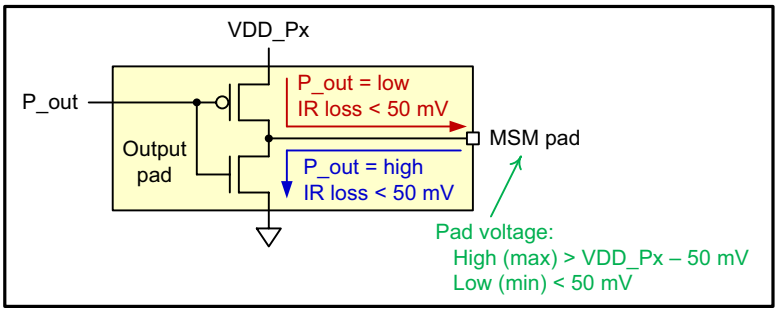


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time ($\mathbf{T_{RISE}}$) and fall time ($\mathbf{T_{FALL}}$) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5 SDRAM memory that is attached to the top of the SM8475/SM8475P chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8450, SM8450P, and SM8475 Recommendations* (80-VP300-18).

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SM8475/SM8475P device supports up to six D-PHY or C-PHY camera interfaces.

Table 3-8 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v3.0	Following features are not supported: ■ Raw6/7 data formats ■ All DPCM formats ■ LRTE with EPD over DPHY ■ EoTp ■ USL ■ sROI
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v2.0	Following features are not supported: ■ Bidirectional lanes ■ Alternate low power (ALP) mode

3.8.1.1 Camera MLCK

The SM8475/SM8475P camera master clocks (CAM_MCLK[7:0]) supports 19.2/24 MHz with jitter specification < 400 ps.

3.8.2 Audio support

The SM8475/SM8475P supports the WCD9380/WCD9385 audio codec IC to provide the system's audio functions. SM8475/SM8475P audio-related interface options with the WCD include:

- Digital microphone: Section 3.9.7
- SWR: Section 3.9.8
- I^2S: Section 3.9.10
- PCM/TDM: Section 3.9.11
- I^2C/I3C: Section 3.9.13
- SPI: Section 3.9.14

See the *WCD9380/WCD9385 Audio Codec Device Specification* (80-PL335-1) for performance characteristics.

3.8.3 Display support

The SM8475/SM8475P device supports up to two D-PHY or C-PHY displays.

Table 3-9 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface v1.3.1	Following features are not supported: ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission
MIPI Alliance Specification for Display Serial Interface 2 v2.0	Following features are not supported: ■ Peripheral reset timer ■ Packed pixel stream, 24-bit YCbCr, 4:2:2 format ■ Packed pixel stream, 36-bit RGB, 12-12-12 format ■ Packed pixel stream, 12-bit YCbCr, 4:2:0 format ■ Sync event payloads ■ Interlaced video transmission ■ Packed pixel stream, 20-bit YCbCr 4:2:2 format
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

3.8.4 DMB support

The SM8475/SM8475P supports an external DMB solution using the following interface options:

- SPI: Section 3.9.14
- SD: Section 3.9.1

3.9 Connectivity

The connectivity functions supported by the SM8475/SM8475P that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- eUSB2 host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- Digital microphone PDM interface
- SoundWire (SWR) interface
- Serial low-power inter-chip media bus (SLIMbus) interface

- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Touchscreen connections
- Through proper configuration of the 22 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - I3C

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

Table 3-10 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical layer Specification version 3.0	Secure Digital: Physical layer Specification version 3.0 Feature Exception: DDR50 mode not supported; SDR104 mode supports up to 74 Mbps SDR25 mode supports up to 18.5 Mbps HS mode supports up to 18.5 Mbps
SDIO Card Specification version 3.0	SDIO Card Specification version 3.0 Feature Exception: DDR50 mode supports up to 37.5Mbps; SDR50 mode supports up to 37.5Mbps

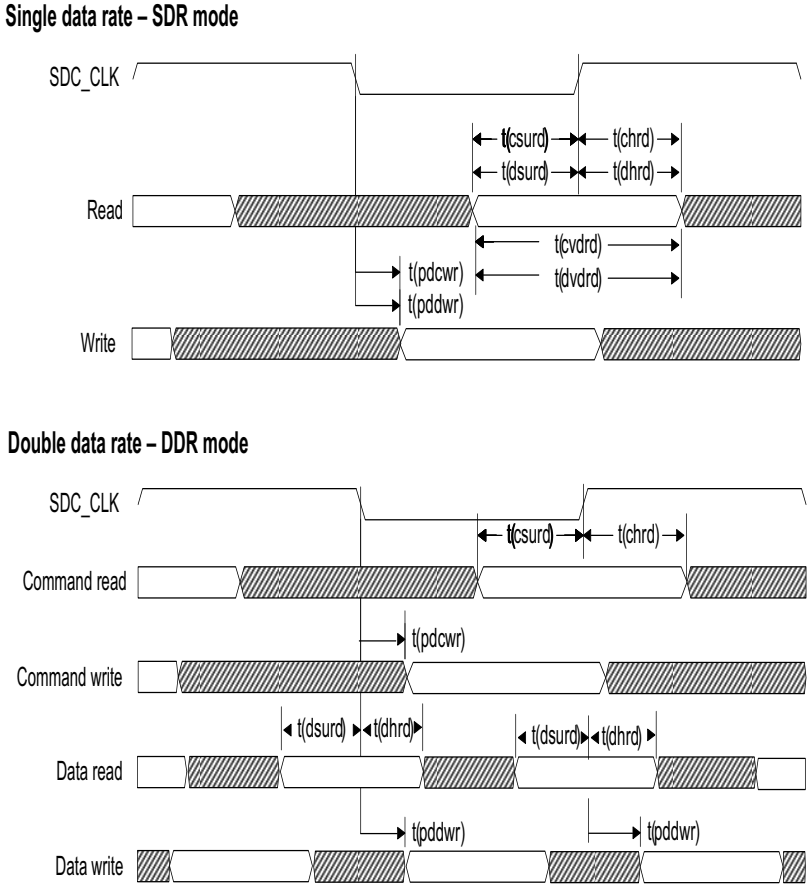


Figure 3-5 SD interface timing

NOTE: SD interface timing parameters can be found at the standards mentioned above.

3.9.2 USB interfaces

Table 3-11 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	U1 and U2 stages are not enabled in USB3 Gen1 and Gen2 Device Mode due to interoperability concerns
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)
Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 1.1 Specification	None

3.9.3 DisplayPort

Table 3-12 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4a	None

3.9.4 PCIe interface

Table 3-13 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Base Specification Revision 3.0	None

3.9.5 UFS interface

Table 3-14 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None

3.9.6 UIM interface

Table 3-15 Supported UIM standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.7 Digital microphone PDM interface

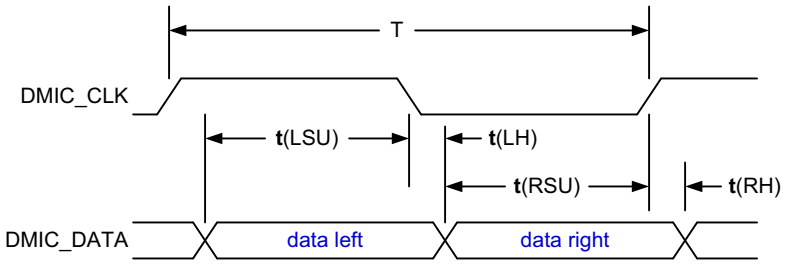


Figure 3-6 Digital microphone PDM interface timing

Table 3-16 Digital microphone timing

Parameter		Min	Typ	Max	Units
1/T	DMIC clock frequency	0.6	–	12.288	MHz
	DMIC clock duty cycle	45	–	55	%
t(LSU)	Data left setup time to clock falling edge	10	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	ns

3.9.8 SoundWire (SWR) interface

Table 3-17 Supported SWR standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for SoundWire Version 1.2	None

SM8475/SM8475P SoundWire PHY timing parameters, as specified in Table 3-18, are compliant to clock and data specifications.

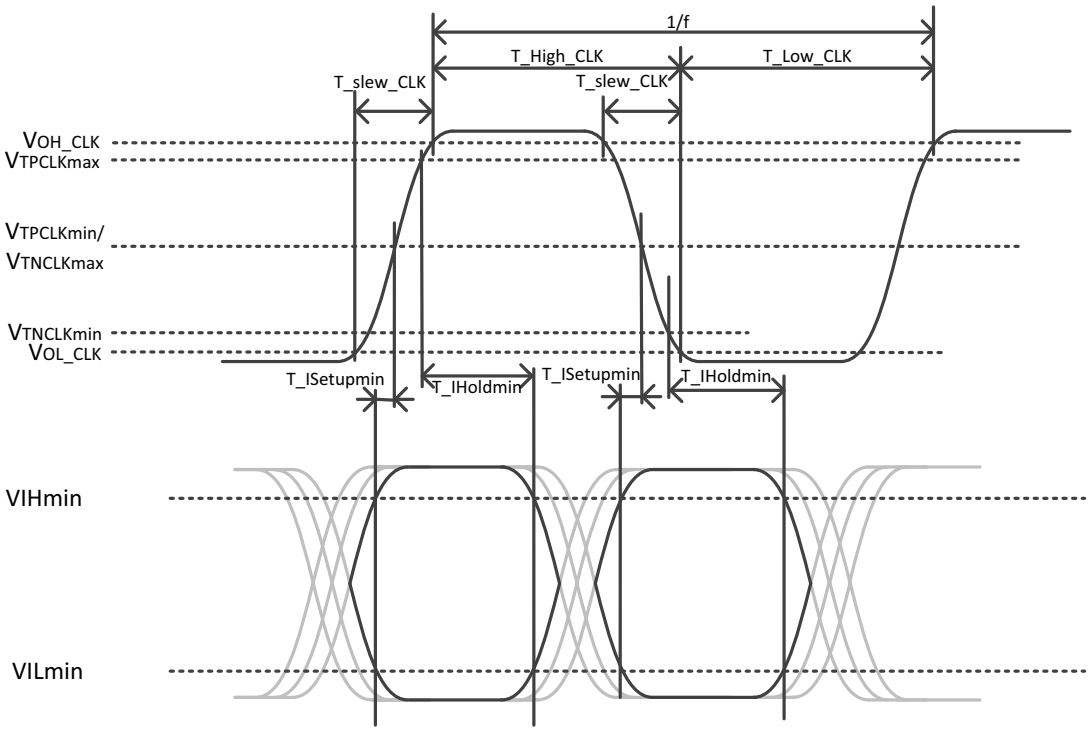


Figure 3-7 PHY timing – clock output/input and data input

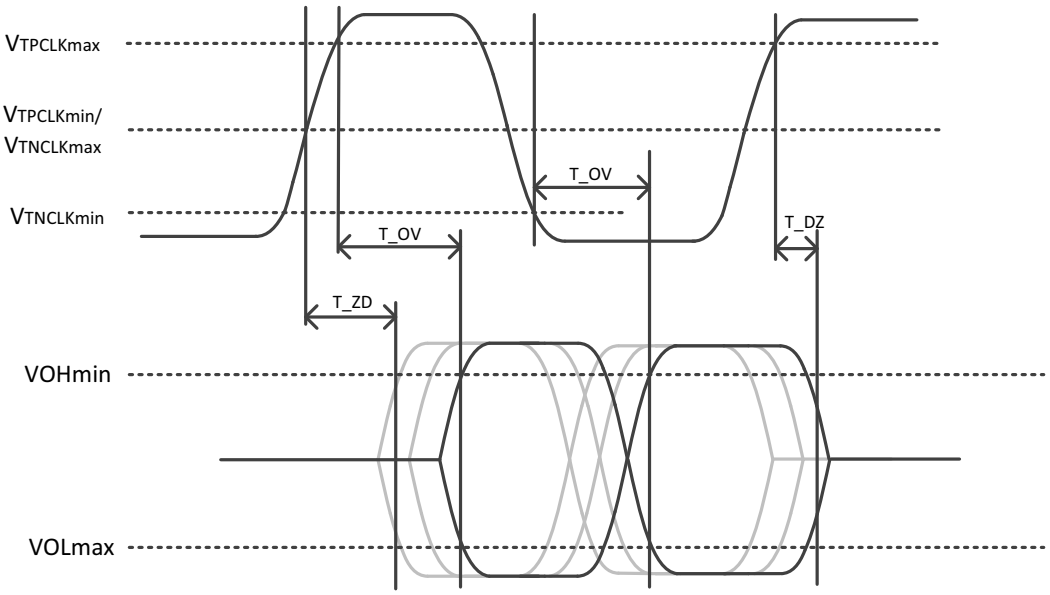


Figure 3-8 PHY timing – clock output and data output

Table 3-18 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Units
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	25.6	ns
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	3	–	ns
t_IHold_min_Data_1V8	Input hold time	–	4	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.9.9 SLIMbus interface

Table 3-19 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 2.0	None

3.9.10 I²S interfaces

There are two I²S interface types supported by the SM8475/SM8475P:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI²S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-20 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

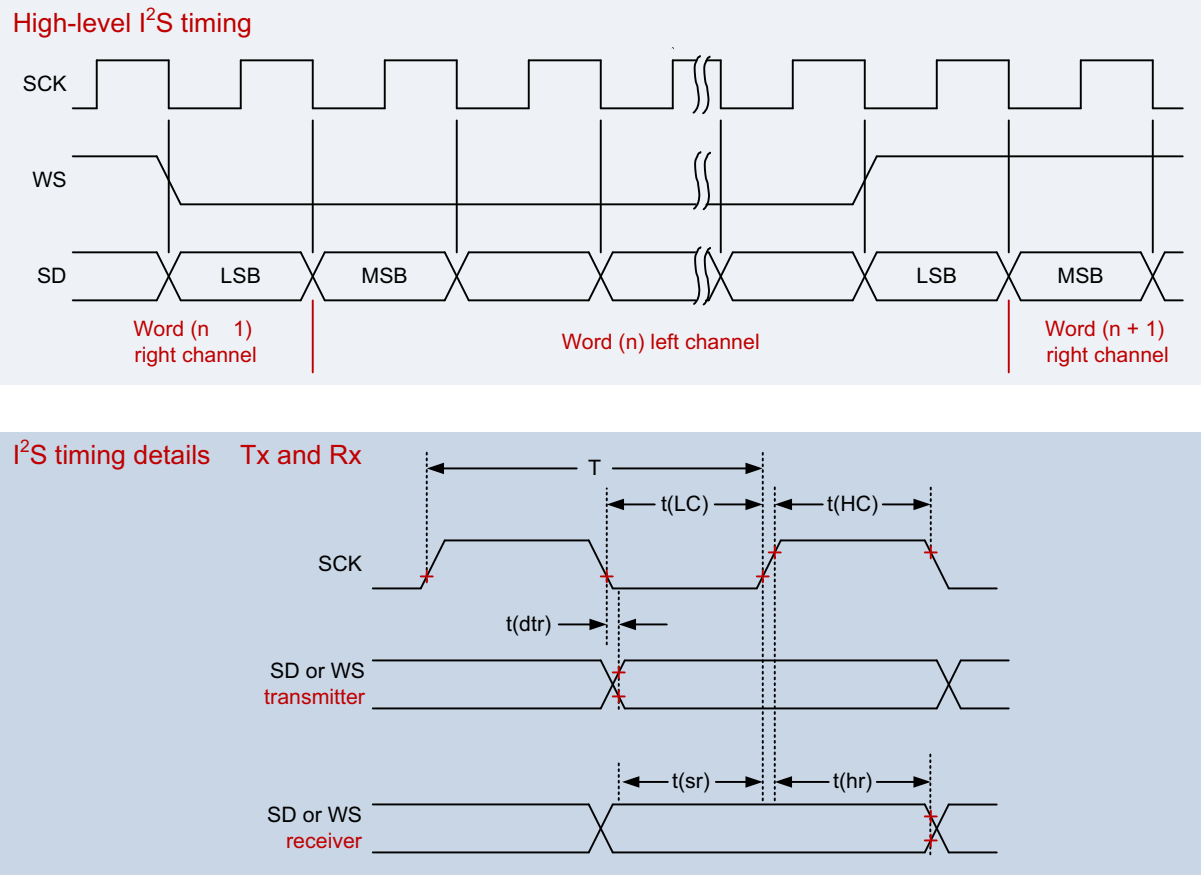


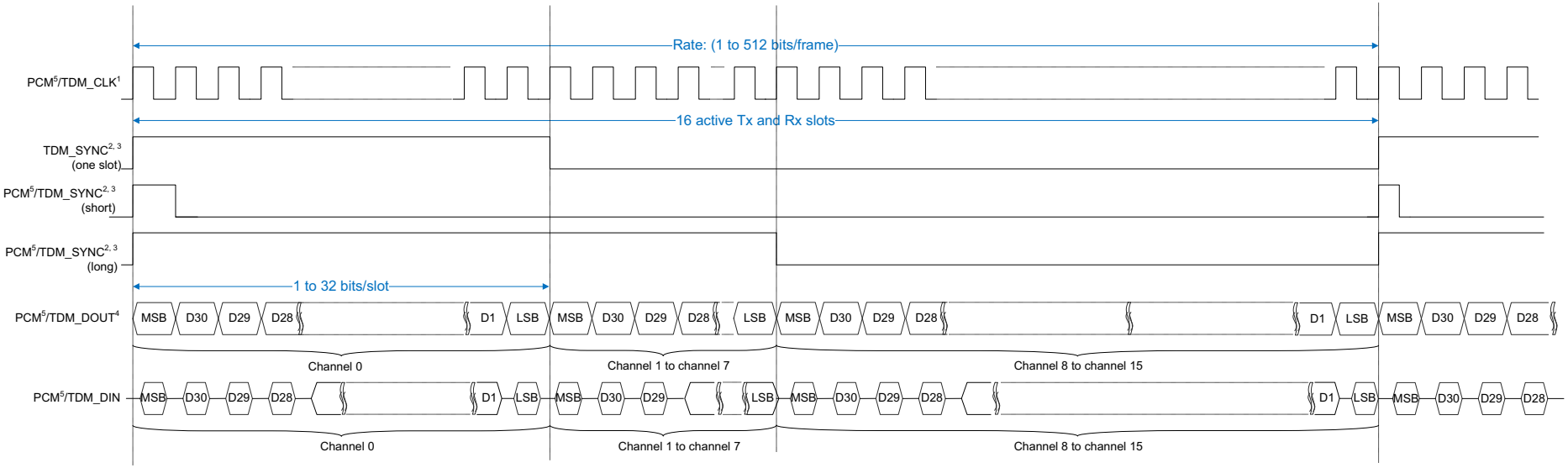
Figure 3-9 I²S timing diagram

Table 3-21 I²S interface timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60 × T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	8.14	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60 × T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	8.14	ns

1. Load capacitance is between 10 pF and 40 pF

3.9.11 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-10 PCM/TDM audio format with different sync modes

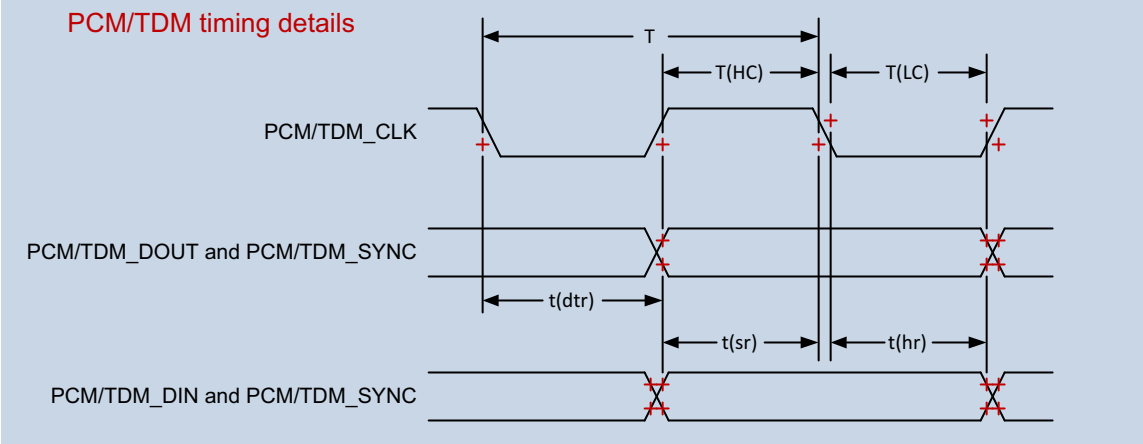


Figure 3-11 PCM/TDM timing diagram

Table 3-22 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.40 × T	0.60 × T	ns
t(LC)	Clock low		0.40 × T	0.60 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns
Slave mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.40 × T	0.60 × T	ns
t(LC)	Clock low		0.40 × T	0.60 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC input setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC input hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns

1. Load capacitance is between 10 pF to 40 pF.

3.9.12 Touchscreen connections

Touchscreen panels are supported using I^2C buses (Section 3.9.13) and GPIOs configured as discrete digital inputs (Section 3.5). Additional specifications are not required.

3.9.13 I2C/I3C interface

Table 3-23 Supported I2C/I3C standards and exceptions

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.9.14 Serial peripheral interface

The SM8475/SM8475P supports SPI as a master only. Any one of the 22 QUP ports can be configured as an SPI master.

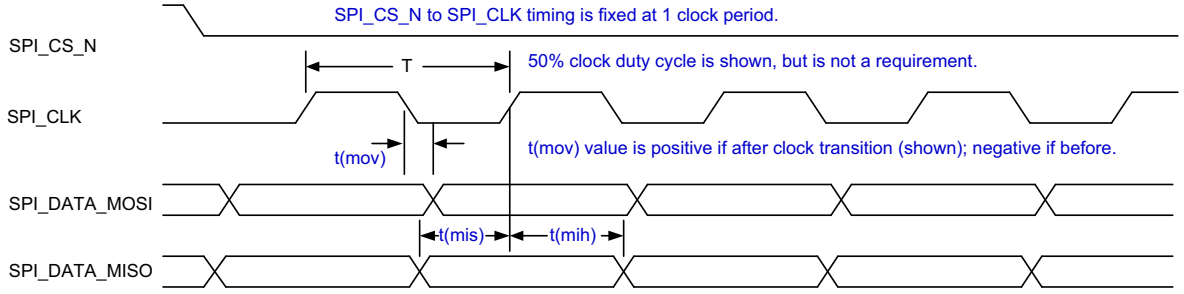


Figure 3-12 SPI master timing diagram

Table 3-24 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

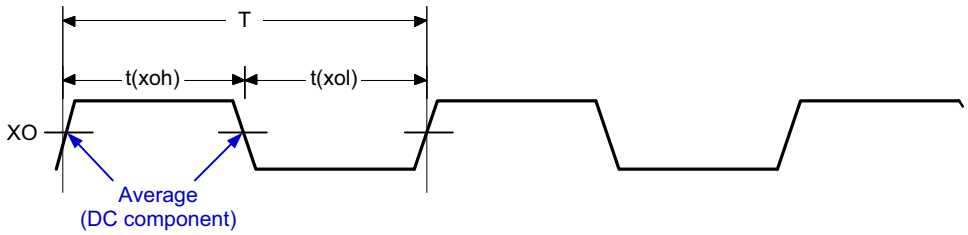


Figure 3-13 XO timing parameters

Table 3-25 CXO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See *Section 3.6.3 76.8 MHz XO crystal requirements* of PMK8350/PMK8450/PMK8475 *Data Sheet* (80-PT197-1) for more information.

3.10.1.2 Sleep clock

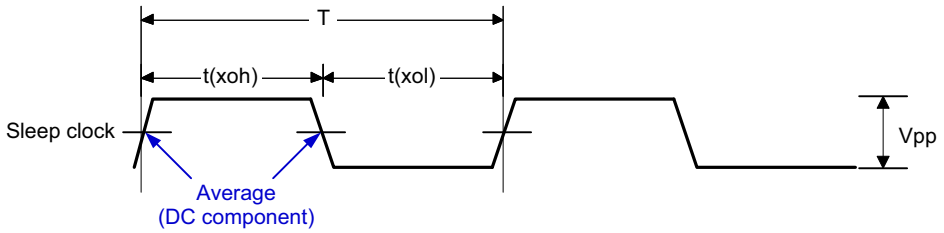


Figure 3-14 Sleep-clock timing parameters

Table 3-26 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.521	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.5.

3.10.3 JTAG

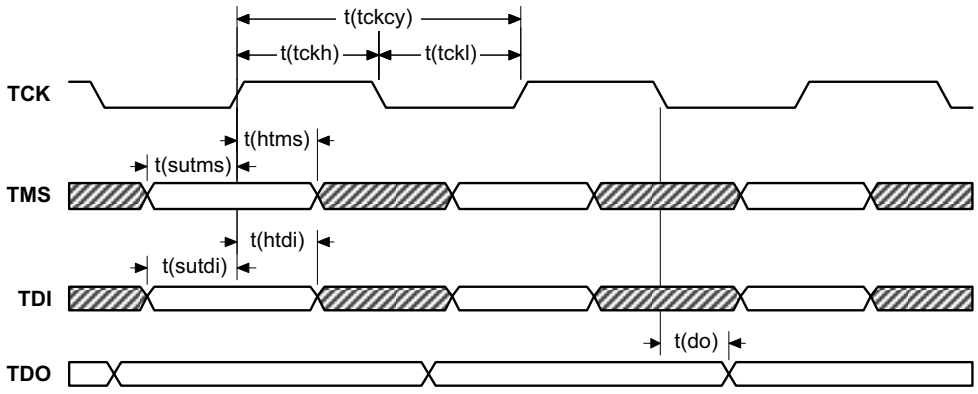


Figure 3-15 JTAG interface timing diagram

Table 3-27 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

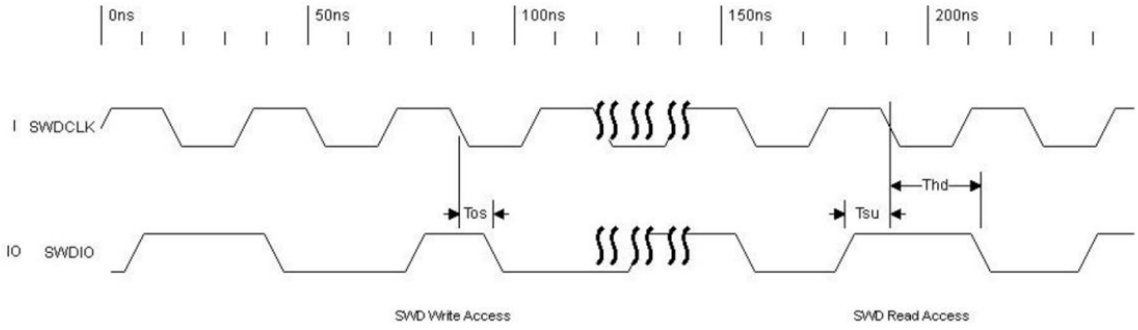


Figure 3-16 SWD write and read AC timing diagram

Table 3-28 SWD write and read AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T-7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	4	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	1	–	ns

NOTE: SWDCLK runs at 20 MHz or lower.

3.11 Power management interface

The digital I/Os must meet the logic-level requirements specified in Section 3.5.

3.11.1 System power management interface (SPMI)

Table 3-29 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM8475/SM8475P is available in the MPSP1518B that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1518B has a 15.0 mm by
14.0 mm body, with a maximum height of 0.57 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1518B outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download the *Package Outline Drawing, MPSP1518B, 15.0 × 14.0 × 0.57 mm, ST94, M127, SB167, PB 496NSP, PL1, MEP* (NT90-26575-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-26575-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the **Related Files** line that is located directly underneath the PDF link.

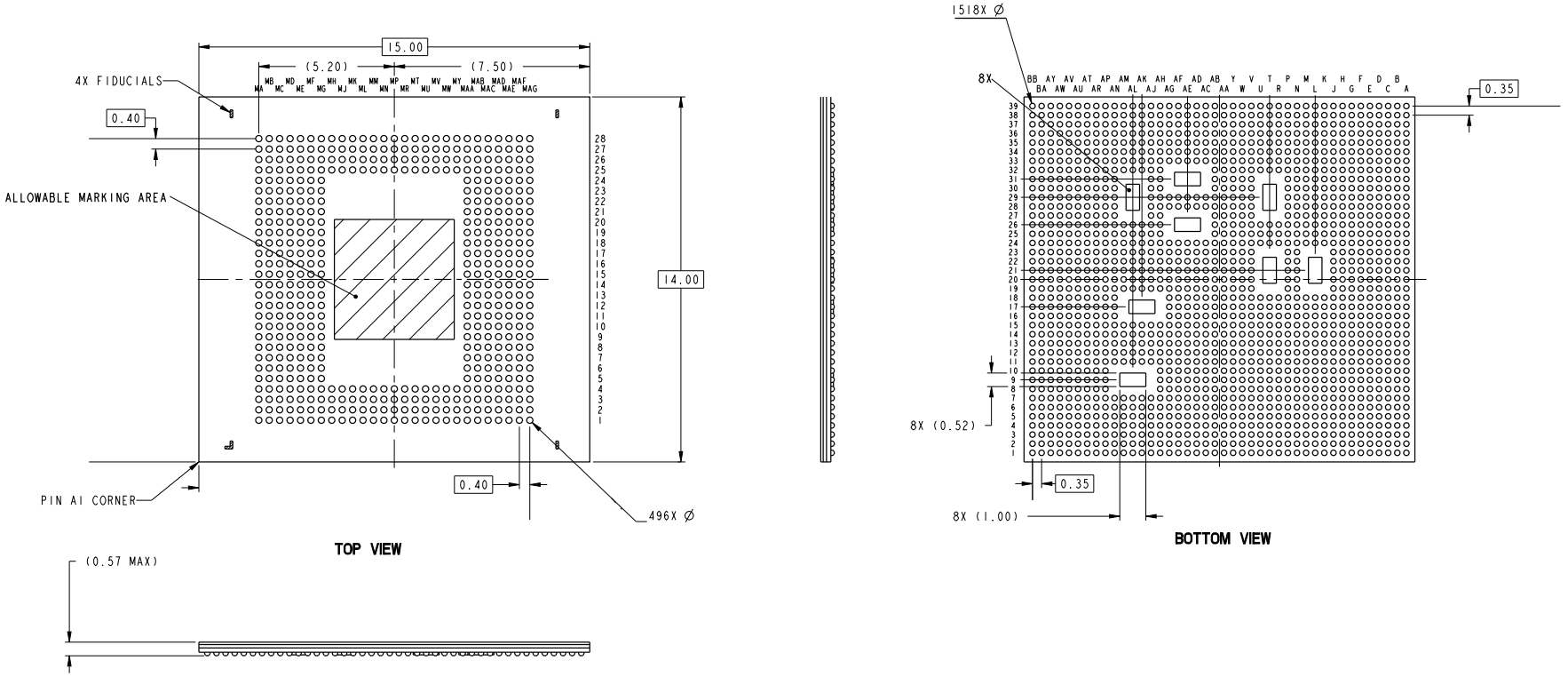


Figure 4-1 MPSP1518B outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

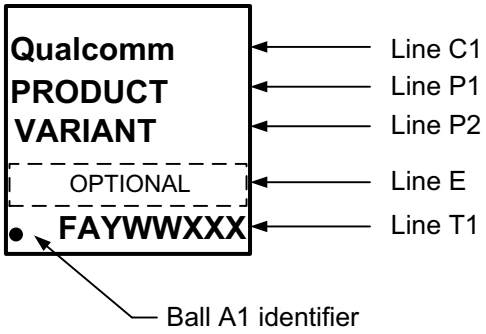


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ SM8475 ■ SM8475P
P2	VARIANT	PRR-BB ■ See Table 4-4 for the assigned values.
E	OPTIONAL	Blank (sample type ES1) ES2 (sample type ES2)
T1	FAYWWXXX	F = supply source code F = F (TSMC) A = assembly site code ■ A = C (Amkor, Korea) ■ A = X (Shinko, Japan) Y = single/last digit of year WW = two digit work week of current year XXX = serial number
	•	Ball A1 indicator

NOTE: For complete marking definitions of all SM8475/SM8475P variants and revisions, see the *SM8475/SM8475P Device Revision Guide* (80-27620-4).

Table 4-2 QFPROM JTAG register <0x221C21B8>

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants (see Table 4-4).
bits [19:0]	JTAG_ID	These bits map to bits of the hardware revision number (see Table 4-4).

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8475	-1	-MPSP	1518	B		-MT	-00	-0	AC
Example 2	SM-8475P	-1	-MPSP	1518	B		-MT	-00	-0	AC

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8475-1-MPSP1518B-MT-00-0-AC
- Example 2: SM-8475P-1-MPSP1518B-MT-00-0-AC

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	FEATURE_ID [2]	Hardware revision number	Source configuration code (S) [3]	Comments	Sample date
SM8475	ES1	100-AC	0x00	0x0 01D9 0E1	0	SM8475, MPSP1518B, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.57 mm height	02/21/2022
	ES2 [4]	100-AC	0x00	0x0 01D9 0E1	0	SM8475, MPSP1518B, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.57 mm height	04/01/2022
	CS	100-AC CS date code is as follows: ■ Amkor: 214 ■ Shinko: 214	0x00	0x0 01D9 0E1	0	SM8475, MPSP1518B, 1 × Prime at 3.2 GHz, 3 × Gold at 2.75 GHz, 4 × Silver at 2 GHz, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.57 mm height	04/30/2022
	ES	100-AB	0xA	0x0 01D9 0E1	0	SM8475, MPSP1518B, 1 × Prime at 3 GHz, 3 × Gold at 2.5 GHz, 4 × Silver at 1.8 GHz, LPDDR5, AON camera, 800 MHz mmW, 200 MHz sub-6 with ULCA, LTE, 0.57 mm height	8/12/2022
SM8475P	ES	100-AC	0x00	0x0 01DA 0E1	0	SM8475P, MPSP1518B, 1 × Prime, 3 × Gold, 4 × Silver, LPDDR5, AON camera, no modem, 0.57 mm height	05/31/2022
SM8475P	CS	100-AC CS date code is as follows: ■ Amkor: 223 ■ Shinko: 224	0x00	0x0 01DA 0E1	0	SM8475P, MPSP1518B, 1 × Prime at 3.2 GHz, 3 × Gold at 2.75 GHz, 4 × Silver at 2 GHz, LPDDR5, AON camera, no modem, 0.57 mm height	06/30/2022

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. However, Feature_ID is same for ES1 and ES2 sample. See Table 4-5 for ES identification.
3. S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-5.
4. CPU frequency uplift SKU.

Table 4-5 SM8475 ES/CS identification (AC SKU)

ES sample [1]	Date code YWW	Lot code (see 80-VK055-1)
ES1	≤ 209	Any lot code is ES1
ES1	210, 211	Start from x0x is ES1 (x - dynamic number)
ES2	210, 211	Start from x1x is ES2 (x - dynamic number)
ES2	≥ 212	Any lot code is ES2
CS	≥ 214	Any lot code is CS

1. See ES4 software release notes on how to check SM8475 ES1, ES2 - CPU frequency in software.

Table 4-6 SM8475P CS identification

CS sample [1]	Date code YWW	Lot code (see 80-VK055-1)
CS	■ Amkor: ≥ 223 ■ Shinko: ≥ 224	Any lot code is CS

1. See CS software release notes on how to check SM8475P CS - CPU frequency in software.

Table 4-7 Source configuration code

S value	Die	F value = F
0	Digital	TSMC

4.3.1 Daisy chain devices

For daisy chain part information, contact the Qualcomm Sales team for support.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-8.

Table 4-8 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **SM8475/SM8475P rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory baking before use. After baking, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8475/SM8475P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

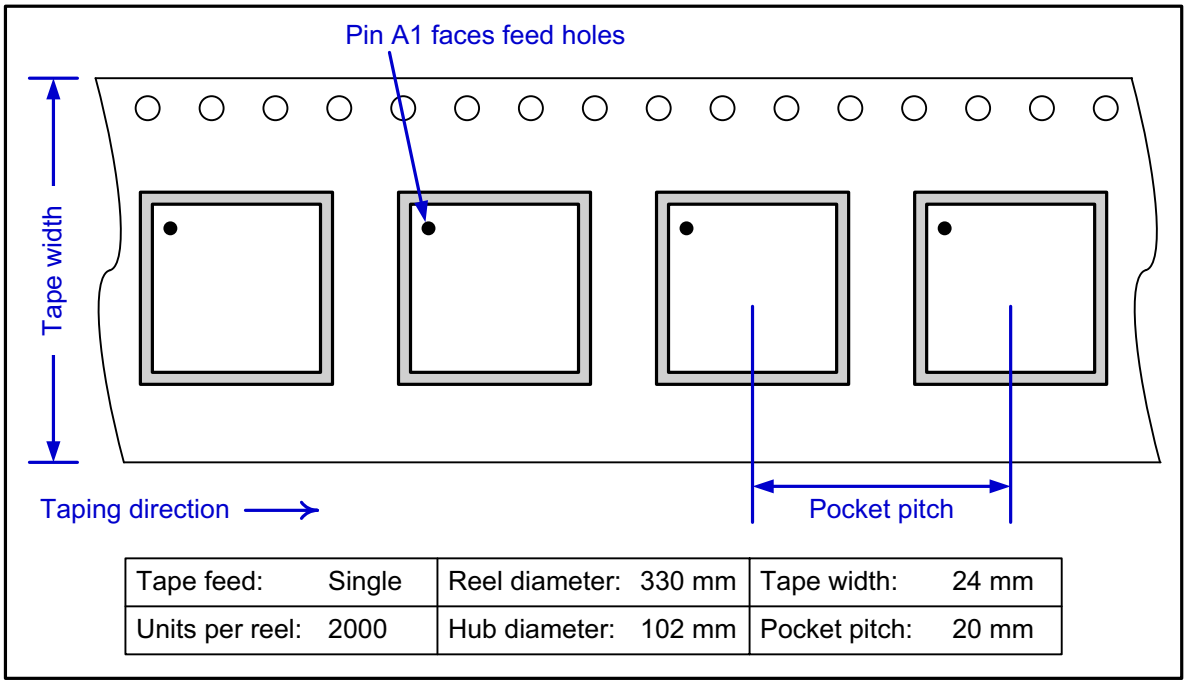
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8475/SM8475P tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

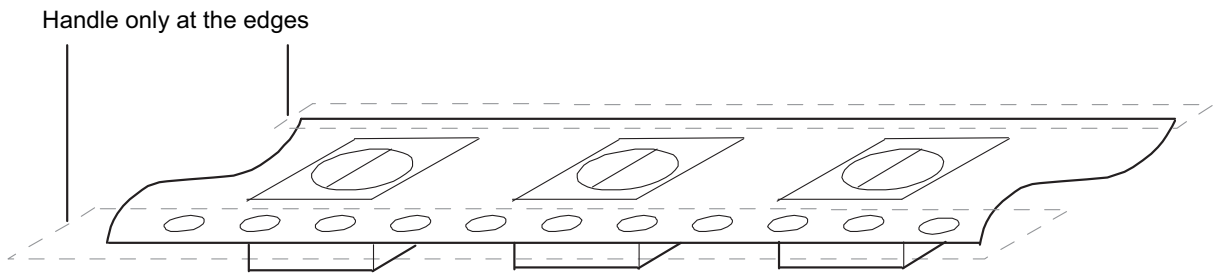


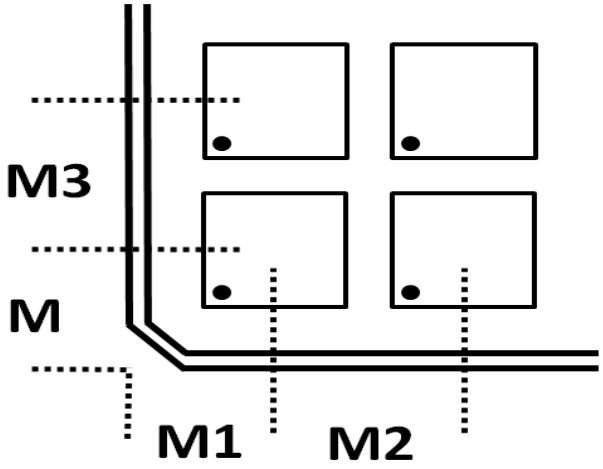
Figure 5-2 Tape handling

5.1.2 Matrix tray information – available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	6 × 15 (90)
M	15.45 mm
M1	14.00 mm
M2	20.50 mm
M3	21.00 mm

Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Storage

5.2.1 Bagged storage conditions

SM8475/SM8475P devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See the *IC Products Packing Method* document (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM8475/SM8475P if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SM8475/SM8475P if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

5.4.1 Lot code detail

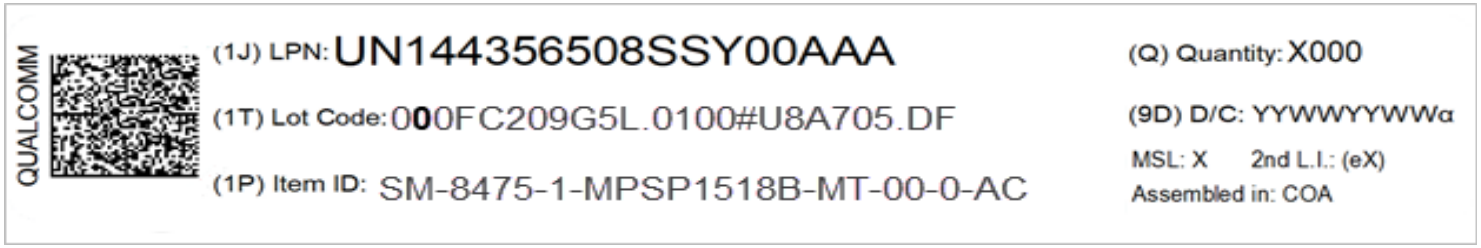


Figure 5-4 Lot code detail

NOTE: The second digit of the lot code, highlighted in Figure 5-4 describes how to differentiate between SM8475 - ES1 and ES2. The highlighted digit should be **0** for ES1 and **1** for ES2.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualification summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	567	Pass
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	368	<100
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	368	>10
ESD ─ Human body model (HBM) rating per JS001 (Total samples from one wafer lot)	21	Pass ± 1 kV
ESD ─ Charged device model (CDM) rating per C101 (Total samples from one wafer lot)	3	Pass ± 250 kV
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 105°C (Total samples from one wafer lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 105°C (Total samples from one wafer lot)	6	Pass

Table 7-2 SM8475/SM8475P-LPDDR5 package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Shinko Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C (Total samples from three different assembly lots)	558	558	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 700 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning**: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots)	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C (Total samples from three different assembly lots)	96	96	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (Total samples from three different assembly lots)	231	231	Pass
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See the note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

7.2 Device characteristics

Table 7-3 Device characteristics

Device name	SM8475/SM8475P
Package type	MPSP1518B
Package body size	15.0 × 14.0 × 0.57 mm
Lead composition	SAC125/Ni
Fab process	4 nm
Fab sites	TSMC
Assembly sites	■ Amkor, Korea ■ Shinko, Japan
Solder ball pitch	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	July 2021	Initial release
AB	August 2021	■ Table 1-1 *SM8475 features*: Updated this table ■ Chapter 2 *Pin definitions*: Added this chapter
AC	February 08, 2022	■ Global change: Updated eUSB to eUSB2 ■ Device description: Updated the package dimensions from 14.0 × 15.0 mm × 0.57 mm to 15.0 × 14.0 mm × 0.57 mm ■ Table 1-1 *SM8475 features*: □ Updated memory support feature □ Updated the package dimensions from 14.0 × 15.0 mm × 0.57 mm to 15.0 × 14.0 mm × 0.57 mm ■ Section 3 *Electrical specifications*: Added this chapter ■ Section 4.2 Part marking: Added part marking information ■ Section 4.3 Device ordering information: Added ES device ordering details ■ Section 4.4 Device moisture sensitivity level: Added this section ■ Section 5 *Carrier, storage, and handling information*: Added this chapter ■ Section 6 *PCB mounting guidelines*: Added this chapter ■ Section 7 *Part reliability*: Added this chapter
AD	March 2022	■ Table 4-1 *Device marking line definitions*: Updated the details for line E - ES1 and ES2 identification ■ Table 4-4 *Device identification details*: Updated the following □ Updated the modem information □ Added ES2 sample details □ Updated the table footnotes for ES2 - CPU frequency uplift SKU ■ Table 4-6 *ES identification*: Added this table ■ Section 5.4.1 *Lot code detail*: Added this section

Revision	Date	Description
AE	April 2022	■ Figure 3-5 *SD interface timing*: Updated this figure (removed HS400 mode input and output timing) ■ Table 1-1 *SM8475 features*: Added the core frequency and cache information ■ Table 2-1 *I/O description (pad type) parameters*: Removed PX710 and PX711 ■ Table 2-3 *MSM bottom pin descriptions – general-purpose input/output ports*: Updated the voltage pad characteristics of AW26, AW27, AW28, AW29, AY22, AY23, AY24, AY25, AY26, AY27, AY28, AY29, AY30, AY31, BA23, BA24, BA25, BA27, BA28, BA29, BA30, BA32, BA33, BB25, BB26, BB27, BB28, and BA26 ■ minimum and maximum values for the following tables: □ Table 3-1 *Absolute maximum ratings* □ Table 3-2 *Operating conditions for voltage rails with AVS Type-1* □ Table 3-3 *Operating conditions for non AVS voltage rails* ■ Added minimum and maximum values for the following tables: □ Table 3-5 *DC specification of 1.8 V GPIOs* □ Table 3-6 *UFS clock DC characteristics (VDD_PX10)* □ Table 3-7 *SDC2 1.2 V mode DC specifications (VDD_PX14)* □ Table 3-16 *Digital microphone timing* □ Table 3-18 *PHY timing parameters (1.8 V systems)* □ Table 3-21 *I2S interface timing parameters* □ Table 3-22 *PCM/TDM interface timing parameters* □ Table 3-24 *SPI master timing characteristics* □ Table 3-25 *CXO timing parameters* □ Table 3-26 *Sleep-clock timing parameters* □ Table 3-27 *JTAG interface timing characteristics* □ Table 3-28 *SWD write and read AC timing parameters* ■ Deleted UIM 1.8 V mode DC specifications table and the contents are updated in Table 3-5 *DC specification of 1.8 V GPIOs* ■ Table 4-4 *Device identification details*: Added CS device details ■ Added reliability data for the following tables: □ Table 7-1 *Silicon reliability results* □ Table 7-2 *SM8475-LPDDR5 package reliability results* ■ Added assembly site code for the following tables: □ Table 4-1 *Device marking line definitions* □ Table 7-3 *Device characteristics* ■ Section 3.9 *Connectivity*: Replaced USB with eUSB2
AF	May 17, 2022	■ Table 1-1 *SM8475 features*: Corrected the cache information from 128 MB to 128 KB for kyro Silver ■ Table 3-3 *Operating conditions for non AVS voltage rails*: Corrected the net name description detail for VDD_A_USB_SS_DP_0P9 ■ Table 4-6 *ES/CS identification*: □ Updated the table title □ Updated the table for CS sample

Revision	Date	Description
AG	May 20, 2022	■ Table 7-2 *SM8475-LPDDR5 package reliability results*: □ Updated the Temperature cycle status (TC700) for Amkor and Shinko sample size □ Updated the High-temperature storage life ECD date from 5/18/2022 to 5/31/2022
AH	May 27, 2022	■ Table 7-2 *SM8475-LPDDR5 package reliability results*: □ Updated the test status for High-temperature storage life (HTS1000) Amkor and Shinko sample size
Revision AI was omitted in accordance with QTI document conventions		
AJ	July 2022	■ Global change: Updated the document for SM8475P ■ Figure 1-2 *SM8475P functional block diagram and example application*: Added this figure ■ Table 1-1 *SM8475/SM8475P features*: □ Updated the debug list □ RF (SM8475P does not support the RF features listed here) □ PMIC (PMR735B is not applicable for SM8475P) ■ Table 4-1 *Device marking line definitions*: Updated the table for SM8475P ■ Table 4-3 *Device identification code*: Updated the table for SM8475P ■ Table 4-4 *Device identification details*: □ Updated the table for SM8475 AB SKU device details □ Updated the table for SM8475P ■ Table 4-5 *SM8475 ES/CS identification (AC SKU)*: Updated the table title ■ Table 4-6 *SM8475P CS identification*: Added this table

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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