Device description

The SDM845 includes the next generation of the Qualcomm® Snapdragon™ 800 series processor and LTE modem.

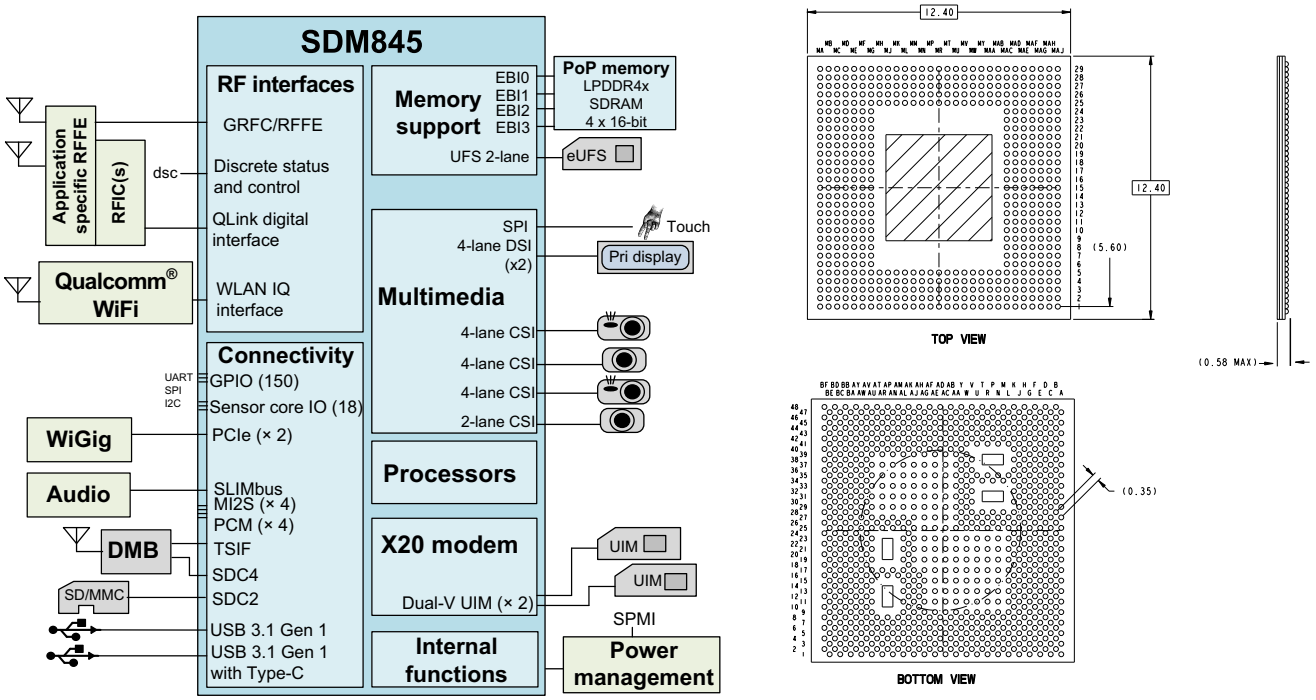
Key processor and memory characteristics include:

- 10 nm LPE FinFET process for lower active power dissipation and faster peak CPU performance
- 12.4 × 12.4 mm MEP
- A customized 64-bit ARM v8-compliant octacore Qualcomm® Kryo™ 385 applications processor
- Qualcomm® Adreno™ 630 graphics processing unit (GPU) 4K 60 fps or 2 × 2K 90 fps
- Audio DSP for low-power audio subsystem (LPASS)
- Compute DSP with Qualcomm® Hexagon™ Vector Extensions (HVX) processor
- Dedicated low-power Snapdragon sensor core with DSP to support always-on use cases
- Secure processor
- Four-channel package-on-package (PoP) high-speed memory, LPDDR4x SDRAM
- 3 MB system cache

Key features (see Section 1.2 for details)

- Always-on subsystem with RPMh for hardware-based resource and power management
- Qualcomm® Snapdragon™ Universal Bandwidth Compression (UBWC) 2.0, 2x compression with camera, display, and DSP
- Integrated X20 LTE modem to support latest air interfaces including 5 x CA up to 1.2 Gbps
- Two 4-lane DSI D-PHY 1.2 at 2.5 Gbps per lane
- 3840 × 2400 display at 60 fps, 2560 buffer width (10 layers blending), and VESA DSC 1.1
- A complete 4K60 entertainment system 4K60 10b encode + 4k60 10b decode
- Qualcomm Spectra™ 280 camera: dual 14-bit image signal processing (ISP) + Lite ISP: 16 + 16 + 2 megapixels (MP) to support 32 MP/30 fps
- Three 4-lane CSI with C-PHY/D-PHY and one 2-lane CSI with D-PHY to support 4 + 4 + 4 + 2
- 1 x UFS 2.1, 2 x USB 3.1, DisplayPort
- One 1-lane PCIe Gen 2 and one 1-lane PCIe Gen 3
- WLAN 802.11ac and Bluetooth 5.0 with the WCN3990 device; WiGig (802.11ad/60 GHz) with the QCA6335 + QCA6310 device

SDM845 high-level block diagram and 914B MPSP drawing



Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

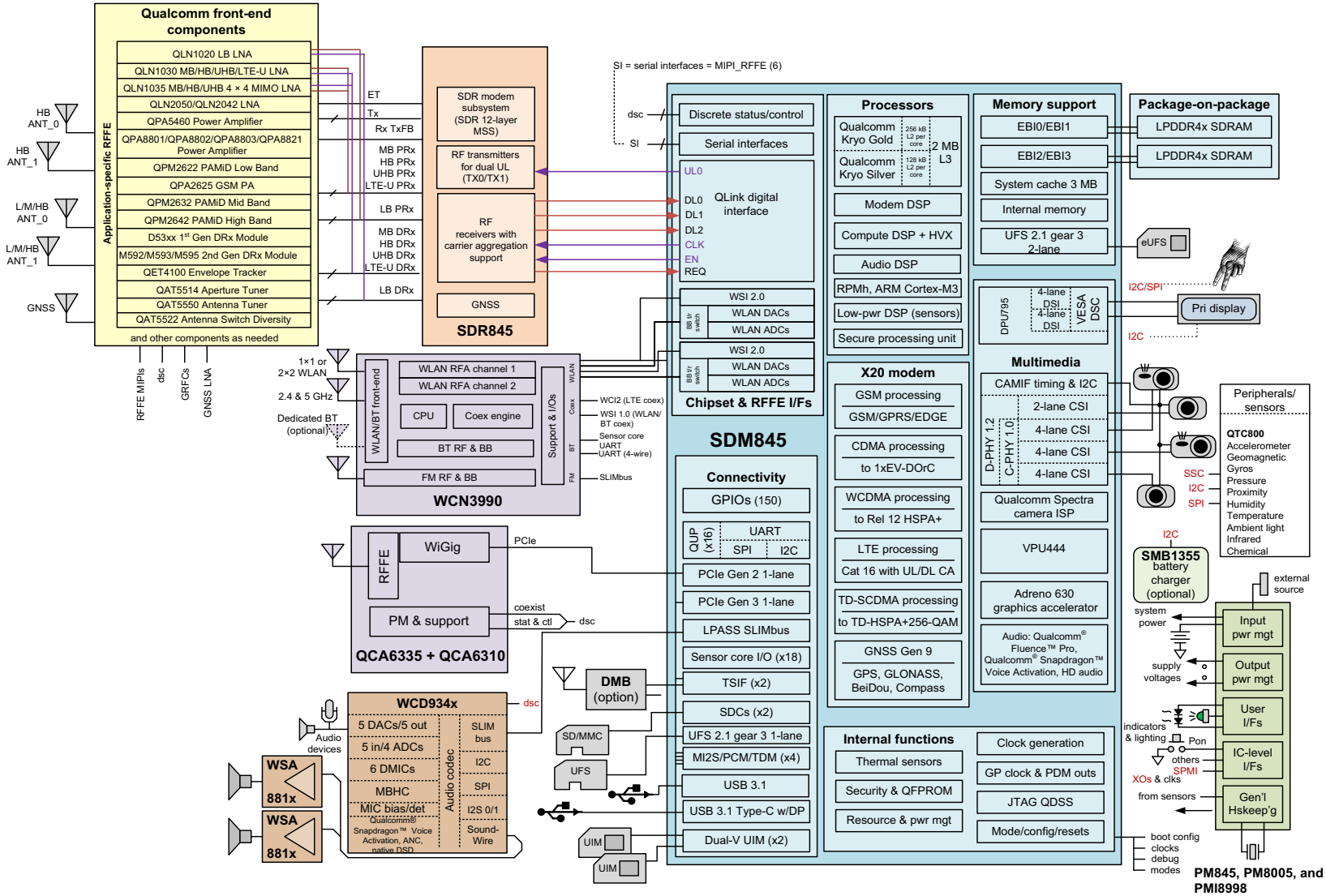


Figure 1-1 SDM845 functional block diagram and example application

1.2 SDM845 features

NOTE Some of the hardware features integrated within the SDM845 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SDM845 features.

Table 1-1 SDM845 features

Feature	SDM845 capability
Processors	
Applications	64-bit applications processor (Kryo 385) with 2 MB L3 cache ■ Quad high-performance Kryo cores at 2.649 GHz – Kryo Gold cluster with 256 kB L2 cache per core □ Kryo Gold single-core boost at 2.803 GHz ■ Quad low-power Kryo cores at 1.766 GHz – Kryo Silver cluster with 128 kB L2 cache per core
Digital signal processing	Compute DSP with Hexagon Vector eXtensions (dual-HVX512) and Hexagon coprocessor Audio DSP dedicated to audio subsystem Modem DSP to support 5x DL CA, UL MIMO
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Sensor core	Snapdragon sensor core with dedicated sensor DSP and 1.0 MB memory (512 kB TCM + 512 kB L2) to support always-on low-power use cases
Security	Dedicated secure processing unit
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR4x SDRAM (4x 16-bit) designed for a 1866 MHz clock 3 MB system cache
Other internal memory	256 KB IMEM 1 MB GMEM for graphics
External memory Via UFS Via SDC	 UFS 2.1 gear 3 – 2 lanes for on-board memory SD v3.0 4-bit for SD card

Table 1-1 SDM845 features (cont.)

Feature	SDM845 capability
RF support	
RF operating bands	Defined by the wafer-level RF transceiver device SDR845
Air interfaces	See Table 1-2.
GSM	Yes
CDMA	Yes
WCDMA	Yes
TD-SCDMA	Yes
LTE	Yes (Cat 16+ with 1.2 Gbps capability)
WLAN/Bluetooth	Yes (with WCN3990)
Advanced techniques	Up to 5 DL CA, up to 2 UL CA, 4 × 4 MIMO using single TRx
GNSS – Qualcomm® Location Suite engine	Gen 9; GPS, GLONASS, BeiDou
Multimedia	
Display support	Multistream supported
MIPI_DSI	Two 4-lane; DSI D-PHY 1.2 or C-PHY 1.0; VESA DSC 1.1
DisplayPort	DisplayPort 1.4+ data concurrency over USB
Miracast	Yes; v2.0 (4 k at 30 fps)
Example combinations	■ 3840 × 2400 10-bit 60 fps + 4K60 DisplayPort 10-bit or 4K30 Miracast ■ 2 x 2400 × 2400 120 fps (VR), LTM, 16-layer
General display features	Color depth – 24-bit per pixel; TFT, LTPS, CSTN, and OLED panels
Mobile display processor	DPU 795
Camera interfaces	MIPI CSI configurable in 4 + 4 + 4 + 2 configuration
MIPI_CSI	■ D-PHY: 2.5 Gbps/lane on 4-lane CSI and 2-lane CSI ■ C-PHY: ~17 Gbps (2.5 G symbols per trio per second) on 4-lane CSI
Performance	■ Qualcomm Spectra 280 ISP to support up to seven cameras (three concurrent) ■ Real-time sensor input resolution: 16 +16 + 2 MP ■ 32 MP 30 fps ZSL with a dual ISP ■ 16 MP 30 ZSL with a single ISP
Video applications performance	VPU444 4K60 decode for H.264 High Profile, H.265 Main 10 Profile and VP9 Profile 2 4K60 encode for H.264 High Profile, H.265 Main 10 Profile 4K30 encode for VP8 Support for HDR 10-bit video playback (HLG, HDR10) Support for HDR 10-bit capture (HLG)
Graphics	■ Adreno 630 – 4K 60 fps UI or 2x 2k × 2k 90 fps UI ■ OpenGL ES 3.2 + AEP, DX next, Vulkan 2 ■ OpenCL 2.0 full profile, RenderScript

Table 1-1 SDM845 features (cont.)

Feature	SDM845 capability
Audio	Dedicated LPASS audio DSP with 1 MB L2 cache
Codec	Integrated within the WCD9340/WCD9341 high-fidelity audio codec: ■ Five DACs; five outputs ■ Five differential analog inputs; four ADCs ■ Six digital microphones ■ Open DSP CPE voice activation subsystem for ultra low-power voice wake-up ■ Native DSD (WCD9341 only), MBHC, and ANC ■ 130 dB dynamic range ■ 32-bit DAC ■ 44.1 kHz family native playback ■ 5 GPIOs
Speaker amplifier	Integrated within the WSA8810/WSA8815 class D/G, low noise smart amplifier: ■ 2 W/4 W output power into 8 Ω load ■ Integrated SmartBoost ■ Integrated feedback speaker protection for excursion and temperature control of the transducers ■ Supports receiver assist speaker (RAS) or speaker as receiver (SAR) with handset ANC
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	QCELP, EVS, EVRC, EVRC-B, EVRC-WB; G.7Gen, G.729A/AB; GSM-FR, GSM-EFR, and GSM-HR; AMR-NB and AMR-WB
Audio codec support	MP3; aacPlus, eAAC; WMA 9/Pro
Enhanced audio	■ Surround sound: advanced multichannel ■ Fluence™ Pro noise cancellation; enhanced speaker protection ■ Qualcomm enhanced 3D audio solution, Qualcomm stereo audio expansion feature, and Qualcomm intelligent mixing algorithm
Digital mobile broadcast (DMB)	External IC required with TSIF or SDIO interface
Connectivity	
Qualcomm universal peripheral (QUP) ports	16, 4 bits each; multiplexed serial interface functions
UART	UART interface available on all QUPs. HS-UART available on GPIO QUP6/QUP7 and Snapdragon sensor core QUP3/QUP4/QUP5
I^2C	I^2C interface available on all QUPs up to 1 Mbps for touch, sensors, near field communicator (NFC), and so on; dedicated controller for each port
SPI	SPI interfaces available on all QUPs for cameras, sensors, and so on; dedicated controller for each port
CCI I^2C	Two dedicated I^2C interfaces for camera
UIM	Two – dual voltage (1.8 V/2.95 V)
USB	2x USB 3.1, one can support Type-C with DisplayPort
PCIe	Two – One Gen 2 1-lane with PHY 2.1 and one Gen 3 1-lane with PHY 3.0
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card; DMB; eSD boot

Table 1-1 SDM845 features (cont.)

Feature	SDM845 capability
TSIF	DMB support
Audio interfaces	
SLIMbus	Two; highly multiplexed, high-speed; baseline WCD9340/WCD9341
MI2S	Full duplex stereo or up to quad channel Tx/Rx MI2S (x3) ■ Up to eight channels for multichannel Tx/Rx audio applications (x1) ■ Half duplex stereo Rx MI2S (x1)
PCM/TDM	Up to four interfaces: 16 active Tx and Rx slots per individual interface ■ Up to 512 bits/frame and 32 bits/slot ■ Short, long, and one-slot sync mode ■ Maximum clock frequency of 24.576 MHz
Wireless connectivity	WCN3990 2 × 2 802.11ac RF QCA6335 and QCA6310 (802.11ad/60 GHz)
Touchscreen support	Capacitive panels via ext IC (I^2C, SPI, and interrupts) QTC800 Qualcomm® improveTouch™ controller
DMB support	Via external DMB device (SDC or TSIF)
Configurable GPIOs	
Number of GPIO ports	150 – GPIO_0 to GPIO_149
Number of sensor I/Os	18 – SSC_0 to SSC_17
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment, hardware supported KeyStore
Crypto engines	Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), inline crypto engine (FIPS-compliant)
TrustZone services	Secure file system, fast trusted storage
DRM support in hardware	PlayReady SL2000/SL3000, Widevine level 1, ISDB-T
QFPROM	640 bits available for OEM use
Access control	Programmable security domain protection and sand-boxing FlexSKU over-the-air feature
Boot sequence	■ 1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) modem PBL; 7) SP PBL; 8) VPU444, audio, Snapdragon sensor core, compute ■ Emergency boot over USB 3.1
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem

Table 1-1 SDM845 features (cont.)

Feature	SDM845 capability
Chipset and RF front-end (RFFE) interface features	
WTR RF transceivers QLink digital interface Power management	 ■ Three downlink lanes and one uplink lane ■ Improved layout, routing, package, and signal integrity 2-line SPMI; plus other lines, as needed, via GPIOs
Wireless connectivity WLAN baseband data Bluetooth	 I/ Q differential pair interface UART interface
Fabrication technology and package	
Digital die	10 nm FinFET process for lower active power dissipation, faster peak CPU
PoP – small, thermally efficient package Bottom pin array Top pin array	914B MPSP: 12.4 × 12.4 × 0.58 mm max (without memory device on top) 914-pin picoscale package (914 PSP); 0.35 mm pitch 556-pin nanoscale package (556 NSP); 0.4 mm pitch

1.2.1 Air interface features

Table 1-2 Key modem features

Standard	Feature descriptions
LTE	
Category	16
Carrier aggregation	FDD and TDD; up to 80 MHz
CA direction	Uplink and downlink
Other LTE support	■ FeICIC-IC ■ ePDCCH ■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ 4-way Rx diversity ■ 8 × 4 MIMO
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1xSLTE and 1xSRLTE ■ hVoLTE and hSRLTE
Multi-SIM	
3G	3G + GSM DSDS
4G	4G + GSM DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility

Table 1-2 Key modem features (cont.)

Standard	Feature descriptions
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite engine with global navigation satellite system (GNSS) support	
Gen 9	GPS and GLONASS (GNSS), BeiDou/Compass, and Galileo

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN3990	802.11ac, 2 × 2 MIMO
With QCA6335 + QCA6310	WiGig – 802.11ad, 60 GHz
Bluetooth	
With WCN3990	Bluetooth 5.x and earlier

2 Pin definitions

The SDM845 is the lower device within a PoP system, as illustrated and explained in Figure 2-1.

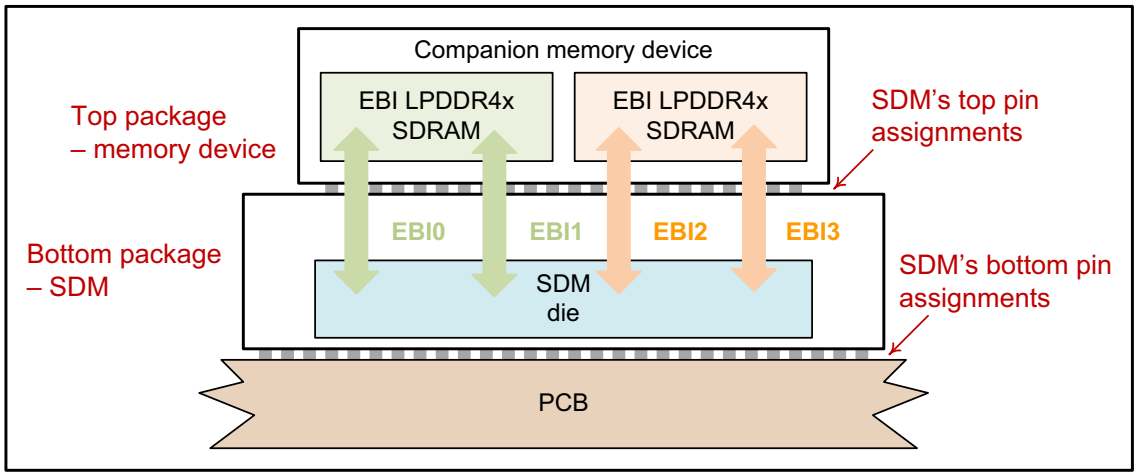


Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SDM845 bottom pins (Section 2.2)
- SDM845 top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (hi-Z) output

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX_2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX_6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX_10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.8 V
PX_13	Pad group 13 (secure processor); 1.85 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin assignments – bottom

2.2.1 Pin map – bottom

The SDM845 is available in the 914B MPSP. Its bottom surface is equivalent to a 914 PSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details and Section 2.3 for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11" × 17" sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.

- Download the *SDM845 Pin Assignment and GPIO Configuration Spreadsheet* (80-P6348-1A) – this Microsoft Excel spreadsheet lists all SDM845 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE Click the following link to download the pin assignment spreadsheet (80-P6348-1A) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-P6348-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

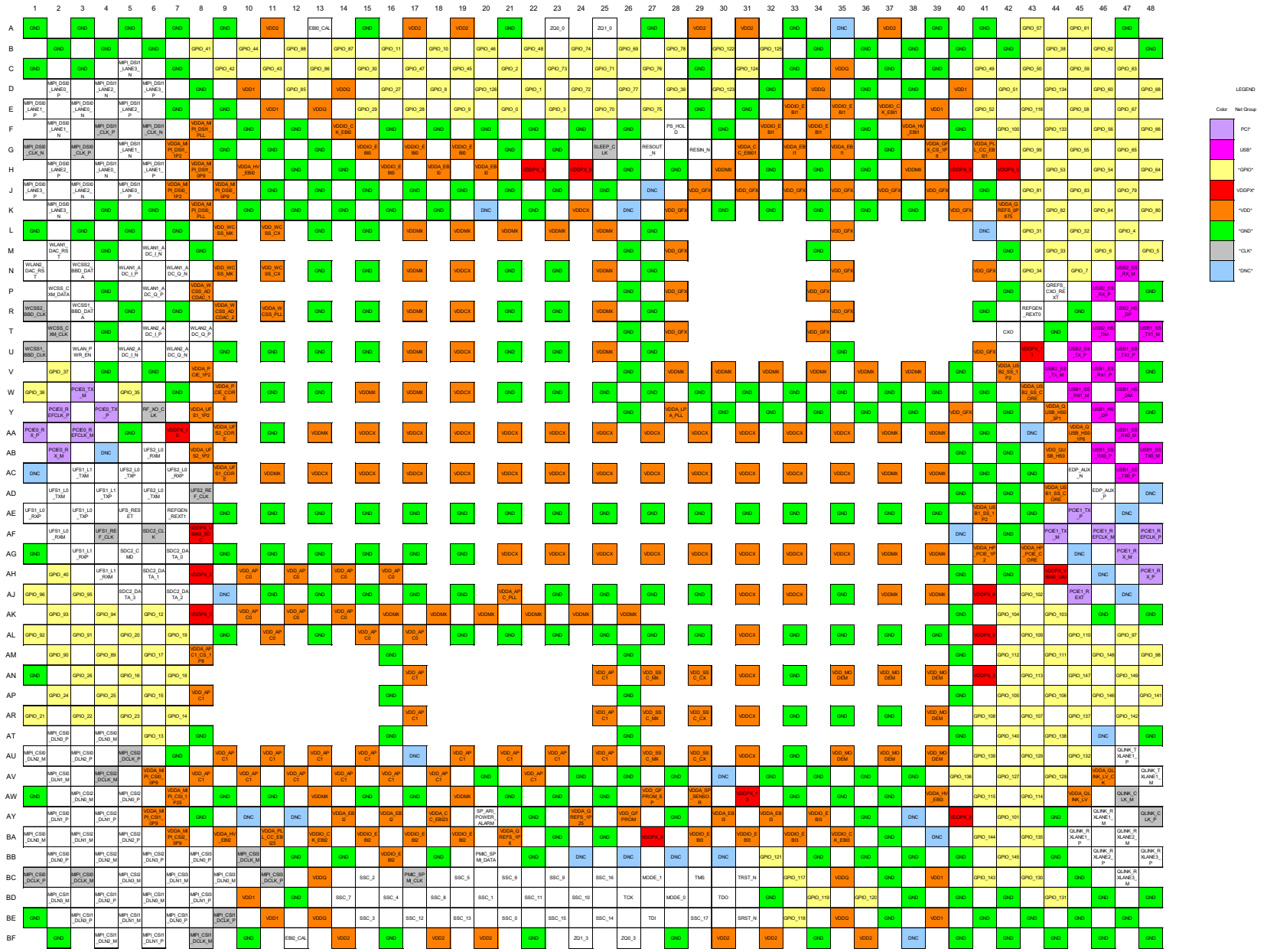


Figure 2-2 SDM845 bottom pin assignments

2.2.2 Pin descriptions – bottom

The bottom pins are described in Table 2-2 through Table 2-4.

Table 2-2 Bottom pin descriptions – general pins

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
T42	CXO	–	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
A13	EBI0_CAL	–	PX_3	AI	EBI0 LPDDR4x calibration resistor
BF12	EBI2_CAL	–	PX_3	AI	EBI2 LPDDR4x calibration resistor
AC45	EDP_AUX_N	–	PX_3	AI, AO	DisplayPort auxiliary channel – negative
AD46	EDP_AUX_P	–	PX_3	AI, AO	DisplayPort auxiliary channel – positive
BC3	MIPI_CSI0_DCLK_M	MIPI_CSI0_TLN0_A	CSI	AI	MIPI CSI 0, differential clock – minus
BC1	MIPI_CSI0_DCLK_P	–	CSI	AI	MIPI CSI 0, differential clock – plus
BA1	MIPI_CSI0_DLN0_M	MIPI_CSI0_TLN0_C	CSI	AI, AO	MIPI CSI 0, differential lane 0 – minus
BB2	MIPI_CSI0_DLN0_P	MIPI_CSI0_TLN0_B	CSI	AI, AO	MIPI CSI 0, differential lane 0 – plus
AV2	MIPI_CSI0_DLN1_M	MIPI_CSI0_TLN1_B	CSI	AI, AO	MIPI CSI 0, differential lane 1 – minus
AY2	MIPI_CSI0_DLN1_P	MIPI_CSI0_TLN1_A	CSI	AI, AO	MIPI CSI 0, differential lane 1 – plus
AU1	MIPI_CSI0_DLN2_M	MIPI_CSI0_TLN2_A	CSI	AI, AO	MIPI CSI 0, differential lane 2– minus
AU3	MIPI_CSI0_DLN2_P	MIPI_CSI0_TLN1_C	CSI	AI, AO	MIPI CSI 0, differential lane 2 – plus
AT4	MIPI_CSI0_DLN3_M	MIPI_CSI0_TLN2_C	CSI	AI, AO	MIPI CSI 0, differential lane 3 – minus
AT2	MIPI_CSI0_DLN3_P	MIPI_CSI0_TLN2_B	CSI	AI, AO	MIPI CSI 0, differential lane 3 – plus
BF8	MIPI_CSI1_DCLK_M	MIPI_CSI1_TLN0_A	CSI	AI	MIPI CSI 1, differential clock – minus
BE9	MIPI_CSI1_DCLK_P	–	CSI	AI	MIPI CSI 1, differential clock – plus
BD6	MIPI_CSI1_DLN0_M	MIPI_CSI1_TLN0_C	CSI	AI, AO	MIPI CSI 1, differential lane 0 – minus
BE7	MIPI_CSI1_DLN0_P	MIPI_CSI1_TLN0_B	CSI	AI, AO	MIPI CSI 1, differential lane 0 – plus
BE5	MIPI_CSI1_DLN1_M	MIPI_CSI1_TLN1_B	CSI	AI, AO	MIPI CSI 1, differential lane 1 – minus
BF6	MIPI_CSI1_DLN1_P	MIPI_CSI1_TLN1_A	CSI	AI, AO	MIPI CSI 1, differential lane 1– plus
BF4	MIPI_CSI1_DLN2_M	MIPI_CSI1_TLN2_A	CSI	AI, AO	MIPI CSI 1, differential lane 2 – minus
BD4	MIPI_CSI1_DLN2_P	MIPI_CSI1_TLN1_C	CSI	AI, AO	MIPI CSI 1, differential lane 2 – plus
BD2	MIPI_CSI1_DLN3_M	MIPI_CSI1_TLN2_C	CSI	AI, AO	MIPI CSI 1, differential lane 3 – minus
BE3	MIPI_CSI1_DLN3_P	MIPI_CSI1_TLN2_B	CSI	AI, AO	MIPI CSI 1, differential lane 3 – plus
AV4	MIPI_CSI2_DCLK_M	MIPI_CSI2_TLN0_A	CSI	AI	MIPI CSI 2, differential clock – minus
AU5	MIPI_CSI2_DCLK_P	–	CSI	AI	MIPI CSI 2, differential clock – plus
AW3	MIPI_CSI2_DLN0_M	MIPI_CSI2_TLN0_C	CSI	AI, AO	MIPI CSI 2, differential lane 0 – minus
AW5	MIPI_CSI2_DLN0_P	MIPI_CSI2_TLN0_B	CSI	AI, AO	MIPI CSI 2, differential lane 0 – plus
BA3	MIPI_CSI2_DLN1_M	MIPI_CSI2_TLN1_B	CSI	AI, AO	MIPI CSI 2, differential lane 1 – minus
AY4	MIPI_CSI2_DLN1_P	MIPI_CSI2_TLN1_A	CSI	AI, AO	MIPI CSI 2, differential lane 1 – plus
BB4	MIPI_CSI2_DLN2_M	MIPI_CSI2_TLN2_A	CSI	AI, AO	MIPI CSI 2, differential lane 2– minus
BA5	MIPI_CSI2_DLN2_P	MIPI_CSI2_TLN1_C	CSI	AI, AO	MIPI CSI 2, differential lane 2 – plus
BC5	MIPI_CSI2_DLN3_M	MIPI_CSI2_TLN2_C	CSI	AI, AO	MIPI CSI 2, differential lane 3 – minus
BB6	MIPI_CSI2_DLN3_P	MIPI_CSI2_TLN2_B	CSI	AI, AO	MIPI CSI 2, differential lane 3 – plus

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB10	MIPI_CSI3_DCLK_M	–	CSI	AI	MIPI CSI 3, differential clock – minus (available on product revision [RR] = 01; see Table 4-3)
BC11	MIPI_CSI3_DCLK_P	–	CSI	AI	MIPI CSI 3, differential clock – plus (available on product revision [RR] = 01; see Table 4-3)
BC9	MIPI_CSI3_DLN0_M	–	CSI	AI, AO	MIPI CSI 3, differential lane 0 – minus (available on product revision [RR] = 01; see Table 4-3)
BB8	MIPI_CSI3_DLN0_P	–	CSI	AI, AO	MIPI CSI 3, differential lane 0 – plus (available on product revision [RR] = 01; see Table 4-3)
BC7	MIPI_CSI3_DLN1_M	–	CSI	AI, AO	MIPI CSI 3, differential lane 1 – minus (available on product revision [RR] = 01; see Table 4-3)
BD8	MIPI_CSI3_DLN1_P	–	CSI	AI, AO	MIPI CSI 3, differential lane 1 – plus (available on product revision [RR] = 01; see Table 4-3)
G1	MIPI_DSI0_CLK_N	–	DSI	AO	MIPI display serial interface 0 clock – negative
G3	MIPI_DSI0_CLK_P	–	DSI	AO	MIPI display serial interface 0 clock – positive
E3	MIPI_DSI0_LANE0_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
D2	MIPI_DSI0_LANE0_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
F2	MIPI_DSI0_LANE1_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
E1	MIPI_DSI0_LANE1_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
J3	MIPI_DSI0_LANE2_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
H2	MIPI_DSI0_LANE2_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
K2	MIPI_DSI0_LANE3_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
J1	MIPI_DSI0_LANE3_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
F6	MIPI_DSI1_CLK_N	–	DSI	AO	MIPI display serial interface 1 clock – negative
F4	MIPI_DSI1_CLK_P	–	DSI	AO	MIPI display serial interface 1 clock – positive
H4	MIPI_DSI1_LANE0_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
J5	MIPI_DSI1_LANE0_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
G5	MIPI_DSI1_LANE1_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
H6	MIPI_DSI1_LANE1_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
D4	MIPI_DSI1_LANE2_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
E5	MIPI_DSI1_LANE2_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
C5	MIPI_DSI1_LANE3_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
D6	MIPI_DSI1_LANE3_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
BD28	MODE_0	–	PX_3	DI-S PD	Mode control bit 0 – unconnected for native mode
BC27	MODE_1	–	PX_3	DI-S PD	Mode control bit 1 – unconnected for native mode
AA3	PCIE0_REFCLK_M	–	–	AO	PCIe 0 Gen 2 reference clock – minus
Y2	PCIE0_REFCLK_P	–	–	AO	PCIe 0 Gen 2 reference clock – plus
AB2	PCIE0_RX_M	–	–	AI	PCIe 0 Gen 2 receive – minus
AA1	PCIE0_RX_P	–	–	AI	PCIe 0 Gen 2 receive – plus
W3	PCIE0_TX_M	–	–	AO	PCIe 0 Gen 2 transmit – minus
Y4	PCIE0_TX_P	–	–	AO	PCIe 0 Gen 2 transmit – plus
AF46	PCIE1_REFCLK_M	–	–	AO	PCIe 1 Gen 3 reference clock – minus
AF48	PCIE1_REFCLK_P	–	–	AO	PCIe 1 Gen 3 reference clock – plus

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AJ45	PCIE1_REXT	–	–	AI, AO	PCIe 1 external resistor
AG47	PCIE1_RX_M	–	–	AI	PCIe 1receive – minus
AH48	PCIE1_RX_P	–	–	AI	PCIe 1receive – plus
AF44	PCIE1_TX_M	–	–	AO	PCIe 1transmit – minus
AE45	PCIE1_TX_P	–	–	AO	PCIe 1transmit – plus
BC17	PMIC_SPMI_CLK	–	PX_3	B	Slave and PBUS interface for PMICs – clock
BB20	PMIC_SPMI_DATA	–	PX_3	DO	Slave and PBUS interface for PMICs – data
F28	PS_HOLD	–	PX_3	DO	Power-supply hold signal to PMIC
AW47	QLINK_CLK_M	–	–	AO	QLink clock – minus
AY48	QLINK_CLK_P	–	–	AO	QLink clock – plus
AY46	QLINK_RXLANE1_M	–	–	AI	QLink downlink lane 1 – minus
BA45	QLINK_RXLANE1_P	–	–	AI	QLink downlink lane 1 – plus
BA47	QLINK_RXLANE2_M	–	–	AI	QLink downlink lane 2 – minus
BB46	QLINK_RXLANE2_P	–	–	AI	QLink downlink lane 2– plus
BC47	QLINK_RXLANE3_M	–	–	AI	QLink downlink lane 3 – minus
BB48	QLINK_RXLANE3_P	–	–	AI	QLink downlink lane 3 – plus
AV48	QLINK_TXLANE1_M	–	–	AO	QLink uplink lane 1 – minus
AU47	QLINK_TXLANE1_P	–	–	AO	QLink uplink lane 1 – plus
P44	QREFS_CXO_REXT	–	PX_11	AI, AO	External resistor for on-die clocking
R43	REFGEN_REXT0	–	PX_3	AI	East-side high-speed interface – external resistor
AE7	REFGEN_REXT1	–	PX_3	AI	West-side high-speed interface – external resistor
G29	RESIN_N	–	PX_3	DI	Reset input
G27	RESOUT_N	–	PX_3	DO	Reset output
Y6	RF_XO_CLK	–	PX_3	DI	WLAN reference clock
AF6	SDC2_CLK	–	PX_2	DO	Secure digital controller 2 clock
AG5	SDC2_CMD	–	PX_2	DO	Secure digital controller 2 command
AG7	SDC2_DATA_0	–	PX_2	DO	Secure digital controller 2 data bit 0
AH6	SDC2_DATA_1	–	PX_2	DO	Secure digital controller 2 data bit 1
AJ7	SDC2_DATA_2	–	PX_2	DO	Secure digital controller 2 data bit 2
AJ5	SDC2_DATA_3	–	PX_2	DO	Secure digital controller 2 data bit 3
G25	SLEEP_CLK	–	PX_3	DI	Sleep clock
AY20	SP_ARI_POWER_ALARM	–	PX_13	–	–
BE31	SRST_N	–	PX_3	DI-PU	JTAG reset for debug
BD26	TCK	–	PX_3	DI-PU	JTAG clock input
BE27	TDI	–	PX_3	DI-PU:nppdkp	JTAG data input
BD30	TDO	–	PX_3	DO-Z	JTAG data output
BC29	TMS	–	PX_3	DI-PU:nppdkp	JTAG mode select input
BC31	TRST_N	–	PX_3	DI-PD:nppukp	JTAG reset
AE5	UFS_RESET	–	PX_10	DO-Z PD:nppukp	UFS reset

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AF2	UFS1_L0_RXM	–	PX_10	AI	UFS 1 receive lane 0 – minus
AE1	UFS1_L0_RXP	–	PX_10	AI	UFS 1 receive lane 0 – plus
AD2	UFS1_L0_TXM	–	PX_10	AO	UFS 1 transmit lane 0 – minus
AE3	UFS1_L0_TXP	–	PX_10	AO	UFS 1 transmit lane 0 – plus
AH4	UFS1_L1_RXM	–	PX_10	AI	UFS 1 receive lane 1 – minus
AG3	UFS1_L1_RXP	–	PX_10	AI	UFS 1 receive lane 1 – plus
AC3	UFS1_L1_TXM	–	PX_10	AO	UFS 1 transmit lane 1 – minus
AD4	UFS1_L1_TXP	–	PX_10	AO	UFS 1 transmit lane 1 – plus
AF4	UFS1_REF_CLK	–	PX_10	DO-Z PD:nppukp	UFS 1 reference clock
AB6	UFS2_L0_RXM	–	PX_10	AI	UFS 2 receive lane 0 – minus (the UFS2 interface is not supported on SDM845)
AC7	UFS2_L0_RXP	–	PX_10	AI	UFS 2 receive lane 0 – plus (the UFS2 interface is not supported on SDM845)
AD6	UFS2_L0_TXM	–	PX_10	AO	UFS 2 transmit lane 0 – minus (the UFS2 interface is not supported on SDM845)
AC5	UFS2_L0_TXP	–	PX_10	AO	UFS 2 transmit lane 0 – plus (the UFS2 interface is not supported on SDM845)
AD8	UFS2_REF_CLK	–	PX_10	DO-Z PD:nppukp	UFS 2 reference clock (the UFS2 interface is not supported on SDM845)
W47	USB1_HS_DM	–	–	AI, AO	USB high-speed 1 data – minus
Y46	USB1_HS_DP	–	–	AI, AO	USB high-speed 1 data – plus
AA47	USB1_SS_RX0_M	–	–	AI	USB super-speed 1 receive 0 – minus
AB46	USB1_SS_RX0_P	–	–	AI	USB super-speed 1 receive 0 – plus
W45	USB1_SS_RX1_M	–	–	AI	USB super-speed 1 receive 1 – minus
V46	USB1_SS_RX1_P	–	–	AI	USB super-speed 1 receive 1 – plus
AB48	USB1_SS_TX0_M	–	–	AO	USB super-speed 1 transmit 0 – minus
AC47	USB1_SS_TX0_P	–	–	AO	USB super-speed 1 transmit 0 – plus
T48	USB1_SS_TX1_M	–	–	AO	USB super-speed 1 transmit 1 – minus
U47	USB1_SS_TX1_P	–	–	AO	USB super-speed 1 transmit 1 – plus
T46	USB2_HS_DM	–	–	AI, AO	USB high-speed 2 data – minus
R47	USB2_HS_DP	–	–	AI, AO	USB high-speed 2 data – plus
N47	USB2_SS_RX_M	–	–	AI	USB super-speed 2 receive – minus
P46	USB2_SS_RX_P	–	–	AI	USB super-speed 2 receive – plus
V44	USB2_SS_TX_M	–	–	AO	USB super-speed 2 transmit – minus
U45	USB2_SS_TX_P	–	–	AO	USB super-speed 2 transmit – plus
T2	WCSS_CXM_CLK	–	PX_3	DO	WLAN coexistence module command clock (WSI 1.0)
P2	WCSS_CXM_DATA	–	PX_3	B	WLAN coexistence module command data (WSI 1.0)
U1	WCSS1_BBD_CLK	–	PX_3	DO	WLAN chain 1 baseband command clock (WSI 2.0)
R3	WCSS1_BBD_DATA	–	PX_3	B	WLAN chain 1 baseband command data (WSI 2.0)
R1	WCSS2_BBD_CLK	–	PX_3	DO	WLAN chain 2 baseband command clock (WSI 2.0)
N3	WCSS2_BBD_DATA	–	PX_3	B	WLAN chain 2 baseband command data (WSI 2.0)

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
U3	WLAN_PWR_EN	–	PX_3	DO	WLAN power enable
M6	WLAN1_ADC_I_N	–	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase minus
N5	WLAN1_ADC_I_P	–	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase plus
N7	WLAN1_ADC_Q_N	–	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature minus
P6	WLAN1_ADC_Q_P	–	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature plus
M2	WLAN1_DAC_RST	–	PX_3	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
U5	WLAN2_ADC_I_N	–	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase minus
T6	WLAN2_ADC_I_P	–	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase plus
U7	WLAN2_ADC_Q_N	–	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature minus
T8	WLAN2_ADC_Q_P	–	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature plus
N1	WLAN2_DAC_RST	–	PX_3	AI, AO	WLAN chain 2 digital-to-analog converter external resistor
A23	ZQ0_0	–	PX_3	AI	LPDDR4x ZQ resistor for lower x16 memory in rank 0
BF26	ZQ0_3	–	PX_3	AI	LPDDR4x ZQ resistor for upper x16 memory in rank 0
A25	ZQ1_0	–	PX_3	AI	LPDDR4x ZQ resistor for lower x16 memory in rank 1
BF24	ZQ1_3	–	PX_3	AI	LPDDR4x ZQ resistor for upper x16 memory in rank 1

1. See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function–carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SDM845 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click the following link to download the pin assignment spreadsheet (80-P6348-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-P6348-1A

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-3 Bottom pin descriptions – general-purpose input/output ports

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AN47	GPIO_149	–	RFFE1_CLK	PX_3	B-PD:nppukp	Configurable I/O RF front-end 1 interface clock
AM46	GPIO_148	–	RFFE1_DATA	PX_3	B-PD:nppukp	Configurable I/O RF front-end 1 interface data
AN45	GPIO_147	–	RFFE2_CLK GRFC33	PX_3	B-PD:nppukp	Configurable I/O RF front-end 2 interface clock Generic RF controller bit 33
AP46	GPIO_146	–	RFFE2_DATA GRFC34	PX_3	B-PD:nppukp	Configurable I/O RF front-end 2 interface data Generic RF controller bit 34
BB42	GPIO_145	Y	GPS_TX_AGGRESSOR_MIRA	PX_3	B-PD:nppukp	Configurable I/O Tx level may degrade GNSS receiver (A)
BA41	GPIO_144	–		PX_3	B-PD:nppukp	Configurable I/O
BC41	GPIO_143	–	GRFC5 GPS_TX_AGGRESSOR_MIRD	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 5 Tx level may degrade GNSS receiver (D)
AR47	GPIO_142	–	RFFE5_CLK	PX_3	B-PD:nppukp	Configurable I/O RF front-end 5 interface clock
AP48	GPIO_141	–	RFFE5_DATA	PX_3	B-PD:nppukp	Configurable I/O RF front-end 5 interface data
AT42	GPIO_140	–	RFFE4_CLK GRFC36	PX_3	B-PD:nppukp	Configurable I/O RF front-end 4 interface clock Generic RF controller bit 36
AU41	GPIO_139	–	RFFE4_DATA	PX_3	B-PD:nppukp	Configurable I/O RF front-end 4 interface data
AT44	GPIO_138	–	RFFE3_CLK GRFC32	PX_3	B-PD:nppukp	Configurable I/O RF front-end 3 interface clock Generic RF controller bit 32
AR45	GPIO_137	–	RFFE3_DATA GRFC35	PX_3	B-PD:nppukp	Configurable I/O RF front-end 3 interface data Generic RF controller bit 35
AV40	GPIO_136	–	GRFC1	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 1
BA43	GPIO_135	–	GRFC0 PA_INDICATOR_1_OR_2	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 0 PA transmit indicator
D44	GPIO_134	–	–	PX_3	B-PD:nppukp	Configurable I/O
F44	GPIO_133	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AU45	GPIO_132	Y	GRFC2	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 2

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BD44	GPIO_131	–	QLINK_ENABLE	PX_3	B-PD:nppukp	Configurable I/O QLink enable
BC43	GPIO_130	Y	QLINK_REQUEST	PX_3	B-PD:nppukp	Configurable I/O QLink request
AU43	GPIO_129	Y	GPS_TX_AGGRESSOR_MIRC	PX_3	B-PD:nppukp	Configurable I/O Tx level may degrade GNSS receiver (C)
AV44	GPIO_128	Y	GPS_TX_AGGRESSOR_MIRB	PX_3	B-PD:nppukp	Configurable I/O Tx level may degrade GNSS receiver (B)
AV42	GPIO_127	Y	GRFC3	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 3
D20	GPIO_126	Y	–	PX_3	B-PD:nppukp	Configurable I/O
B32	GPIO_125	Y	QUP_L6_9_CS	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 6: SPI_CS3
C31	GPIO_124	Y	QUP_L5_9_CS QDSS_GPIO_TRACECLK_LOCA	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 5: SPI_CS2 QDSS trace clock A
D30	GPIO_123	Y	QUP_L4_9_CS QDSS_GPIO_TRACECTL_LOCA	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 4: SPI_CS1 QDSS trace control A
B30	GPIO_122	Y	QDSS_GPIO_TRACEDATA_LOCA(5)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 5 A
BB32	GPIO_121	Y	QDSS_GPIO_TRACEDATA_LOCA(4)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 4 A
BD36	GPIO_120	Y	QDSS_GPIO_TRACEDATA_LOCA(3)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 3 A
BD34	GPIO_119	Y	QDSS_GPIO_TRACEDATA_LOCA(2)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 2 A
BE33	GPIO_118	Y	QDSS_GPIO_TRACEDATA_LOCA(1)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 1 A
BC33	GPIO_117	Y	QDSS_GPIO_TRACEDATA_LOCA(0)	PX_3	B-PD:nppukp	Configurable I/O QDSS trace data bit 0 A
E43	GPIO_116	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AW41	GPIO_115	Y	GRFC9 GPS_TX_AGGRESSOR_MIRF	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 9 Tx level may degrade GNSS receiver (F)
AW43	GPIO_114	–	GRFC8 GPS_TX_AGGRESSOR_MIRE	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 8 Tx level may degrade GNSS receiver E
AN43	GPIO_113	Y	UIM_BATT_ALARM EDP_HOT_PLUG_DETECT	PX_3	B-PD:nppukp	Configurable I/O UIM battery alarm
AM42	GPIO_112	Y	UIM1_PRESENT	PX_3	B-PD:nppukp	Configurable I/O UIM1 presence detection
AM44	GPIO_111	–	UIM1_RESET	PX_5	B-PD:nppukp	Configurable I/O UIM1 reset (dual voltage)
AL45	GPIO_110	–	UIM1_CLK	PX_5	B-PD:nppukp	Configurable I/O UIM1 clock (dual voltage)
AL43	GPIO_109	–	UIM1_DATA	PX_5	B-PD:nppukp	Configurable I/O UIM1 data (dual voltage)
AR41	GPIO_108	Y	UIM2_PRESENT QUP_L3(13)	PX_3	B-PD:nppukp	Configurable I/O UIM2 presence detection QUP 13, lane 3: SPI_CS0/UART_RX

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AR43	GPIO_107	–	UIM2_RESET QUP_L2(13) QUP_L6_8_CS	PX_6	B-PD:nppukp	Configurable I/O UIM2 reset (dual voltage) QUP 13, lane 2: SPI_CLK/UART_TX QUP 8, lane 6: SPI_CS3
AP44	GPIO_106	–	UIM2_CLK QUP_L1(13) QUP_L5_8_CS	PX_6	B-PD:nppukp	Configurable I/O UIM2 clock (dual voltage) QUP 13, lane 1: SPI_MOSI/UART_RFR/I2C_SCL QUP 8, lane 5: SPI_CS2
AP42	GPIO_105	–	UIM2_DATA QUP_L0(13) QUP_L4_8_CS	PX_6	B-PD:nppukp	Configurable I/O UIM2 data (dual voltage) QUP 13, lane 0: SPI_MISO/UART_CTS/I2C_SDA QUP 8, lane 4: SPI_CS1
AK42	GPIO_104	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AK44	GPIO_103	Y	PCI_E1_CLKREQN	PX_3	B-PU:nppukp	Configurable I/O PCIe 1 clock request
AJ43	GPIO_102	–	PCI_E1_RST_N	PX_3	B-PD:nppukp	Configurable I/O PCIe 1 reset
AY42	GPIO_101	Y	GRFC4	PX_3	B-PD:nppukp	Configurable I/O Generic RF controller bit 4
F42	GPIO_100	–	–	PX_3	B-PD:nppukp	Configurable I/O
G43	GPIO_99	–	–	PX_3	B-PD:nppukp	Configurable I/O
AM48	GPIO_98	–	RFFE6_DATA MDP_VSYNC_S_MIRB	PX_3	B-PD:nppukp	Configurable I/O RF front-end 6 interface data MDP vertical sync – secondary B
AL47	GPIO_97	Y	RFFE6_CLK GRFC37 MDP_VSYNC_P_MIRB	PX_3	B-PD:nppukp	Configurable I/O RF front-end 6 interface clock Generic RF controller bit 37 MDP vertical sync – primary B
AJ1	GPIO_96	Y	TSIF2_SYNC SDC4_DATA(0) QUP_L3(7)	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 2 sync Secure digital controller 4 data bit 0 QUP 7, lane 3: SPI_CS0/UART_RX
AJ3	GPIO_95	Y	TSIF2_DATA SDC4_DATA(1) QUP_L2(7) QSPI_CLK GP_PDM_MIRA[0]	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 2 data Secure digital controller 4 data bit 1 QUP 7, lane 2: SPI_CLK/UART_TX Quad SPI clock (available on product revision [RR] = 01; see Table 4-3) General-purpose PDM output 0 A
AK4	GPIO_94	–	TSIF2_EN SDC4_DATA(2) QUP_L1(7) QSPI_DATA(3)	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 2 enable Secure digital controller 4 data bit 2 QUP 7, lane 1: SPI_MOSI/UART_RFR/I2C_SCL Quad SPI data bit 3 (available on product revision [RR] = 01; see Table 4-3)
AK2	GPIO_93	–	TSIF2_CLK SDC4_CLK QUP_L0(7) QSPI_DATA(2) QDSS_GPIO_TRACEDATA_LOCA(13)	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 2 clock Secure digital controller 4 clock QUP 7, lane 0: SPI_MISO/UART_CTS/I2C_SDA Quad SPI data bit 2 (available on product revision [RR] = 01; see Table 4-3) QDSS trace data bit 13 A
AL1	GPIO_92	Y	TSIF2_ERROR SDC4_DATA(3) QUP_L3(4) QSPI_DATA(1)	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 2 error Secure digital controller 4 clock data bit 3 QUP 4, lane 3: SPI_CS0/UART_RX Quad SPI data bit 1 (available on product revision [RR] = 01; see Table 4-3)

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AL3	GPIO_91	Y	TSIF1_DATA SDC4_CMD QUP_L2(4) QSPI_DATA(0) QDSS_CTI_TRIG1_IN_MIRB	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 1 data Secure digital controller 4 command QUP 4, lane 2: SPI_CLK/UART_TX Quad SPI data bit 0 (available on product revision [RR] = 01; see Table 4-3) QDSS trigger input 1 B
AM2	GPIO_90	–	TSIF1_EN MDP_VSYNC0_OUT QUP_L1(4) QSPI_CS_N_0 MDP_VSYNC1_OUT MDP_VSYNC2_OUT MDP_VSYNC3_OUT QDSS_CTI_TRIG1_OUT_MIRB	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 1 enable MDP vertical sync QUP 4, lane 1: SPI_MOSI/UART_RFR/I2C_SCL Quad SPI chip select 0 (available on product revision [RR] = 01; see Table 4-3) MDP vertical sync MDP vertical sync MDP vertical sync QDSS trigger output 1 B
AM4	GPIO_89	Y	TSIF1_CLK QUP_L0(4) QSPI_CS_N_1	PX_3	B-PD:nppukp	Configurable I/O Transport stream interface 1 clock QUP 4, lane 0: SPI_MISO/UART_CTS/I2C_SDA Quad SPI chip select 1 (available on product revision [RR] = 01; see Table 4-3)
B12	GPIO_88	Y	QUP_L3(5)	PX_3	B-PD:nppukp	Configurable I/O QUP 5, lane 3: SPI_CS0/UART_RX
B14	GPIO_87	–	QUP_L2(5)	PX_3	B-PD:nppukp	Configurable I/O QUP 5, lane 2: SPI_CLK/UART_TX
C13	GPIO_86	Y	QUP_L1(5) GP_PDM_MIRA[1]	PX_3	B-PD:nppukp	Configurable I/O QUP 5, lane 1: SPI_MOSI/UART_RFR/I2C_SCL General-purpose PDM output 1 A
D12	GPIO_85	Y	QUP_L0(5)	PX_3	B-PD:nppukp	Configurable I/O QUP 5, lane 0: SPI_MISO/UART_CTS/I2C_SDA
K46	GPIO_84	Y	QUP_L3(15)	PX_3	B-PD:nppukp	Configurable I/O QUP 15, lane 3: SPI_CS0/UART_RX
J45	GPIO_83	–	SEC_MI2S_DATA1/PCM2_DOUT QUP_L2(15)	PX_3	B-PD:nppukp	Configurable I/O Secondary MI2S serial data channel 1 QUP 15, lane 2: SPI_CLK/UART_TX
K44	GPIO_82	–	SEC_MI2S_DATA0/PCM2_DIN QUP_L1(15)	PX_3	B-PD:nppukp	Configurable I/O Secondary MI2S serial data channel 0 QUP 15, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
J43	GPIO_81	–	SEC_MI2S_WS/PCM2_SYNC QUP_L0(15)	PX_3	B-PD:nppukp	Configurable I/O Secondary MI2S serial data word select QUP 15, lane 0: SPI_MISO/UART_CTS/I2C_SDA
K48	GPIO_80	Y	SEC_MI2S_SCK/PCM2_CLK QDSS_GPIO_TRACEDATA_LOCA(12)	PX_3	B-PD:nppukp	Configurable I/O Secondary MI2S clock QDSS trace data bit 12 A
J47	GPIO_79	Y	SEC_MI2S_MCLK GP_PDM_MIRA[2] QDSS_GPIO_TRACEDATA_LOCA(11)	PX_3	B-PD:nppukp	Configurable I/O Secondary MI2S master clock General-purpose PDM output 2 A QDSS trace data bit 11 A
B28	GPIO_78	Y	TER_MI2S_DATA1/PCM3_DOUT GCC_GP1_CLK_MIRB	PX_3	B-PD:nppukp	Configurable I/O Tertiary MI2S serial data channel 1 Global general-purpose clock 1 B
D26	GPIO_77	Y	TER_MI2S_DATA0/PCM3_DIN QDSS_GPIO_TRACEDATA_LOCA(10)	PX_3	B-PD:nppukp	Configurable I/O Tertiary MI2S serial data channel 0 QDSS trace data bit 10 A
C27	GPIO_76	–	TER_MI2S_WS/PCM3_SYNC QDSS_GPIO_TRACEDATA_LOCA(9)	PX_3	B-PD:nppukp	Configurable I/O Tertiary MI2S word select QDSS trace data bit 9 A

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
E27	GPIO_75	–	TER_MI2S_SCK/PCM3_CLK QDSS_GPIO_TRACEDATA_LOCA(8)	PX_3	B-PD:nppukp	Configurable I/O Tertiary MI2S clock QDSS trace data bit 8 A
B24	GPIO_74	–	BTFM_SLIMBUS_CLK TER_MI2S_MCLK	PX_3	B-PD:nppukp	Configurable I/O Bluetooth/FM SLIMbus clock Tertiary MI2S master clock
C23	GPIO_73	Y	BTFM_SLIMBUS_DATA	PX_3	B-PD:nppukp	Configurable I/O Bluetooth/FM SLIMbus data
D24	GPIO_72	–	LPASS_SLIMBUS_DATA1 SPKR_I2S_WS	PX_3	B-PD:nppukp	Configurable I/O Low-power audio SLIMbus data 1 Speaker I^2S word select
C25	GPIO_71	Y	LPASS_SLIMBUS_DATA0 SPKR_I2S_DATA_OUT	PX_3	B-PD:nppukp	Configurable I/O Low-power audio SLIMbus data 0 Speaker I^2S clock
E25	GPIO_70	–	LPASS_SLIMBUS_CLK SPKR_I2S_SCK	PX_3	B-PD:nppukp	Configurable I/O Low-power audio SLIMbus data 1 Speaker I^2S clock
B26	GPIO_69	–	SPKR_I2S_MCLK AUDIO_REF_CLK	PX_3	B-PD:nppukp	Configurable I/O Speaker I^2S master clock Audio reference clock
D48	GPIO_68	Y	PRI_MI2S_DATA1/PCM1_DOUT QUP_L3(8)	PX_3	B-PD:nppukp	Configurable I/O Primary MI2S data channel 1 QUP 8, lane 3: SPI_CS0/UART_RX
E47	GPIO_67	–	PRI_MI2S_DATA0/PCM1_DIN QUP_L2(8)	PX_3	B-PD:nppukp	Configurable I/O Primary MI2S data channel 0 QUP 8, lane 2: SPI_CLK/UART_TX
F48	GPIO_66	Y	PRI_MI2S_WS/PCM1_SYNC QUP_L1(8)	PX_3	B-PD:nppukp	Configurable I/O Primary MI2S word select QUP 8, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
G47	GPIO_65	–	PRI_MI2S_SCK/PCM1_CLK QUP_L0(8)	PX_3	B-PD:nppukp	Configurable I/O Primary MI2S clock QUP 8, lane 0: SPI_MISO/UART_CTS/I2C_SDA
H48	GPIO_64	Y	PRI_MI2S_MCLK	PX_3	B-PD:nppukp	Configurable I/O Primary MI2S master clock
C47	GPIO_63	Y	QUA_MI2S_DATA3 GP_PDM_MIRB[2] QDSS_CTI_TRIG1_IN_MIRA	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S data channel 3 General-purpose PDM output 2 B QDSS trigger input 1 A
B46	GPIO_62	Y	QUA_MI2S_DATA2 QDSS_CTI_TRIG1_OUT_MIRA	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S data channel 2 QDSS trigger output 1 A
A45	GPIO_61	Y	QUA_MI2S_DATA1/PCM4_DOUT	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S data channel 1
D46	GPIO_60	Y	QUA_MI2S_DATA0/PCM4_DIN	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S data channel 0
C45	GPIO_59	Y	QUA_MI2S_WS/PCM4_SYNC GCC_GP3_CLK_MIRA	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S word select Global general-purpose clock 3 A
E45	GPIO_58	Y	QUA_MI2S_SCK/PCM4_CLK GCC_GP2_CLK_MIRA	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S clock Global general-purpose clock 2 A
A43	GPIO_57	Y	QUA_MI2S_MCLK GCC_GP1_CLK_MIRA	PX_3	B-PD:nppukp	Configurable I/O Quaternary MI2S master clock Global general-purpose clock 1 A
F46	GPIO_56	Y	QUP_L1(10)	PX_3	B-PD:nppukp	Configurable I/O QUP 10, lane 1: SPI_MOSI/UART_RFR/I2C_SCL

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
G45	GPIO_55	–	QUP_L0(10)	PX_3	B-PD:nppukp	Configurable I/O QUP 10, lane 0: SPI_MISO/UART_CTS/I2C_SDA
H46	GPIO_54	Y	QUP_L3(10) GP_PDM_MIRB[0]	PX_3	B-PD:nppukp	Configurable I/O QUP 10, lane 3: SPI_CS0/UART_RX General-purpose PDM output 0 B
H44	GPIO_53	Y	QUP_L2(10)	PX_3	B-PD:nppukp	Configurable I/O QUP 10, lane 2: SPI_CLK/UART_TX
E41	GPIO_52	Y	QUP_L3(12) QDSS_CTI_TRIG0_IN_MIRA	PX_3	B-PD:nppukp	Configurable I/O QUP 12, lane 3: SPI_CS0/UART_RX QDSS trigger input 0 A
D42	GPIO_51	–	QUP_L2(12) QDSS_CTI_TRIG0_OUT_MIRA	PX_3	B-PD:nppukp	Configurable I/O QUP 12, lane 2: SPI_CLK/UART_TX QDSS trigger output 0 A
C43	GPIO_50	–	QUP_L1(12)	PX_3	B-PD:nppukp	Configurable I/O QUP 12, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
C41	GPIO_49	Y	QUP_L0(12)	PX_3	B-PD:nppukp	Configurable I/O QUP 12, lane 0: SPI_MISO/UART_CTS/I2C_SDA
B22	GPIO_48	Y	QUP_L3(6)	PX_3	B-PD:nppukp	Configurable I/O QUP 6, lane 3: SPI_CS0/UART_RX
C17	GPIO_47	–	QUP_L2(6)	PX_3	B-PU:nppukp	Configurable I/O QUP 6, lane 2: SPI_CLK/UART_TX
B20	GPIO_46	Y	QUP_L1(6)	PX_3	B-PD:nppukp	Configurable I/O QUP 6, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
C19	GPIO_45	–	QUP_L0(6)	PX_3	B-PD:nppukp	Configurable I/O QUP 6, lane 0: SPI_MISO/UART_CTS/I2C_SDA
B10	GPIO_44	Y	QUP_L3(3) QDSS_GPIO_TRACEDATA_LOCA(15)	PX_3	B-PD:nppukp	Configurable I/O QUP 3, lane 3: SPI_CS0/UART_RX QDSS trace data bit 15 A
C11	GPIO_43	Y	QUP_L2(3) QDSS_GPIO_TRACEDATA_LOCA(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 3, lane 2: SPI_CLK/UART_TX QDSS trace data bit 14 A
C9	GPIO_42	–	QUP_L1(3) QDSS_GPIO_TRACEDATA_LOCA(7)	PX_3	B-PD:nppukp	Configurable I/O QUP 3, lane 1: SPI_MOSI/UART_RFR/I2C_SCL QDSS trace data bit 7 A
B8	GPIO_41	Y	QUP_L0(3) QDSS_GPIO_TRACEDATA_LOCA(6)	PX_3	B-PD:nppukp	Configurable I/O QUP 3, lane 0: SPI_MISO/UART_CTS/I2C_SDA QDSS trace data bit 6 A
AH2	GPIO_40	Y	SD_WRITE_PROTECT TSIF1_ERROR	PX_3	B-PD:nppukp	Configurable I/O Secure digital card write protection Transport stream interface 1 error
D28	GPIO_39	Y	LPASS_SLIMBUS_DATA2	PX_3	B-PD:nppukp	Configurable I/O Low-power audio SLIMbus data 2
B44	GPIO_38	Y	USB_PHY_PS	PX_3	B-PD:nppukp	Configurable I/O USB PHY port select
V2	GPIO_37	Y	QUP_L6_1_CS	PX_3	B-PD:nppukp	Configurable I/O QUP 1, lane 6: SPI_CS3
W1	GPIO_36	Y	PCI_E0_CLKREQN QUP_L5_1_CS	PX_3	B-PU:nppukp	Configurable I/O PCIe 0 clock request QUP 1, lane 5: SPI_CS2
W5	GPIO_35	–	PCI_E0_RST_N QUP_L4_1_CS	PX_3	B-PD:nppukp	Configurable I/O PCIe 0 reset QUP 1, lane 4: SPI_CS1
N43	GPIO_34	Y	QUP_L3(11) QUP_L1(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 11, lane 3: SPI_CS0/UART_RX QUP 14, lane 1: SPI_MOSI/UART_RFR/I2C_SCL

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
M44	GPIO_33	–	QUP_L2(11) QUP_L0(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 11, lane 2: SPI_CLK/UART_TX QUP 14, lane 0: SPI_MISO/UART_CTS/I2C_SDA
L45	GPIO_32	Y	QUP_L1(11) QUP_L3(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 11, lane 1: SPI_MOSI/UART_RFR/I2C_SCL QUP 14, lane 3: SPI_CS0/UART_RX
L43	GPIO_31	Y	QUP_L0(11) QUP_L2(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 11, lane 0: SPI_MISO/UART_CTS/I2C_SDA QUP 14, lane 2: SPI_CLK/UART_TX
C15	GPIO_30	Y	QUP_L3(2) QDSS_GPIO_TRACECTL_LOCB	PX_3	B-PD:nppukp	Configurable I/O QUP 2, lane 3: SPI_CS0/UART_RX QDSS trace control B
E15	GPIO_29	–	QUP_L2(2) GP_MN QDSS_GPIO_TRACEDATA_LOCB(15)	PX_3	B-PD:nppukp	Configurable I/O QUP 2, lane 2: SPI_CLK/UART_TX General-purpose M/N:D counter output QDSS trace data 15 B
E17	GPIO_28	–	QUP_L1(2) QDSS_GPIO_TRACEDATA_LOCB(14)	PX_3	B-PD:nppukp	Configurable I/O QUP 2, lane 1: SPI_MOSI/UART_RFR/I2C_SCL QDSS trace data 14 B
D16	GPIO_27	–	QUP_L0(2) QDSS_GPIO_TRACEDATA_LOCB(13)	PX_3	B-PD:nppukp	Configurable I/O QUP 2, lane 0: SPI_MISO/UART_CTS/I2C_SDA QDSS trace data 13 B
AN3	GPIO_26	Y	CCI_ASYNC_IN0 QDSS_GPIO_TRACEDATA_LOCB(12)	PX_3	B-PD:nppukp	Configurable I/O Camera control interface async 0 QDSS trace data 12 B
AP4	GPIO_25	–	CCI_TIMER4 CCI_ASYNC_IN2 QDSS_GPIO_TRACEDATA_LOCB(11)	PX_3	B-PD:nppukp	Configurable I/O Camera control interface timer 4 Camera control interface async 2 QDSS trace data 11 B
AP2	GPIO_24	Y	CCI_TIMER3 CCI_ASYNC_IN1 QDSS_GPIO_TRACEDATA_LOCB(10)	PX_3	B-PD:nppukp	Configurable I/O Camera control interface timer 3 Camera control interface async 1 QDSS trace data 10 B
AR5	GPIO_23	–	CCI_TIMER2 QDSS_GPIO_TRACEDATA_LOCB(9)	PX_3	B-PD:nppukp	Configurable I/O Camera control interface timer 2 QDSS trace data 9 B
AR3	GPIO_22	Y	CCI_TIMER1 GCC_GP3_CLK_MIRB QDSS_GPIO_TRACECLK_LOCB	PX_3	B-PD:nppukp	Configurable I/O Camera control interface timer 1 Global general-purpose clock 3 B QDSS trace clock B
AR1	GPIO_21	–	CCI_TIMER0 GCC_GP2_CLK_MIRB QDSS_GPIO_TRACEDATA_LOCB(8)	PX_3	B-PD:nppukp	Configurable I/O Camera control interface timer 0 Global general-purpose clock 2 B QDSS trace data 8 B
AL5	GPIO_20	Y	CCI_I2C_SCL1 QUP_L3(1) QDSS_GPIO_TRACEDATA_LOCB(7)	PX_3	B-PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 clock QUP 1, lane 3: SPI_CS0/UART_RX QDSS trace data 7 B
AL7	GPIO_19	–	CCI_I2C_SDA1 QUP_L2(1) QDSS_GPIO_TRACEDATA_LOCB(6)	PX_3	B-PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 serial data QUP 1, lane 2: SPI_CLK/UART_TX QDSS trace data 6 B
AN7	GPIO_18	–	CCI_I2C_SCL0 QUP_L1(1) QDSS_GPIO_TRACEDATA_LOCB(5)	PX_3	B-PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 clock QUP 1, lane 1: SPI_MOSI/UART_RFR/I2C_SCL QDSS trace data 5 B
AM6	GPIO_17	–	CCI_I2C_SDA0 QUP_L0(1) QDSS_GPIO_TRACEDATA_LOCB(4)	PX_3	B-PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 serial data QUP 1, lane 0: SPI_MISO/UART_CTS/I2C_SDA QDSS trace data 4 B

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
AN5	GPIO_16	–	CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB(3)	PX_3	B-PD:nppukp	Configurable I/O Camera master clock 3 QDSS trace data 3 B
AP6	GPIO_15	–	CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB(2)	PX_3	B-PD:nppukp	Configurable I/O Camera master clock 2 QDSS trace data 2 B
AR7	GPIO_14	–	CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB(1)	PX_3	B-PD:nppukp	Configurable I/O Camera master clock 1 QDSS trace data 1 B
AT6	GPIO_13	–	CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB(0)	PX_3	B-PD:nppukp	Configurable I/O Camera master clock 0 QDSS trace data 0 B
AK6	GPIO_12	–	MDP_VSYNC_E TSIF1_SYNC	PX_3	B-PD:nppukp	Configurable I/O MDP vertical sync – external Transport stream interface 1 sync
B16	GPIO_11	Y	MDP_VSYNC_S_MIRA	PX_3	B-PD:nppukp	Configurable I/O MDP vertical sync – secondary A
B18	GPIO_10	Y	MDP_VSYNC_P_MIRA QUP_L6_0_CS	PX_3	B-PD:nppukp	Configurable I/O MDP vertical sync – primary A QUP 0, lane 6: SPI_CS3
E19	GPIO_9	–	QUP_L5_0_CS	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 5: SPI_CS2
D18	GPIO_8	–	QUP_L4_0_CS GP_PDM_MIRB[1]	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 4: SPI_CS1 General-purpose PDM output 1 B
N45	GPIO_7	–	QUP_L1(9)	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
M46	GPIO_6	–	QUP_L0(9)	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 0: SPI_MISO/UART_CTS/I2C_SDA
M48	GPIO_5	Y	QUP_L3(9) QDSS_CTI_TRIG0_IN_MIRB	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 3: SPI_CS0/UART_RX QDSS trigger input 0 B
L47	GPIO_4	–	QUP_L2(9) QDSS_CTI_TRIG0_OUT_MIRB	PX_3	B-PD:nppukp	Configurable I/O QUP 9, lane 2: SPI_CLK/UART_TX QDSS trigger output 0 B
E23	GPIO_3	Y	QUP_L3(0)	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 3: SPI_CS0/UART_RX
C21	GPIO_2	–	QUP_L2(0)	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 2: SPI_CLK/UART_TX
D22	GPIO_1	Y	QUP_L1(0)	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 1: SPI_MOSI/UART_RFR/I2C_SCL
E21	GPIO_0	–	QUP_L0(0)	PX_3	B-PD:nppukp	Configurable I/O QUP 0, lane 0: SPI_MISO/UART_CTS/I2C_SDA
Snapdragon sensor core I/O pins						
BE21	SSC_0	Y	QUP_IO_L0_0	PX_3	B-PD:nppukp	QUP 0 lane 0: I2C1_SDA
BD20	SSC_1	–	QUP_IO_L1_0	PX_3	B-PD:nppukp	QUP 0 lane 1: I2C1_SCL
BC15	SSC_2	Y	QUP_IO_L0_1	PX_3	B-PD:nppukp	QUP 1 lane 0: SPI1_MISO/I2C2_SDA
BE15	SSC_3	–	QUP_IO_L1_1	PX_3	B-PD:nppukp	QUP 1 lane 1: SPI1_MOSI/I2C2_SCL
BD16	SSC_4	–	QUP_IO_L2_1	PX_3	B-PD:nppukp	QUP 1 lane 2: SPI1_CLK
BC19	SSC_5	–	QUP_IO_L3_1	PX_3	B-PD:nppukp	QUP 1 lane 3: SPI1_CS0

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
				Voltage	Type	
BC21	SSC_6	–	QUP_IO_L4_1 QUP_IO_L4_2 QUP_IO_L2_0	PX_3	B-PD:nppukp	QUP 1 lane 4: SPI1_CS1 QUP 2 lane 4: SPI2_CS1 QUP 0 lane 2: UART4_TX
BD14	SSC_7	–	QUP_IO_L5_1 QUP_IO_L5_2 QUP_IO_L3_0	PX_3	B-PD:nppukp	QUP 1 lane 5: SPI1_CS2 QUP 2 lane 5: SPI2_CS2 QUP 0 lane 3: UART4_RX
BD18	SSC_8	–	QUP_IO_L0_2	PX_3	B-PD:nppukp	QUP 2 lane 0: SPI2_MISO
BC23	SSC_9	–	QUP_IO_L1_2	PX_3	B-PD:nppukp	QUP 2 lane 1: SPI2_MOSI
BD24	SSC_10	–	QUP_IO_L2_2	PX_3	B-PD:nppukp	QUP 2 lane 2: SPI2_CLK
BD22	SSC_11	–	QUP_IO_L3_2	PX_3	B-PD:nppukp	QUP 2 lane 3: SPI2_CS0
BE17	SSC_12	–	QUP_IO_L2_3	PX_3	B-PD:nppukp	QUP 3 lane 2: UART1_TX (If QUP3 is used as I2C_SDA on SSC_16, then the UART function is not available)
BE19	SSC_13	Y	QUP_IO_L3_3	PX_3	B-PD:nppukp	QUP 3 lane 3: UART1_RX (If QUP3 is used as I2C_SCL on SSC_17, then the UART function is not available)
BE25	SSC_14	–	QUP_IO_L2_4 QUP_IO_L0_5	PX_3	B-PD:nppukp	QUP 4 lane 2: UART2_TX QUP 5 lane 0: SPI3_MISO
BE23	SSC_15	Y	QUP_IO_L3_4 QUP_IO_L1_5	PX_3	B-PD:nppukp	QUP 4 lane 3: UART2_RX QUP 5 lane 1: SPI3_MOSI
BC25	SSC_16	–	QUP_IO_L2_5 QUP_IO_L0_4 QUP_IO_L0_3	PX_3	B-PD:nppukp	QUP 5 lane 2: SPI3_CLK/UART3_TX QUP 4 lane 0: UART2_CTS QUP 3 lane 0: I2C3_SDA (If QUP3 is used as UART_TX on SSC_12, then the I^2C function is not available)
BE29	SSC_17	Y	QUP_IO_L3_5 QUP_IO_L1_4 QUP_IO_L1_3	PX_3	B-PD:nppukp	QUP 5 lane 3: SPI3_CS0/UART3_RX QUP 4 lane 1: UART2_RFR QUP 3 lane 1: I2C3_SCL (If QUP3 is used as UART_TX on SSC_13, then the I^2C function is not available)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #	Pad name	Functional description
A35, J27, K20, K26, L41, AA43, AB4, AC1, AD48, AE47, AF40, AG45, AH46, AJ9, AJ47, AT46, AU17, AV30, AY10, AY12, AY38, BA39, BB24, BB26, BB28, BB30, BF38	DNC	Do not connect; connected internally, do not connect externally
A1, A3, A5, A7, A9, A15, A21, A27, A33, A39, A41, A47, B2, B4, B6, B34, B36, B38, B40, B42, B48, C1, C3, C7, C29, C33, C37, C39, D8, D32, D36, D38, E7, E9, E29, E31, F10, F12, F16, F18, F20, F22, F24, F26, F30, F36, F40, G9, G11, G13, G21, G23, G37, H12, H14, H26, H28, H32, H34, H36, J11, J13, J15, J17, J19, J21, J23, J25, J41, K4, K6, K10, K12, K14, K16, K18, K22, K30, K32, K34, K36, K38, L1, L3, L5, L7, L13, L15, L27, M4, M8, M26, M34, M42, N13, N15, N21, N23, N27, P4, P26, P42, P48, R5, R7, R13, R15, R21, R23, R27, R41, R45, T4, T26, T44, U9, U11, U13, U15, U21, U23, U27, U35, V4, V6, V26, V40, V48, W7, W11, W13, W21, W23, W25, W27, W29, W31, W33, W35, W37, W39, W41, Y26, Y30, Y32, Y34, Y36, Y38, Y42, Y48, AA5, AA11, AA41, AB40, AB42, AC41, AC43, AD40, AD42, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25, AE27, AE29, AE31, AE33, AE35, AE37, AE39, AE43, AF42, AG1, AG9, AG11, AG13, AG15, AG17, AG19, AH40, AH42, AJ11, AJ13, AJ15, AJ17, AJ19, AJ23, AJ25, AJ27, AJ29, AJ35, AK40, AK46, AK48, AL9, AL13, AL19, AL21, AL23, AL25, AL27, AL29, AL33, AL35, AL37, AL39, AM16, AM26, AM40, AN1, AN33, AP16, AP26, AP40, AR33, AR35, AR37, AT8, AT16, AT26, AT40, AT48, AU7, AU33, AV20, AV24, AV26, AV28, AV32, AV34, AV36, AV38, AW1, AW9, AW11, AW15, AW17, AW21, AW23, AW25, AW33, AW35, AW37, AY8, AY22, AY28, AY36, AY44, BA23, BA25, BA37, BB12, BB14, BB18, BB22, BB34, BB36, BB38, BB40, BB44, BC37, BC45, BD12, BD32, BD38, BD40, BD42, BD46, BD48, BE1, BE37, BE41, BE43, BE45, BE47, BF2, BF10, BF16, BF22, BF28, BF34, BF40, BF42, BF44, BF46, BF48	GND	Ground
AH10, AH12, AH14, AH16, AK10, AK12, AK14, AL11, AL15, AL17	VDD_APC0	Power for Kryo Silver application processor
AN17, AN25, AP8, AR17, AR25, AU9, AU11, AU13, AU15, AU19, AU21, AU23, AU25, AV8, AV10, AV12, AV14, AV16, AV18, AV22	VDD_APC1	Power for Kryo Gold application processor
J29, J31, J33, J35, J37, J39, K28, K40, L35, M28, N35, N41, P28, P34, R35, T28, T34, U41, Y40	VDD_GFX	Power for graphics
AN35, AN37, AN39, AR39, AU35, AU37, AU39	VDD_MODEM	Power for modem circuits
AY26	VDD_QFPROM	Power for programming the QFPROM;
AW27	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor
AB44	VDD_QUSB_HS0	Power for USB HS0 core circuits
AN29, AR29, AU29	VDD_SSC_CX	Power for Snapdragon sensor core
AN27, AR27, AU27	VDD_SSC_MX	Power for Snapdragon sensor core
L11, N11	VDD_WCSS_CX	Power for WCSS circuits
L9, N9	VDD_WCSS_MX	Power for WCSS circuits
D10, D40, E11, E39, BC39, BD10, BE11, BE39	VDD1	Power for PoP DDR memory core – 1.8 V (top VDD2)
A11, A17, A19, A29, A31, A37, BF14, BF18, BF20, BF30, BF32, BF36	VDD2	Power for PoP DDR memory core – 1.2 V (top VDD2)
AJ21	VDDA_APC_PLL	Power for application processor PLL circuits
AM8	VDDA_APC1_CS_1P8	Power for APC1 1.8 V circuits
G31	VDDA_CC_EBI01	Power for EBI0/EBI1 clock circuits
AY18	VDDA_CC_EBI23	Power for EBI2/EBI3 clock circuits
H18, H20	VDDA_EBI0	Power for EBI0 PHY circuits
G33, G35	VDDA_EBI1	Power for EBI1 PHY circuits

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AY14, AY16	VDDA_EBI2	Power for EBI2 PHY circuits
AY30, AY32	VDDA_EBI3	Power for EBI3 PHY circuits
G39	VDDA_GFX_CS_1P8	Power for graphics 1.8 V circuits
AG41	VDDA_HP_PCIE_1P2	Power for PCIE Gen 3, 1.2 V circuits
AG43	VDDA_HP_PCIE_CORE	Power for PCIE Gen 3 core circuits
H10	VDDA_HV_EBI0	Power for EBI0 PHY high-voltage circuits
F38	VDDA_HV_EBI1	Power for EBI1 PHY high-voltage circuits
BA9	VDDA_HV_EBI2	Power for EBI2 PHY high-voltage circuits
AW39	VDDA_HV_EBI3	Power for EBI3 PHY high-voltage circuits
Y28	VDDA_LPA_PLL	Power for audio circuits
AW7	VDDA_MIPI_CSI_1P25	Power for MIPI CSI 1.25 V circuits
AV6	VDDA_MIPI_CSI0_0P9	Power for MIPI CSI0 0.9 V circuits
AY6	VDDA_MIPI_CSI1_0P9	Power for MIPI CSI1 0.9 V circuits
BA7	VDDA_MIPI_CSI2_0P9	Power for MIPI CSI2 0.9 V circuits
J9	VDDA_MIPI_DSI0_0P9	Power for MIPI DSI0 0.9 V circuits
J7	VDDA_MIPI_DSI0_1P2	Power for MIPI DSI0 1.2 V circuits
K8	VDDA_MIPI_DSI0_PLL	Power for MIPI DSI0 PLL circuits
H8	VDDA_MIPI_DSI1_0P9	Power for MIPI DSI1 0.9 V circuits
G7	VDDA_MIPI_DSI1_1P2	Power for MIPI DSI1 1.2 V circuits
F8	VDDA_MIPI_DSI1_PLL	Power for MIPI DSI1 PLL circuits
V8	VDDA_PCIE_1P2	Power for PCIe 1.2 V I/O circuitry
W9	VDDA_PCIE_CORE	Power for PCIe core circuitry
G41	VDDA_PLL_CC_EBI01	Power for EBI0/EBI1 PLL circuits
BA11	VDDA_PLL_CC_EBI23	Power for EBI2/EBI3 PLL circuits
AW45	VDDA_QLINK_LV	Power for QLink circuits
AV46	VDDA_QLINK_LV_CK	Power for QLink clock circuits
K42	VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits
AY24	VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits
BA21	VDDA_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits
AA45	VDDA_QUSB_HS0_1P8	Power for USB HS0 circuits 1.8 V
Y44	VDDA_QUSB_HS0_3P1	Power for USB HS0 circuits 3.075 V
AW29	VDDA_SP_SENSOR	Power for secure processing unit sensors
Y8	VDDA_UFS1_1P2	Power for UFS 1.2 V circuits
AC9	VDDA_UFS1_CORE	Power for UFS core circuits
AB8	VDDA_UFS2_1P2	Power for UFS 1.2 V circuits
AA9	VDDA_UFS2_CORE	Power for UFS core circuits
AE41	VDDA_USB1_SS_1P2	Power for USB SS 1.2 V circuits
AD44	VDDA_USB1_SS_CORE	Power for USB SS core circuits
V42	VDDA_USB2_SS_1P2	Power for USB SS 1.2 V circuits
W43	VDDA_USB2_SS_CORE	Power for USB SS core circuits
P8	VDDA_WCSS_ADCDAC_1	Power for WCSS ADC and DAC

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad #	Pad name	Functional description
R9	VDDA_WCSS_ADCDAC_2	Power for WCSS ADC and DAC
R11	VDDA_WCSS_PLL	Power for WCSS PLL circuits
K24, N19, R19, U19, W19, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA35, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC27, AC29, AC31, AC33, AC35, AG21, AG23, AG25, AG27, AG29, AG31, AG33, AG35, AJ31, AJ33, AL31, AN31, AR31, AU31	VDDCX	Power for digital core circuits
F14	VDDIO_CK_EBI0	Power for EBI0 I/O clock circuits
E37	VDDIO_CK_EBI1	Power for EBI1 I/O clock circuits
BA13	VDDIO_CK_EBI2	Power for EBI2 I/O clock circuits
BA35	VDDIO_CK_EBI3	Power for EBI3 I/O clock circuits
G15, G17, G19, H16	VDDIO_EBI0	Power for EBI0 I/O memory circuits
E33, E35, F32, F34	VDDIO_EBI1	Power for EBI1 I/O memory circuits
BA15, BA17, BA19, BB16	VDDIO_EBI2	Power for EBI2 I/O memory circuits
AY34, BA29, BA31, BA33	VDDIO_EBI3	Power for EBI3 I/O memory circuits
H30, H38, L17, L19, L21, L23, L25, N17, N25, R17, R25, U17, U25, V28, V30, V32, V34, V36, V38, W15, W17, AA13, AA37, AA39, AC11, AC37, AC39, AG37, AG39, AJ37, AJ39, AK16, AK18, AK20, AK22, AK24, AK26, AW13, AW19	VDDMX	Power for on-chip memory
AA7	VDDPX_10	Power for pad group 10 – UFS pad
U43	VDDPX_11	Power for pad group 11 – CXO pad
AW31	VDDPX_13	Power for pad group 13
AH8	VDDPX_2	Power for pad group 2 – SDC2 pads
H22, H24, H40, H42, AK8, AN41, AY40, BA27	VDDPX_3	Power for pad group 3 – most I/O pads
AL41	VDDPX_5	Power for pad group 5 – UIM1 pads
AJ41	VDDPX_6	Power for pad group 6 – UIM2 pads
AF8	VDDPX_VBIAS_SDC	Reference voltage for SDC
AH44	VDDPX_VBIAS_UIM	Reference voltage for UIM
C35, D14, D34, E13, BC13, BC35, BE13, BE35	VDDQ	Power for PoP DDR pads (top VDDQ)

2.3 Pin assignments – top

2.3.1 Pin map – top

The SDM845 is available in the 914B MPSP; its top surface is similar to a 556 NSP. See Chapter 4 for package details and Section 2.2 for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3.

The text within Figure 2-3 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available and defined in Section 2.2.1.

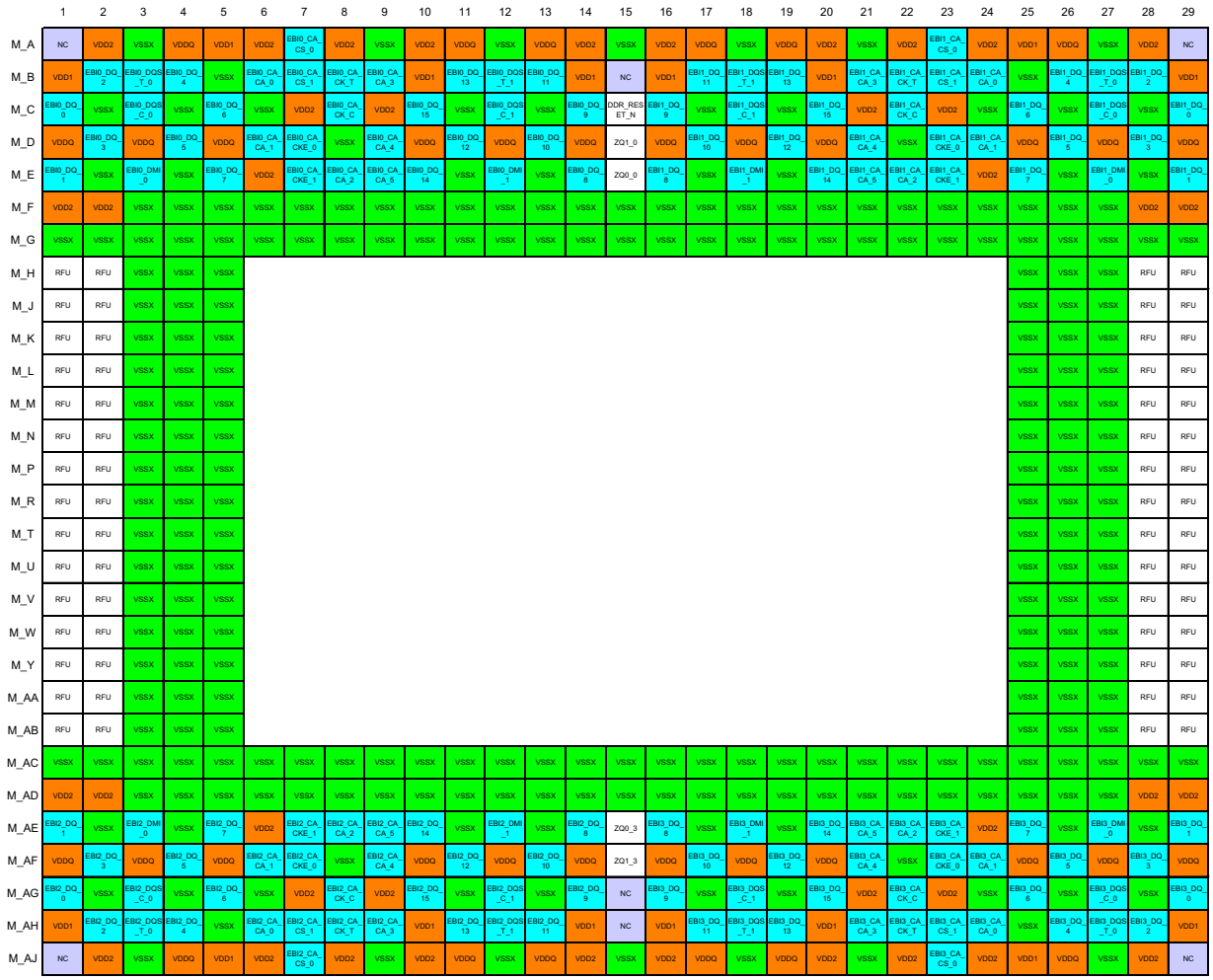


Figure 2-3 SDM845 top pin assignments

2.3.2 Pin descriptions – top

Descriptions of SDM845 top pins are presented in Table 2-5.

Table 2-5 Top pin descriptions – general pins

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
M_C15	DDR_RESET_N		EBI	DO	LPDDR4x reset (shared by EBIs)
M_B6	EBI0_CA_0		EBI	DO	EBI0 LPDDR4x command/address 0 bit 0
M_D6	EBI0_CA_1		EBI	DO	EBI0 LPDDR4x command/address 0 bit 1
M_E8	EBI0_CA_2		EBI	DO	EBI0 LPDDR4x command/address 0 bit 2
M_B9	EBI0_CA_3		EBI	DO	EBI0 LPDDR4x command/address 0 bit 3
M_D9	EBI0_CA_4		EBI	DO	EBI0 LPDDR4x command/address 0 bit 4
M_E9	EBI0_CA_5		EBI	DO	EBI0 LPDDR4x command/address 0 bit 5
M_C8	EBI0_CK_C		EBI	DO	EBI0 CA0 LPDDR4x differential clock (C)
M_B8	EBI0_CK_T		EBI	DO	EBI0 CA0 LPDDR4x differential clock (T)
M_D7	EBI0_CKE_0		EBI	DO	EBI0 CA0 LPDDR4x clock enable 0
M_E7	EBI0_CKE_1		EBI	DO	EBI0 CA0 LPDDR4x clock enable 1
M_A7	EBI0_CS_0		EBI	DO	EBI0 CA0 LPDDR4x chip select 0
M_B7	EBI0_CS_1		EBI	DO	EBI0 CA0 LPDDR4x chip select 1
M_E3	EBI0_DMI_0		EBI	DO	EBI0 LPDDR4x data mask for byte 0
M_E12	EBI0_DMI_1		EBI	DO	EBI0 LPDDR4x data mask for byte 1
M_C1	EBI0_DQ_0		EBI	B	EBI0 LPDDR4x data bit 0
M_E1	EBI0_DQ_1		EBI	B	EBI0 LPDDR4x data bit 1
M_D13	EBI0_DQ_10		EBI	B	EBI0 LPDDR4x data bit 10
M_B13	EBI0_DQ_11		EBI	B	EBI0 LPDDR4x data bit 11
M_D11	EBI0_DQ_12		EBI	B	EBI0 LPDDR4x data bit 12
M_B11	EBI0_DQ_13		EBI	B	EBI0 LPDDR4x data bit 13
M_E10	EBI0_DQ_14		EBI	B	EBI0 LPDDR4x data bit 14
M_C10	EBI0_DQ_15		EBI	B	EBI0 LPDDR4x data bit 15
M_B2	EBI0_DQ_2		EBI	B	EBI0 LPDDR4x data bit 2
M_D2	EBI0_DQ_3		EBI	B	EBI0 LPDDR4x data bit 3
M_B4	EBI0_DQ_4		EBI	B	EBI0 LPDDR4x data bit 4
M_D4	EBI0_DQ_5		EBI	B	EBI0 LPDDR4x data bit 5
M_C5	EBI0_DQ_6		EBI	B	EBI0 LPDDR4x data bit 6
M_E5	EBI0_DQ_7		EBI	B	EBI0 LPDDR4x data bit 7
M_E14	EBI0_DQ_8		EBI	B	EBI0 LPDDR4x data bit 8
M_C14	EBI0_DQ_9		EBI	B	EBI0 LPDDR4x data bit 9
M_C3	EBI0_DQS_C_0		EBI	B	EBI0 LPDDR4x differential data strobe for byte 0 (C)
M_C12	EBI0_DQS_C_1		EBI	B	EBI0 LPDDR4x differential data strobe for byte 1 (C)
M_B3	EBI0_DQS_T_0		EBI	B	EBI0 LPDDR4x differential data strobe for byte 0 (T)
M_B12	EBI0_DQS_T_1		EBI	B	EBI0 LPDDR4x differential data strobe for byte 1 (T)
M_B24	EBI1_CA_0		EBI	DO	EBI1 LPDDR4x command/address 0 bit 0

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
M_D24	EBI1_CA_1		EBI	DO	EBI1 LPDDR4x command/address 0 bit 1
M_E22	EBI1_CA_2		EBI	DO	EBI1 LPDDR4x command/address 0 bit 2
M_B21	EBI1_CA_3		EBI	DO	EBI1 LPDDR4x command/address 0 bit 3
M_D21	EBI1_CA_4		EBI	DO	EBI1 LPDDR4x command/address 0 bit 4
M_E21	EBI1_CA_5		EBI	DO	EBI1 LPDDR4x command/address 0 bit 5
M_C22	EBI1_CK_C		EBI	DO	EBI1 CA0 LPDDR4x differential clock (C)
M_B22	EBI1_CK_T		EBI	DO	EBI1 CA0 LPDDR4x differential clock (T)
M_D23	EBI1_CKE_0		EBI	DO	EBI1 CA0 LPDDR4x clock enable 0
M_E23	EBI1_CKE_1		EBI	DO	EBI1 CA0 LPDDR4x clock enable 1
M_A23	EBI1_CS_0		EBI	DO	EBI1 CA0 LPDDR4x chip select 0
M_B23	EBI1_CS_1		EBI	DO	EBI1 CA0 LPDDR4x chip select 1
M_E27	EBI1_DMI_0		EBI	DO	EBI1 LPDDR4x data mask for byte 0
M_E18	EBI1_DMI_1		EBI	DO	EBI1 LPDDR4x data mask for byte 1
M_C29	EBI1_DQ_0		EBI	B	EBI1 LPDDR4x data bit 0
M_E29	EBI1_DQ_1		EBI	B	EBI1 LPDDR4x data bit 1
M_D17	EBI1_DQ_10		EBI	B	EBI1 LPDDR4x data bit 10
M_B17	EBI1_DQ_11		EBI	B	EBI1 LPDDR4x data bit 11
M_D19	EBI1_DQ_12		EBI	B	EBI1 LPDDR4x data bit 12
M_B19	EBI1_DQ_13		EBI	B	EBI1 LPDDR4x data bit 13
M_E20	EBI1_DQ_14		EBI	B	EBI1 LPDDR4x data bit 14
M_C20	EBI1_DQ_15		EBI	B	EBI1 LPDDR4x data bit 15
M_B28	EBI1_DQ_2		EBI	B	EBI1 LPDDR4x data bit 2
M_D28	EBI1_DQ_3		EBI	B	EBI1 LPDDR4x data bit 3
M_B26	EBI1_DQ_4		EBI	B	EBI1 LPDDR4x data bit 4
M_D26	EBI1_DQ_5		EBI	B	EBI1 LPDDR4x data bit 5
M_C25	EBI1_DQ_6		EBI	B	EBI1 LPDDR4x data bit 6
M_E25	EBI1_DQ_7		EBI	B	EBI1 LPDDR4x data bit 7
M_E16	EBI1_DQ_8		EBI	B	EBI1 LPDDR4x data bit 8
M_C16	EBI1_DQ_9		EBI	B	EBI1 LPDDR4x data bit 9
M_C27	EBI1_DQS_C_0		EBI	B	EBI1 LPDDR4x differential data strobe for byte 0 (C)
M_C18	EBI1_DQS_C_1		EBI	B	EBI1 LPDDR4x differential data strobe for byte 1 (C)
M_B27	EBI1_DQS_T_0		EBI	B	EBI1 LPDDR4x differential data strobe for byte 0 (T)
M_B18	EBI1_DQS_T_1		EBI	B	EBI1 LPDDR4x differential data strobe for byte 1 (T)
M_AH6	EBI2_CA_0		EBI	DO	EBI2 LPDDR4x command/address 0 bit 0
M_AF6	EBI2_CA_1		EBI	DO	EBI2 LPDDR4x command/address 0 bit 1
M_AE8	EBI2_CA_2		EBI	DO	EBI2 LPDDR4x command/address 0 bit 2
M_AH9	EBI2_CA_3		EBI	DO	EBI2 LPDDR4x command/address 0 bit 3
M_AF9	EBI2_CA_4		EBI	DO	EBI2 LPDDR4x command/address 0 bit 4
M_AE9	EBI2_CA_5		EBI	DO	EBI2 LPDDR4x command/address 0 bit 5
M_AG8	EBI2_CK_C		EBI	DO	EBI2 CA0 LPDDR4x differential clock (C)

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
M_AH8	EBI2_CK_T		EBI	DO	EBI2 CA0 LPDDR4x differential clock (T)
M_AF7	EBI2_CKE_0		EBI	DO	EBI2 CA0 LPDDR4x clock enable 0
M_AE7	EBI2_CKE_1		EBI	DO	EBI2 CA0 LPDDR4x clock enable 1
M_AJ7	EBI2_CS_0		EBI	DO	EBI2 CA0 LPDDR4x chip select 0
M_AH7	EBI2_CS_1		EBI	DO	EBI2 CA0 LPDDR4x chip select 1
M_AE3	EBI2_DMI_0		EBI	DO	EBI2 LPDDR4x data mask for byte 0
M_AE12	EBI2_DMI_1		EBI	DO	EBI2 LPDDR4x data mask for byte 1
M_AG1	EBI2_DQ_0		EBI	B	EBI2 LPDDR4x data bit 0
M_AE1	EBI2_DQ_1		EBI	B	EBI2 LPDDR4x data bit 1
M_AF13	EBI2_DQ_10		EBI	B	EBI2 LPDDR4x data bit 10
M_AH13	EBI2_DQ_11		EBI	B	EBI2 LPDDR4x data bit 11
M_AF11	EBI2_DQ_12		EBI	B	EBI2 LPDDR4x data bit 12
M_AH11	EBI2_DQ_13		EBI	B	EBI2 LPDDR4x data bit 13
M_AE10	EBI2_DQ_14		EBI	B	EBI2 LPDDR4x data bit 14
M_AG10	EBI2_DQ_15		EBI	B	EBI2 LPDDR4x data bit 15
M_AH2	EBI2_DQ_2		EBI	B	EBI2 LPDDR4x data bit 2
M_AF2	EBI2_DQ_3		EBI	B	EBI2 LPDDR4x data bit 3
M_AH4	EBI2_DQ_4		EBI	B	EBI2 LPDDR4x data bit 4
M_AF4	EBI2_DQ_5		EBI	B	EBI2 LPDDR4x data bit 5
M_AG5	EBI2_DQ_6		EBI	B	EBI2 LPDDR4x data bit 6
M_AE5	EBI2_DQ_7		EBI	B	EBI2 LPDDR4x data bit 7
M_AE14	EBI2_DQ_8		EBI	B	EBI2 LPDDR4x data bit 8
M_AG14	EBI2_DQ_9		EBI	B	EBI2 LPDDR4x data bit 9
M_AG3	EBI2_DQS_C_0		EBI	B	EBI2 LPDDR4x differential data strobe for byte 0 (C)
M_AG12	EBI2_DQS_C_1		EBI	B	EBI2 LPDDR4x differential data strobe for byte 1 (C)
M_AH3	EBI2_DQS_T_0		EBI	B	EBI2 LPDDR4x differential data strobe for byte 0 (T)
M_AH12	EBI2_DQS_T_1		EBI	B	EBI2 LPDDR4x differential data strobe for byte 1 (T)
M_AH24	EBI3_CA_0		EBI	DO	EBI3 LPDDR4x command/address 0 bit 0
M_AF24	EBI3_CA_1		EBI	DO	EBI3 LPDDR4x command/address 0 bit 1
M_AE22	EBI3_CA_2		EBI	DO	EBI3 LPDDR4x command/address 0 bit 2
M_AH21	EBI3_CA_3		EBI	DO	EBI3 LPDDR4x command/address 0 bit 3
M_AF21	EBI3_CA_4		EBI	DO	EBI3 LPDDR4x command/address 0 bit 4
M_AE21	EBI3_CA_5		EBI	DO	EBI3 LPDDR4x command/address 0 bit 5
M_AG22	EBI3_CK_C		EBI	DO	EBI3 CA0 LPDDR4x differential clock (C)
M_AH22	EBI3_CK_T		EBI	DO	EBI3 CA0 LPDDR4x differential clock (T)
M_AF23	EBI3_CKE_0		EBI	DO	EBI3 CA0 LPDDR4x clock enable 0
M_AE23	EBI3_CKE_1		EBI	DO	EBI3 CA0 LPDDR4x clock enable 1
M_AJ23	EBI3_CS_0		EBI	DO	EBI3 CA0 LPDDR4x chip select 0
M_AH23	EBI3_CS_1		EBI	DO	EBI3 CA0 LPDDR4x chip select 1
M_AE27	EBI3_DMI_0		EBI	DO	EBI3 LPDDR4x data mask for byte 0

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
M_AE18	EBI3_DMI_1		EBI	DO	EBI3 LPDDR4x data mask for byte 1
M_AG29	EBI3_DQ_0		EBI	B	EBI3 LPDDR4x data bit 0
M_AE29	EBI3_DQ_1		EBI	B	EBI3 LPDDR4x data bit 1
M_AF17	EBI3_DQ_10		EBI	B	EBI3 LPDDR4x data bit 10
M_AH17	EBI3_DQ_11		EBI	B	EBI3 LPDDR4x data bit 11
M_AF19	EBI3_DQ_12		EBI	B	EBI3 LPDDR4x data bit 12
M_AH19	EBI3_DQ_13		EBI	B	EBI3 LPDDR4x data bit 13
M_AE20	EBI3_DQ_14		EBI	B	EBI3 LPDDR4x data bit 14
M_AG20	EBI3_DQ_15		EBI	B	EBI3 LPDDR4x data bit 15
M_AH28	EBI3_DQ_2		EBI	B	EBI3 LPDDR4x data bit 2
M_AF28	EBI3_DQ_3		EBI	B	EBI3 LPDDR4x data bit 3
M_AH26	EBI3_DQ_4		EBI	B	EBI3 LPDDR4x data bit 4
M_AF26	EBI3_DQ_5		EBI	B	EBI3 LPDDR4x data bit 5
M_AG25	EBI3_DQ_6		EBI	B	EBI3 LPDDR4x data bit 6
M_AE25	EBI3_DQ_7		EBI	B	EBI3 LPDDR4x data bit 7
M_AE16	EBI3_DQ_8		EBI	B	EBI3 LPDDR4x data bit 8
M_AG16	EBI3_DQ_9		EBI	B	EBI3 LPDDR4x data bit 9
M_AG27	EBI3_DQS_C_0		EBI	B	EBI3 LPDDR4x differential data strobe for byte 0 (C)
M_AG18	EBI3_DQS_C_1		EBI	B	EBI3 LPDDR4x differential data strobe for byte 1 (C)
M_AH27	EBI3_DQS_T_0		EBI	B	EBI3 LPDDR4x differential data strobe for byte 0 (T)
M_AH18	EBI3_DQS_T_1		EBI	B	EBI3 LPDDR4x differential data strobe for byte 1 (T)
M_E15	ZQ0_0		–	AI	LPDDR4x ZQ resistor for lower x16 memory in rank 0 (shared by EBIs)
M_AE15	ZQ0_3		–	AI	LPDDR4x ZQ resistor for lower x16 memory in rank 1 (shared by EBIs)
M_D15	ZQ1_0		–	AI	LPDDR4x ZQ resistor for upper x16 memory in rank 0 (shared by EBIs)
M_AF15	ZQ1_3		–	AI	LPDDR4x ZQ resistor for upper x16 memory in rank 1 (shared by EBIs)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Top pin descriptions – ground, NC, reserved, and power supply pins

Pad #	Pad name	Functional description
M_A3, M_A9, M_A12, M_A15, M_A18, M_A21, M_A27, M_B5, M_B25, M_C2, M_C4, M_C6, M_C11, M_C13, M_C17, M_C19, M_C24, M_C26, M_C28, M_D8, M_D22, M_E2, M_E4, M_E11, M_E13, M_E17, M_E19, M_E26, M_E28, M_F3, M_F4, M_F5, M_F6, M_F7, M_F8, M_F9, M_F10, M_F11, M_F12, M_F13, M_F14, M_F15, M_F16, M_F17, M_F18, M_F19, M_F20, M_F21, M_F22, M_F23, M_F24, M_F25, M_F26, M_F27, M_G1, M_G2, M_G3, M_G4, M_G5, M_G6, M_G7, M_G8, M_G9, M_G10, M_G11, M_G12, M_G13, M_G14, M_G15, M_G16, M_G17, M_G18, M_G19, M_G20, M_G21, M_G22, M_G23, M_G24, M_G25, M_G26, M_G27, M_G28, M_G29, M_H3, M_H4, M_H5, M_H25, M_H26, M_H27, M_J3, M_J4, M_J5, M_J25, M_J26, M_J27, M_K3, M_K4, M_K5, M_K25, M_K26, M_K27, M_L3, M_L4, M_L5, M_L25, M_L26, M_L27, M_M3, M_M4, M_M5, M_M25, M_M26, M_M27, M_N3, M_N4, M_N5, M_N25, M_N26, M_N27, M_P3, M_P4, M_P5, M_P25, M_P26, M_P27, M_R3, M_R4, M_R5, M_R25, M_R26, M_R27, M_T3, M_T4, M_T5, M_T25, M_T26, M_T27, M_U3, M_U4, M_U5, M_U25, M_U26, M_U27, M_V3, M_V4, M_V5, M_V25, M_V26, M_V27, M_W3, M_W4, M_W5, M_W25, M_W26, M_W27, M_Y3, M_Y4, M_Y5, M_Y25, M_Y26, M_Y27, M_AA3, M_AA4, M_AA5, M_AA25, M_AA26, M_AA27, M_AB3, M_AB4, M_AB5, M_AB25, M_AB26, M_AB27, M_AC1, M_AC2, M_AC3, M_AC4, M_AC5, M_AC6, M_AC7, M_AC8, M_AC9, M_AC10, M_AC11, M_AC12, M_AC13, M_AC14, M_AC15, M_AC16, M_AC17, M_AC18, M_AC19, M_AC20, M_AC21, M_AC22, M_AC23, M_AC24, M_AC25, M_AC26, M_AC27, M_AC28, M_AC29, M_AD3, M_AD4, M_AD5, M_AD6, M_AD7, M_AD8, M_AD9, M_AD10, M_AD11, M_AD12, M_AD13, M_AD14, M_AD15, M_AD16, M_AD17, M_AD18, M_AD19, M_AD20, M_AD21, M_AD22, M_AD23, M_AD24, M_AD25, M_AD26, M_AD27, M_AE2, M_AE4, M_AE11, M_AE13, M_AE17, M_AE19, M_AE26, M_AE28, M_AF8, M_AF22, M_AG2, M_AG4, M_AG6, M_AG11, M_AG13, M_AG17, M_AG19, M_AG24, M_AG26, M_AG28, M_AH5, M_AH25, M_AJ3, M_AJ9, M_AJ12, M_AJ15, M_AJ18, M_AJ21, M_AJ27	VSSX	Ground
M_A1, M_A29, M_AJ1, M_AJ29, M_B15, M_AG15, M_AH15	NC	No connect; not connected internally.
M_H1, M_H2, M_H28, M_H29, M_J1, M_J2, M_J28, M_J29, M_K1, M_K2, M_K28, M_K29, M_L1, M_L2, M_L28, M_L29, M_M1, M_M2, M_M28, M_M29, M_N1, M_N2, M_N28, M_N29, M_P1, M_P2, M_P28, M_P29, M_R1, M_R2, M_R28, M_R29, M_T1, M_T2, M_T28, M_T29, M_U1, M_U2, M_U28, M_U29, M_V1, M_V2, M_V28, M_V29, M_W1, M_W2, M_W28, M_W29, M_Y1, M_Y2, M_Y28, M_Y29, M_AA1, M_AA2, M_AA28, M_AA29, M_AB1, M_AB2, M_AB28, M_AB29	RFU	Reserved
M_A5, M_A25, M_B1, M_B10, M_B14, M_B16, M_B20, M_B29, M_AH1, M_AH10, M_AH14, M_AH16, M_AH20, M_AH29, M_AJ5, M_AJ25	VDD1	Power for memory core (bottom VDD1)
M_A2, M_A6, M_A8, M_A10, M_A14, M_A16, M_A20, M_A22, M_A24, M_A28, M_C7, M_C9, M_C21, M_C23, M_E6, M_E24, M_F1, M_F2, M_F28, M_F29, M_AD1, M_AD2, M_AD28, M_AD29, M_AE6, M_AE24, M_AG7, M_AG9, M_AG21, M_AG23, M_AJ2, M_AJ6, M_AJ8, M_AJ10, M_AJ14, M_AJ16, M_AJ20, M_AJ22, M_AJ24, M_AJ28	VDD2	Power for memory core (bottom VDD2)
M_A4, M_A11, M_A13, M_A17, M_A19, M_A26, M_D1, M_D3, M_D5, M_D10, M_D12, M_D14, M_D16, M_D18, M_D20, M_D25, M_D27, M_D29, M_AF1, M_AF3, M_AF5, M_AF10, M_AF12, M_AF14, M_AF16, M_AF18, M_AF20, M_AF25, M_AF27, M_AF29, M_AJ4, M_AJ11, M_AJ13, M_AJ17, M_AJ19, M_AJ26	VDDQ	Power for memory I/O (bottom VDDQ)

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_APC0	Power for Kryo Silver application processor	-0.3	1.19	V
VDD_APC1	Power for Kryo Gold application processor	-0.3	1.33	V
VDD_SSC_CX	Power for Snapdragon sensor core	-0.3	1.19	V
VDD_SSC_MX	Power for Snapdragon sensor core	-0.3	1.19	V
VDD_MODEM	Power for modem circuits	-0.3	1.19	V
VDD_GFX	Power for graphics	-0.3	1.19	V
VDDCX	Power for digital core circuits	-0.3	1.19	V
VDDMX VDDA_MIPI_DSI0_0P9 VDDA_MIPI_DSI1_0P9 VDDA_LPA_PLL VDDA_APC_PLL	Power for memory circuits and analog PLL circuits	-0.3	1.19	V
VDDA_EBI0 VDDA_EBI1 VDDA_CC_EBI01 VDDA_CC_EBI23	Power for EBI PHY circuits	-0.3	1.19	V
VDDA_WCSS_CX VDDA_WCSS_MX VDDA_WCSS_PLL	Power for WCSS core circuits	-0.3	0.95	V
VDDA_WCSS_ADCDAC_1 VDDA_WCSS_ADCDAC_2	Power for WCSS ADC and DAC circuits	-0.3	1.5	V
VDDPX_5 VDDPX_6	Power for UIM pads	-0.3	3.33	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDDA_QREFS_1P8 VDDA_GFX_CS_1P8 VDDA_APC1_CS_1P8 VDDA_QUSB_HS0_1P8 VDDPX_11 VDD_QFPROM VDD_QFPROM_SP	Power for analog 1.8 V PHY circuits and clock circuits	-0.3	2.07	V
VDDPX_10	Power for pad group 10 – UFS pad	-0.3	1.38	V
VDDA_QUSB_HS0 VDDA_QLINK_LV VDDA_QLINK_LV_CK VDDA_QREFS_0P875 VDDA_UFS2_CORE VDDA_USB2_SS_CORE VDDA_USB1_SS_CORE VDDA_PLL_CC_EBI01 VDDA_PLL_CC_EBI23 VDDA_PCIE_CORE VDDA_UFS1_CORE VDDA_HP_PCIE_CORE VDDA_MIPI_DSI0_PLL VDDA_MIPI_DSI1_PLL VDDA_MIPI_CSI0_0P9 VDDA_MIPI_CSI1_0P9 VDDA_MIPI_CSI2_0P9 VDDA_SP_SENSOR	Power for analog 0.9 V PHY circuits	-0.3	1.01	V
VDDA_QUSB_HS0_3P1	Power for USB HS0 circuits – 3.075 V	-0.3	3.52	V
VDD2	Power for PoP DDR memory core – 1.2 V (top VDD2)	-0.3	See note [1]	V
VDDPX_3 VDD1	Power for pad group 3 – most I/O pads PoP DDR memory core – 1.8 V (top VDD1)	-0.3	2.09	V
VDDA_HV_EBI0 VDDA_HV_EBI1 VDDA_HV_EBI2 VDDA_HV_EBI3 VDDA_PCIE_1P2 VDDA_UFS1_1P2 VDDA_HP_PCIE_1P2 VDDA_UFS2_1P2 VDDA_USB2_SS_1P2 VDDA_USB1_SS_1P2 VDDA_MIPI_CSI_1P25 VDDA_MIPI_DSI0_1P2 VDDA_MIPI_DSI1_1P2	Power for analog 1.2 V circuits	-0.3	1.38	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDDPX_2	Power for pad group 2 – SDC2 pads	-0.3	3.33	V
VDDIO_EBI0 VDDIO_EBI1 VDDIO_EBI2 VDDIO_EBI3 VDDIO_CK_EBI0 VDDIO_CK_EBI1 VDDIO_CK_EBI2 VDDIO_CK_EBI3 VDDQ	Power for EBI I/O circuits	-0.3	0.72	V
VDDPX_13	Power for anti-replay island (secure processor)	-0.3	2.09	V

1. See the LPDDR4X data sheet for the VDD_DDR_CORE_1P1 absolute maximum ratings.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2 and Table 3-3). The SDM845 device meets all performance specifications listed in Section 3.5 through Section 3.11, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor			
	Turbo	0.640	1.080	V
	Nominal-L1	0.600	1.005	V
	Nominal	0.560	0.891	V
	SVS-L1	0.520	0.891	V
	SVS	0.520	0.891	V
	Low-SVS	0.520	0.891	V
VDD_APC1	Kryo Gold application processor			
	Boost	0.760	1.240	V
	Turbo-L2	0.740	1.240	V
	Turbo-L1	0.620	1.184	V
	Nominal-L1	0.600	1.005	V
	Nominal	0.560	0.891	V
	SVS-L1	0.520	0.891	V
	SVS	0.520	0.891	V
	Low-SVS	0.520	0.891	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_SSC_CX	Snapdragon sensor core			
	Turbo	0.660	1.071	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.790	V
	Low-SVS	0.485	0.728	V
VDD_SSC_MX	Snapdragon sensor core memory			
	Turbo	0.740	1.076	V
	Nominal	0.740	1.001	V
	SVS-L1 [2]	0.740	0.860	V
VDD_MODEM	Modem circuits			
	Turbo	0.660	1.076	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low-SVS	0.485	0.724	V
VDD_GFX	Graphics			
	Turbo-L1	0.700	1.148	V
	Turbo	0.660	1.076	V
	Nominal-L1	0.625	1.000	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low-SVS	0.485	0.724	V
VDDCX	Digital core circuits			
	Turbo	0.660	1.076	V
	Nominal	0.595	0.939	V
	SVS-L1	0.545	0.860	V
	SVS	0.505	0.794	V
	Low-SVS	0.485	0.724	V
	Retention [2]	0.400	0.560	V
VDDMX	Memory circuits and analog PLL circuits			
VDDA_MIPI_DSI0_0P9	Turbo	0.740	1.076	V
VDDA_MIPI_DSI1_0P9	Nominal	0.740	1.000	V
VDDA_LPA_PLL	SVS-L1 [2]	0.740	0.860	V
VDDA_APC_PLL	Retention [2]	0.540	0.644	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDDA_EBI0	EBI PHY circuits			
VDDA_EBI1	Turbo	0.720	1.076	V
VDDA_CC_EBI01	Nominal	0.700	1.000	V
VDDA_CC_EBI23	SVS-L1	0.625	0.939	V
	SVS	0.625	0.807	V
	Low-SVS	0.505	0.794	V
VDDA_WCSS_CX	WCSS circuits			
VDDA_WCSS_MX	Nominal [2]	0.740	0.860	V
VDDA_WCSS_PLL				

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for this power domain is a static setting. There is no scaling.

Table 3-3 Operating conditions

Parameter		Min	Typ [1]	Max	Unit
Power-supply voltages					
VDDA_WCSS_ADCDAC_1 VDDA_WCSS_ADCDAC_2	Power for WCSS ADC and DAC circuits	1.17	1.304	1.36	V
VDDPX_5	Power for UIM pads	1.7	1.808	1.9	V
VDDPX_6		2.72	2.928	3.03	V
VDDA_QREFS_1P8 VDDA_GFX_CS_1P8 VDDA_APC1_CS_1P8 VDDA_QUSB_HS0_1P8 VDDPX_11 VDD_QFPROM VDD_QFPROM_SP	Power for analog 1.8 V PHY circuits and clock circuits	1.72	1.8	1.88	V
VDDPX_10	Power for pad group 10 – UFS pad	1.15	1.2	1.25	V

Table 3-3 Operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDDA_QUSB_HS0 VDDA_QLINK_LV VDDA_QLINK_LV_CK VDDA_QREFS_0P875 VDDA_UFS2_CORE VDDA_USB2_SS_CORE VDDA_USB1_SS_CORE VDDA_PLL_CC_EBI01 VDDA_PLL_CC_EBI23 VDDA_PCIE_CORE VDDA_UFS1_CORE VDDA_HP_PCIE_CORE VDDA_MIPI_DSI0_PLL VDDA_MIPI_DSI1_PLL VDDA_MIPI_CSI0_0P9 VDDA_MIPI_CSI1_0P9 VDDA_MIPI_CSI2_0P9 VDDA_SP_SENSOR	Power for analog 0.9 V PHY circuits	0.83	0.88	0.92	V
VDDA_QUSB_HS0_3P1	Power for USB HS0 circuits – 3.075 V	2.96	3.088	3.2	V
VDD2	Power for PoP DDR memory core – 1.2 V (top VDD2)	1.07	1.1	1.17	V
VDDPX_3 VDD1	Power for pad group 3 – most I/O pads PoP DDR memory core – 1.8 V (top VDD1)	1.7	1.8	1.9	V
VDDA_HV_EBI0 VDDA_HV_EBI1 VDDA_HV_EBI2 VDDA_HV_EBI3 VDDA_PCIE_1P2 VDDA_UFS1_1P2 VDDA_HP_PCIE_1P2 VDDA_UFS2_1P2 VDDA_USB2_SS_1P2 VDDA_USB1_SS_1P2 VDDA_MIPI_CSI_1P25 VDDA_MIPI_DSI0_1P2 VDDA_MIPI_DSI1_1P2	Power for analog 1.2 V circuits	1.15	1.2	1.25	V
VDDPX_2	Power for pad group 2 – SDC2 pads	1.7 2.72	1.808 2.96	1.9 3.03	V V

Table 3-3 Operating conditions (cont.)

Parameter		Min	Typ [1]	Max	Unit
VDDIO_EBI0 VDDIO_EBI1 VDDIO_EBI2 VDDIO_EBI3 VDDIO_CK_EBI0 VDDIO_CK_EBI1 VDDIO_CK_EBI2 VDDIO_CK_EBI3 VDDQ	Power for EBI I/O circuits	0.57	0.60	0.64	V
VDDPX_13	Power for anti-replay island (secure processor)	1.70	1.856	1.90	V
Thermal conditions					
T_J	Device junction temperature	–	–	+85	°C
T_A [2]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. Typical voltages represent the recommended output settings of the companion PMIC device.
2. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.

3.3 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SDM845 Linux Android Current Consumption Data* (80-P6348-7).

3.4 Dhrystone and rock bottom maximum power

Table 3-4 Dhrystone and rock bottom maximum power

SDM version	Kryo Gold octa core Dhrystone (W) at 85°C (Tj) [1, 2, 3]	Rock bottom (mW) at 30°C (Tj) [4]
SDM845	7 W	7.5 mW

1. This Kryo octa core Dhrystone specification applies to SDM845 CS devices that run Kryo quad Gold cores at 2649.6 MHz and Kryo quad Silver cores at 1766.4 MHz.
2. Dhrystone power should be measured on the VDD_APC0 and VDD_APC1 rails, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).
4. Rock bottom (VDD_CORE and VDD_MEM) should be measured at VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at retention voltage. See AIR1 in Table 3-1 (Test definitions) of *SDM845 Linux Android Current Consumption Data* (80-P6348-7) for test setup.

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SDM845 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-5 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDPX_3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDPX_3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	1.0	µA
I_{IL}	Input low leakage current [1]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [1]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	µA (kΩ)

Table 3-5 DC specification of 1.8 V GPIOs and WCSS WSI I/Os (cont.)

Parameter	Description	Min	Max	Units
V_{OH}	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
2. Pin voltage = VDDPX_3 maximum. For keeper pins, pin voltage = VDDPX_3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDDPX_3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX_3 maximum.

Table 3-6 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX_2	–	VDDPX_2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDPX_2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDDPX_2	–	VDDPX_2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDPX_2	V

Table 3-7 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ

Table 3-7 SDC 1.8 V mode DC specifications (cont.)

Parameter	Description	Min	Typ	Max	Units
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-8 UICC 3 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worse-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 ×VDDPX_x (RST, CLK) and 0.4 V (I/O). The worse-case V_{OL} is used in this table.

Table 3-9 UICC 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ

Table 3-9 UICC 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6) (cont.)

Parameter	Description	Min	Typ	Max	Units
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 × VDDPX_x (RST, CLK) and 0.3 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-10 Digital I/O characteristics for VDDPX_10 nominal (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDDPX_10	V
V_{OH}	Output high-level voltage	0.75 × VDDPX_10	VDDPX_10	V
$R_{PULL-UP}$	Pull-up resistance	100	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	100	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	µA

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in TBD-Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = -\left(\frac{\%drive \times 450}{100}\right) mV$$

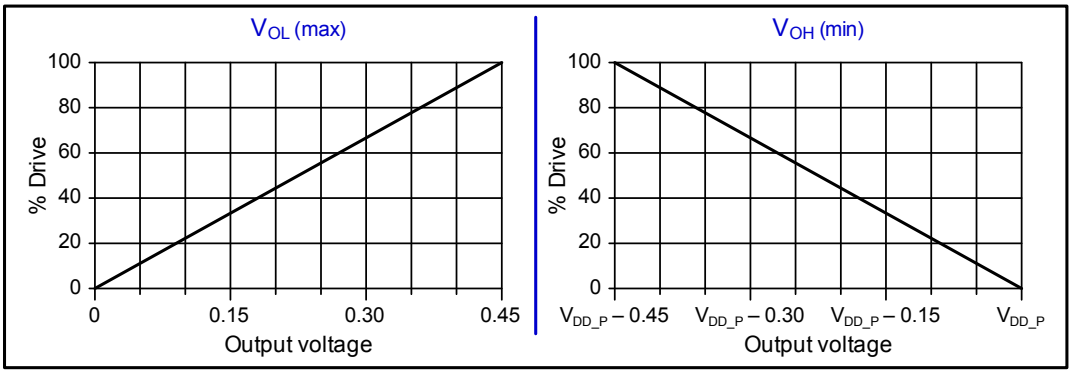


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DDPX_x})

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SDM845 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

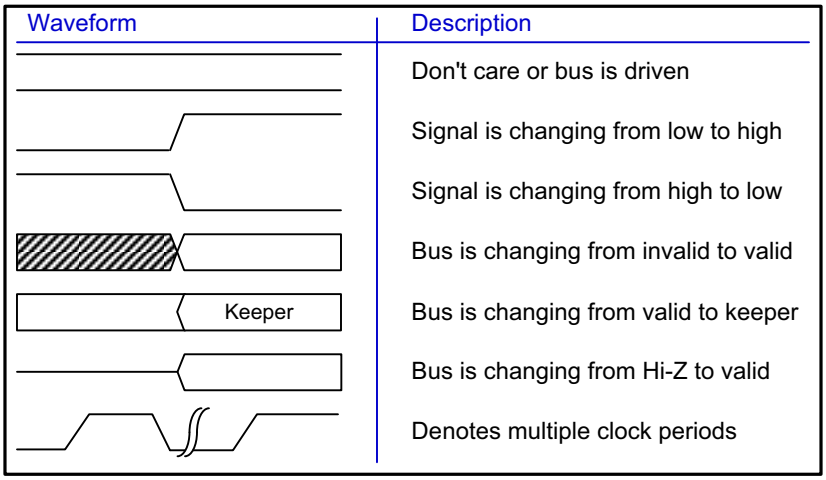


Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SDM845 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

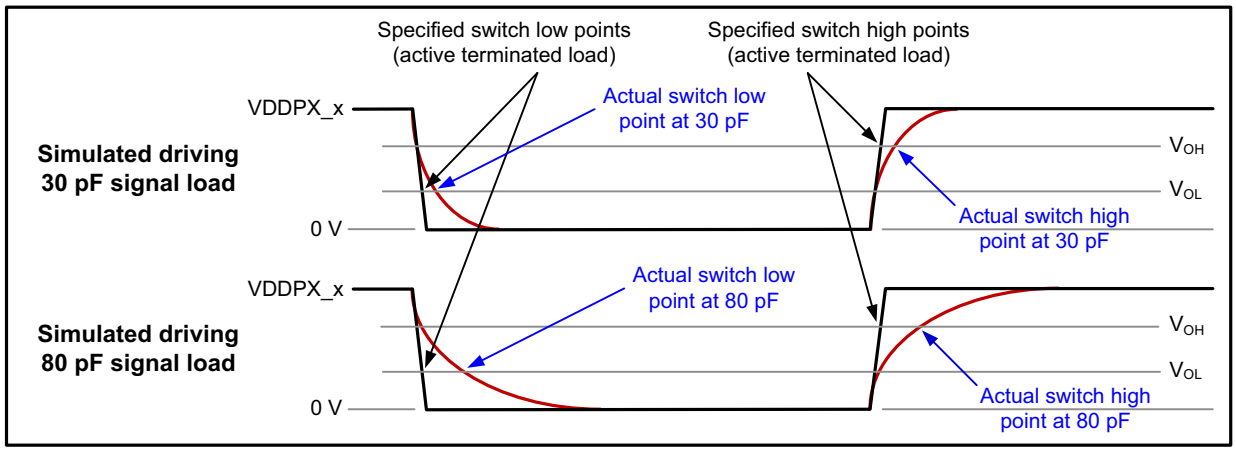


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SDM845 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SDM845 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

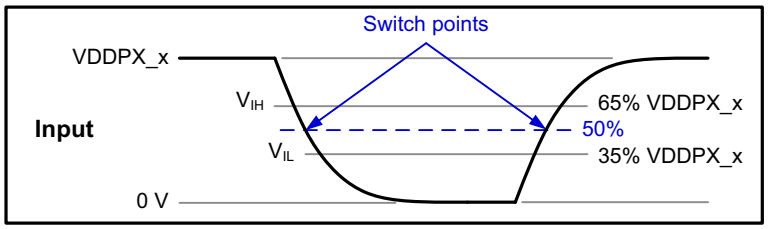


Figure 3-4 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX_x} - 50 mV or more
- V_{OL} ~ 50 mV or less

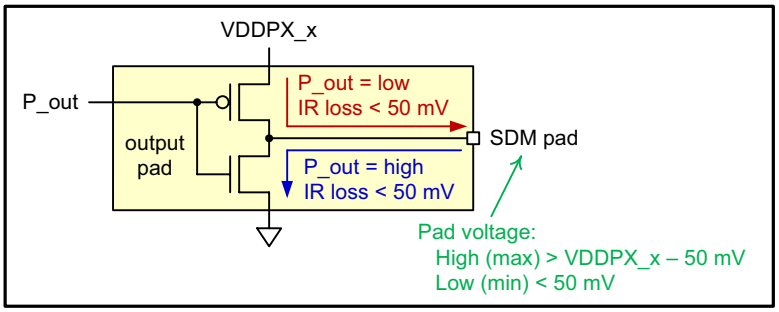


Figure 3-5 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will get worse and hold time numbers may get better.

3.7.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR4x SDRAM memory that is attached to the top of the SDM845 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SDM845 Recommendations* (80-VP300-14).

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SDM845 device supports up to three DPHY or CPHY camera interfaces.

Table 3-11 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported; DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	The maximum supported data rate is 1.5 Gsps.

3.8.2 Audio support

The SDM845 supports the WCD9340/WCD9341 audio codec IC to provide the system's audio functions. SDM845 audio-related interface options with the WCD include:

- SLIMbus: Section 3.9.7
- I^2S: Section 3.9.8
- PCM/TDM: Section 3.9.9
- I^2C: Section 3.9.12

See the *WCD9340/WCD9341 Audio Codec Device Specification* (80-P4986-1) for performance characteristics.

3.8.3 Display support

The SDM845 device supports up to two DPHY or CPHY displays.

Table 3-12 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

3.8.4 DMB support

The SDM845 supports an external DMB solution using the following interface options:

- TSIF: Section 3.9.10
- SD: Section 3.9.1

3.9 Connectivity

The connectivity functions supported by the SDM845 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Transport stream interface (TSIF) interfaces
- Touchscreen connections
- Through proper configuration of the 16 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)

Pertinent specifications for these functions are detailed in the following subsections.

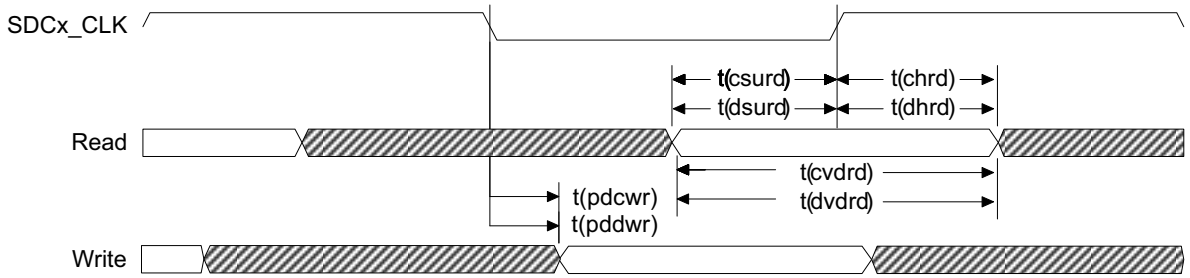
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

Table 3-13 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Single data rate – SDR mode



Double data rate – DDR mode

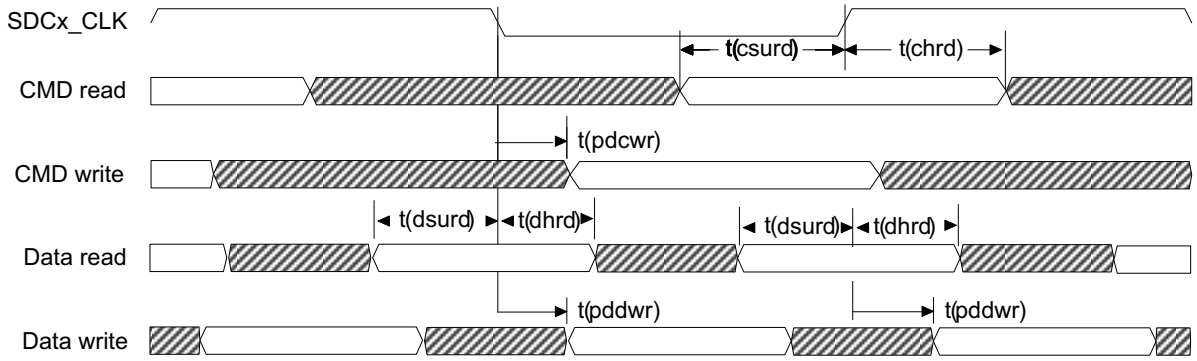


Figure 3-6 SD interface timing

3.9.2 USB interfaces

Table 3-14 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None

3.9.3 DisplayPort

Table 3-15 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	HBR3

3.9.4 PCIe interface

Table 3-16 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	None

3.9.5 UFS interface

Table 3-17 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 2.1	None

3.9.6 UICC interface

Table 3-18 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.7 SLIMbus interface

Table 3-19 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.9.8 I^2S interfaces

There are two I^2S interface types supported by the SDM845:

- Legacy I^2S interfaces for primary and secondary microphones and speakers
- The multiple I^2S (MI2S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-20 Supported I^2S standards and exceptions

Applicable standards	Feature exceptions
Philips I^2S Bus Specifications revised June 5, 1996	None

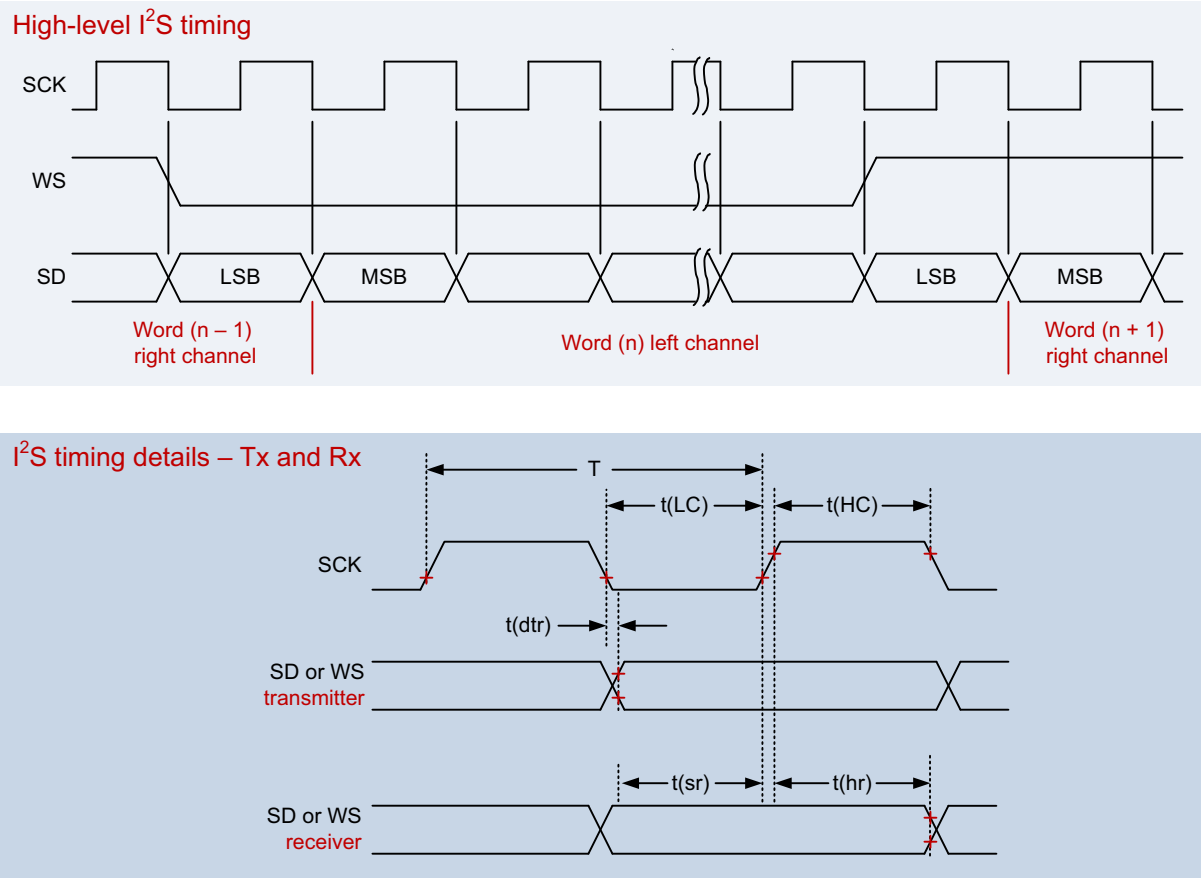


Figure 3-7 I²S timing diagram

Table 3-21 I²S interface timing

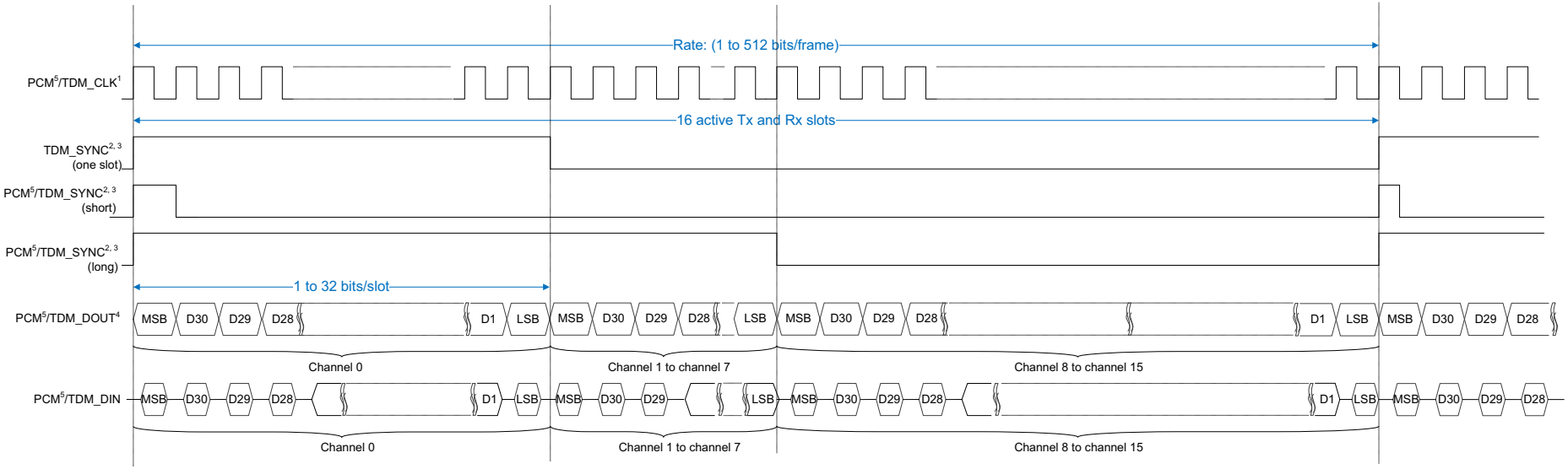
Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns

Table 3-21 I²S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

1. Load capacitance is between 10 and 40 pF.

3.9.9 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-8 PCM/TDM audio format with different sync modes

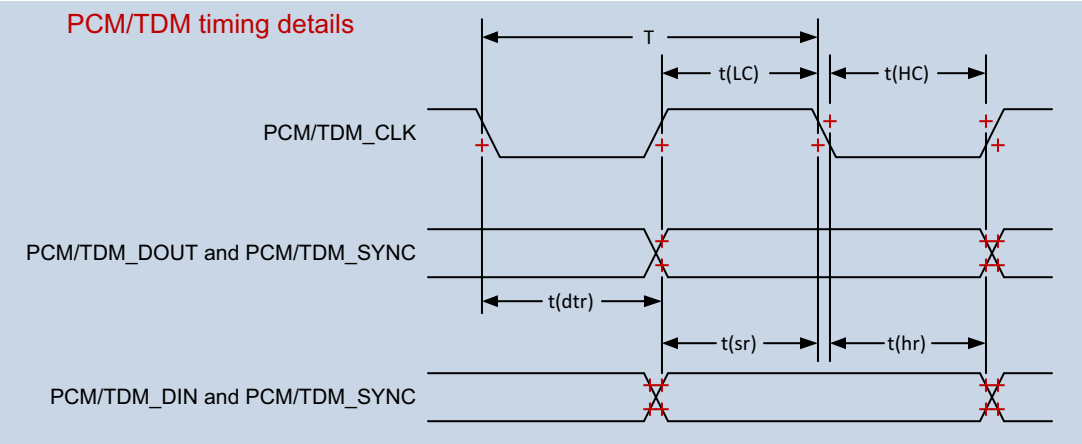


Figure 3-9 PCM/TDM timing diagram

Table 3-22 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		0	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	12.21	ns
Slave mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		0	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	10.17	ns

1. Load capacitance is between 10 to 40 pF.
2. End-to-end testing for the TDM clock is completed up to 12.288 MHz.

3.9.10 TSIF

Table 3-23 Supported TSIF standards and exceptions

Applicable standard	Feature exceptions
ITU-T H.222.0 Transport Stream (HTS); also known as *ISO/IEC 13818-1*	None

3.9.11 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.9.12) and GPIOs configured as discrete digital inputs (Section 3.5). Additional specifications are not required.

3.9.12 I^{2}C interface

Table 3-24 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions
I^{2}C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

3.9.13 Serial peripheral interface

The SDM845 supports SPI as a master only. Any one of the 16 QUP ports can be configured as an SPI master.

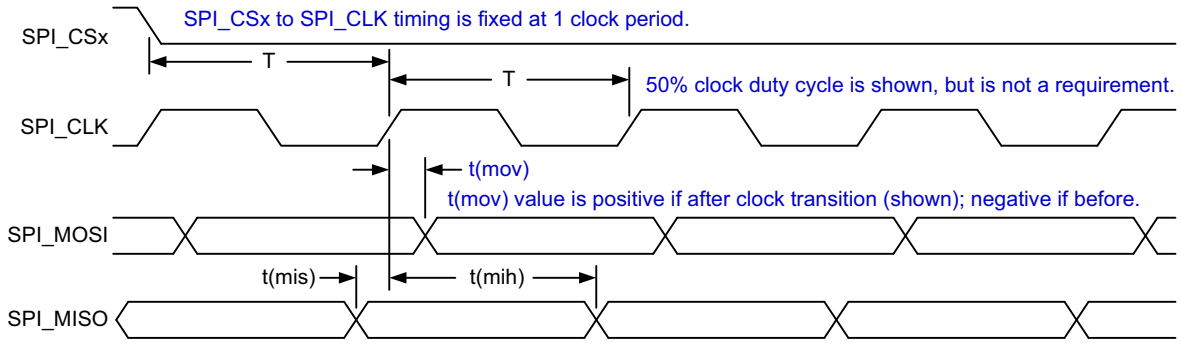


Figure 3-10 SPI master timing diagram

Table 3-25 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns

Table 3-25 SPI master timing characteristics (cont.)

Parameter	Comments	Min	Typ	Max	Unit
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

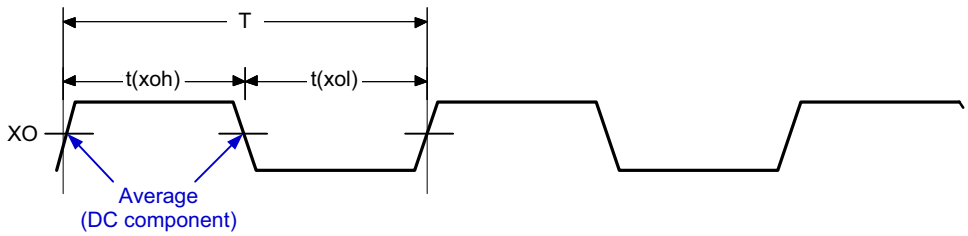


Figure 3-11 XO timing parameters

Table 3-26 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19) and *GPS Quality, 19.2 MHz 2016 Package Size, TH+Xtal Mini-Specification* (80-V9690-26) documents for more information.

3.10.1.2 Sleep clock

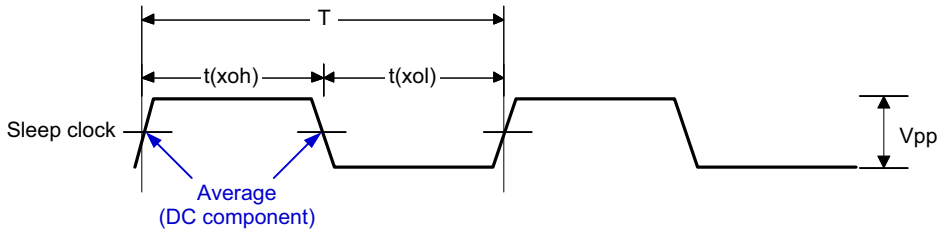


Figure 3-12 Sleep-clock timing parameters

Table 3-27 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.5.

3.10.3 JTAG

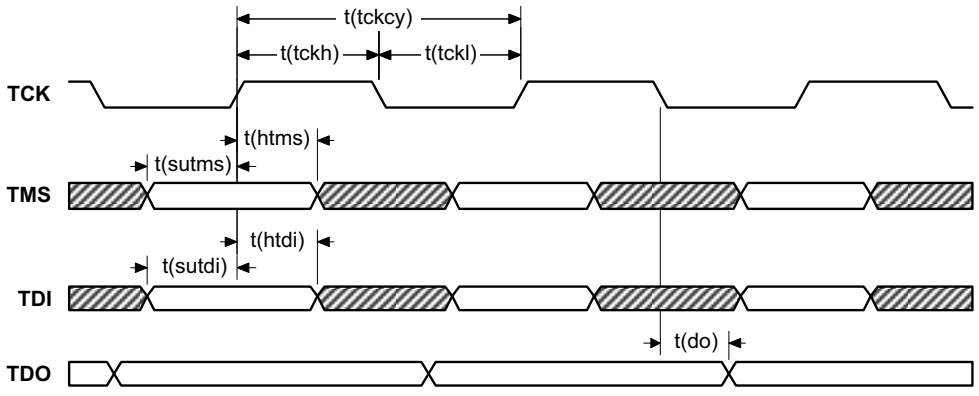


Figure 3-13 JTAG interface timing diagram

Table 3-28 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

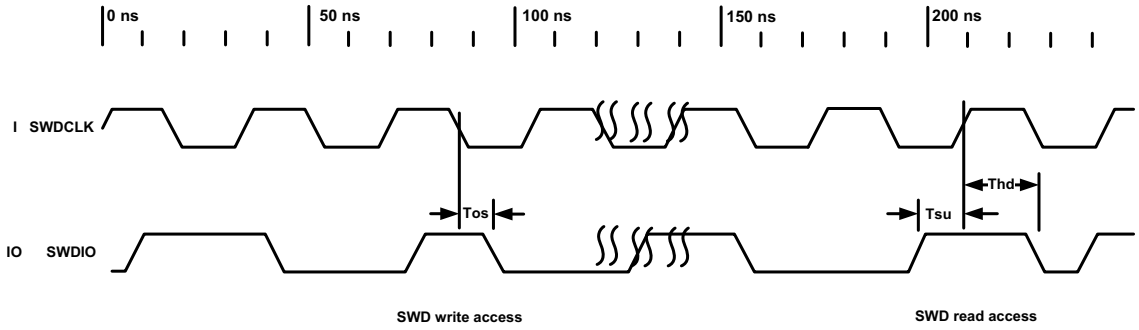


Figure 3-14 SWD write and read AC timing diagram

Table 3-29 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

NOTE SWDCLK runs at 20 MHz or lower.

3.11 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in TBD-[Table 2-2 and Table 2-3]. The digital I/Os must meet the logic-level requirements specified in Section 3.5. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.11.1 RF front end (RFFE)

Table 3-30 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None

3.11.2 System power management interface (SPMI)

Table 3-31 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SDM845 device is available in the 914B MPSP, a 12.4 × 12.4 × 0.58 mm PoP system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 914 PSP, and it accepts memory modules from above that are equivalent to a 556 NSP. The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE Click the following links to download *Package Outline Drawing, 914B MPSP, 12.4 × 12.4 × 0.58 mm, SB136, ST100, M135, PB 556 NSP, PL1, MEP* (NT90-PA607-2) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PA607-2

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

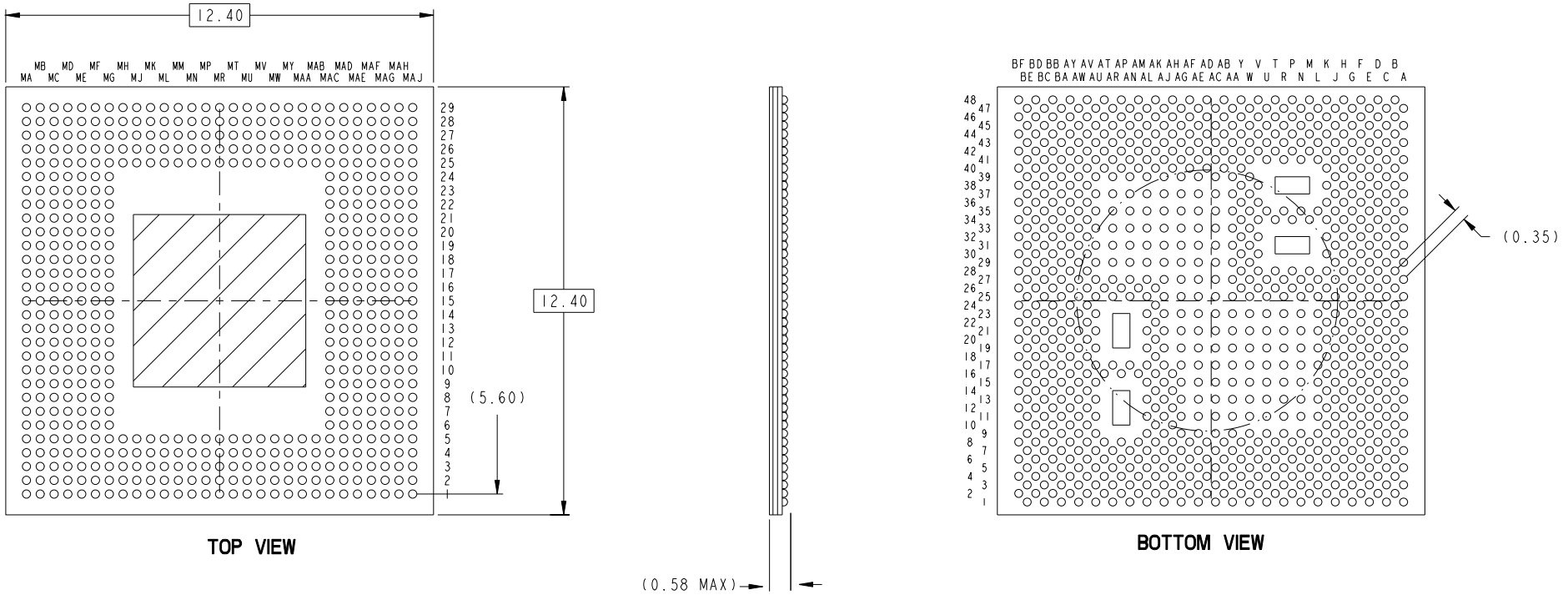


Figure 4-1 Simplified 914B MPSP outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

NOTE The coplanarity specification for the SDM845 bottom package is TBD µm.

4.2 Part marking

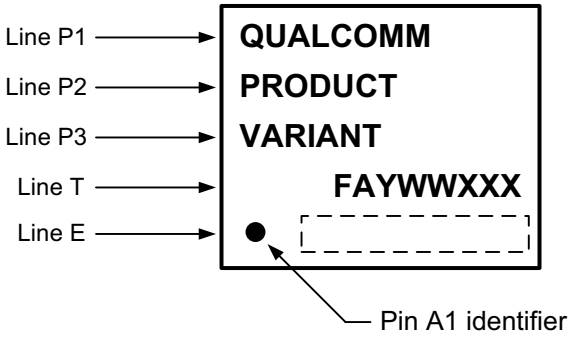


Figure 4-2 SDM845 device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm company name or logo
P2	PRODUCT	QTI product name ■ SDM845
P3	VARIANT	PRR-BB ■ P = product configuration code (see Table 4-3) ■ RR = product revision (see Table 4-3) ■ BB = feature code (see Table 4-3)
T	FAYWWXXX	F = supply source code ■ F = J (Samsung) A = assembly site code ■ A = C (Amkor, Korea) ■ A = X (Amkor, Japan) Y = single-digit year WW = work week (based on calendar year) XXX = traceability number
E	● Blank or random	Ball A1 indicator Additional content as necessary; SB2 (only used for some ES2.0 samples with a single-core Kryo Gold CPU at 2803.2 MHz maximum frequency)

NOTE For complete marking definitions of all SDM845 variants and revisions, see the *SDM845 Device Revision Guide* (80-P6348-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 QFPROM_CORR_PTE_ROW0_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-3.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	SDM-845	— B	— 914B	MPSP	— TR	— 00	— 0	— AA

'CCC' is not a fixed length; it depends on the # of pins in the package

Package type varies in the # of characters

Feature code (BB) may not be included when identifying older devices.

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

Figure 4-3 SDM845 example device identification code

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	Hardware revision number	FEATURE_ID [2]	S value	Comments	Sample date
SDM845	ES1	B00-AA	0x0 008B 0E1	A	0	SDM845, 914B MPSP, 12 layers; 5x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA, UHD, 12.4 × 12.4 MEP	5/2017
	ES2.0	B01-AA	0x1 008B 0E1	A	0	SDM845, 914B MPSP, 12 layers; 5x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA, UHD, 12.4 × 12.4 MEP	8/2017
	ES2.0.1/CS [3]	102-AA	0x2 008B 0E1	2	0	SDM845, 914B MPSP; 10 layers; 5x CA; CDMA, GSM, LTE, TD-SCDMA, WCDMA; UHD; 12.4 × 12.4 MEP	10/2017
		F02-AA	0x2 008B 0E1	A	0	SDM845, 914B MPSP; 8 layers; 4x CA; CDMA, GSM, LTE, TD-SCDMA, WCDMA; UHD; 12.4 × 12.4 MEP	10/2017
		B02-AA	0x2 008B 0E1	6	0	SDM845, 914B MPSP; 12 layers; 5x CA; CDMA, GSM, LTE, TD-SCDMA, WCDMA; UHD; 12.4 × 12.4 MEP	10/2017
SDA845	ES2.0.1/CS [3]	A02-AA	0x2 008E 0E1	0	0	SDA845, 914B MPSP, no modem, UHD, 12.4 × 12.4 MEP	10/2017

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
3. SDM845/SDA845 v2.0.1 devices with a date code of YWW ≥ 742 are CS parts.

4.3.2 Daisy-chain devices

The SDM845 daisy-chain ordering part number is TP-914BMPSP-1 and TP-914BMPSP-3.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-4.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SDM845 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SDM845 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SDM845 Package Thermal Model Icepak* (HS11-P6348-5HW) and the *SDM845 Package Thermal Model FloTHERM* (HS11-P6348-6HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P6348-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P6348-6HW

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NOTE Make this document a favorite to be notified of any changes. For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

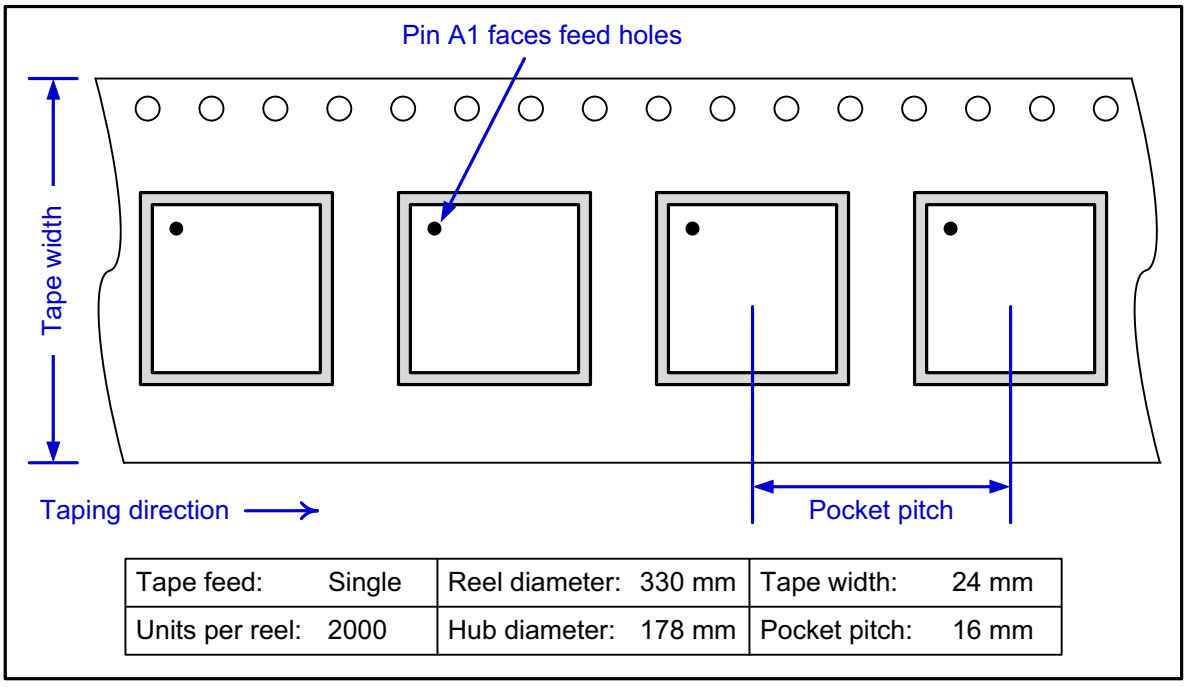
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SDM845 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

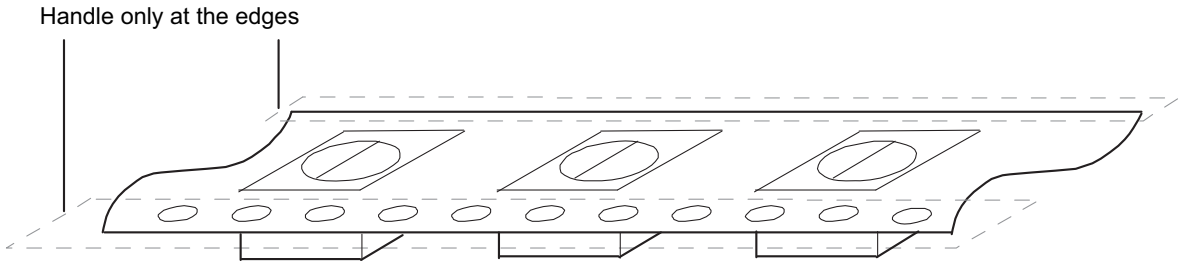


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

SDM845 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SDM845 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SDM845 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the SDM845 ESD ratings.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its Sn/Ag/Cu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy-chain components.

Ordering information is given in Section 4.3.2.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the following link to download *Daisy Chain Interconnect, 914C MPSP, 12.4 × 12.4 mm*, (DS90-PA607-3) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-PA607-3

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For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary

NOTE The silicon reliability results will be provided in November 2017 and the package reliability results will be provided in December 2017.

7.2 Qualification sample description

Device characteristics

Device name:	SDM845
Package type:	914B MPSP
Package body size:	12.4 mm × 12.4 mm × 0.58 mm
Lead count:	914
Lead composition:	SAC125/Ni
Fab process:	10 nm FinFET
Fab sites:	Samsung
Assembly sites:	Amkor, Korea; Amkor, Japan
Solder ball pitch:	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	December 2016	Initial release
B	January 2017	Globally changed UFS 2.0 to UFS 2.1 Globally changed package dimensions to 12.4 × 12.4 Device description page 1: Corrected the secure processor features Figure 1-1 SDM845 functional block diagram and example application: ■ Corrected the name for video core to VPU444 and display engine to DPU795 ■ Corrected the WCD934x feature support ■ Corrected the camera name to Spectra ■ Corrected the PAMID part number Table 1-1 SDM845 features: ■ Corrected the name for video core to VPU444 and display engine to DPU795 ■ Corrected the secure processor features ■ Corrected the target frequencies for Kryo Gold/silver ■ Clarified the last level cache as system cache ■ Corrected the QUP numbers that support HS-UART ■ Corrected the QUP numbers that support I^3C ■ Clarified the number of USB3.1 ports Section 2.2.1 Pin map – bottom: Added the link to the *SDM845 Pin Assignment and GPIO Configuration Spreadsheet (80-P6348-1A)* Table 2-3 Bottom pin descriptions – general-purpose input/output ports: ■ Corrected the chip select description for GPIO_92 and GPIO_95 ■ Corrected the QUP numbers which support I^3C ■ Added the PCM signals which are multiplexed with I^2S ■ Corrected GPIO_20 as wakeup capable pin Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins: Corrected the pin names for AW27 and AY26 Table 2-6 Top pin descriptions – ground, NC, reserved, and power supply pins: Corrected the description for VDD pins for the LPDDR4x device

Revision	Date	Description
C	March 2017	■ Global updates: □ Updated the EBI description from dual-channel to four-channel □ Updated the package outline drawing (NT90) – changed top side from 366 NSP to 556 NSP to expand the number of ground pins □ Changed IZat to Qualcomm Location Suite throughout □ Removed QCA6290 support ■ Key features (see Section 1.2 for details): Updated the camera bullet ■ Updated the following features in Table 1-1 SDM845 features: □ Digital signal processing □ System memory via PoP and EBI □ Camera interfaces □ Security ■ Figure 2-3 SDM845 top pin assignments and Table 2-6 Top pin descriptions – ground, NC, reserved, and power supply pins: Added VSSX (ground) pins
D	June 1, 2017	■ Figure 1-1 SDM845 functional block diagram and example application: Removed SDR660 from the diagram ■ Table 1-1 SDM845 features: □ Revised the Kryo core target frequencies □ Revised the number of channels for PoP memory □ Removed SDR660 ■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: □ Revised the pad types from PD to PU for the following: – GPIO_103 – GPIO_45 – GPIO_36 □ Revised wake-up function, configuration function, and functional descriptions for Snapdragon sensor core I/O pins ■ Added the following sections: □ Section 3.2 Operating conditions □ Section 4.2 Part marking □ Section 4.3 Device ordering information □ Section 4.4 Device moisture sensitivity level □ Section 4.5 Thermal characteristics
E	June 26, 2017	■ Table 1-1 SDM845 features: Updated the sensor core memory to 1.0 MB ■ Corrected the pin name for top side pins M_AG15 and M_AH15 as NC ■ Figure 4-3 SDM845 example device identification code: Corrected the product name to add a hyphen and added the shipping package note

Revision	Date	Description
F	November 2017	■ Global updates □ Removed *(Advance Information)* from title □ Removed the I^3C feature throughout this document □ Removed the UFS2 feature throughout this document □ Updated the RR code definition in Chapter 2 *Pin definitions* ■ Table 1-1 *SDM845 features*: Updated the Kryo Gold cluster and Kryo Silver cluster frequencies, the video applications performance entry, and the audio section ■ Table 2-3 *Bottom pin descriptions – general-purpose input/output ports*: Updated the pin direction to pull-up (PU) for GPIO_47 and pull-down (PD) for GPIO_45 ■ Added content to Section 3.1 *Absolute maximum ratings* ■ Added Table 3-2 *Operating conditions for voltage rails with AVS Type-1* and removed entries from Table 3-3 *Operating conditions* accordingly ■ Updated TBD values in Table 3-3 *Operating conditions* ■ Added Section 3.3 *Digital logic characteristics* through Section 3.11 *RF and power management interfaces* ■ Table 4-1 *Device marking line definitions*: Added the Amkor, Japan assembly site to the line T and additional content information ■ Figure 4-3 *SDM845 example device identification code*: Corrected the P code value ■ Table 4-3 *Device identification details*: Added the ES2.0.1/CS entries ■ Added content to Chapter 5 *Carrier, handling, and storage information* ■ Added content to Chapter 6 *PCB mounting guidelines* ■ Added a note to Section 7.1 *Reliability qualifications summary* ■ Added content to Section 7.2 *Qualification sample description*

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

Document release date: November 3, 2017

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