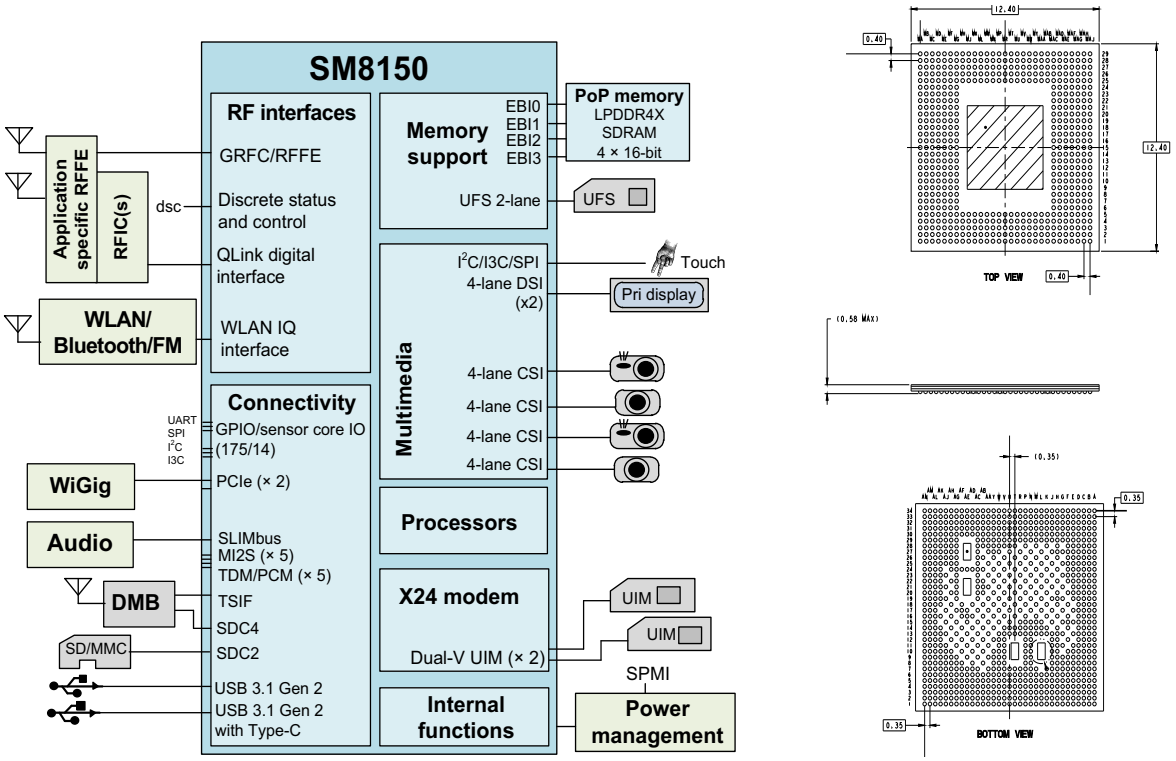
Qualcomm Technologies, Inc.

Device description

SM8150 is the new generation Qualcomm® Snapdragon™ premium-tier processor with integrated LTE modem. It is designed with the 7 nm process, for superior performance and power efficiency. SM8150 includes the following key components:

- Qualcomm® Kryo™ 485 CPU built on Arm Cortex technology
- Integrated Snapdragon X24 LTE modem with Cat20 download speeds up to 2.0 Gbps
- Qualcomm® Adreno™ 640 GPU for the highest in graphics performance and power efficiency
- Qualcomm® Hexagon™ 696 DSP with quad Hexagon Vector eXtensions (HVX) processor for vision processing and machine learning
- Qualcomm Spectra™ 380 image processing engine for the ultimate photography and videography experiences
- Adreno 554 VPU for high-quality, Ultra HD video encode and decode
- Adreno 895 DPU for on-device and external ultra HD display support
- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9340/WCD9341 audio codec for low power voice processing and audiophile quality audio playback
- Qualcomm® All-Ways Aware™ Sensor Technology for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU230) for advanced secure use cases
- Qualcomm® Neural Processing Unit (NPU130) for high-performance machine learning use cases
- Integrated 802.11ac, 2 × 2 MIMO and Bluetooth 5.1
- Qualcomm® Location Suite with support for GPS, GLONASS, BeiDou, Galileo, and QZSS systems
- Quad-channel package-on-package (PoP) high-speed LPDDR4X SDRAM with optional low-power features.
- UFS 3.0 Gear 4 Rate A support

SM8150/SM8150P high-level block diagram and 893 MPSP drawing



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Contents

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1 Introduction

NOTE: Unless otherwise specified, SM8150 refers to the SM8150 and SM8150P chipsets throughout this document. Wherever appropriate, exceptions are specified.

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

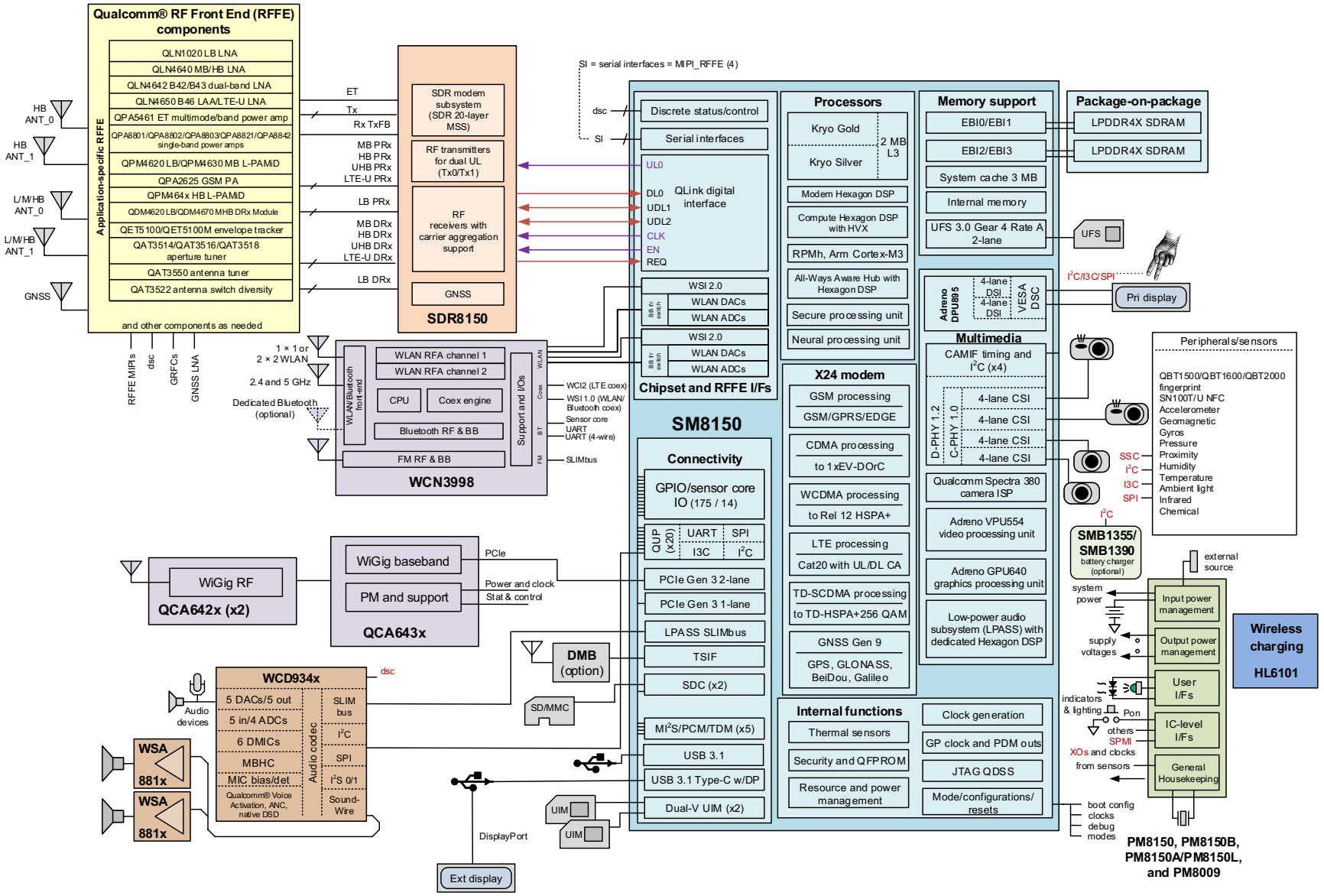

Figure 1-1 SM8150 functional block diagram and example application

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1.2 SM8150/SM8150P features

NOTE: Some of the hardware features integrated within the SM8150/SM8150P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8150/SM8150P features.

Table 1-1 SM8150/SM8150P features

Feature	SM8150/SM8150P capability
Processors	
Applications	Kryo 485 – 64-bit applications processor with a 2 MB L3 cache ■ Quad high-performance Kryo Gold cores □ Three Kryo Gold cores with a 256 KB L2 cache per core, F_{max} at 2.419 GHz □ One Kryo Gold prime core with a 512 KB L2 cache, F_{max} at 2.842 GHz for SM8150 AB variant, F_{max} at 2.956 GHz for SM8150 AC variant. ■ Quad low-power Kryo Silver cores with a 128 KB L2 cache per core, F_{max} at 1.786 GHz
Digital signal processing	Compute Hexagon DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Coprocessor (Hexagon CP) 1.1 ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ Targeting up to 1.5 GHz and with a 1.0 MB L2 cache ■ The HCP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. Audio Hexagon DSP dedicated to audio subsystem, targeting up to 1.5 GHz and with a 512 KB L2 cache Modem Hexagon DSP to support 7x DLCA, 2x ULCA, and 20-layer MIMO Sensor Hexagon DSP in the Qualcomm All-Ways Aware Hub to support always-on, low-power use cases, and with 1.0 MB memory All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Artificial intelligence	Qualcomm NPU130 dedicated neural processing unit for performance and always-on neural network (NN) use cases. It incorporates a NN matrix engine to ensure efficient execution of various neural networks and their parameters. The NPU may be used for typical imaging, video, audio, and data-based NN use cases and will typically be used in conjunction with the compute Hexagon DSP subsystem.
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR4X SDRAM with optional low-power features (16-bit) designed for a 2133 MHz clock system cache
External memory Via UFS Via SDC	 UFS 3.0 Gear 4 Rate A – for on-board memory SD v3.0 4-bit for SD card

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Table 1-1 SM8150/SM8150P features (cont.)

Feature	SM8150/SM8150P capability
RF support	
RF operating bands	Defined by the RF transceiver device
Air interfaces	See Table 1-2 (not applicable to SM8150P except for WLAN/Bluetooth).
GSM	Yes
CDMA	Yes
WCDMA	Yes
TD-SCDMA	Yes
LTE	Yes (Cat20 with 2.0 Gbps DL capability)
WLAN/Bluetooth	Yes (with WCN3998)
Advanced techniques	Up to seven DL CA across five bands, up to two ULCA, and up to 20DL layers
GNSS – Qualcomm Location Suite engine	Gen 9; GPS L1 and L2/L5, GLONASS, BeiDou, and Galileo
Multimedia	
Adreno display processing unit (DPU)	Adreno DPU 895, supports up to three 4K display (one internal display through DSI and two external display through DisplayPort)
Display interface	Two 4-lane DSI D-PHY 1.2 or two 3-trio C-PHY v1.1 with VESA DSC v1.1
	DisplayPort v1.4 at 8.1 Gbps/lane over Type-C with support for MST and VESA DSC v1.1 and FEC (USB3 and USB2 concurrency supported)
	Miracast – up to 4K60
Display performance	3840 × 2400 [1] at 60 Hz (or 120 Hz in VR mode), up to 30 bpp
	Two 2560 × 2560 [1] at 120 Hz for dual-panel VR displays, up to 30 bpp
	4096 buffer width, and 16 hardware-layer composition
Display processing	Qualcomm® TruPalette™ Display Feature– HDR10+ and HDR10 tone mapping, color gamut mapping, six-zone, memory color, and picture adjust
Pixel processing	Qualcomm® Low-Power Picture Enhancement display – compression [Qualcomm® Universal Bandwidth Compression (UBWC 3.0, DSC v1.1)], CABL, FOSS, Assertive Display v4, Q-sync, and destination scaler with DE
Camera support	
Performance	Qualcomm Spectra 380 ISP to support up to eight cameras (four concurrent) ■ Real-time sensor input resolution: 20 + 20 + 2 + 2 ■ 32 MP 30 fps ZSL with a dual ISP ■ Hardware 2PD support and improved face detection ■ Hardware depth map engine and improved zzHDR
Camera interface	MIPI CSI configurable in 4 + 4 + 4 + 4 configuration ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port ■ C-PHY v1.0: 5.71 Gbps/trio on three trios per port

Table 1-1 SM8150/SM8150P features (cont.)

Feature	SM8150/SM8150P capability
Adreno video processing unit (VPU)	■ Adreno VPU 554 – fifth-generation UHD video processing unit ■ Video decode up to 4K120 or 8K30 ■ Video encode up to 4K60 ■ Concurrent 4K60 decode and 4K30 encode for wireless display ■ Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs ■ Native encode support for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs ■ Improved encoder with up to 30% reduction in bit rate for same subjective quality video ■ New computer vision processor (CVP) for object detection and tracking
Adreno graphic processing unit (GPU)	■ Adreno GPU 640, F_{max} at 585 MHz for SM8150 AB variant, 675 MHz for SM8150 AC variant – 4K 60 fps UI or 2X 2k 60 fps UI ■ OpenGL ES 3.2, Vulkan and Vulkan Compute, DX12.x ■ OpenCL 2.0 full profile, DirectCompute

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Table 1-1 SM8150/SM8150P features (cont.)

Feature	SM8150/SM8150P capability
Audio	
Codec	Integrated within the WCD9340/WCD9341 high-fidelity audio codec: ■ Five DACs; five outputs ■ Five differential analog inputs; four ADCs ■ Six digital microphones ■ Hexagon Access CPE voice activation subsystem for ultra low-power voice wake-up ■ Native DSD (WCD9341 only), MBHC, and ANC ■ 130 dB dynamic range ■ 32-bit DAC ■ 44.1 kHz family native playback ■ Five GPIOs
Speaker amplifier	Integrated within the WSA8810/WSA8815 class D/G, low noise smart amplifier: ■ 2 W/4 W output power into 8 Ω load ■ Integrated SmartBoost ■ Integrated feedback speaker protection for excursion and temperature control of the transducers ■ Support for receiver assist speaker (RAS) or speaker as receiver (SAR) with handset ANC
Low-power audio subsystem (LPASS)	
Processing	■ Dedicated audio LPASS Hexagon DSP with a 512 kB L2 cache ■ Qualcomm® Voice Suite voice processing engine to offload voice user interface and voice call processing ■ Fluence echo cancellation and noise suppression ■ Qualcomm® Voice Activation ■ Qualcomm® Audio Post-processing
Codecs	■ Voice codecs: enhanced voice services, EVRC, EVRC-B, EVRC-WB; GSM-FR, GSM-EFR, and GSM-HR; AMR-NB and AMR-WB ■ Audio codecs: AAC, AAC-LC, HE-AAC v1, HE-AAC v2, FLAC
Audio interfaces	SLIMbus (2x): ■ WCD9340/WCD9341 and WCN3998 MI^{2}S: ■ Two full duplex stereo or up to quad channel (x4) ■ Up to eight channels for multichannel Tx/Rx audio applications (x1) PCM/TDM: ■ Up to five interfaces: up to 32 channels per individual interface ■ Up to 512 bits/frame and 32 bits/slot ■ Short, long, and one-slot sync mode ■ Maximum clock frequency of 24.576 MHz
Digital mobile broadcast (DMB)	External IC required with the TSIF or SDIO interface

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Table 1-1 SM8150/SM8150P features (cont.)

Feature	SM8150/SM8150P capability
Connectivity	
Qualcomm universal peripheral (QUP) ports	20:7 bits each for four QUPs and 4 bits each for the other QUPs; multiplexed serial interface functions
UART	UART interface available on all QUPs. HS-UART available on GPIO QUP6/QUP7/QUP11/QUP12/QUP13/QUP14/QUP15/QUP16 Qualcomm All-Ways Aware Hub
I^2C	I^2C interface available on all QUPs up to 1 Mbps for touch, sensors, near field communicator (NFC), and so on; dedicated controller for each port
I3C	I3C interface available on GPIO QUP3/QUP4/QUP8/QUP9 and Qualcomm All-Ways Aware Hub QUP0/QUP1
SPI	SPI interfaces available on all QUPs for cameras, sensors, and so on; dedicated controller for each port
CCI I^2C	Four dedicated I^2C interfaces for camera
UIM	Two – dual voltage (1.8 V/2.95 V)
USB	USB 3.1, support Type-C with DisplayPort v 1.4
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card and DMB
TSIF	DMB support
Wireless connectivity	WCN3998 2 × 2 802.11ac RFQCA643x/QCA642x 802.11ad at 60 GHz
Touchscreen support	Capacitive panels via ext IC (I^2C, I3C, SPI, and interrupts)
Fingerprint support	QBT1500/QBT1600/QBT2000 ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display
DMB support	Via external DMB device (SDC or TSIF)
Configurable GPIOs	
Number of GPIO ports	175 – GPIO_0 to GPIO_174
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	SPU-230 with certification enabling iUICC and payments, Secure Boot 3.0, secure debug, secure key provisioning, TrustZone, Qualcomm® Trusted Execution Environment v5, hardware supported KeyStore, combined image signing
Crypto engines	Crypto engine v5 (CE5), Qualcomm to submit for FIPS certification
TrustZone services	Secure file system, fast trusted storage
DRM support in hardware	PlayReady SL2000/SL3000, Widevine level 1, and level 3, ISDB-T
QFPROM	640 bits available for OEM use
Access control	Programmable security domain protection and sand-boxing

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Table 1-1 SM8150/SM8150P features (cont.)

Feature	SM8150/SM8150P capability
Boot sequence	■ 1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) modem; 7) SP; 8) VPU, camera, LPASS, Qualcomm All-Ways Aware Hub, compute SS, and NPU ■ Emergency boot over USB 3.1
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset and RF front end (RFFE) interface features	
SDR RF transceivers	
QLink digital interface	■ One dedicated downlink lane, one dedicated uplink lane, and two bidirectional uplink/downlink lanes ■ Improved layout, routing, package, and signal integrity
Power management	2-line SPMI; plus other lines, as needed, via GPIOs
Wireless connectivity	
WLAN baseband data	I/Q differential pair interface
Bluetooth	UART interface
Fabrication technology and package	
Digital die	7 nm process
PoP – small, thermally efficient package	MPSP893: 12.4 × 12.4 × 0.58 mm max (without memory device on top)
Bottom pin array	Bottom: 893-pin picoscale package (893 PSP); 0.35 mm pitch
Top pin array	Top: 556-pin nanoscale package (556 NSP); 0.4 mm pitch

1. Higher resolution and wider aspect ratio displays can be supported. Exact panel details and timings required to determine if it can be supported.

1.2.1 Air interface features

Table 1-2 Key modem features (not applicable to SM8150P)

Standard	Feature descriptions
LTE	
Category	20
Carrier aggregation	FDD and TDD; downlink up to 140 MHz, uplink up to 40 MHz
CA direction	Uplink and downlink
Other LTE support	■ FeICIC-IC ■ ePDCCH ■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ 4-way Rx diversity ■ 8 × 4 MIMO

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Table 1-2 Key modem features (not applicable to SM8150P)

Standard	Feature descriptions
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1xSLTE and 1xSRLTE ■ hVoLTE and hSRLTE
Multi-SIM	
3G	3G + GSM DSDS
4G	4G + GSM DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CnE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Table 1-3 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite engine with global navigation satellite system (GNSS) support	
Gen 9	GPS, GLONASS, BeiDou, and Galileo

Table 1-4 Wireless connectivity summary by standard

Standard	Feature descriptions
WLAN	
With WCN3998	802.11ac, 2 × 2 MIMO
Bluetooth	
With WCN3998	Bluetooth 5.1 and earlier

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2 Pin definitions

The SM8150 is the lower device within a PoP system, as illustrated and explained in Figure 2-1.

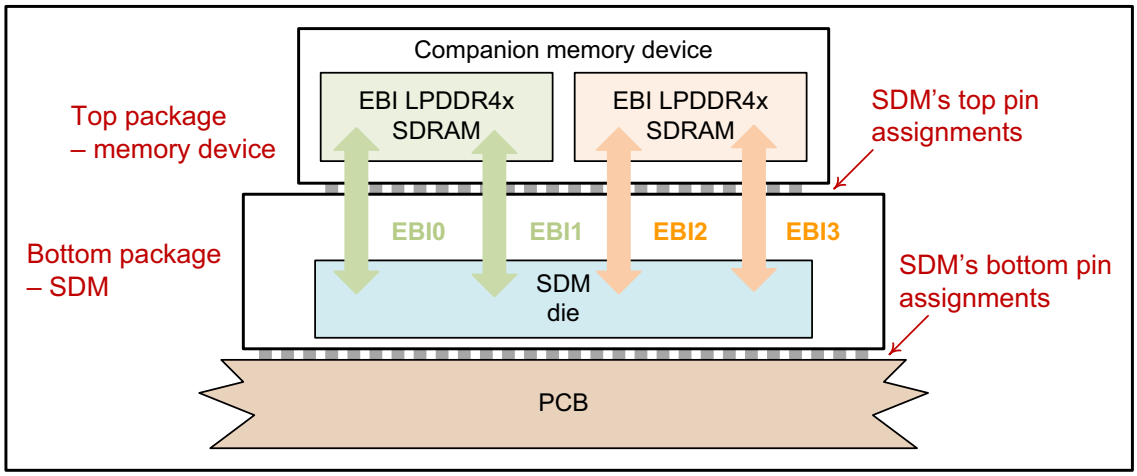

Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8150 bottom pins (Section 2.2)
- SM8150 top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O parameter definitions

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input

Table 2-1 I/O parameter definitions (cont.)

Symbol	Description
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX_0	Pad group 0 (control signals); 1.8 V
PX_2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX_6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX_10	Pad group 10 (UFS1_REF_CLK and UFS1_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.8 V
PX_13	Pad group 13 (secure processor unit [SPU]); 1.85 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

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2.2 Pin assignments – bottom

2.2.1 Pin map – bottom

The SM8150 is available in the MPSP893. Its bottom surface is equivalent to an 893 PSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details and Section 2.3 for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inches × 11 inches hard copy. Other viewing options are available:

- Print that one page on an 11 inches × 17 inches sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.
- Download the *SM8150 Pin Assignment and GPIO Configuration Spreadsheet* (80-PD867-1A) – this Microsoft Excel spreadsheet lists all SM8150 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PD867-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PD867-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

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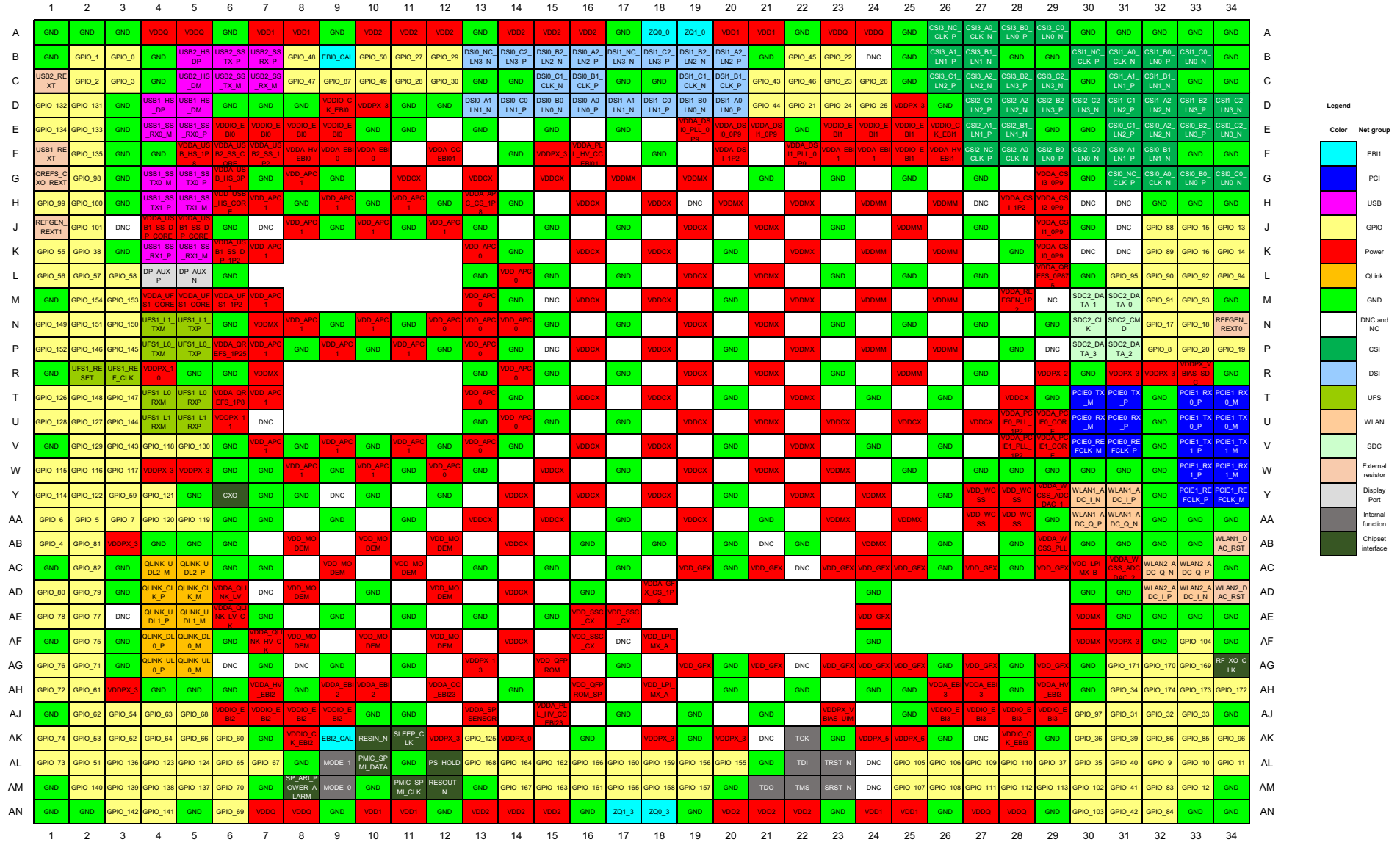

Figure 2-2 SM8150 bottom pin assignments

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2.2.2 Pin descriptions – bottom

Table 2-2 Bottom pin descriptions – primary pins

Pin #	Pin name	Pad voltage	Pad type	Functional description
G32	CSI0_A0_CLK_N	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – negative MIPI CSI 0 (CPHY), trio lane 0 – A
F31	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – positive MIPI CSI 0 (CPHY), trio lane 1 – A
E32	CSI0_A2_LN2_N	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – negative MIPI CSI 0 (CPHY), trio lane 2 – A
G33	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – positive MIPI CSI 0 (CPHY), trio lane 0 – B
F32	CSI0_B1_LN1_N	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – negative MIPI CSI 0 (CPHY), trio lane 1 – B
E33	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – negative MIPI CSI 0 (CPHY), trio lane 2 – B
G34	CSI0_C0_LN0_N	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – negative MIPI CSI 0 (CPHY), trio lane 0 – C
E31	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – positive MIPI CSI 0 (CPHY), trio lane 1 – C
E34	CSI0_C2_LN3_N	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – negative MIPI CSI 0 (CPHY), trio lane 2 – C
G31	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – positive MIPI CSI 0 (CPHY), no connect
B31	CSI1_A0_CLK_N	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – negative MIPI CSI 1 (CPHY), trio lane 0 – A
C31	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – positive MIPI CSI 1 (CPHY), trio lane 1 – A
D32	CSI1_A2_LN2_N	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – negative MIPI CSI 1 (CPHY), trio lane 2 – A
B32	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – positive MIPI CSI 1 (CPHY), trio lane 0 – B
C32	CSI1_B1_LN1_N	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – negative MIPI CSI 1 (CPHY), trio lane 1 – B
D33	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – positive MIPI CSI 1 (CPHY), trio lane 2 – B
B33	CSI1_C0_LN0_N	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – negative MIPI CSI 1 (CPHY), trio lane 0 – C
D31	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – positive MIPI CSI 1 (CPHY), trio lane 1 – C
D34	CSI1_C2_LN3_N	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – negative MIPI CSI 1 (CPHY), trio lane 2 – C

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
B30	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – positive MIPI CSI 1 (CPHY), no connect
F28	CSI2_A0_CLK_N	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – negative MIPI CSI 2 (CPHY), trio lane 0 – A
E27	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – positive MIPI CSI 2 (CPHY), trio lane 1 – A
D28	CSI2_A2_LN2_N	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – negative MIPI CSI 2 (CPHY), trio lane 2 – A
F29	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – positive MIPI CSI 2 (CPHY), trio lane 0 – B
E28	CSI2_B1_LN1_N	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – negative MIPI CSI 2 (CPHY), trio lane 1 – B
D29	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – positive MIPI CSI 2 (CPHY), trio lane 2 – B
F30	CSI2_C0_LN0_N	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – negative MIPI CSI 2 (CPHY), trio lane 0 – C
D27	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – positive MIPI CSI 2 (CPHY), trio lane 1 – C
D30	CSI2_C2_LN3_N	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – negative MIPI CSI 2 (CPHY), trio lane 2 – C
F27	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – positive MIPI CSI 2 (CPHY), no connect
A27	CSI3_A0_CLK_N	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – negative MIPI CSI 3 (CPHY), trio lane 0 – A
B26	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – positive MIPI CSI 3 (CPHY), trio lane 1 – A
C27	CSI3_A2_LN2_N	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – negative MIPI CSI 3 (CPHY), trio lane 2 – A
A28	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – positive MIPI CSI 3 (CPHY), trio lane 0 – B
B27	CSI3_B1_LN1_N	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – negative MIPI CSI 3 (CPHY), trio lane 1 – B
C28	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – positive MIPI CSI 3 (CPHY), trio lane 2 – B
A29	CSI3_C0_LN0_N	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – negative MIPI CSI 3 (CPHY), trio lane 0 – C
C26	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – positive MIPI CSI 3 (CPHY), trio lane 1 – C
C29	CSI3_C2_LN3_N	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – negative MIPI CSI 3 (CPHY), trio lane 2 – C

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
A26	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – positive MIPI CSI 3 (CPHY), no connect
Y6	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
D16	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – positive MIPI DSI 0 (CPHY), trio lane 0 – A
D13	DSI0_A1_LN1_N	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – negative MIPI DSI 0 (CPHY), trio lane 1 – A
B16	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – positive MIPI DSI 0 (CPHY), trio lane 2 – A
D15	DSI0_B0_LN0_N	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – negative MIPI DSI 0 (CPHY), trio lane 0 – B
C16	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – positive MIPI DSI 0 (CPHY), trio lane 1 – B
B15	DSI0_B2_LN2_N	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – negative MIPI DSI 0 (CPHY), trio lane 2 – B
D14	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – positive MIPI DSI 0 (CPHY), trio lane 0 – C
C15	DSI0_C1_CLK_N	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – negative MIPI DSI 0 (CPHY), trio lane 1 – C
B14	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – positive MIPI DSI 0 (CPHY), trio lane 2 – C
B13	DSI0_NC_LN3_N	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – negative MIPI DSI 0 (CPHY), no connect
D20	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – positive MIPI DSI 1 (CPHY), trio lane 0 – A
D17	DSI1_A1_LN1_N	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – negative MIPI DSI 1 (CPHY), trio lane 1 – A
B20	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – positive MIPI DSI 1 (CPHY), trio lane 2 – A
D19	DSI1_B0_LN0_N	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – negative MIPI DSI 1 (CPHY), trio lane 0 – B
C20	DSI1_B1_CLK_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – positive MIPI DSI 1 (CPHY), trio lane 1 – B
B19	DSI1_B2_LN2_N	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – negative MIPI DSI 1 (CPHY), trio lane 2 – B
D18	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – positive MIPI DSI 1 (CPHY), trio lane 0 – C
C19	DSI1_C1_CLK_N	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – negative MIPI DSI 1 (CPHY), trio lane 1 – C

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
B18	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – positive MIPI DSI 1 (CPHY), trio lane 2 – C
B17	DSI1_NC_LN3_N	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – negative MIPI DSI 1 (CPHY), no connect
B9	EBI0_CAL	PX_3	AI	EBI0/1 LPDDR4X calibration resistor
AK9	EBI2_CAL	PX_3	AI	EBI2/3 LPDDR4X calibration resistor
L5	DP_AUX_N	–	AI, AO	DisplayPort auxiliary channel – negative
L4	DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – positive
AM9	MODE_0	PX_0	DI-S PD	Mode control bit 0 – unconnected for native mode
AL9	MODE_1	PX_0	DI-S PD	Mode control bit 1 – unconnected for native mode
V30	PCIE0_REFCLK_M	–	AO	PCIe 0 Gen 3 reference clock – minus
V31	PCIE0_REFCLK_P	–	AO	PCIe 0 Gen 3 reference clock – plus
U30	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – minus
U31	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – plus
T30	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – minus
T31	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – plus
Y34	PCIE1_REFCLK_M	–	AO	PCIe 1 Gen 3 reference clock – minus
Y33	PCIE1_REFCLK_P	–	AO	PCIe 1 Gen 3 reference clock – plus
T34	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive 0 – minus
T33	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive 0 – plus
W34	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive 1 – minus
W33	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive 1 – plus
U34	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit 0 – minus
U33	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit 0 – plus
V34	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit 1 – minus
V33	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit 1 – plus
AM11	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
AL10	PMIC_SPMI_DATA	PX_0	B	Slave and PBUS interface for PMICs – data
AL12	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
AD5	QLINK_CLK_M	–	AO	QLink clock – minus
AD4	QLINK_CLK_P	–	AO	QLink clock – plus
AF5	QLINK_DL0_M	–	AI	QLink downlink lane 0 – minus
AF4	QLINK_DL0_P	–	AI	QLink downlink lane 0 – plus
AE5	QLINK_UDL1_M	–	AI	QLink uplink/downlink lane 1 – minus
AE4	QLINK_UDL1_P	–	AI	QLink uplink/downlink lane 1 – plus
AC4	QLINK_UDL2_M	–	AI	QLink uplink/downlink lane 2 – minus

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AC5	QLINK_UDL2_P	–	AI	QLink uplink/downlink lane 2 – plus
AG5	QLINK_UL0_M	–	AO	QLink uplink lane 0 – minus
AG4	QLINK_UL0_P	–	AO	QLink uplink lane 0 – plus
G1	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-die clocking
N34	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
J1	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
AK10	RESIN_N	PX_0	DI	Reset input
AM12	RESOUT_N	PX_3	DO	Reset output
AG34	RF_XO_CLK	PX_3	DI	WLAN reference clock
N30	SDC2_CLK	PX_2	DO	Secure digital controller 2 clock
N31	SDC2_CMD	PX_2	B	Secure digital controller 2 command
M31	SDC2_DATA_0	PX_2	B	Secure digital controller 2 data bit 0
M30	SDC2_DATA_1	PX_2	B	Secure digital controller 2 data bit 1
P31	SDC2_DATA_2	PX_2	B	Secure digital controller 2 data bit 2
P30	SDC2_DATA_3	PX_2	B	Secure digital controller 2 data bit 3
AK11	SLEEP_CLK	PX_3	DI	Sleep clock
AM8	SP_ARI_POWER_ ALARM	PX_13	DI	Battery removal alarm for secure processor unit
AM23	SRST_N	PX_3	DI-PU	JTAG reset for debug
AK22	TCK	PX_3	DI-PU	JTAG clock input
AL22	TDI	PX_3	DI-PU:nppdkp	JTAG data input
AM21	TDO	PX_3	DO-Z	JTAG data output
AM22	TMS	PX_3	DI-PU:nppdkp	JTAG mode select input
AL23	TRST_N	PX_3	DI-PD:nppukp	JTAG reset
R2	UFS1_RESET	PX_10	DO-Z PD:nppukp	UFS reset
T4	UFS1_L0_RXM	–	AI	UFS receive lane 0 – minus
T5	UFS1_L0_RXP	–	AI	UFS receive lane 0 – plus
P4	UFS1_L0_TXM	–	AO	UFS transmit lane 0 – minus
P5	UFS1_L0_TXP	–	AO	UFS transmit lane 0 – plus
U4	UFS1_L1_RXM	–	AI	UFS receive lane 1 – minus
U5	UFS1_L1_RXP	–	AI	UFS receive lane 1 – plus
N4	UFS1_L1_TXM	–	AO	UFS transmit lane 1 – minus
N5	UFS1_L1_TXP	–	AO	UFS transmit lane 1 – plus
R3	UFS1_REF_CLK	PX_10	DO-Z PD:nppukp	UFS reference clock

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
D5	USB1_HS_DM	–	AI, AO	USB high-speed 1 data – minus
D4	USB1_HS_DP	–	AI, AO	USB high-speed 1 data – plus
F1	USB1_REXT	–	AI, AO	External resistor for USB high-speed 1
E4	USB1_SS_RX0_M	–	AI	USB super-speed 1 receive 0 – minus
E5	USB1_SS_RX0_P	–	AI	USB super-speed 1 receive 0 – plus
K5	USB1_SS_RX1_M	–	AI	USB super-speed 1 receive 1 – minus
K4	USB1_SS_RX1_P	–	AI	USB super-speed 1 receive 1 – plus
G4	USB1_SS_TX0_M	–	AO	USB super-speed 1 transmit 0 – minus
G5	USB1_SS_TX0_P	–	AO	USB super-speed 1 transmit 0 – plus
H5	USB1_SS_TX1_M	–	AO	USB super-speed 1 transmit 1 – minus
H4	USB1_SS_TX1_P	–	AO	USB super-speed 1 transmit 1 – plus
C5	USB2_HS_DM	–	AI, AO	USB high-speed 2 data – minus
B5	USB2_HS_DP	–	AI, AO	USB high-speed 2 data – plus
C1	USB2_REXT	–	AI, AO	External resistor for USB high-speed 2
C7	USB2_SS_RX_M	–	AI	USB super-speed 2 receive – minus
B7	USB2_SS_RX_P	–	AI	USB super-speed 2 receive – plus
C6	USB2_SS_TX_M	–	AO	USB super-speed 2 transmit – minus
B6	USB2_SS_TX_P	–	AO	USB super-speed 2 transmit – plus
Y30	WLAN1_ADC_I_N	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase minus
Y31	WLAN1_ADC_I_P	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase plus
AA31	WLAN1_ADC_Q_N	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature minus
AA30	WLAN1_ADC_Q_P	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature plus
AB34	WLAN1_DAC_RST	PX_3	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
AD33	WLAN2_ADC_I_N	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase minus
AD32	WLAN2_ADC_I_P	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase plus
AC32	WLAN2_ADC_Q_N	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature minus
AC33	WLAN2_ADC_Q_P	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature plus
AD34	WLAN2_DAC_RST	PX_3	AI, AO	WLAN chain 2 digital-to-analog converter external resistor
A18	ZQ0_0	PX_3	AI	LPDDR4X ZQ resistor for lower x16 memory in rank 0

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Table 2-2 Bottom pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AN18	ZQ0_3	PX_3	AI	LPDDR4X ZQ resistor for upper x16 memory in rank 0
A19	ZQ1_0	PX_3	AI	LPDDR4X ZQ resistor for lower x16 memory in rank 1
AN17	ZQ1_3	PX_3	AI	LPDDR4X ZQ resistor for upper x16 memory in rank 1

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function–carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM8150/SM8150P GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

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NOTE: Click the following link to download the pin assignment spreadsheet (*SM8150 Pin Assignment and GPIO Configuration Spreadsheet* (80-PD867-1A)) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PD867-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-3 Bottom pin descriptions – GPIO pins

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
B3	GPIO_0 [1]		3	PD:nppukp	Configurable I/O	N
		QUP_L0[0]			QUP 0, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
B2	GPIO_1		3	PD:nppukp	Configurable I/O	N
		QUP_L1[0]			QUP 0, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
C2	GPIO_2		3	PD:nppukp	Configurable I/O	N
		QUP_L2[0]			QUP 0, lane 2: SPI_CLK/UART_TX	
C3	GPIO_3		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[0]			QUP 0, lane 3: SPI_CS0/UART_RX	
AB1	GPIO_4		3	PD:nppukp	Configurable I/O	N
		QUP_L2[6]			QUP 6, lane 2: SPI_CLK/UART_TX	
AA2	GPIO_5		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[6]			QUP 6, lane 3: SPI_CS0/UART_RX	
AA1	GPIO_6		3	PD:nppukp	Configurable I/O	N
		QUP_L0[6]			QUP 6, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QUP_L6_0_CS			QUP 0, lane 6: SPI_CS3	
AA3	GPIO_7		3	PD:nppukp	Configurable I/O	N
		QUP_L1[6]			QUP 6, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QUP_L5_0_CS			QUP 0, lane 5: SPI_CS2	
P32	GPIO_8		3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA			MDP vertical sync – primary A	
AL32	GPIO_9		3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA			MDP vertical sync – secondary A	
		QUP_L0[10]			QUP 10, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AL33	GPIO_10		3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_E			MDP vertical sync – external	
		DP_HOT_PLUG_DETECT			DisplayPort hot plug detect	
		QUP_L1[10]			QUP 10, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
AL34	GPIO_11		3	PD:nppukp	Configurable I/O	N
		QUP_L2[10]			QUP 10, lane 2: SPI_CLK/UART_TX	
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
AM33	GPIO_12		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[10]			QUP 10, lane 3: SPI_CS0/UART_RX	
J34	GPIO_13		3	PD:nppukp	Configurable I/O	N
		CAM_MCLK0			Camera master clock 0	
		QDSS_GPIO_TRACEDATA_LOCB[0]			QDSS trace data 0 B	
K34	GPIO_14		3	PD:nppukp	Configurable I/O	N
		CAM_MCLK1			Camera master clock 1	
		QDSS_GPIO_TRACEDATA_LOCB[1]			QDSS trace data 1 B	
J33	GPIO_15		3	PD:nppukp	Configurable I/O	N
		CAM_MCLK2			Camera master clock 2	
		QDSS_GPIO_TRACEDATA_LOCB[2]			QDSS trace data 2 B	
K33	GPIO_16		3	PD:nppukp	Configurable I/O	N
		CAM_MCLK3			Camera master clock 3	
		QDSS_GPIO_TRACEDATA_LOCB[3]			QDSS trace data 3 B	
N32	GPIO_17		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Dedicated camera control interface I^2C 0 serial data	
		QDSS_GPIO_TRACEDATA_LOCB[4]			QDSS trace data 4 B	
N33	GPIO_18		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Dedicated camera control interface I^2C 0 clock	
		QDSS_GPIO_TRACEDATA_LOCB[5]			QDSS trace data 5 B	
P34	GPIO_19		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Dedicated camera control interface I^2C 1 serial data	
		QDSS_GPIO_TRACEDATA_LOCB[6]			QDSS trace data 6 B	
P33	GPIO_20		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Dedicated camera control interface I^2C 1 clock	
		QDSS_GPIO_TRACEDATA_LOCB[7]			QDSS trace data 7 B	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
D22	GPIO_21		3	PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera control interface timer 0	
		GCC_GP2_CLK_MIRB			Global general-purpose clock 2 B	
		QDSS_GPIO_TRACEDATA_LOCB[8]			QDSS trace data 8 B	
B23	GPIO_22		3	PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera control interface timer 1	
		GCC_GP3_CLK_MIRB			Global general-purpose clock 3 B	
		QDSS_GPIO_TRACECLK_LOCB			QDSS trace clock B	
C23	GPIO_23		3	PD:nppukp	Configurable I/O	N
		CCI_TIMER2			Camera control interface timer 2	
		QUP_L0[18]			QUP 18, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QDSS_GPIO_TRACEDATA_LOCB[9]			QDSS trace data 9 B	
D23	GPIO_24		3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3			Camera control interface timer 3	
		CCI_ASYNC_IN1			Camera control interface async 1	
		QUP_L1[18]			QUP 18, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QDSS_GPIO_TRACEDATA_LOCB[10]			QDSS trace data 10 B	
D24	GPIO_25		3	PD:nppukp	Configurable I/O	N
		CCI_TIMER4			Camera control interface timer 4	
		CCI_ASYNC_IN2			Camera control interface async 2	
		QUP_L2[18]			QUP 18, lane 2: SPI_CLK/UART_TX	
		QDSS_GPIO_TRACEDATA_LOCB[11]			QDSS trace data 11 B	
C24	GPIO_26		3	PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN0			Camera control interface async 0	
		QUP_L3[18]			QUP 18, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_LOCB[12]			QDSS trace data 12 B	
B11	GPIO_27		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[15]			QUP 15, lane 0: SPI_MISO/UART_ CTS/I2C_SDA	
		GP_MN			General-purpose M/N:D counter output	
		QDSS_GPIO_TRACEDATA_LOCB[15]			QDSS trace data 15 B	
C11	GPIO_28		3	PD:nppukp	Configurable I/O	Y
		QUP_L1[15]			QUP 15, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QDSS_GPIO_TRACECTL_LOCB			QDSS trace control B	
B12	GPIO_29		3	PD:nppukp	Configurable I/O	N
		QUP_L2[15]			QUP 15, lane 2: SPI_CLK/UART_TX	
		QDSS_GPIO_TRACEDATA_LOCB[13]			QDSS trace data 13 B	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
C12	GPIO_30		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[15]			QUP 15, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_LOCB[14]			QDSS trace data 14 B	
AJ31	GPIO_31		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Dedicated camera control interface I^2C 2 serial data	
		QDSS_GPIO_TRACEDATA_LOCA[13]			QDSS trace data 13 A	
AJ32	GPIO_32		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Dedicated camera control interface I^2C 2 clock	
		QDSS_GPIO_TRACEDATA_LOCA[0]			QDSS trace data 0 A	
AJ33	GPIO_33		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA3			Dedicated camera control interface I^2C 3 serial data	
		QUP_L5_9_CS			QUP 9, lane 5: SPI_CS2	
		QDSS_GPIO_TRACEDATA_LOCA[1]			QDSS trace data 1 A	
AH31	GPIO_34		3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL3			Dedicated camera control interface I^2C 3 clock	
		QUP_L6_9_CS			QUP 9, lane 6: SPI_CS3	
AL30	GPIO_35		3	PD:nppukp	Configurable I/O	N
		PCIE0_RST_N (optional)			PCIe 0 reset [2]	
AK30	GPIO_36		3	PU:nppdkp	Configurable I/O	Y
		PCIE0_CLKREQ_N			PCIe 0 clock request	
AL29	GPIO_37		3	PD:nppukp	Configurable I/O	Y
		QUP_L4_9_CS			QUP 9, lane 4: SPI_CS1	
K2	GPIO_38		3	PD:nppukp	Configurable I/O	Y
		USB_PHY_PS			USB PHY port select	
AK31	GPIO_39		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[9]			QUP 9, lane 0: SPI_MISO/ UART_CTS/I2C_SDA/I3C_SDA	
		QDSS_GPIO_TRACEDATA_LOCA[6]			QDSS trace data 6 A	
AL31	GPIO_40		3	PD:nppukp	Configurable I/O	N
		QUP_L1[9]			QUP 9, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL/I3C_SCL	
		QDSS_GPIO_TRACEDATA_LOCA[7]			QDSS trace data 7 A	
AM31	GPIO_41		3	PD:nppukp	Configurable I/O	Y
		QUP_L2[9]			QUP 9, lane 2: SPI_CLK/UART_TX	
		QDSS_GPIO_TRACEDATA_LOCA[14]			QDSS trace data 14 A	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AN31	GPIO_42		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[9]			QUP 9, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_LOCA[15]			QDSS trace data 15 A	
C21	GPIO_43		3	PD:nppukp	Configurable I/O	N
		QUP_L0[13]			QUP 13, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
D21	GPIO_44		3	PD:nppukp	Configurable I/O	N
		QUP_L1[13]			QUP 13, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
B22	GPIO_45		3	PU:nppdkp	Configurable I/O	N
		QUP_L2[13]			QUP 13, lane 2: SPI_CLK/UART_TX	
		QDSS_CTI_TRIG0_OUT_MIRB			QDSS trigger output 0 B	
C22	GPIO_46		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[13]			QUP 13, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG0_IN_MIRB			QDSS trigger input 0 B	
C8	GPIO_47		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[14]			QUP 14, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QDSS_GPIO_TRACEDATA_LOCA[12]			QDSS trace data 12 A	
B8	GPIO_48		3	PD:nppukp	Configurable I/O	Y
		QUP_L1[14]			QUP 14, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QDSS_GPIO_TRACEDATA_LOCA[10]			QDSS trace data 10 A	
C10	GPIO_49		3	PD:nppukp	Configurable I/O	Y
		QUP_L2[14]			QUP 14, lane 2: SPI_CLK/UART_TX	
		QDSS_CTI_TRIG1_OUT_MIRA			QDSS trigger output 0 A	
B10	GPIO_50		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[14]			QUP 14, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG1_IN_MIRA			QDSS trigger input 0 A	
AL2	GPIO_51		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[4]			QUP 4, lane 0: SPI_MISO/ UART_CTS/I2C_SDA/I3C_SDA	
AK3	GPIO_52		3	PD:nppukp	Configurable I/O	N
		QUP_L1[4]			QUP 4, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL/I3C_SCL	
AK2	GPIO_53		3	PD:nppukp	Configurable I/O	Y
		QUP_L2[4]			QUP 4, lane 2: SPI_CLK/UART_TX	
AJ3	GPIO_54		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[4]			QUP 4, lane 3: SPI_CS0/UART_RX	
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
K1	GPIO_55		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[17]			QUP 17, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QUP_L2[19]			QUP 19, lane 2: SPI_CLK/UART_TX	
L1	GPIO_56		3	PD:nppukp	Configurable I/O	Y
		QUP_L1[17]			QUP 17, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QUP_L3[19]			QUP 19, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG1_IN_MIRB			QDSS trigger input 1 B	
L2	GPIO_57		3	PD:nppukp	Configurable I/O	N
		QUP_L2[17]			QUP 17, lane 2: SPI_CLK/UART_TX	
		QUP_L0[19]			QUP 19, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QDSS_CTI_TRIG0_OUT_MIRA			QDSS trigger output 0 A	
L3	GPIO_58		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[17]			QUP 17, lane 3: SPI_CS0/UART_RX	
		QUP_L1[19]			QUP 19, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
		QDSS_CTI_TRIG1_OUT_MIRB			QDSS trigger output 1 B	
		QDSS_CTI_TRIG0_IN_MIRA			QDSS trigger input 0 A	
Y3	GPIO_59		3	PD:nppukp	Configurable I/O	N
		QUP_L4_0_CS			QUP 0, lane 4: SPI_CS1	
AK6	GPIO_60		3	PD:nppukp	Configurable I/O	Y
		GPS_TX_AGGRESSOR_MIRA			Tx level may degrade GNSS receiver (A)	
AH2	GPIO_61		3	PD:nppukp	Configurable I/O	Y
		QLINK_REQUEST			QLink request	
AJ2	GPIO_62		3	PD:nppukp	Configurable I/O	N
		QLINK_ENABLE			QLink enable	
AJ4	GPIO_63		3	PD:nppukp	Configurable I/O	N
		WMSS_RESET_N			WTR/SDR modem subsystem reset output	
AK4	GPIO_64		3	PD:nppukp	Configurable I/O	N
		GRFC8			Generic RF controller bit 8	
		BOOT_CONFIG[2]			Boot configuration bit 2 [1]	
AL6	GPIO_65		3	PD:nppukp	Configurable I/O	N
		GRFC9			Generic RF controller bit 9	
		BOOT_CONFIG[0]			Boot configuration bit 0 [1]	
AK5	GPIO_66		3	PD:nppukp	Configurable I/O	N
		GRFC10			Generic RF controller bit 10	

Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AL7	GPIO_67		3	PD:nppukp	Configurable I/O	N
		GRFC11			Generic RF controller bit 11	
		BOOT_CONFIG[4]			Boot configuration bit 4 [1]	
AJ5	GPIO_68		3	PD:nppukp	Configurable I/O	Y
		GRFC12			Generic RF controller bit 12	
		PA_INDICATOR_1_OR_2			PA transmit indicator	
		BOOT_CONFIG[1]			Boot configuration bit 1 [1]	
AN6	GPIO_69		3	PD:nppukp	Configurable I/O	N
		MSS_LTE_COXM_TXD			UART Tx for LTE coexistence	
		BOOT_CONFIG[3]			Boot configuration bit 3 [1]	
AM6	GPIO_70		3	PD:nppukp	Configurable I/O	Y
		MSS_LTE_COXM_RXD			UART Rx for LTE coexistence	
AG2	GPIO_71		3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front end 0 interface data	
		GRFC0			Generic RF controller bit 0	
		BOOT_CONFIG[10]			Boot configuration bit 10 [1]	
AH1	GPIO_72		3	PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front end 0 interface clock	
		GRFC1			Generic RF controller bit 1	
AL1	GPIO_73		3	PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front end 1 interface data	
		GRFC2			Generic RF controller bit 2	
		BOOT_CONFIG[11]			Boot configuration bit 11 [1]	
AK1	GPIO_74		3	PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front end 1 interface clock	
		GRFC3			Generic RF controller bit 3	
AF2	GPIO_75		3	PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front end 2 interface data	
		GRFC4			Generic RF controller bit 4	
AG1	GPIO_76		3	PD:nppukp	Configurable I/O	Y
		RFFE2_CLK			RF front end 2 interface clock	
		GRFC5			Generic RF controller bit 5	
		GPS_TX_AGGRESSOR_MIRD			Tx level may degrade GNSS receiver (D)	
AE2	GPIO_77		3	PD:nppukp	Configurable I/O	Y
		RFFE3_DATA			RF front end 3 interface data	
		GRFC6			Generic RF controller bit 6	
		GPS_TX_AGGRESSOR_MIRE			Tx level may degrade GNSS receiver (E)	
		BOOT_CONFIG[9]			Boot configuration bit 9 [1]	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AE1	GPIO_78		3	PD:nppukp	Configurable I/O	N
		RFFE3_CLK			RF front end 3 interface clock	
		GRFC7			Generic RF controller bit 7	
AD2	GPIO_79		3	PD:nppukp	Configurable I/O	N
		GRFC13			Generic RF controller bit 13	
AD1	GPIO_80		3	PD:nppukp	Configurable I/O	N
		GRFC14			Generic RF controller bit 14	
AB2	GPIO_81		3	PD:nppukp	Configurable I/O	Y
		GRFC15			Generic RF controller bit 15	
		GPS_TX_AGGRESSOR_MIRB			Tx level may degrade GNSS receiver (B)	
		QUP_L4_1_CS			QUP 1, lane 4: SPI_CS1	
		MDP_VSYNC_P_MIRB			MDP vertical sync – primary B	
AC2	GPIO_82		3	PD:nppukp	Configurable I/O	N
		GRFC16			Generic RF controller bit 16	
		GPS_TX_AGGRESSOR_MIRC			Tx level may degrade GNSS receiver (C)	
		QUP_L5_1_CS			QUP 1, lane 5: SPI_CS2	
		MDP_VSYNC_S_MIRB			MDP vertical sync – secondary B	
AM32	GPIO_83		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[12]			QUP 12, lane 0: SPI_MISO/UART_ CTS/I2C_SDA	
		QUP_L3[16]			QUP 16, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_LOCA[2]			QDSS trace data 2 A	
AN32	GPIO_84		3	PD:nppukp	Configurable I/O	N
		QUP_L1[12]			QUP 12, lane 1: SPI_MOSI/UART_ RFR/I2C_SCL	
		QUP_L2[16]			QUP 16, lane 2: SPI_CLK/UART_TX	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
AK33	GPIO_85		3	PD:nppukp	Configurable I/O	N
		QUP_L2[12]			QUP 12, lane 2: SPI_CLK/UART_TX	
		QUP_L1[16]			QUP 16, lane 1: SPI_MOSI/UART_ RFR/I2C_SCL	
AK32	GPIO_86		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[12]			QUP 12, lane 3: SPI_CS0/UART_RX	
		QUP_L0[16]			QUP 16, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
C9	GPIO_87		3	PD:nppukp	Configurable I/O	Y
J32	GPIO_88		3	PD:nppukp	Configurable I/O	Y
		TSIF1_CLK			Transport stream interface 1 clock	
		QUP_L0[8]			QUP 8, lane 0: SPI_MISO/ UART_CTS/I2C_SDA/I3C_SDA	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
K32	GPIO_89		3	PD:nppukp	Configurable I/O	N
		TSIF1_EN			Transport stream interface 1 enable	
		QUP_L1[8]			QUP 8, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL/I3C_SCL	
L32	GPIO_90		3	PD:nppukp	Configurable I/O	Y
		TSIF1_DATA			Transport stream interface 1 data	
		QUP_L2[8]			QUP 8, lane 2: SPI_CLK/UART_TX	
		SDC4_CMD			Secure digital controller 4 command	
M32	GPIO_91		3	PD:nppukp	Configurable I/O	Y
		TSIF1_SYNC			Transport stream interface 1 sync	
		QUP_L3[8]			QUP 8, lane 3: SPI_CS0/UART_RX	
		SDC4_DATA[3]			Secure digital controller 4 data bit 3	
L33	GPIO_92		3	PD:nppukp	Configurable I/O	N
		TSIF2_CLK			Transport stream interface 2 clock	
		QUP_L2[11]			QUP 11, lane 2: SPI_CLK/UART_TX	
		SDC4_CLK			Secure digital controller 4 clock	
M33	GPIO_93		3	PD:nppukp	Configurable I/O	Y
		TSIF2_EN			Transport stream interface 2 enable	
		QUP_L3[11]			QUP 11, lane 3: SPI_CS0/UART_RX	
		SDC4_DATA[2]			Secure digital controller 4 clock data bit 2	
L34	GPIO_94		3	PD:nppukp	Configurable I/O	N
		TSIF2_DATA			Transport stream interface 2 data	
		QUP_L0[11]			QUP 11, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		SDC4_DATA[1]			Secure digital controller 4 clock data bit 1	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
L31	GPIO_95		3	PD:nppukp	Configurable I/O	Y
		TSIF2_SYNC			Transport stream interface 2 sync	
		QUP_L1[11]			QUP 11, lane 1: SPI_MOSI/UART_ RFR/I2C_SCL	
		SDC4_DATA[0]			Secure digital controller 4 data bit 0	
		QUP_L4_8_CS			QUP 8, lane 4: SPI_CS1	
AK34	GPIO_96		3	PD:nppukp	Configurable I/O	Y
		TSIF2_ERROR			Transport stream interface 2 error	
		QUP_L5_8_CS			QUP 8, lane 5: SPI_CS2	
AJ30	GPIO_97		3	PD:nppukp	Configurable I/O	Y
		SD_WRITE_PROTECT			Secure digital card write protection	
		TSIF1_ERROR			Transport stream interface 1 error	
		QUP_L6_8_CS			QUP 8, lane 6: SPI_CS3	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
G2	GPIO_98		3	PD:nppukp	Configurable I/O	N
		QUP_L0[7]			QUP 7, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
H1	GPIO_99		3	PD:nppukp	Configurable I/O	N
		QUP_L1[7]			QUP 7, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
H2	GPIO_100		3	PD:nppukp	Configurable I/O	N
		QUP_L2[7]			QUP 7, lane 2: SPI_CLK/UART_TX	
J2	GPIO_101		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[7]			QUP 7, lane 3: SPI_CS0/UART_RX	
AM30	GPIO_102		3	PD:nppukp	Configurable I/O	N
		PCIE1_RST_N (optional)			PCIe 1 reset [2]	
AN30	GPIO_103		3	PU:nppdkp	Configurable I/O	Y
		PCIE1_CLKREQ_N			PCIe 1 clock request	
AF33	GPIO_104		3	PD:nppukp	Configurable I/O	Y
AL25	GPIO_105		6	PD:nppukp	Configurable I/O	N
		UIM2_DATA			UIM2 data (dual voltage)	
AL26	GPIO_106		6	PD:nppukp	Configurable I/O	N
		UIM2_CLK			UIM2 clock (dual voltage)	
AM25	GPIO_107		6	PD:nppukp	Configurable I/O	N
		UIM2_RESET			UIM2 reset (dual voltage)	
AM26	GPIO_108		3	PD:nppukp	Configurable I/O	Y
		UIM2_PRESENT			UIM2 presence detection	
AL27	GPIO_109		5	PD:nppukp	Configurable I/O	N
		UIM1_DATA			UIM1 data (dual voltage)	
AL28	GPIO_110		5	PD:nppukp	Configurable I/O	N
		UIM1_CLK			UIM1 clock (dual voltage)	
AM27	GPIO_111		5	PD:nppukp	Configurable I/O	N
		UIM1_RESET			UIM1 reset (dual voltage)	
AM28	GPIO_112		3	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT			UIM1 presence detection	
AM29	GPIO_113		3	PD:nppukp	Configurable I/O	Y
		UIM_BATT_ALARM			UIM battery alarm	
Y1	GPIO_114		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[1]			QUP 1, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
W1	GPIO_115		3	PD:nppukp	Configurable I/O	N
		QUP_L1[1]			QUP 1, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
W2	GPIO_116		3	PD:nppukp	Configurable I/O	N
		QUP_L2[1]			QUP 1, lane 2: SPI_CLK/UART_TX	
W3	GPIO_117		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[1]			QUP 1, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_LOCA[3]			QDSS trace data 3 A	
V4	GPIO_118		3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[4]			QDSS trace data 4 A	
AA5	GPIO_119		3	PD:nppukp	Configurable I/O	Y
		QUP_L2[5]			QUP 5, lane 2: SPI_CLK/UART_TX	
		QDSS_GPIO_TRACEDATA_LOCA[5]			QDSS trace data 5 A	
AA4	GPIO_120		3	PD:nppukp	Configurable I/O	Y
		QUP_L3[5]			QUP 5, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACECTL_LOCA			QDSS trace control A	
Y4	GPIO_121		3	PD:nppukp	Configurable I/O	Y
		QUP_L0[5]			QUP 5, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
		QDSS_GPIO_TRACECLK_LOCA			QDSS trace clock A	
Y2	GPIO_122		3	PD:nppukp	Configurable I/O	Y
		QUP_L1[5]			QUP 5, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
AL4	GPIO_123		3	PD:nppukp	Configurable I/O	Y
		QUP_L6_1_CS			QUP 1, lane 6: SPI_CS3	
AL5	GPIO_124		3	PD:nppukp	Configurable I/O	Y
AK13	GPIO_125		3	PD:nppukp	Configurable I/O	Y
T1	GPIO_126		3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_SCK/PCM2_CLK			Secondary MI2S clock	
		QUP_L0[2]			QUP 2, lane 0: SPI_MISO/ UART_CTS/I2C_SDA	
U2	GPIO_127		3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_WS/PCM2_SYNC			Secondary MI2S serial data word select	
		QUP_L1[2]			QUP 2, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL	
U1	GPIO_128		3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_DATA0/PCM2_DIN			Secondary MI2S serial data channel 0	
		QUP_L2[2]			QUP 2, lane 2: SPI_CLK/UART_TX	
V2	GPIO_129		3	PD:nppukp	Configurable I/O	Y
		SEC_MI2S_DATA1/PCM2_DOUT			Secondary MI2S serial data channel 1	
		QUP_L3[2]			QUP 2, lane 3: SPI_CS0/UART_RX	
V5	GPIO_130		3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_MCLK			Secondary MI2S master clock	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
D2	GPIO_131		3	PD:nppukp	Configurable I/O	N
		TER_MI2S_DATA1/PCM3_DOUT			Tertiary MI2S serial data channel 1	
		GCC_GP1_CLK_MIRB			Global general-purpose clock 1 B	
D1	GPIO_132		3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_MCLK			Tertiary MI2S master clock	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
		QDSS_GPIO_TRACEDATA_LOCA[11]			QDSS trace data 11 A	
E2	GPIO_133		3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_SCK/PCM3_CLK			Tertiary MI2S clock	
		QDSS_GPIO_TRACEDATA_LOCA[8]			QDSS trace data 8 A	
E1	GPIO_134		3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_WS/PCM3_SYNC			Tertiary MI2S serial data word select	
		QDSS_GPIO_TRACEDATA_LOCA[9]			QDSS trace data 9 A	
F2	GPIO_135		3	PD:nppukp	Configurable I/O	N
		TER_MI2S_DATA0/PCM3_DIN			Tertiary MI2S serial data channel 0	
AL3	GPIO_136		3	PD:nppukp	Configurable I/O	Y
		QUA_MI2S_MCLK			Quaternary MI2S master clock	
		GCC_GP1_CLK_MIRA			Global general-purpose clock 1 A	
		FORCED_USB_BOOT			Forced USB boot [1]	
AM5	GPIO_137		3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_SCK/PCM4_CLK			Quaternary MI2S clock	
		GCC_GP2_CLK_MIRA			Global general-purpose clock 2 A	
AM4	GPIO_138		3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_WS/PCM4_SYNC			Quaternary MI2S serial data word select	
		GCC_GP3_CLK_MIRA			Global general-purpose clock 3 A	
AM3	GPIO_139		3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA0/PCM4_DIN			Quaternary MI2S serial data channel 0	
AM2	GPIO_140		3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA1/PCM4_DOUT			Quaternary MI2S serial data channel 1	
AN4	GPIO_141		3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA2			Quaternary MI2S serial data channel 2	
AN3	GPIO_142		3	PD:nppukp	Configurable I/O	Y
		QUA_MI2S_DATA3			Quaternary MI2S serial data channel 3	
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
V3	GPIO_143		3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_MCLK			Primary MI2S master clock	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
U3	GPIO_144		3	PD:nppukp	Configurable I/O	Y
		PRI_MI2S_SCK/PCM1_CLK			Primary MI2S clock	
		QUP_L0[3]			QUP 3, lane 0: SPI_MISO/ UART_CTS/I2C_SDA/I3C_SDA	
P3	GPIO_145		3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_WS/PCM1_SYNC			Primary MI2S word select	
		QUP_L1[3]			QUP 3, lane 1: SPI_MOSI/ UART_RFR/I2C_SCL/I3C_SCL	
P2	GPIO_146		3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_DATA0/PCM1_DIN			Primary MI2S serial data channel 0	
		QUP_L2[3]			QUP 3, lane 2: SPI_CLK/UART_TX	
T3	GPIO_147		3	PD:nppukp	Configurable I/O	Y
		PRI_MI2S_DATA1/PCM1_DOUT			Primary MI2S serial data channel 1	
		QUP_L3[3]			QUP 3, lane 3: SPI_CS0/UART_RX	
T2	GPIO_148		3	PD:nppukp	Configurable I/O	N
		QUIN_MI2S_MCLK			Quinary MI2S master clock	
		AUDIO_REF_CLK			Audio reference clock	
N1	GPIO_149		3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_CLK			Low-power audio SLIMbus clock	
		QUIN_MI2S_SCK/PCM5_CLK			Quinary MI^{2}S clock	
N3	GPIO_150		3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA0			Low-power audio SLIMbus data 0	
		QUIN_MI2S_DATA0/PCM5_DIN			Quinary MI^{2}S data 0	
N2	GPIO_151		3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_DATA1			Low-power audio SLIMbus data 1	
		QUIN_MI2S_WS/PCM5_SYNC			Quinary MI^{2}S word select	
P1	GPIO_152		3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA2			Low-power audio SLIMbus data 2	
		QUIN_MI2S_DATA1/PCM5_DOUT			Quinary MI^{2}S data 1	
M3	GPIO_153		3	PD:nppukp	Configurable I/O	Y
		BTFM_SLIMBUS_DATA			Bluetooth/FM SLIMbus data	
M2	GPIO_154		3	PD:nppukp	Configurable I/O	N
		BTFM_SLIMBUS_CLK			Bluetooth/FM SLIMbus clock	
AL20	GPIO_155		3	PD:nppukp	Configurable I/O	N
		SSC_0			SSC I/O 0 (power-on default)	
AL19	GPIO_156		3	PD:nppukp	Configurable I/O	N
		SSC_1			SSC I/O 1 (power-on default)	
AM19	GPIO_157		3	PD:nppukp	Configurable I/O	N
		SSC_2			SSC I/O 2 (power-on default)	

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Table 2-3 Bottom pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AM18	GPIO_158		3	PD:nppukp	Configurable I/O	N
		SSC_3			SSC I/O 3 (power-on default)	
AL18	GPIO_159		3	PD:nppukp	Configurable I/O	N
		SSC_4			SSC I/O 4 (power-on default)	
AL17	GPIO_160		3	PD:nppukp	Configurable I/O	N
		SSC_5			SSC I/O 5 (power-on default)	
AM16	GPIO_161		3	PD:nppukp	Configurable I/O	N
		SSC_6			SSC I/O 6 (power-on default)	
AL15	GPIO_162		3	PD:nppukp	Configurable I/O	N
		SSC_7			SSC I/O 7 (power-on default)	
AM15	GPIO_163		3	PD:nppukp	Configurable I/O	N
		SSC_8			SSC I/O 8 (power-on default)	
AL14	GPIO_164		3	PD:nppukp	Configurable I/O	N
		SSC_9			SSC I/O 9 (power-on default)	
AM17	GPIO_165		3	PD:nppukp	Configurable I/O	N
		SSC_10			SSC I/O 10 (power-on default)	
AL16	GPIO_166		3	PD:nppukp	Configurable I/O	N
		SSC_11			SSC I/O 11 (power-on default)	
AM14	GPIO_167		3	PD:nppukp	Configurable I/O	N
		SSC_12			SSC I/O 12 (power-on default)	
AL13	GPIO_168		3	PD:nppukp	Configurable I/O	N
		SSC_13			SSC I/O 13 (power-on default)	
AG33	GPIO_169		3	PD:nppukp	Configurable I/O	N
		WCSS1_BBD_RFA_CMD_CLK			WLAN chain 1 baseband command clock (WSI 2.0) – power-on default	
AG32	GPIO_170		3	PD:nppukp	Configurable I/O	N
		WCSS1_BBD_RFA_CMD_DATA			WLAN chain 1 baseband command data (WSI 2.0) – power-on default	
AG31	GPIO_171		3	PD:nppukp	Configurable I/O	N
		WCSS2_BBD_RFA_CMD_CLK			WLAN chain 2 baseband command clock (WSI 2.0) – power-on default	
AH34	GPIO_172		3	PD:nppukp	Configurable I/O	N
		WCSS2_BBD_RFA_CMD_DATA			WLAN chain 2 baseband command data (WSI 2.0) – power-on default	
AH33	GPIO_173		3	PD:nppukp	Configurable I/O	N
		WCSS_CXM_RFA_CMD_CLK			WLAN coexistence module command clock (WSI 1.0) – power-on default	
AH32	GPIO_174		3	PD:nppukp	Configurable I/O	N
		WCSS_CXM_RFA_CMD_DATA			WLAN coexistence module command data (WSI 1.0) – power-on default	

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1. The boot configuration function of this GPIO is only active at the time of boot, before RESOUT_N is deasserted. See the *SM8150 Pin Assignment and GPIO Configuration Spreadsheet* (80-PD867-1A) for detailed GPIO configurations.
2. PCIE0_RST_N / PCIE1_RST_N is a software implementation as bit bang on the same GPIO.

Table 2-4 Bottom pin descriptions – power-supply pins

Pin #	Pin name	Functional description
K13, L14, M13, N12, N13, N14, P13, R14, T13, U14, V13, W12	VDD_APC0	Power for Kryo Silver application processor
G8, H7, H9, H11, J8, J10, J12, K7, M7, N8, N10, P7, P9, P11, T7, V7, V9, V11, W8, W10	VDD_APC1	Power for Kryo Gold application processor
AC19, AC21, AC23, AC24, AC25, AC27, AC29, AE24, AG19, AG21, AG23, AG24, AG25, AG27, AG29	VDD_GFX	Power for graphics
AF18, AH18	VDD_LPI_MX_A	Power for low-power island circuits
AC30	VDD_LPI_MX_B	Power for low-power island circuits
AB8, AB10, AB12, AC9, AC11, AD8, AD12, AF8, AF10, AF12	VDD_MODEM	Power for modem circuits
AG15	VDD_QFPROM	Power for programming the QFPROM
AH16	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit
AE16, AE17, AF16	VDD_SSC_CX	Power for Snapdragon sensor core
H6	VDD_USB_HS_CORE	Power for USB high-speed (HS) core circuits
AA27, Y27, AA28, Y28	VDD_WCSS	Power for WCSS circuits
A7, A8, A20, A21, AN10, AN11, AN24, AN25	VDD1	Power for PoP DDR memory core – 1.8 V (top VDD2)
A10, A11, A12, A14, A15, A16, AN13, AN14, AN15, AN20, AN21, AN22	VDD2	Power for PoP DDR memory core – 1.2 V (top VDD2)
H13	VDDA_APC_CS_1P8	Power for application processor current-sensor 1.8 V circuits
F12	VDDA_CC_EBI01	Power for EBI0/EBI1 clock circuits
AH12	VDDA_CC_EBI23	Power for EBI2/EBI3 clock circuits
H28	VDDA_CSI_1P2	Power for MIPI CSI0/1/2/3 1.2 V circuits
K29	VDDA_CSI0_0P9	Power for MIPI CSI0 0.9 V circuits
J29	VDDA_CSI1_0P9	Power for MIPI CSI1 0.9 V circuits
H29	VDDA_CSI2_0P9	Power for MIPI CSI2 0.9 V circuits
G29	VDDA_CSI3_0P9	Power for MIPI CSI3 0.9 V circuits
E20	VDDA_DSI0_0P9	Power for MIPI DSI0 0.9 V circuits
E19	VDDA_DSI0_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V circuits
E21	VDDA_DSI1_0P9	Power for MIPI DSI1 0.9 V circuits

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Table 2-4 Bottom pin descriptions – power-supply pins (cont.)

Pin #	Pin name	Functional description
F22	VDDA_DSI1_PLL_0P9	Power for MIPI DSI1 PLL 0.9 V circuits
F20	VDDA_DSI_1P2	Power for MIPI DSI0/1 1.2 V circuits
F9, F10	VDDA_EBI0	Power for EBI0 PHY circuits
F23, F24	VDDA_EBI1	Power for EBI1 PHY circuits
AH9, AH10	VDDA_EBI2	Power for EBI2 PHY circuits
AH26, AH27	VDDA_EBI3	Power for EBI3 PHY circuits
AD18	VDDA_GFX_CS_1P8	Power for graphics current sensor 1.8 V circuits
F8	VDDA_HV_EBI0	Power for EBI0 PHY high-voltage circuits
F26	VDDA_HV_EBI1	Power for EBI1 PHY high-voltage circuits
AH7	VDDA_HV_EBI2	Power for EBI2 PHY high-voltage circuits
AH29	VDDA_HV_EBI3	Power for EBI3 PHY high-voltage circuits
V29	VDDA_PCIE1_CORE	Power for PCIE1 (2-lane) core circuits
V28	VDDA_PCIE1_PLL_1P2	Power for PCIE1 (2-lane) PLL 1.2 V circuits
U29	VDDA_PCIE0_CORE	Power for PCIE0 (1-lane) core circuits
U28	VDDA_PCIE0_PLL_1P2	Power for PCIE0 (1-lane) PLL 1.2 V circuits
F16	VDDA_PLL_HV_CC_EBI01	Power for EBI0/EBI1 PLL high-voltage circuits
AJ15	VDDA_PLL_HV_CC_EBI23	Power for EBI2/EBI3 PLL high-voltage circuits
AF7	VDDA_QLINK_HV_CK	Power for QLink high-voltage clock circuits
AD6	VDDA_QLINK_LV	Power for QLink low-voltage circuits
AE6	VDDA_QLINK_LV_CK	Power for QLink low-voltage clock circuits
P6	VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits
T6	VDDA_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits
AJ13	VDDA_SP_SENSOR	Power for secure processor unit sensors
L29	VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits
M6	VDDA_UFS1_1P2	Power for UFS 1.2 V circuits
M4	VDDA_UFS1_CORE	Power for UFS core circuits
M5		
M28	VDDA_REFGEN_1P2	Power for REFGEN circuits
F5	VDDA_USB_HS_1P8	Power for USB1/2 HS 1.8 V circuits
G6	VDDA_USB_HS_3P1	Power for USB1/2 HS 3.1 V circuits
F7	VDDA_USB2_SS_1P2	Power for USB2 SS 1.2 V circuits
F6	VDDA_USB2_SS_CORE	Power for USB2 SS core circuits
K6	VDDA_USB1_SS_DP_1P2	Power for USB1 SS and DP 1.2 V circuits
J4, J5	VDDA_USB1_SS_DP_ CORE	Power for USB1 SS and DP core circuits
Y29	VDDA_WCSS_ADCDAC_1	Power for WCSS ADC and DAC – chain 1

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Table 2-4 Bottom pin descriptions – power-supply pins (cont.)

Pin #	Pin name	Functional description
AC31	VDDA_WCSS_ADCDAC_2	Power for WCSS ADC and DAC – chain 2
AB29	VDDA_WCSS_PLL	Power for WCSS PLL circuits
AA13, AA15, AA19, AB14, AD14, AF14, G11, G13, G15, H16, H18, J19, K16, K18, L19, M16, M18, N19, P16, P18, R19, T16, T18, T28, U19, U23, U25, U27, V16, V18, W15, W19, Y14, Y16, Y18	VDDCX	Power for digital core circuits
D9	VDDIO_CK_EBI0	Power for EBI0 I/O clock circuits
E26	VDDIO_CK_EBI1	Power for EBI1 I/O clock circuits
AK8	VDDIO_CK_EBI2	Power for EBI2 I/O clock circuits
AK28	VDDIO_CK_EBI3	Power for EBI3 I/O clock circuits
E6, E7, E8, E9	VDDIO_EBI0	Power for EBI0 I/O memory circuits
E23, E24, E25, F25	VDDIO_EBI1	Power for EBI1 I/O memory circuits
AJ6, AJ7, AJ8, AJ9	VDDIO_EBI2	Power for EBI2 I/O memory circuits
AJ26, AJ27, AJ28, AJ29	VDDIO_EBI3	Power for EBI3 I/O memory circuits
H24, H26, J25, K24, K26, M24, M26, P24, P26, R25	VDDMM	Power for multimedia subsystem circuits
AA23, AA25, AB24, AE30, AF30, G17, G19, H20, H22, J21, K22, L21, M22, N7, N21, P22, R7, R21, T22, U21, V22, W21, W23, Y22, Y24	VDDMX	Power for on-chip memory
AK14	VDDPX_0	Power for pad group 0 – control signals
R4	VDDPX_10	Power for pad group 10 – UFS
U6	VDDPX_11	Power for pad group 11 – CXO pad
AG13	VDDPX_13	Power for pad group 13 – secure processor unit (SPU)
R29	VDDPX_2	Power for pad group 2 – SDC2 pads
AB3, AF31, AH3, AK12, AK18, AK20, D10, D25, F15, R31, R32, W4, W5	VDDPX_3	Power for pad group 3 – most I/O pads
AK24	VDDPX_5	Power for pad group 5 – UIM1 pads
AK25	VDDPX_6	Power for pad group 6 – UIM2 pads
R33	VDDPX_VBIAS_SDC	Reference voltage for SDC
AJ23	VDDPX_VBIAS_UIM	Reference voltage for UIM
A4, A5, A23, A24, AN7, AN8, AN27, AN28	VDDQ	Power for PoP DDR pads (top VDDQ)

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Table 2-5 Bottom pin descriptions – ground pins

Pin #	Pin name	Functional description
AA32, Y32, AB32, AB33, AA29, A1, A2, A3, A6, A9, A13, A17, A22, A25, A30, A31, A32, A33,A34, AA6, AA7, AA9, AA11, AA17, AA21, AA33, AA34, AB4, AB5, AB6, AB16, AB18, AB20, AB22,AB26, AB28, AB30, AB31, AC1, AC3, AC6, AC7, AC13, AC15, AC17, AC20, AC26, AC28, AC34, AD3, AD10, AD16, AD24, AD30, AD31, AE7, AE9, AE11, AE13, AE15, AE31, AE32, AE33, AE34, AF1, AF3, AF6, AF24, AF32, AF34, AG3, AG7, AG9, AG11, AG17, AG20, AG26, AG28, AG30, AH4, AH5, AH6, AH8, AH14, AH20, AH22, AH24, AH25, AH28, AH30, AJ1, AJ10, AJ11, AJ17, AJ19, AJ21, AJ25, AJ34, AK7, AK16, AK19, AK23, AK26, AK29, AL8, AL11, AL21, AM1, AM7, AM10, AM13, AM20, AM34, AN1, AN2, AN5, AN9, AN12, AN16, AN19, AN23, AN26, AN29, AN33, AN34, B1, B4, B21, B25, B28, B29, B34, C4, C13, C14, C17, C18, C25, C30, C33, C34, D3, D6, D7, D8, D11, D12, D26, E3, E10, E11, E13, E15, E17, E22, E29, E30, F3, F4, F14, F18, F33, F34, G3, G7, G9, G21, G23, G25, G27, G30, H3, H8, H10, H12, H14, H32, H33, H34, J6, J9, J11, J13, J15, J17, J23, J27, J30, K3, K14, K20, K28, L6, L13,L15, L17, L23, L25, L27, L30, M1, M14, M20, M34, N6, N9, N11, N15, N17, N23, N25, N27, N29, P8, P10, P12, P14, P20, P28, R1, R5, R6, R13, R15, R17, R23, R27, R30, R34, T14, T20, T24, T26, T29, T32, U13, U15, U17, U32, V1, V6, V8, V10, V12, V14, V20, V24, V26, V32, W6, W7, W9, W11, W13, W17, W25, W27, W28, W29, W30, W31, W32, Y5, Y7, Y8, Y10, Y12, Y20, Y26	GND	Ground

Table 2-6 Bottom pin descriptions – DNC and NC pins

Pin #	Pin name	Functional description
M15, P15, Y9, U7, AG8, AG6, AD7, H19, AF17, H27, AG22, AC22, J7, AB21, AL24, AM24, B24, AK27, AK21, AE3, P29, J3, J31, H31, H30, K31, K30	DNC	Do not connect; connected internally, do not connect externally
M29	NC	No connect; not connected internally

2.3 Pin assignments – top

2.3.1 Pin map – top

The SM8150/SM8150P is available in the MPSP893; its top surface is similar to a 556 NSP. See Chapter 4 for package details and Section 2.2 for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3.

The text within Figure 2-3 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available and defined in Section 2.2.1.

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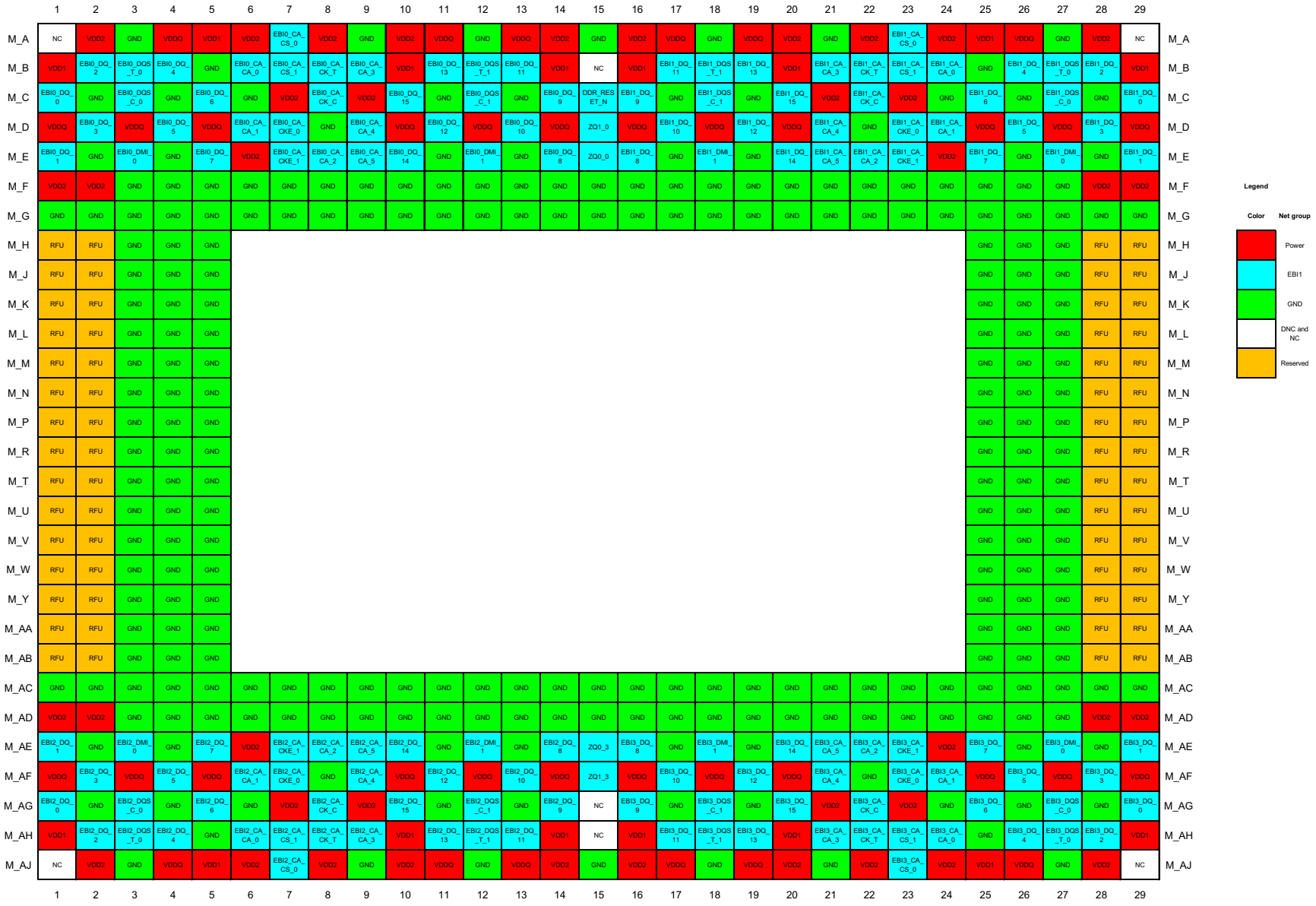

Figure 2-3 SM8150 top pin assignments

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2.3.2 Pin descriptions – top

Table 2-7 Top pin descriptions – primary pins

Pin #	Pin name	Pin voltage	Pin type	Functional description
M_C15	DDR_RESET_N	EBI	DO	LPDDR4X reset (shared by EBIs)
M_B6	EBI0_CA_CA_0	EBI	DO	EBI0 LPDDR4X command/address 0 bit 0
M_D6	EBI0_CA_CA_1	EBI	DO	EBI0 LPDDR4X command/address 0 bit 1
M_E8	EBI0_CA_CA_2	EBI	DO	EBI0 LPDDR4X command/address 0 bit 2
M_B9	EBI0_CA_CA_3	EBI	DO	EBI0 LPDDR4X command/address 0 bit 3
M_D9	EBI0_CA_CA_4	EBI	DO	EBI0 LPDDR4X command/address 0 bit 4
M_E9	EBI0_CA_CA_5	EBI	DO	EBI0 LPDDR4X command/address 0 bit 5
M_C8	EBI0_CA_CK_C	EBI	DO	EBI0 LPDDR4X differential clock (C)
M_B8	EBI0_CA_CK_T	EBI	DO	EBI0 LPDDR4X differential clock (T)
M_D7	EBI0_CA_CKE_0	EBI	DO	EBI0 LPDDR4X clock enable 0
M_E7	EBI0_CA_CKE_1	EBI	DO	EBI0 LPDDR4X clock enable 1
M_A7	EBI0_CA_CS_0	EBI	DO	EBI0 LPDDR4X chip select 0
M_B7	EBI0_CA_CS_1	EBI	DO	EBI0 LPDDR4X chip select 1
M_E3	EBI0_DMI_0	EBI	DO	EBI0 LPDDR4X data mask for byte 0
M_E12	EBI0_DMI_1	EBI	DO	EBI0 LPDDR4X data mask for byte 1
M_C1	EBI0_DQ_0	EBI	B	EBI0 LPDDR4X data bit 0
M_E1	EBI0_DQ_1	EBI	B	EBI0 LPDDR4X data bit 1
M_D13	EBI0_DQ_10	EBI	B	EBI0 LPDDR4X data bit 10
M_B13	EBI0_DQ_11	EBI	B	EBI0 LPDDR4X data bit 11
M_D11	EBI0_DQ_12	EBI	B	EBI0 LPDDR4X data bit 12
M_B11	EBI0_DQ_13	EBI	B	EBI0 LPDDR4X data bit 13
M_E10	EBI0_DQ_14	EBI	B	EBI0 LPDDR4X data bit 14
M_C10	EBI0_DQ_15	EBI	B	EBI0 LPDDR4X data bit 15
M_B2	EBI0_DQ_2	EBI	B	EBI0 LPDDR4X data bit 2
M_D2	EBI0_DQ_3	EBI	B	EBI0 LPDDR4X data bit 3
M_B4	EBI0_DQ_4	EBI	B	EBI0 LPDDR4X data bit 4
M_D4	EBI0_DQ_5	EBI	B	EBI0 LPDDR4X data bit 5
M_C5	EBI0_DQ_6	EBI	B	EBI0 LPDDR4X data bit 6
M_E5	EBI0_DQ_7	EBI	B	EBI0 LPDDR4X data bit 7
M_E14	EBI0_DQ_8	EBI	B	EBI0 LPDDR4X data bit 8
M_C14	EBI0_DQ_9	EBI	B	EBI0 LPDDR4X data bit 9
M_C3	EBI0_DQS_C_0	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 (C)

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Table 2-7 Top pin descriptions – primary pins (cont.)

Pin #	Pin name	Pin voltage	Pin type	Functional description
M_C12	EBI0_DQS_C_1	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 (C)
M_B3	EBI0_DQS_T_0	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 (T)
M_B12	EBI0_DQS_T_1	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 (T)
M_B24	EBI1_CA_CA_0	EBI	DO	EBI1 LPDDR4X command/address 0 bit 0
M_D24	EBI1_CA_CA_1	EBI	DO	EBI1 LPDDR4X command/address 0 bit 1
M_E22	EBI1_CA_CA_2	EBI	DO	EBI1 LPDDR4X command/address 0 bit 2
M_B21	EBI1_CA_CA_3	EBI	DO	EBI1 LPDDR4X command/address 0 bit 3
M_D21	EBI1_CA_CA_4	EBI	DO	EBI1 LPDDR4X command/address 0 bit 4
M_E21	EBI1_CA_CA_5	EBI	DO	EBI1 LPDDR4X command/address 0 bit 5
M_C22	EBI1_CA_CK_C	EBI	DO	EBI1 LPDDR4X differential clock (C)
M_B22	EBI1_CA_CK_T	EBI	DO	EBI1 LPDDR4X differential clock (T)
M_D23	EBI1_CA_CKE_0	EBI	DO	EBI1 LPDDR4X clock enable 0
M_E23	EBI1_CA_CKE_1	EBI	DO	EBI1 LPDDR4X clock enable 1
M_A23	EBI1_CA_CS_0	EBI	DO	EBI1 LPDDR4X chip select 0
M_B23	EBI1_CA_CS_1	EBI	DO	EBI1 LPDDR4X chip select 1
M_E27	EBI1_DMI_0	EBI	DO	EBI1 LPDDR4X data mask for byte 0
M_E18	EBI1_DMI_1	EBI	DO	EBI1 LPDDR4X data mask for byte 1
M_C29	EBI1_DQ_0	EBI	B	EBI1 LPDDR4X data bit 0
M_E29	EBI1_DQ_1	EBI	B	EBI1 LPDDR4X data bit 1
M_D17	EBI1_DQ_10	EBI	B	EBI1 LPDDR4X data bit 10
M_B17	EBI1_DQ_11	EBI	B	EBI1 LPDDR4X data bit 11
M_D19	EBI1_DQ_12	EBI	B	EBI1 LPDDR4X data bit 12
M_B19	EBI1_DQ_13	EBI	B	EBI1 LPDDR4X data bit 13
M_E20	EBI1_DQ_14	EBI	B	EBI1 LPDDR4X data bit 14
M_C20	EBI1_DQ_15	EBI	B	EBI1 LPDDR4X data bit 15
M_B28	EBI1_DQ_2	EBI	B	EBI1 LPDDR4X data bit 2
M_D28	EBI1_DQ_3	EBI	B	EBI1 LPDDR4X data bit 3
M_B26	EBI1_DQ_4	EBI	B	EBI1 LPDDR4X data bit 4
M_D26	EBI1_DQ_5	EBI	B	EBI1 LPDDR4X data bit 5
M_C25	EBI1_DQ_6	EBI	B	EBI1 LPDDR4X data bit 6
M_E25	EBI1_DQ_7	EBI	B	EBI1 LPDDR4X data bit 7
M_E16	EBI1_DQ_8	EBI	B	EBI1 LPDDR4X data bit 8
M_C16	EBI1_DQ_9	EBI	B	EBI1 LPDDR4X data bit 9

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Table 2-7 Top pin descriptions – primary pins (cont.)

Pin #	Pin name	Pin voltage	Pin type	Functional description
M_C27	EBI1_DQS_C_0	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 (C)
M_C18	EBI1_DQS_C_1	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 (C)
M_B27	EBI1_DQS_T_0	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 (T)
M_B18	EBI1_DQS_T_1	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 (T)
M_AH6	EBI2_CA_CA_0	EBI	DO	EBI2 LPDDR4X command/address 0 bit 0
M_AF6	EBI2_CA_CA_1	EBI	DO	EBI2 LPDDR4X command/address 0 bit 1
M_AE8	EBI2_CA_CA_2	EBI	DO	EBI2 LPDDR4X command/address 0 bit 2
M_AH9	EBI2_CA_CA_3	EBI	DO	EBI2 LPDDR4X command/address 0 bit 3
M_AF9	EBI2_CA_CA_4	EBI	DO	EBI2 LPDDR4X command/address 0 bit 4
M_AE9	EBI2_CA_CA_5	EBI	DO	EBI2 LPDDR4X command/address 0 bit 5
M_AG8	EBI2_CA_CK_C	EBI	DO	EBI2 LPDDR4X differential clock (C)
M_AH8	EBI2_CA_CK_T	EBI	DO	EBI2 LPDDR4X differential clock (T)
M_AF7	EBI2_CA_CKE_0	EBI	DO	EBI2 LPDDR4X clock enable 0
M_AE7	EBI2_CA_CKE_1	EBI	DO	EBI2 LPDDR4X clock enable 1
M_AJ7	EBI2_CA_CS_0	EBI	DO	EBI2 LPDDR4X chip select 0
M_AH7	EBI2_CA_CS_1	EBI	DO	EBI2 LPDDR4X chip select 1
M_AE3	EBI2_DMI_0	EBI	DO	EBI2 LPDDR4X data mask for byte 0
M_AE12	EBI2_DMI_1	EBI	DO	EBI2 LPDDR4X data mask for byte 1
M_AG1	EBI2_DQ_0	EBI	B	EBI2 LPDDR4X data bit 0
M_AE1	EBI2_DQ_1	EBI	B	EBI2 LPDDR4X data bit 1
M_AF13	EBI2_DQ_10	EBI	B	EBI2 LPDDR4X data bit 10
M_AH13	EBI2_DQ_11	EBI	B	EBI2 LPDDR4X data bit 11
M_AF11	EBI2_DQ_12	EBI	B	EBI2 LPDDR4X data bit 12
M_AH11	EBI2_DQ_13	EBI	B	EBI2 LPDDR4X data bit 13
M_AE10	EBI2_DQ_14	EBI	B	EBI2 LPDDR4X data bit 14
M_AG10	EBI2_DQ_15	EBI	B	EBI2 LPDDR4X data bit 15
M_AH2	EBI2_DQ_2	EBI	B	EBI2 LPDDR4X data bit 2
M_AF2	EBI2_DQ_3	EBI	B	EBI2 LPDDR4X data bit 3
M_AH4	EBI2_DQ_4	EBI	B	EBI2 LPDDR4X data bit 4
M_AF4	EBI2_DQ_5	EBI	B	EBI2 LPDDR4X data bit 5
M_AG5	EBI2_DQ_6	EBI	B	EBI2 LPDDR4X data bit 6
M_AE5	EBI2_DQ_7	EBI	B	EBI2 LPDDR4X data bit 7
M_AE14	EBI2_DQ_8	EBI	B	EBI2 LPDDR4X data bit 8

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Table 2-7 Top pin descriptions – primary pins (cont.)

Pin #	Pin name	Pin voltage	Pin type	Functional description
M_AG14	EBI2_DQ_9	EBI	B	EBI2 LPDDR4X data bit 9
M_AG3	EBI2_DQS_C_0	EBI	B	EBI2 LPDDR4X differential data strobe for byte 0 (C)
M_AG12	EBI2_DQS_C_1	EBI	B	EBI2 LPDDR4X differential data strobe for byte 1 (C)
M_AH3	EBI2_DQS_T_0	EBI	B	EBI2 LPDDR4X differential data strobe for byte 0 (T)
M_AH12	EBI2_DQS_T_1	EBI	B	EBI2 LPDDR4X differential data strobe for byte 1 (T)
M_AH24	EBI3_CA_CA_0	EBI	DO	EBI3 LPDDR4X command/address 0 bit 0
M_AF24	EBI3_CA_CA_1	EBI	DO	EBI3 LPDDR4X command/address 0 bit 1
M_AE22	EBI3_CA_CA_2	EBI	DO	EBI3 LPDDR4X command/address 0 bit 2
M_AH21	EBI3_CA_CA_3	EBI	DO	EBI3 LPDDR4X command/address 0 bit 3
M_AF21	EBI3_CA_CA_4	EBI	DO	EBI3 LPDDR4X command/address 0 bit 4
M_AE21	EBI3_CA_CA_5	EBI	DO	EBI3 LPDDR4X command/address 0 bit 5
M_AG22	EBI3_CA_CK_C	EBI	DO	EBI3 LPDDR4X differential clock (C)
M_AH22	EBI3_CA_CK_T	EBI	DO	EBI3 LPDDR4X differential clock (T)
M_AF23	EBI3_CA_CKE_0	EBI	DO	EBI3 LPDDR4X clock enable 0
M_AE23	EBI3_CA_CKE_1	EBI	DO	EBI3 LPDDR4X clock enable 1
M_AJ23	EBI3_CA_CS_0	EBI	DO	EBI3 LPDDR4X chip select 0
M_AH23	EBI3_CA_CS_1	EBI	DO	EBI3 LPDDR4X chip select 1
M_AE27	EBI3_DMI_0	EBI	DO	EBI3 LPDDR4X data mask for byte 0
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR4X data mask for byte 1
M_AG29	EBI3_DQ_0	EBI	B	EBI3 LPDDR4X data bit 0
M_AE29	EBI3_DQ_1	EBI	B	EBI3 LPDDR4X data bit 1
M_AF17	EBI3_DQ_10	EBI	B	EBI3 LPDDR4X data bit 10
M_AH17	EBI3_DQ_11	EBI	B	EBI3 LPDDR4X data bit 11
M_AF19	EBI3_DQ_12	EBI	B	EBI3 LPDDR4X data bit 12
M_AH19	EBI3_DQ_13	EBI	B	EBI3 LPDDR4X data bit 13
M_AE20	EBI3_DQ_14	EBI	B	EBI3 LPDDR4X data bit 14
M_AG20	EBI3_DQ_15	EBI	B	EBI3 LPDDR4X data bit 15
M_AH28	EBI3_DQ_2	EBI	B	EBI3 LPDDR4X data bit 2
M_AF28	EBI3_DQ_3	EBI	B	EBI3 LPDDR4X data bit 3
M_AH26	EBI3_DQ_4	EBI	B	EBI3 LPDDR4X data bit 4
M_AF26	EBI3_DQ_5	EBI	B	EBI3 LPDDR4X data bit 5
M_AG25	EBI3_DQ_6	EBI	B	EBI3 LPDDR4X data bit 6
M_AE25	EBI3_DQ_7	EBI	B	EBI3 LPDDR4X data bit 7

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Table 2-7 Top pin descriptions – primary pins (cont.)

Pin #	Pin name	Pin voltage	Pin type	Functional description
M_AE16	EBI3_DQ_8	EBI	B	EBI3 LPDDR4X data bit 8
M_AG16	EBI3_DQ_9	EBI	B	EBI3 LPDDR4X data bit 9
M_AG27	EBI3_DQS_C_0	EBI	B	EBI3 LPDDR4X differential data strobe for byte 0 (C)
M_AG18	EBI3_DQS_C_1	EBI	B	EBI3 LPDDR4X differential data strobe for byte 1 (C)
M_AH27	EBI3_DQS_T_0	EBI	B	EBI3 LPDDR4X differential data strobe for byte 0 (T)
M_AH18	EBI3_DQS_T_1	EBI	B	EBI3 LPDDR4X differential data strobe for byte 1 (T)
M_E15	ZQ0_0	–	AI	LPDDR4X ZQ resistor for lower x16 memory in rank 0 (shared by EBIs)
M_AE15	ZQ0_3	–	AI	LPDDR4X ZQ resistor for upper x16 memory in rank 0 (shared by EBIs)
M_D15	ZQ1_0	–	AI	LPDDR4X ZQ resistor for lower x16 memory in rank 1 (shared by EBIs)
M_AF15	ZQ1_3	–	AI	LPDDR4X ZQ resistor for upper x16 memory in rank 1 (shared by EBIs)

Table 2-8 Top pin descriptions – power-supply pins

Pin #	Pin name	Functional description
M_A5, M_A25, M_AH1, M_AH10, M_AH14, M_AH16, M_AH20, M_AH29, M_AJ5, M_AJ25, M_B1, M_B10, M_B14, M_B16, M_B20, M_B29	VDD1	Power for memory core (bottom VDD1)
M_A2, M_A6, M_A8, M_A10, M_A14, M_A16, M_A20, M_A22, M_A24, M_A28, M_AD1, M_AD2, M_AD28, M_AD29, M_AE6, M_AE24, M_AG7, M_AG9, M_AG21, M_AG23, M_AJ2, M_AJ6, M_AJ8, M_AJ10, M_AJ14, M_AJ16, M_AJ20, M_AJ22, M_AJ24, M_AJ28, M_C7, M_C9, M_C21, M_C23, M_E6, M_E24, M_F1, M_F2, M_F28, M_F29	VDD2	Power for memory core (bottom VDD2)
M_A4, M_A11, M_A13, M_A17, M_A19, M_A26, M_AF1, M_AF3, M_AF5, M_AF10, M_AF12, M_AF14, M_AF16, M_AF18, M_AF20, M_AF25, M_AF27, M_AF29, M_AJ4, M_AJ11, M_AJ13, M_AJ17, M_AJ19, M_AJ26, M_D1, M_D3, M_D5, M_D10, M_D12, M_D14, M_D16, M_D18, M_D20, M_D25, M_D27, M_D29	VDDQ	Power for memory I/O (bottom VDDQ)

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Table 2-9 Top pin descriptions – ground pins

Pin #	Pin name	Functional description
M_A3, M_A9, M_A12, M_A15, M_A18, M_A21, M_A27, M_AA3, M_AA4, M_AA5, M_AA25, M_AA26, M_AA27, M_AB3, M_AB4, M_AB5, M_AB25, M_AB26, M_AB27, M_AC1, M_AC2, M_AC3, M_AC4, M_AC5, M_AC6, M_AC7, M_AC8, M_AC9, M_AC10, M_AC11, M_AC12, M_AC13, M_AC14, M_AC15, M_AC16, M_AC17, M_AC18, M_AC19, M_AC20, M_AC21, M_AC22, M_AC23, M_AC24, M_AC25, M_AC26, M_AC27, M_AC28, M_AC29, M_AD3, M_AD4, M_AD5, M_AD6, M_AD7, M_AD8, M_AD9, M_AD10, M_AD11, M_AD12, M_AD13, M_AD14, M_AD15, M_AD16, M_AD17, M_AD18, M_AD19, M_AD20, M_AD21, M_AD22, M_AD23, M_AD24, M_AD25, M_AD26, M_AD27, M_AE2, M_AE4, M_AE11, M_AE13, M_AE17, M_AE19, M_AE26, M_AE28, M_AF8, M_AF22, M_AG2, M_AG4, M_AG6, M_AG11, M_AG13, M_AG17, M_AG19, M_AG24, M_AG26, M_AG28, M_AH5, M_AH25, M_AJ3, M_AJ9, M_AJ12, M_AJ15, M_AJ18, M_AJ21, M_AJ27, M_B5, M_B25, M_C2, M_C4, M_C6, M_C11, M_C13, M_C17, M_C19, M_C24, M_C26, M_C28, M_D8, M_D22, M_E2, M_E4, M_E11, M_E13, M_E17, M_E19, M_E26, M_E28, M_F3, M_F4, M_F5, M_F6, M_F7, M_F8, M_F9, M_F10, M_F11, M_F12, M_F13, M_F14, M_F15, M_F16, M_F17, M_F18, M_F19, M_F20, M_F21, M_F22, M_F23, M_F24, M_F25, M_F26, M_F27, M_G1, M_G2, M_G3, M_G4, M_G5, M_G6, M_G7, M_G8, M_G9, M_G10, M_G11, M_G12, M_G13, M_G14, M_G15, M_G16, M_G17, M_G18, M_G19, M_G20, M_G21, M_G22, M_G23, M_G24, M_G25, M_G26, M_G27, M_G28, M_G29, M_H3, M_H4, M_H5, M_H25, M_H26, M_H27, M_J3, M_J4, M_J5, M_J25, M_J26, M_J27, M_K3, M_K4, M_K5, M_K25, M_K26, M_K27, M_L3, M_L4, M_L5, M_L25, M_L26, M_L27, M_M3, M_M4, M_M5, M_M25, M_M26, M_M27, M_N3, M_N4, M_N5, M_N25, M_N26, M_N27, M_P3, M_P4, M_P5, M_P25, M_P26, M_P27, M_R3, M_R4, M_R5, M_R25, M_R26, M_R27, M_T3, M_T4, M_T5, M_T25, M_T26, M_T27, M_U3, M_U4, M_U5, M_U25, M_U26, M_U27, M_V3, M_V4, M_V5, M_V25, M_V26, M_V27, M_W3, M_W4, M_W5, M_W25, M_W26, M_W27, M_Y3, M_Y4, M_Y5, M_Y25, M_Y26, M_Y27	GND	Ground

Table 2-10 Top pin descriptions – no connect pins

Pin #	Pin name	Functional description
M_A1, M_A29, M_AG15, M_AH15, M_AJ1, M_AJ29, M_B15	NC	No connect pins; not connected internally

Table 2-11 Top pin descriptions – reserved pins

Pin #	Pin name	Functional description
M_AA1, M_AA2, M_AA28, M_AA2, M_AB1, M_AB2, M_AB28, M_AB29, M_H1, M_H2, M_H28, M_H29, M_J1, M_J2, M_J28, M_J29, M_K1, M_K2, M_K28, M_K29, M_L1, M_L2, M_L28, M_L29, M_M1, M_M2, M_M28, M_M29, M_N1, M_N2, M_N28, M_N29, M_P1, M_P2, M_P28, M_P29, M_R1, M_R2, M_R28, M_R29, M_T1, M_T2, M_T28, M_T29, M_U1, M_U2, M_U28, M_U29, M_V1, M_V2, M_V28, M_V29, M_W1, M_W2, M_W28, M_W29, M_Y1, M_Y2, M_Y28, M_Y29	RFU	Reserved pins

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3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	-0.3	1.13	V
VDD_APC1	Kryo Gold application processor	-0.3	1.25	V
VDD_GFX	Graphics	-0.3	1.13	V
VDDCX	Digital core circuits	-0.3	1.13	V
VDDMX	On-chip memory	-0.3	1.13	V
VDDMM	Multimedia subsystem circuits	-0.3	1.13	V
VDD_MODEM	Modem circuits	-0.3	1.13	V
VDD_SSC_CX	Snapdragon sensor core	-0.3	1.13	V
VDD_LPI_MX_A/B	Low power island circuits	-0.3	1.13	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDDA_SP_SENSOR	Secure processing unit sensors	-0.3	1.01	V
VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits			
VDDA_CSI0_0P9	MIPI CSI0 0.9 V circuits			
VDDA_CSI1_0P9	MIPI CSI1 0.9 V circuits			
VDDA_CSI2_0P9	MIPI CSI2 0.9 V circuits			
VDDA_CSI3_0P9	MIPI CSI3 0.9 V circuits			
VDDA_DSI0_0P9	MIPI DSI0 0.9 V circuits			
VDDA_DSI0_PLL_0P9	MIPI DSI0 PLL 0.9 V circuits			
VDDA_DSI1_0P9	MIPI DSI1 0.9 V circuits			
VDDA_DSI1_PLL_0P9	MIPI DSI1 PLL 0.9 V circuits			
VDDA_PCIE0_CORE	PCIe0 core circuits			
VDDA_PCIE1_CORE	PCIe1 core circuits			
VDDA_PLL_HV_CC_EBI	EBI high-voltage circuits			
VDDA_QLINK_LV	QLink low-voltage circuits			
VDDA_QLINK_LV_CK	QLink low-voltage clock circuits			
VDDA_UFS1_CORE	UFS core circuits			
VDDA_USB_HS_CORE	USB digital core circuits			
VDDA_USB2_SS_CORE	USB2 SS core circuits			
VDDA_USB1_SS_DP_CORE	USB1 SS and DisplayPort core circuits	-0.3	1.045	V
VDDPX_0	Digital pad circuits – control signals	-0.3	2.09	V
VDDPX_2	Digital pad circuits – SDC2	-0.3	3.33	V
VDDPX_3	Digital pad circuits – most I/Os	-0.3	2.09	V
VDD1	PoP DDR memory core – 1.8 V			
VDDPX_5	Digital pad circuits – UIM1 dual-voltage	-0.3	3.33	V
VDDPX_6	Digital pad circuits – UIM2 dual-voltage	-0.3	3.33	V
VDDPX_10	Digital pad circuits – UFS clock	-0.3	1.41	V
VDDPX_13	Digital pad circuits – SPU	-0.3	2.12	V
VDDPX_11	Digital pad circuits – CXO	-0.3	2.09	V
VDDA_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits			
VDD_QFPROM	Programming the QFPROM			
VDD_QFPROM_SP	Programming the QFPROM, secure processor unit			
VDDA_APC_CS_1P8	Application processor current sensor 1.8 V circuits			
VDDA_GFX_CS_1P8	Graphics current sensor 1.8 V circuits			
VDDA_USB_HS_1P8	USB HS1/2 1.8 V circuits			

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Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDDA_QREFS_1P25 VDDPX_VBIAS_SDC VDDPX_VBIAS_UIM	Reference voltage for QREFS 1.25 V circuits Reference voltage for SDC Reference voltage for UIM	-0.3	1.485	V
VDD2	PoP DDR memory core – 1.1 V	– [1]	– [1]	V
VDDIO_EBI0 VDDIO_EBI1 VDDIO_EBI2 VDDIO_EBI3 VDDIO_CK_EBI0 VDDIO_CK_EBI1 VDDIO_CK_EBI2 VDDIO_CK_EBI3 VDDQ	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits EBI0 I/O clock circuits EBI1 I/O clock circuits EBI2 I/O clock circuits EBI3 I/O clock circuits PoP DDR pads	-0.3	0.70	V
VDDA_EBI0 VDDA_EBI1 VDDA_EBI2 VDDA_EBI3 VDDA_CC_EBI01 VDDA_CC_EBI23	EBI0 PHY circuits EBI1 PHY circuits EBI2 PHY circuits EBI3 PHY circuits EBI0/EBI1 clock circuits EBI2/EBI3 clock circuits	-0.3	1.13	V
VDDA_HV_EBI0 VDDA_HV_EBI1 VDDA_HV_EBI2 VDDA_HV_EBI3 VDDA_CSI_1P2 VDDA_DSI_1P2 VDDA_REFGEN_1P2 VDDA_PCIE0_PLL_1P2 VDDA_PCIE1_PLL_1P2 VDDA_QLINK_HV_CK VDDA_UFS1_1P2 VDDA_USB2_SS_1P2 VDDA_USB1_SS_DP_1P2	EBI0 PHY high-voltage circuits EBI1 PHY high-voltage circuits EBI2 PHY high-voltage circuits EBI3 PHY high-voltage circuits MIPI CSI 1.2 V circuits MIPI DSI 1.2 V circuits REFGEN circuits PCIe0 PLL 1.2 V circuits PCIe1 PLL 1.2 V circuits QLink high-voltage clock circuits UFS 1.2 V circuits USB2 SS 1.2 V circuits USB1 SS and DisplayPort 1.2 V circuits	-0.3	1.38	V
VDDA_USB_HS_3P1	USB HS1/2 3.1 V circuits	-0.3	3.52	V
VDDA_WCSS_ADCDAC_1 VDDA_WCSS_ADCDAC_2	WCSS ADC and DAC – chain 1 WCSS ADC and DAC – chain 2	-0.3	1.49	V
VDD_WCSS VDDA_WCSS_PLL	WCSS circuits WCSS PLL circuits	-0.3	0.935	V
T_S	Storage temperature [2] [3]	-55	150	°C
ESD protection – see Section 7.1.				
Thermal conditions – see Section 4.6.				

1. See the LPDDR4X data sheet for VDD2 minimum and maximum voltages.

2. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
3. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-4). The SM8150 device meets all performance specifications listed in Section 3.6 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor			
	Turbo	0.660	1.030	V
	Nominal-L1	0.640	0.998	V
	Nominal	0.605	0.938	V
	SVS-L1	0.560	0.910	V
	SVS	0.515	0.846	V
	Low-SVS	0.470	0.786	V
VDD_APC1	Qualcomm Kryo Gold application processor			
	Turbo-L3	0.770	1.135	V
	Turbo-L2	0.770	1.063	V
	Turbo-L1	0.770	1.007	V
	Turbo	0.770	0.951	V
	Nominal-L1	0.640	0.911	V
	Nominal	0.605	0.839	V
	SVS-L1	0.560	0.823	V
	SVS	0.515	0.755	V
	Low-SVS	0.470	0.695	V
VDD_SSC_CX	Snapdragon sensor core			
	Turbo	0.660	1.030	V
	Nominal	0.605	0.966	V
	SVS	0.515	0.886	V
	Low-SVS	0.465	0.822	V
	Min-SVS	0.435	0.758	V
VDD_LPI_MX_A/B	Low power island circuits			
	Turbo	0.740	1.030	V
	Nominal	0.695	0.998	V
	SVS	0.695	0.934	V

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Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDDCX	Digital core circuits			
	Turbo-L1	0.700	1.030	V
	Turbo	0.660	0.962	V
	Nominal	0.605	0.894	V
	SVS-L1	0.555	0.874	V
	SVS	0.515	0.810	V
	Low-SVS	0.485	0.750	V
	Retention [2]	0.352	0.480	V
VDDMX	On-chip memory			
	Turbo-L1	0.740	1.030	V
	Turbo	0.740	0.998	V
	Nominal-L1	0.695	0.998	V
	Nominal	0.695	0.962	V
	SVS-L1	0.695	0.942	V
	SVS	0.695	0.898	V
	Retention [2]	0.516	0.668	V
VDDMM	Multimedia subsystem circuits			
	Turbo	0.660	1.030	V
	Nominal	0.605	0.962	V
	SVS-L1	0.555	0.942	V
	SVS	0.515	0.878	V
	Low-SVS	0.465	0.818	V
VDD_MODEM	Modem circuits			
	Turbo-L1	0.700	1.030	V
	Turbo	0.660	1.030	V
	Nominal-L1	0.640	0.962	V
	Nominal	0.605	0.894	V
	SVS-L1	0.555	0.874	V
	SVS	0.515	0.810	V
	Low-SVS	0.465	0.750	V
	Min-SVS	0.455	0.690	V
VDD_GFX	Graphics			
	Nominal-L1 (SM8150 AC only)	0.655	0.974	V
	Nominal	0.605	0.922	V
	SVS-L1	0.555	0.866	V
	SVS	0.515	0.802	V
	Low-SVS	0.475	0.742	V
VDDA_EBI0	EBI PHY and clock circuits:			
VDDA_EBI1	Turbo	0.660	1.030	V
VDDA_EBI2	Nominal	0.640	0.998	V
VDDA_EBI3	SVS-L1	0.605	0.962	V
VDDA_CC_EBI01	SVS	0.555	0.942	V
VDDA_CC_EBI23	Low-SVS	0.515	0.878	V
	Min-SVS	0.465	0.818	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for this mode in this power domain is a static setting. There is no scaling.

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Table 3-3 Operating conditions

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDDA_SP_SENSOR	Secure processing unit sensors	0.83	0.88	0.92	V
VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits				
VDDA_CSI0_0P9	MIPI CSI0 0.9 V circuits				
VDDA_CSI1_0P9	MIPI CSI1 0.9 V circuits				
VDDA_CSI2_0P9	MIPI CSI2 0.9 V circuits				
VDDA_CSI3_0P9	MIPI CSI3 0.9 V circuits				
VDDA_DSI0_0P9	MIPI DSI0 0.9 V circuits				
VDDA_DSI0_PLL_0P9	MIPI DSI0 PLL 0.9 V circuits				
VDDA_DSI1_0P9	MIPI DSI1 0.9 V circuits				
VDDA_DSI1_PLL_0P9	MIPI DSI1 PLL 0.9 V circuits				
VDDA_PCIE0_CORE	PCIe0 core circuits				
VDDA_PCIE1_CORE	PCIe1 core circuits				
VDDA_PLL_HV_CC_EBI	EBI high-voltage circuits				
VDDA_QLINK_LV	QLink low-voltage circuits				
VDDA_QLINK_LV_CK	QLink low-voltage clock circuits				
VDDA_UFS1_CORE	UFS core circuits				
VDDA_USB_HS_CORE	USB digital core circuits				
VDDA_USB2_SS_CORE	USB2 SS core circuits				
VDDA_USB1_SS_DP_CORE	USB1 SS and DisplayPort core circuits	0.87	0.912	0.95	V
VDDPX_0	Digital pad circuits – control signals	1.70	1.80	1.90	V
VDDPX_2	Digital pad circuits – SDC2	1.70 2.72	1.808 2.96	1.90 3.03	V V
VDDPX_3	Digital pad circuits – most I/Os	1.70	1.80	1.90	V
VDD1	PoP DDR memory core – 1.8 V				
VDDPX_5	Digital pad circuits – UIM1 dual-voltage	1.70 2.72	1.808 2.928	1.90 3.03	V V
VDDPX_6	Digital pad circuits – UIM2 dual-voltage	1.70 2.72	1.808 2.928	1.90 3.03	V V
VDDPX_10	Digital pad circuits – UFS clock	1.12	1.20	1.28	V
VDDPX_13	Digital pad circuits – secure processing unit (SPU)	1.70	1.856	1.93	V

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Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDDPX_11	Digital pad circuits – CXO	1.70	1.80	1.90	V
VDDA_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits				
VDD_QFPROM	Programming the QFPROM				
VDD_QFPROM_SP	Programming the QFPROM, secure processor unit				
VDDA_APC_CS_1P8	Application processor current sensor 1.8 V circuits				
VDDA_GFX_CS_1P8	Graphics current sensor 1.8 V circuits				
VDDA_USB_HS_1P8	USB HS1/2 1.8 V circuits				
VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits	1.15	1.25	1.35	V
VDDPX_VBIAS_SDC	Reference voltage for SDC				
VDDPX_VBIAS_UIM	Reference voltage for UIM				
VDD2	PoP DDR memory core – 1.1 V	– [3]	1.128	– [3]	V
VDDIO_EBI0	EBI0 I/O memory circuits	0.57	0.60	0.64	V
VDDIO_EBI1	EBI1 I/O memory circuits				
VDDIO_EBI2	EBI2 I/O memory circuits				
VDDIO_EBI3	EBI3 I/O memory circuits				
VDDIO_CK_EBI0	EBI0 I/O clock circuits				
VDDIO_CK_EBI1	EBI1 I/O clock circuits				
VDDIO_CK_EBI2	EBI2 I/O clock circuits				
VDDIO_CK_EBI3	EBI3 I/O clock circuits				
VDDQ	PoP DDR pads				
VDDA_HV_EBI0	EBI0 PHY high voltage circuits	1.15	1.20	1.25	V
VDDA_HV_EBI1	EBI1 PHY high voltage circuits				
VDDA_HV_EBI2	EBI2 PHY high voltage circuits				
VDDA_HV_EBI3	EBI3 PHY high voltage circuits				
VDDA_CSI_1P2	MIPI CSI 1.2 V circuits				
VDDA_DSI_1P2	MIPI DSI 1.2 V circuits				
VDDA_REFGEN_1P2	REFGEN circuits				
VDDA_PCIE0_PLL_1P2	PCIe0 PLL 1.2 V circuits				
VDDA_PCIE1_PLL_1P2	PCIe1 PLL 1.2 V circuits				
VDDA_QLINK_HV_CK	QLink high-voltage clock circuits				
VDDA_UFS1_1P2	UFS 1.2 V circuits				
VDDA_USB2_SS_1P2	USB2 SS 1.2 V circuits				
VDDA_USB1_SS_DP_1P2	USB1 SS and DisplayPort 1.2 V circuits				
VDDA_USB_HS_3P1	USB HS1/2 3.1 V circuits	2.97	3.072	3.20	V

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Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDDA_WCSS_ADCDAC_1 VDDA_WCSS_ADCDAC_2	WCSS ADC and DAC – chain 1 WCSS ADC and DAC – chain 2	1.25	1.304	1.36	V
VDD_WCSS VDDA_WCSS_PLL	WCSS circuits WCSS PLL circuits	0.675	0.752	0.85	V
Thermal conditions					
T_J	Device junction temperature	-	-	+85	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. See the LPDDR4X data sheet for VDD2 minimum and maximum voltages.

3.3 Power distribution network

The impedances of the distribution networks that deliver power to the SM8150 device are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the minimum/maximum values listed in Table 3-2 to be violated.

The following tables list the PDN maximum impedance specifications.

Table 3-4 PDN specifications

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_APC1	2	13	80	1	G8, H7, H9, H11, J8, J10, J12, K7, M7, N8, N10, P7, P9, P11, T7, V7, V9, V11, W8, 10	G7, G9, H8, H10, H12, J6, J9, J11, J13L6, N6, N9, N11, P8, P10, P12, R6, V6, V8, V10, V12, W6, W7, W9, W11, Y8, Y10
VDD_APC0	5	26	120	1	K13, L14, M13, N12, N13, N14, P13, R14, T13, U14, V13, W12	J13, K14, L13, L15, M14, N11, N15, P12, P14, R13, R15, T14, U13, U15, V12, V14, W11, W13, Y12

Table 3-4 PDN specifications (cont.)

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_GFX	3	18	110	1	AC19, AC21, AC23, AC24, AC25, AC27, AC29, AE24, AG19, AG21, AG23, AG24, AG25, AG27, AG29	AB18, AB20, AB22, AB26, AB28, AB30, AD24, AD30, AF24, AH20, AH22, AH24, AH25, AH28, AH30
VDD_MODEM (SM8150 only)	5	31	150	1	AB8, AB10, AB12, AC9, AC11, AD8, AD12, AF8, AF10, AF12	AA7, AA9, AA11, AC7, AC13, AD10, AE7, AE9, AE11, AE13, AG7, AG9, AG11
VDDMM	5	35	170	1	H24, H26, J25, K24, K26, M24, M26, P24, P26, R25	G23, G25, G27, J23, J27, L23, L25, L27, N23, N25, N27, R23, R27, T24, T26
VDD_LPI_MX_A	150	217	1000	1	AF18, AH18	AG17, AJ17, AJ19
VDD_LPI_MX_B	200	309	1500	1	AC30	AB30, AB31, AD30, AD31
VDD_SSC_CX	70	136	650	1	AE16, AE17, AF16	AD16, AE15, AG17
VDD_WCSS	40	88	500	1	Y27, Y28, AA27, AA28	W27, W28, W29, Y26, AB26, AB28
VDDCX	6	51	320	1	U23, U25, U27, T28	R27, T24, T26, T29, V24, V26
	5	16	100	2	AA13, AA15, AA19, AB14, AD14, AF14, G11, G13, G15, H16, H18, J19, K16, K18, L19, M16, M18, N19, P16, P18, R19, T16, T18, U19, V16, V18, W15, W19, Y14, Y16, Y18	F14, H10, H12, H14, J15, J17, K20, L15, L17, M20, N15, N17, P20, R15, R17, T20, U15, U17, V14, V20, W13, W17, Y12, Y20, AA17, AB16, AB18, AB20, AC13, AC15, AE13, AE15
VDDMX	13	72	450	1	N7, R7	N6, P8, R6
	10	71	450	2	AE30, AF30	AD30, AD31, AE31, AG30
	5	32	200	3	AA23, AA25, AB24, G17, G19, H20, H22, J21, K22, L21, M22, N21, P22, R21, T22, U21, V22, W21, W23, Y22, Y24	F18, G21, G23, J23, K20, L23, M20, N23, P20, R23, T20, V20, V24, W25, Y20, Y26, AA21, AB22, AB26

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1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

Table 3-5 PDN specifications–DDR rails

Power domain	DC resistance (mΩ)	Maximum effective impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDDA_EBI / VDDA_CC_EBI	26	100	1025	1	F9, F10, F12	E10, E11, E13, G9
	26	100	1025	2	F23, F24	E22, G23
	26	100	1025	3	AH9, AH10, AH12	AH14, AH8, AJ10, AJ11
	26	100	1025	4	AH26, AH27	AG26, AH25
VDDIO_EBI /VDDIO_CK_EBI	33	100	1098	1	D9, E6, E7, E8, E9	D6, D7, D8, E10
	33	100	1098	2	E23, E24, E25, E26, F25	D26, E22, G25
	33	100	1098	3	AJ6, AJ7, AJ8, AJ9, AK8	AH5, AH6, AH8, AJ10, AK7, AL8
	33	100	1098	4	AJ26, AJ27, AJ28, AJ29, AK28	AH25, AH28, AH30, AJ25, AK26, AK29

1. The PDN AC effective impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

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Table 3-6 PDN specifications–SerDes rails

Power rail	Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
			R_{mid_freq} (mΩ)	L (pH)			
VREG_L5A_0P88	VDDA_CSI0_0P9	292	176	1125	1	K29	J30, K28, L30
	VDDA_CSI1_0P9	292	176	1125	2	J29	K28, J30, L30
	VDDA_CSI2_0P9	292	176	1125	3	H29	G30
	VDDA_CSI3_0P9	292	176	1125	4	G29	G30
	VDDA_QREFS_ 0P875	175	176	1125	5	L29	K28, J30, L30
	VDDA_PCIE0_CORE	180	117	750	6	U29	T29
	VDDA_PCIE1_CORE	100	98	625	7	V29	W28, W29, W30
	VDDA_QLINK_LV (SM8150 only)	730	235	1500	8	AD6	AC6, AC7
	VDDA_QLINK_LV_CK (SM8150 only)	625	117	750	9	AE6	AE7, AF6
	VDDA_UFS1_CORE	90	119	760	10	M4, M5	L6, N6
	VDDA_USB2_SS_ CORE	192	138	880	11	F6	G7
	VDDA_DSI0_0P9	1200	169	1080	12	E20	E22, F18
	VDDA_DSI1_0P9	1200	169	1080	13	E21	E22, F18
	VDDA_DSI0_PLL_ 0P9	350	169	1080	14	E19	E22, F18
	VDDA_DSI1_PLL_ 0P9	350	169	1080	15	F22	G21, G23
VREG_L18A_0P9	VDDA_USB1_SS_ DP_CORE	104	98	625	1	J4, J5	H3, J6, K3

Table 3-6 PDN specifications–SerDes rails (cont.)

Power rail	Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
			R_{mid_freq} (mΩ)	L (pH)			
VREG_L3C_1P2	VDDA_CSI_1P2	1000	78	500	1	H28	G27, J27
	VDDA_REFGEN_1P2	850	235	1500	2	M28	L27, N27, N29
	VDDA_DSI_1P2	1200	78	500	3	F20	E17, E22, F18, G21, G23
	VDDA_PCIE0_PLL_1P2	1000	235	1500	4	U28	T29
	VDDA_PCIE1_PLL_1P2	1000	235	1500	5	V28	W27, W28, W29
	VDDA_QLINK_HV_CK (SM8150 only)	2400	235	1500	6	AF7	AE7, AF6, AG7
	VDDA_UFS1_1P2	850	235	1500	7	M6	N6
	VDDA_USB1_SS_DP_1P2	500	196	1250	8	K6	J6, L6
	VDDA_USB2_SS_1P2	1000	235	1500	9	F7	G7
VREF_MSM	VDDPX_VBIAS_UIM	-	157	1000	1	AJ23	AH22, AH24, AK23
	VDDPX_VBIAS_SDC	-	157	1000	2	R33	R34, T32

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC Inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8150 Linux Android Current Consumption Data* (80-PD867-7).

3.5 Dhrystone and rock bottom maximum power

Table 3-7 Dhrystone and rock bottom maximum power

SDM version	Kryo octa-core Dhrystone (W) [1, 2, 3]	Rock bottom (mW) [4]
SM8150	7	7

1. This Kryo octa-core Dhrystone specification applies to SM8150 CS devices that run Kryo Gold prime core at 2.842 GHz and the other three Kryo Gold cores at 2.419 GHz and Kryo quad Silver cores at 1.786 GHz.
2. Dhrystone power should be measured on the VDD_APC0 and VDD_APC1 rails, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).
4. Rock bottom power (VDD_CX and VDD_MX) should be measured at the VDD_CX and VDD_MX rails. See AIR1 in Table 3-1 (Test definitions) of *SM8150 Linux Android Current Consumption Data* (80-PD867-7) for the test setup.

3.6 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM8150 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-8 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDPX_3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDPX_3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	1.0	µA
I_{IL}	Input low leakage current [1]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)

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Table 3-8 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [1]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage	VDDPX_3 - 0.45	VDDPX_3	V
V_{OL}	Low-level output voltage	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
2. Pin voltage = VDDPX_3 maximum. For keeper pins, pin voltage = VDDPX_3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDDPX_3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX_3 maximum.

Table 3-9 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX_2	–	VDDPX_2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDPX_2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDDPX_2	–	VDDPX_2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDPX_2	V

Table 3-10 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-11 UICC 3 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 ×VDDPX_x (RST, CLK) and 0.4 V (I/O). The worst-case V_{OL} is used in this table.

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Table 3-12 UICC 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 × VDDPX_x (RST, CLK) and 0.3 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-13 Digital I/O characteristics for VDDPX_10 nominal (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDDPX_10	V
V_{OH}	Output high-level voltage	0.75 × VDDPX_10	VDDPX_10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in Table 2-1). For example, for 1.8 V GPIOs, it can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

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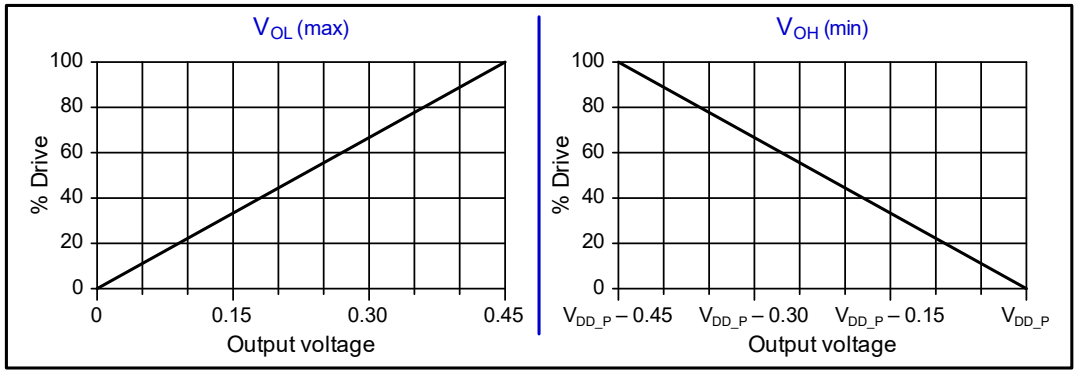

Figure 3-1 IV curve for V_{OL} and V_{OH}Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM8150 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.1.

3.7 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

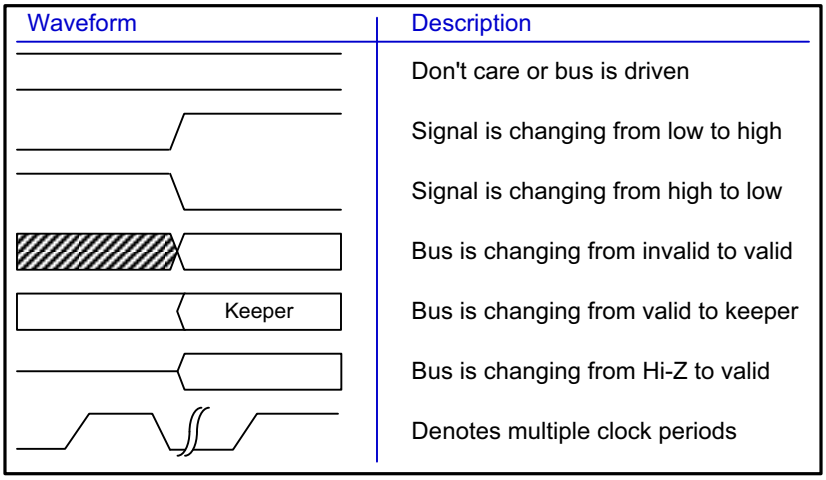

Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.

- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.7.1 Rise and fall time specifications

The testers that characterize SM8150 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

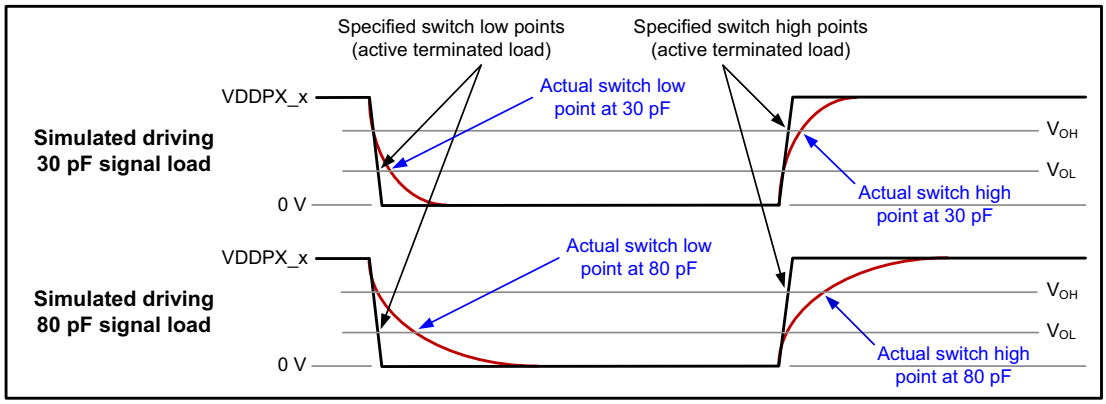

Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8150 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.2 Pad design methodology

The SM8150 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

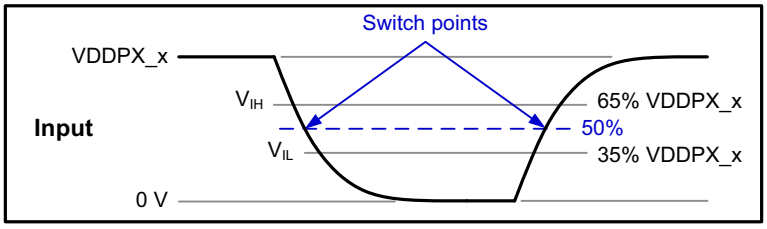

Figure 3-4 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX_x} - 50 mV or more
- V_{OL} ~ 50 mV or less

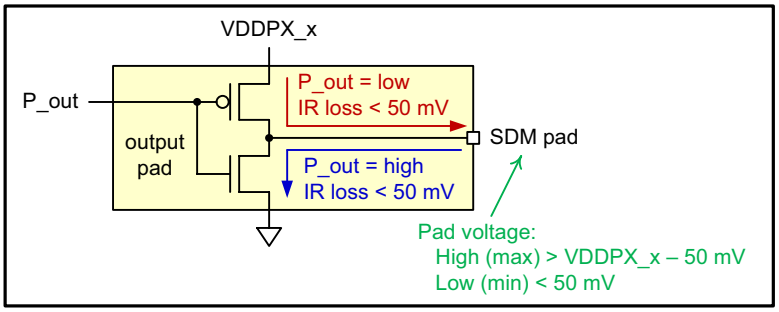

Figure 3-5 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR4X SDRAM memory that is attached to the top of the SM8150 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8150 Recommendations* (80-VP300-15).

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SM8150 device supports up to four DPHY or CPHY camera interfaces.

Table 3-14 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 is not supported; DPCM predictor 2 is not supported.
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	The maximum validated data rate is 1.5 Gsps.

3.9.2 Audio support

The SM8150 supports the WCD9340/WCD9341 audio codec IC to provide the system's audio functions. SM8150 audio-related interface options with the WCD include:

- SLIMbus: Section 3.10.7
- I^2S: Section 3.10.8
- PCM/TDM: Section 3.10.9
- I^2C: Section 3.10.12

See the *WCD9340/WCD9341 Audio Codec Device Specification* (80-P4986-1) for performance characteristics.

3.9.3 Display support

The SM8150 device supports up to two DPHY or CPHY displays.

Table 3-15 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for CPHY v1.1	None

3.9.4 DMB support

The SM8150 supports an external DMB solution using the following interface options:

- TSIF: Section 3.10.10
- SD: Section 3.10.1

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3.10 Connectivity

The connectivity functions supported by the SM8150 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Transport stream interface (TSIF) interfaces
- Touchscreen connections
- Through proper configuration of the 20 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - I3C

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

Table 3-16 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

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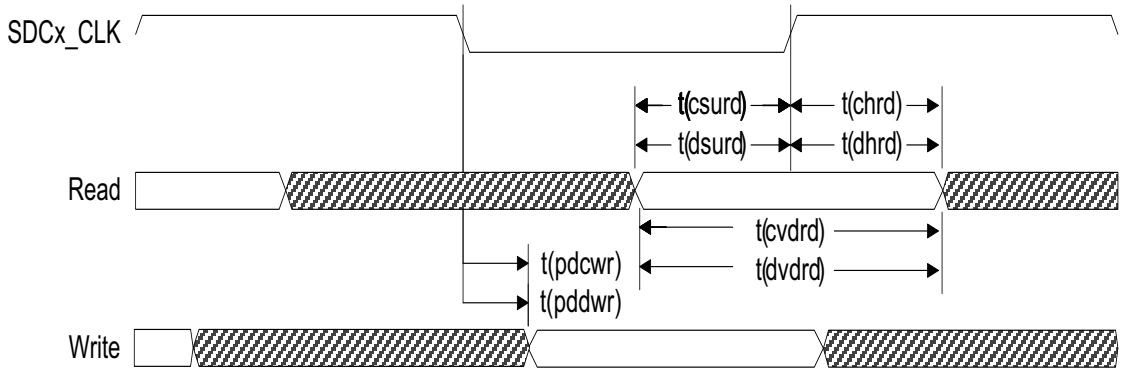
Single data rate – SDR mode



Double data rate – DDR mode

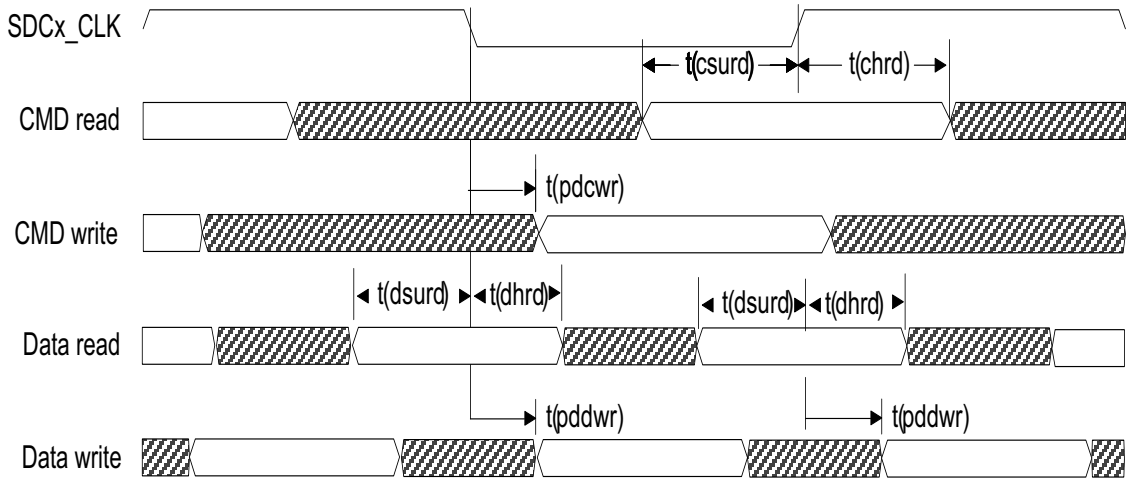


Figure 3-6 SD interface timing

3.10.2 USB interfaces

Table 3-17 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	None
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

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3.10.3 DisplayPort

Table 3-18 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.10.4 PCIe interface

Table 3-19 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link upconfigure capability

3.10.5 UFS interface

Table 3-20 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.0	Rate B

3.10.6 UICC interface

Table 3-21 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.10.7 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.10.8 I^2S interfaces

There are two I^2S interface types supported by the SM8150:

- Legacy I^2S interfaces for primary and secondary microphones and speakers
- The multiple I^2S (MI^2S) interface for microphone and speaker functions

The following information applies to both interface types.

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Table 3-23 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

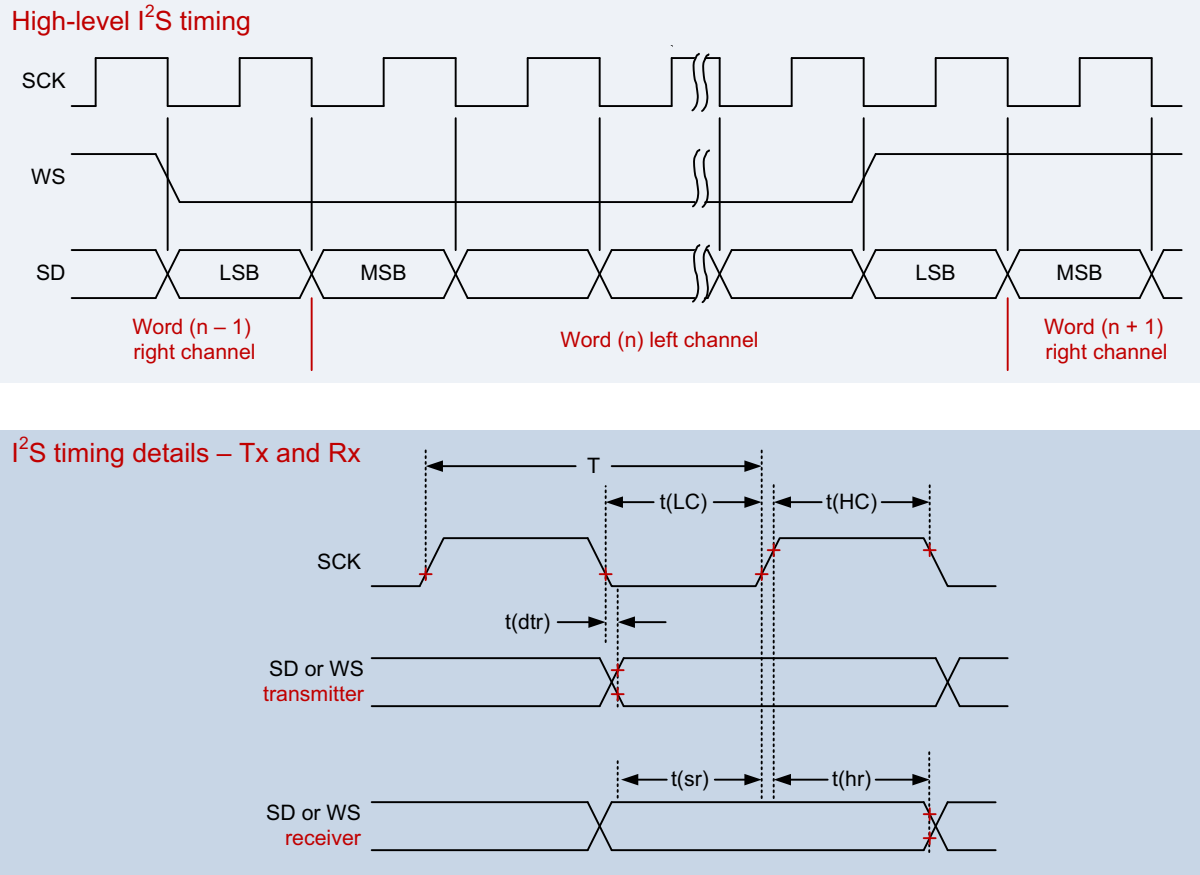

Figure 3-7 I²S timing diagram

Table 3-24 I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

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Table 3-24 I²S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60 × T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

1. Load capacitance is between 10 pF and 40 pF.

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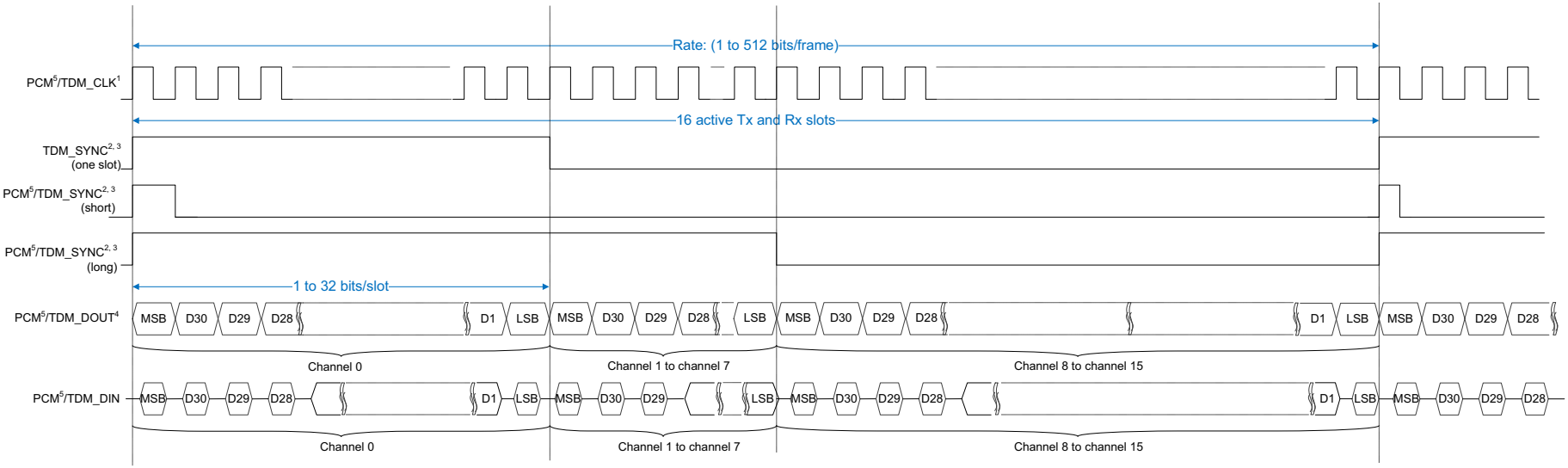
3.10.9 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-8 PCM/TDM audio format with different sync modes

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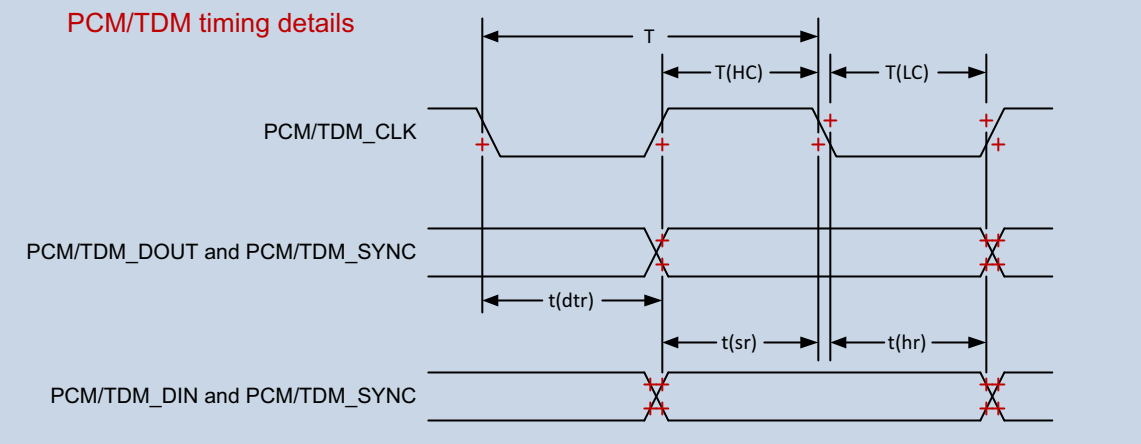

Figure 3-9 PCM/TDM timing diagram

Table 3-25 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns
Slave mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.40 × T	0.60 × T	ns
t(LC)	Clock low		0.40 × T	0.60 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns

1. Load capacitance is between 10 pF to 40 pF.
2. End-to-end testing for the TDM clock is completed up to 12.288 MHz.

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3.10.10 TSIF

Table 3-26 Supported TSIF standards and exceptions

Applicable standard	Feature exceptions
ITU-T H.222.0 Transport Stream (HTS); also known as *ISO/IEC 13818-1*	None

3.10.11 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.10.12) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.12 I^{2}C interface

Table 3-27 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions
I^{2}C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

3.10.13 Serial peripheral interface

The SM8150 supports SPI as a master only. Any one of the 20 QUP ports can be configured as an SPI master.

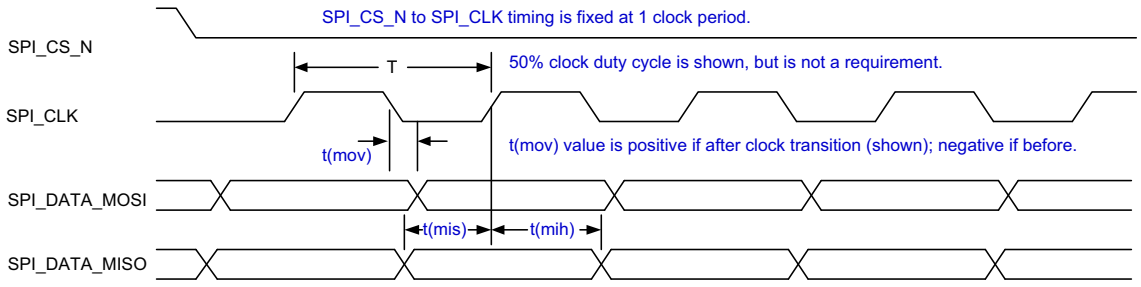

Figure 3-10 SPI master timing diagram

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Table 3-28 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

Table 3-29 SPI master timing characteristics for QUP_17 and QUP_19

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	25 MHz maximum	40	–	–	ns
t(ch)	Clock high	18	–	–	ns
t(cl)	Clock low	18	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	3	–	–	ns
t(mih)	Master input hold	3	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz CXO input

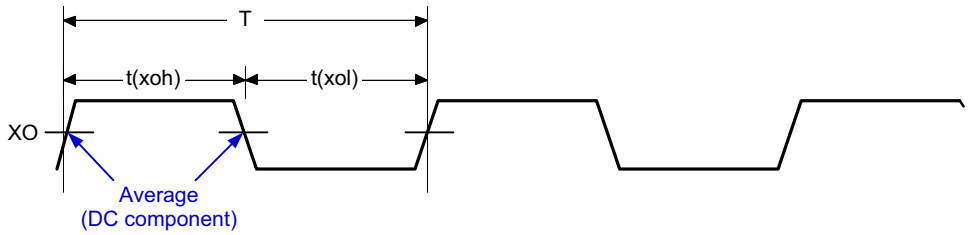

Figure 3-11 XO timing parameters

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Table 3-30 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19) and *GPS Quality, 19.2 MHz 2016 Package Size, TH+Xtal Mini-Specification* (80-V9690-26) documents for more information.

3.11.1.2 Sleep clock

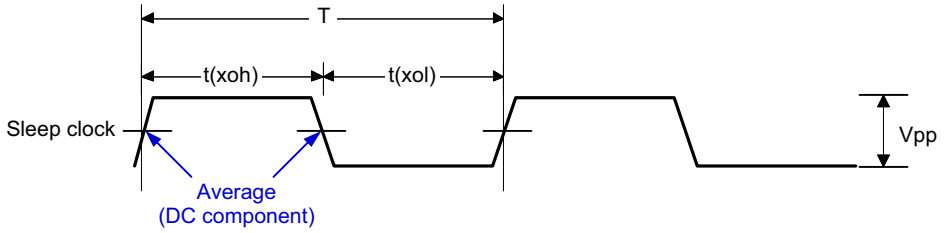

Figure 3-12 Sleep-clock timing parameters

Table 3-31 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

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3.11.3 JTAG

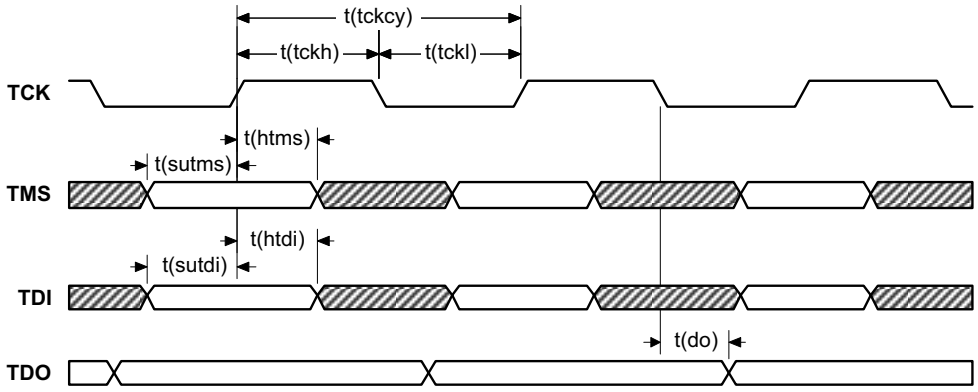

Figure 3-13 JTAG interface timing diagram

Table 3-32 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.11.4 SWD

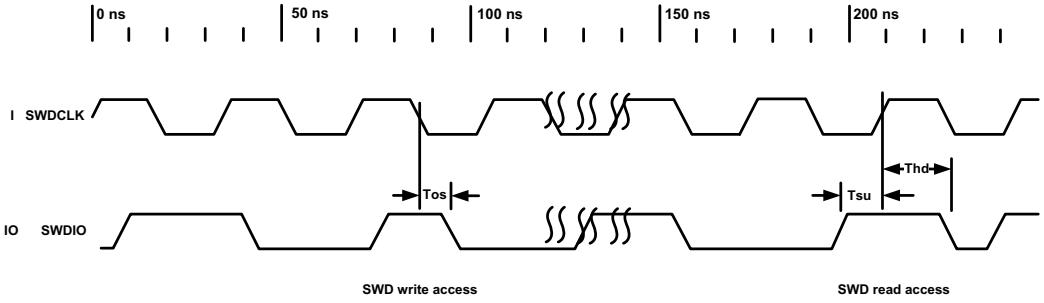

Figure 3-14 SWD write and read AC timing diagram

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Table 3-33 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

Note: SWDCLK runs at 20 MHz or lower.

3.12 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-3. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 Qualcomm RF Front End

Table 3-34 Supported Qualcomm RF Front End standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 2.0	None

Note: Supports v2.1 advanced features.

3.12.2 System power management interface (SPMI)

Table 3-35 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

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4 Mechanical information

4.1 Device physical dimensions

The SM8150 device is available in the MPSP893, a PoP system (height dimension does not include the memory device). Its bottom footprint is equivalent to an 893 PSP, and it accepts memory modules from above that are equivalent to a 556 NSP. The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE: Click the following links to download *Package Outline Drawing, MPSP893, 12.4 × 12.4 × 0.58 mm, SB136, ST94, M147, PB 556 NSP, PL1, MEP* (NT90-PA488-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PA488-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

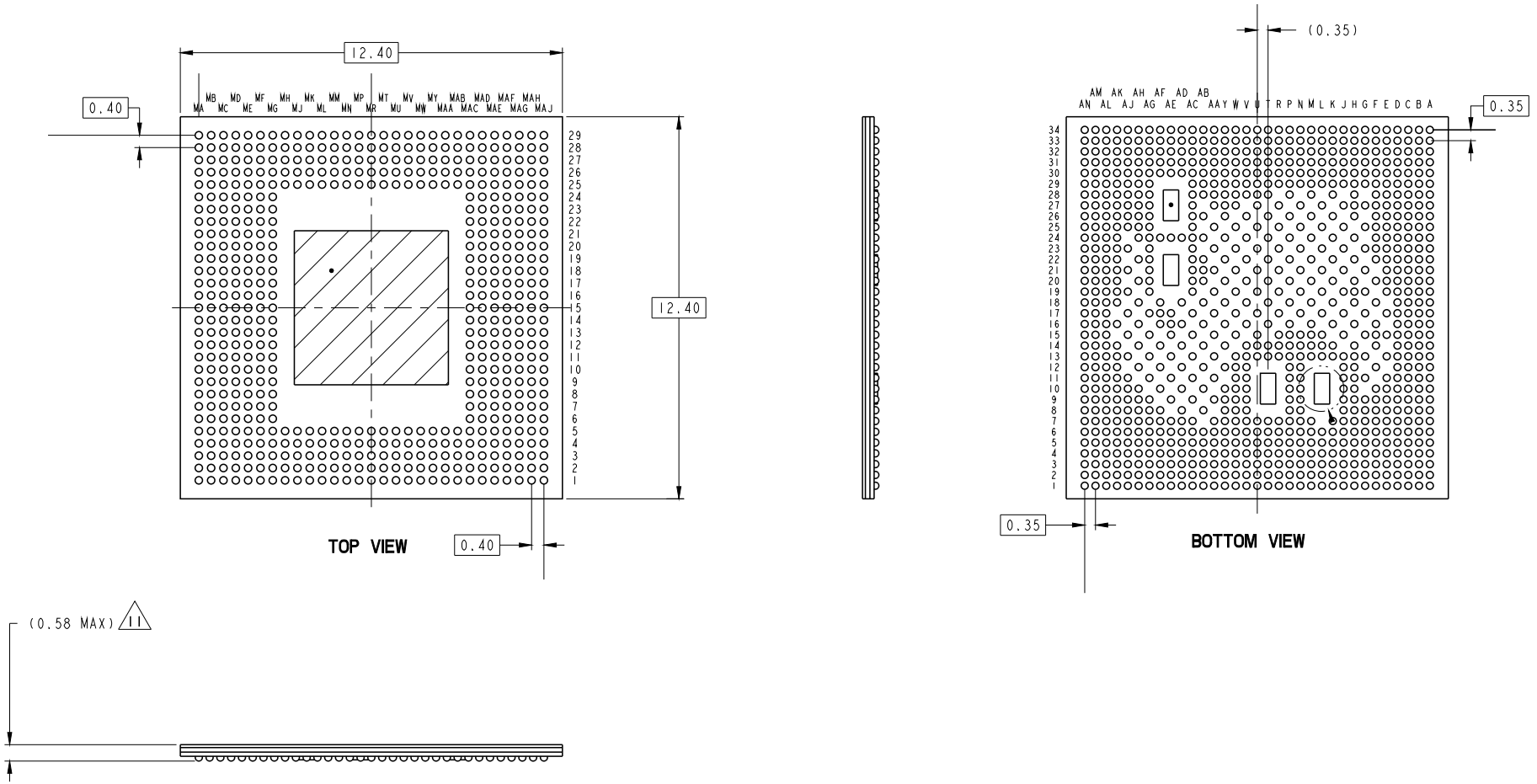

Figure 4-1 Simplified MPSP893 outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

NOTE: The coplanarity specification for the SM8150 bottom package is 100 µm.

4.2 Part marking

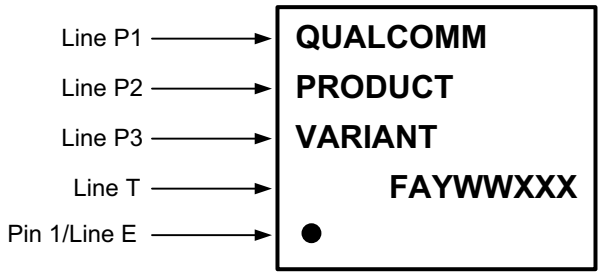

Figure 4-2 SM8150 device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm company name
P2	PRODUCT	QTI product name ■ SM8150 ■ SM8150P
P3	VARIANT	PRR-BB ■ See Table 4-4 for the assigned values.
T	FAYWWXXX	F = supply source code ■ F = F (TSMC) A = assembly site code ■ A = C (Amkor, Korea) ■ A = X (Amkor, Japan) Y = single-digit year WW = work week (based on calendar year) XXX = traceability number
E	● Blank or random	Ball A1 indicator Additional content as necessary

NOTE: For complete marking definitions of all SM8150 variants and revisions, see the *SM8150/SM8150P Device Revision Guide* (80-PD867-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 Related register (0x00780130)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining the feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8150	-1	-MPSP	893			-TR	-00	-0	-AB

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8150-1-MPSP893-TR-00-0-AB

Notes:

- The shipping package is either TR (tape and reel) or MT (matrix tray).
- For ES1, use SDM855 for product name in the identification code.

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Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Hardware revision	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	Hardware revision number	FEATURE_ID [2]	S value	Comments	Sample date
SM8150	ES1	v1.0	100-AB	0x0 00A5 0E1	D	0	SM8150, 893 MPSP; 20 layers; 6x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; 12.4 × 12.4 MEP	04/30/2018
SM8150	ES2	v2.0	101-AB	0x1 00A5 0E1	1	0	SM8150, 893 MPSP; 20 layers; 7x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	08/15/2018
SM8150	ES3	v2.1	102-AB	0x2 00A5 0E1	1	0	SM8150, 893 MPSP; 20 layers; 7x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	09/28/2018
SM8150	CS	v2.2	103-AB	0x3 00A5 0E1	1	0	SM8150, 893 MPSP; 20 layers; 7x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	11/19/2018
SM8150	CS	v2.2	303-AB	0x3 00A5 0E1	2	0	SM8150, 893 MPSP; 16 layers; 6x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	11/19/2018
SM8150	CS	v2.2	503-AB	0x3 00A5 0E1	3	0	SM8150, 893 MPSP; 12 layers; 5x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	11/19/2018

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Table 4-4 Device identification details (cont.)

Device	Sample type	Hardware revision	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	Hardware revision number	FEATURE_ID [2]	S value	Comments	Sample date
SM8150P	CS	v2.2	103-AB	0x3 00A6 0E1	0	0	SM8150P, 893 MPSP; no modem; Gold prime at 2.842 GHz, GPU at 585 MHz; 12.4 × 12.4 MEP	11/19/2018
SM8150	ES	v2.2	103-AC	0x3 00A5 0E1	5	0	SM8150, 893 MPSP; 20 layers; 7x CA, CDMA, GSM, LTE, TD-SCDMA, WCDMA; Gold prime at 2.956 GHz GPU at 675 MHz; 12.4 × 12.4 MEP	04/30/2019
SM8150	ES	v2.2	503-AC	0x3 00A5 0E1	6	0	SM8150, 893 MPSP; 12 layers; 5x CA, CDMA,GSM, LTE, TD-SCDMA,WCDMA; Gold Prime at 2.956 GHz, GPU at 675 MHz; 12.4 × 12.4 MEP	04/30/2019
SM8150P	ES	v2.2	103-AC	0x3 00A6 0E1	3	0	SM8150P, 893 MPSP; Gold Prime at 2.956 GHz, GPU at 675 MHz; 12.4 × 2.4 MEP	TBD

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.

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4.4 Daisy chain devices

The SM8150 daisy chain ordering part number is TP-MPSP893-1.

4.5 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-5.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SM8150/SM8150P rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8150/SM8150P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

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4.6 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SM8150 V1 MEP 6 GB DRAM Package Thermal Model Icepak* (HS11-PD867-5HW) and the *SM8150 V1 MEP 6 GB DRAM Package Thermal Model FloTHERM* (HS11-PD867-6HW) from the CreatePoint website. from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PD867-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PD867-6HW

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes. For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

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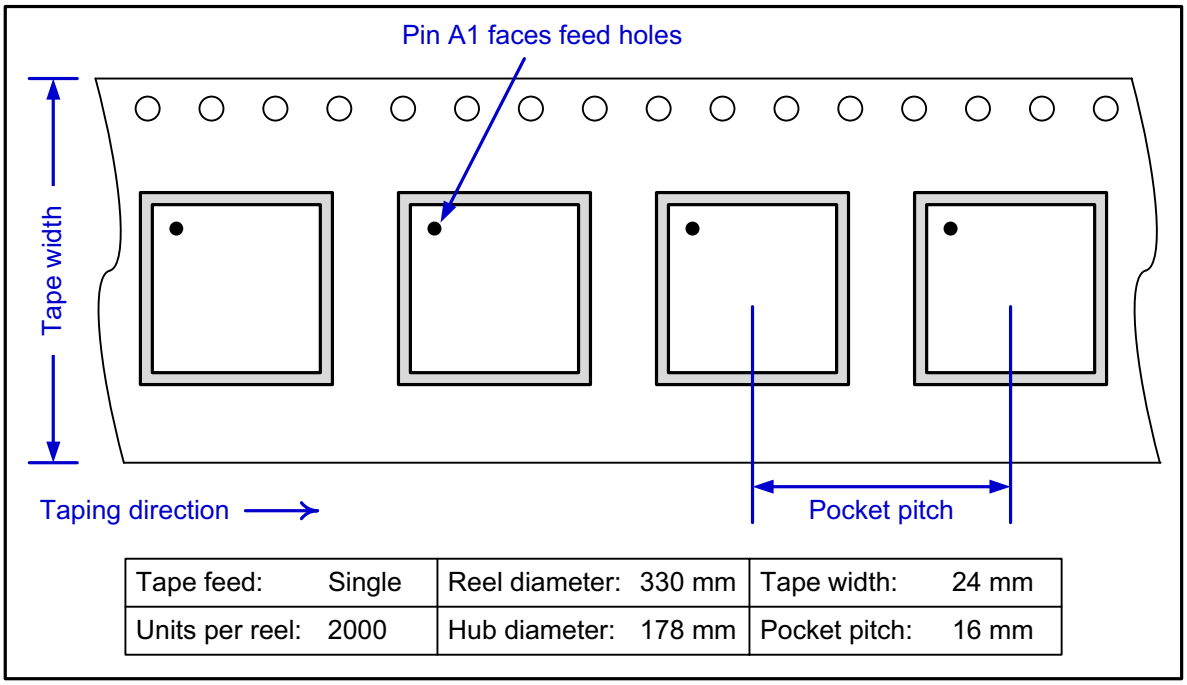
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8150 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

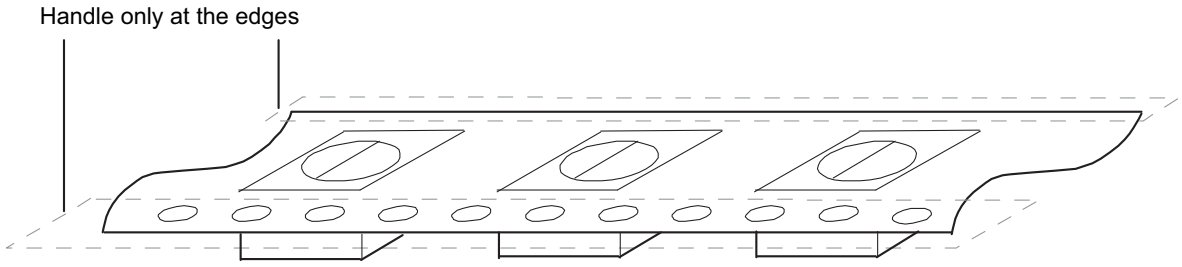


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

SM8150 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.5.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM8150 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SM8150 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

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5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

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6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its Sn/Ag/Cu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy-chain components.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the following link to download *Daisy Chain Interconnect, MPSP893, 12.4 × 12.4 × 0.58 mm,* (DS90-PA488-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-PA488-1

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For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

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7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 and Table 7-2 list the SM8150/SM8150P reliability evaluation report for the 893B MPSP device.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	7728	Pass DPPM < 200
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	4846	Pass FIT < 10
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	4846	> 100
ESD ─ Human body model (HBM) rating JS001 (Total samples from one wafer lot)	3	Pass +/-1000 V
ESD ─ Charged device model (CDM) rating JS002 (Total samples from one wafer lot)	3	Pass +/-250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85°C (Total samples from one wafer lot)	6	Pass

Table 7-2 Package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Amkor Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C Total samples from three different assembly lots	582	582	Pass
Temperature cycle: JESD22-A104 Temp Cycle, Cond B -55C to 125C; 500 and 1000 cycles Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration Total samples from three different assembly lots	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	120	120	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500/ 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

7.2 Device characteristics

Table 7-3 Device characteristics

Category	Definition
Device name	SM8150
Package type	893B MPSP
Package body size	12.4 mm × 12.4 mm × 0.58 mm

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Table 7-3 Device characteristics (cont.)

Category	Definition
Lead count	893
Lead composition	SAC125/Ni
Fab process	7 nm
Fab sites	TSMC
Assembly sites	Amkor, Korea; Amkor, Japan
Solder ball pitch	0.35 mm

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8 Revision history

NOTE: See the *SM8150 Chipset Announcement* (80-PD867-700) for information on critical issues and announcements that may affect the design and schedule. The announcements may affect a single device, multiple devices, or software.

Subscribe to the chipset announcement to be automatically notified (via email) of the future revisions.

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	December 2017	Initial release
B	February 2018	■ Global: Updated WCN3990B to WCN3998, QCA6436 to QCA643x, and QCA6426 to QCA642x though out the doc ■ Figure 1-1 *Functional block diagram*: Updated the WCD9360 and AQT1000 blocks ■ Table 1-1 *SM8150 features*: □ Updated the Kryo Gold target frequency □ Updated the Qualcomm Hexagon coprocessor version □ Updated HS-UART availability for GPIO QUPs ■ Chapter 2 *Pin definitions*: Added the link for the 80-PD867-1A reference document ■ Table 2-3 *Bottom pin descriptions – GPIO pins*: Added PCM functions to the GPIO pins ■ Chapter 3 *Electrical specifications*: Added Section 3.3 *Power distribution network* ■ Chapter 4 *Mechanical information*: Added TBD information for Section 4.3 *Device ordering information*, Section 4.4 *Device moisture sensitivity level*, and Section 4.5 *Thermal characteristics* ■ Chapter 5 *Carrier, handling, and storage information*: Added the TBD information ■ Chapter 6 *PCB mounting guidelines*: Added the TBD information ■ Section 7.2 *Device characteristics*: Added the TBD information
C	March 2018	■ Cover page: Updated the low-power audio subsystem features ■ Figure 1-1 *SM8150 functional block diagram and example application*: Removed AQT1000 and replaced WCD9360 with WCD934x ■ Table 1-1 *SM8150 features*: □ Updated the codec features for WCD9340/WCD9341 support □ Removed the I^2S Hi-Fi DAC section □ Updated the audio interfaces

Revision	Date	Description
D	April 2018	■ *Table 1-1 SM8150 features* □ Updated the application processor target frequency and L2 cache size □ Added QBT1600 to fingerprint support ■ Figure 1-1 SM8150 functional block diagram and example application: □ Removed the I^2C connection for HL6101 □ Added PM8009 to the diagram □ Added QBT1600 to the diagram ■ *Table 2-2 Bottom pin descriptions – primary pins:* Corrected the PCIE0 description to PCIe Gen 3 ■ *Chapter 3 Electrical specifications* □ Added Table 3-1 Absolute maximum ratings □ Added Table 3-2 Operating conditions □ Added Section 3.4 Average operating current through *Section 3.12 RF and power management interfaces* ■ *Chapter 4 Mechanical information* □ Added Section 4.2 Part marking □ Added Section 4.3.1 Specification-compliant devices

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Revision	Date	Description
E	June 2018	■ Global: Changed SDM855 to SM8150, SDA855 to SM8150P, PM855 to PM8150, PM855B to PM8150B, PM855A to PM8150A, PM855L to PM8150L, and SDR855 to SDR8150 ■ SM8150 high-level block diagram and 893 MPSP drawing: Updated the diagram for I2S ■ Figure 1-1 SM8150 functional block diagram and example application: removed QTC800H/801S as improveTouch is defeatured from the chipset. ■ *Table 1-1 SM8150 features* □ Updated 3x UL CA to 2x UL CA □ Removed QTC800H/801S as improveTouch is defeatured from the chipset □ Updated Audio interfaces for MI2S □ Updated PCM/TDM ■ *Table 2-3 Bottom pin descriptions – GPIO pins* □ Updated I2S functions for GPIO_148 to GPIO_152 □ Updated PCIe function names for GPIO_35, 36, 102, and 103 to follow the PCIe naming convention □ Corrected GPIO_155, 157, 158, 160, 164, 166, 168 to No wakeup support □ Added a table footnote to refer 80-PD867-1A for detailed GPIO configurations. ■ Table 3-4 PDN specifications–DDR rails: Updated PDN specs for VDDIO_EBI/VDDIO_CK_EBI ■ Table 3-5 PDN specifications–SerDes rails: Updated PDN specs for VDDA_USB1_SS_DP_CORE as it is changed to VREG_L18A_0P9 ■ Table 3-23 I2S interface timing: Updated t(HC), t(LC), SD and WS input hold time based on characterization data ■ Table 3-34 Supported SPMI standards and exceptions: Updated t(hr), t(dtr), t(HC), t(LC) for Master mode and Slave mode ■ Table 3-28 SPI master timing characteristics for QUP_17 and QUP_19: Corrected SPI max frequency to 25 MHz ■ Figure 4-3 SM8150 example device identification code: Added a note regarding ES1 product name in the identification code

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Revision	Date	Description
F	August 2018	■ Figure 1-1 SM8150 functional block diagram and example application: Updated the number of MIPI_RFFE interfaces SM8150 supports to 4 ■ Table 1-1 SM8150 features: Updated PCM/TDM support to up to 32 channels per individual interface ■ Table 1-2 Key modem features: Corrected carrier aggregation uplink to up to 40 MHz ■ Figure 2-2 SM8150 bottom pin assignments: Corrected pin names for pin U28, U29, V28 and V29 ■ Table 2-3 Bottom pin descriptions – GPIO pins: Removed RFFE4 and RFFE5 support from GPIO_79, PIO_80, GPIO_81, and GPIO82 ■ Table 2-4 Bottom pin descriptions – power-supply pins: Corrected pin name and functional description for pin U28, U29, V28 and V29 ■ Figure 4-3 SM8150 example device identification code: Corrected the table by swapping the Number of pins column and Package type column ■ Table 4-3 Device identification details: □ Corrected ES1 comments to 6x CA □ Added ES2 sample details
G	October 2, 2018	■ Table 1-1 SM8150 features: Updated the application processor maximum operating frequencies for Kryo 485 ■ Table 3-1 Absolute maximum ratings: Updated absolute maximum ratings ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1*:* Added this table ■ Table 3-3 Operating conditions: Updated operating conditions ■ Figure 3-9 PCM/TDM timing diagram: Corrected t(HC) and t(LC) labels on the timing diagram ■ Figure 4-1 Simplified MPSP893 outline drawing: Updated the note for coplanarity specification ■ Table 4-1 Device marking line definitions: Added an assembly site ■ Table 4-3 *Device identification details:* Added ES3 sample details ■ Section 4.5 *Device moisture sensitivity level:* Changed the MSL rating from a target of MSL3 to MSL3
H	October 31, 2018	■ Table 3-1 *Absolute maximum ratings*: Updated absolute maximum rating for VDDA_USB1_SS_DP_CORE and VDDA_WCSS_ADCDAC ■ Table 3-3 *Operating conditions*: Updated operating conditions for VDDA_USB1_SS_DP_CORE, VDDA_WCSS_ADCDAC and Device junction temperature ■ Table 3-7 *Dhrystone and rock bottom maximum power*: Updated Dhrytone and Rock Bottom maximum power specifications ■ Figure 3-10 *SPI master timing diagram*: Updated SPI master timing diagram ■ Table 3-29 *SPI master timing characteristics for QUP_17 and QUP_19:* Updated SPI master timing characteristics ■ Table 4-3 *Device identification details:* Added CS sample details ■ Table 7-1 *Silicon reliability results:* Added this table ■ Table 7-2 *Package reliability results*: Added this table
Revision I was omitted in accordance with QTI document conventions.		

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Revision	Date	Description
J	December 2018	■ Global: Updated the title to SM8150/SM8150P throughout the document ■ Chapter 1 *Introduction*: Added notes to clarify features not applicable to SM8150P ■ Table 2-3 *Bottom pin descriptions – GPIO pins*: Removed QSPI alternate function from GPIO_88 to GPIO_94 as it is not supported ■ Table 3-4 *PDN specifications*: Added a note that VDD_MODEM PDN specs is for SM8150 only ■ Table 3-6 *PDN specifications–SerDes rails*: Added a note that VDDA_QLINK_LV, VDDA_QLINK_LV_CK and VDDA_QLINK_HV_CK PDN specs are for SM8150 only ■ Table 3-14 *Supported MIPI_CSI standards and exceptions*: Updated feature exception that the maximum validated MIPI CSI C-PHY data rate is 1.5 Gsps ■ Table 4-3 *Device identification details*: □ Added SM8150P CS sample details □ Added hardware revision information for all the devices
K	January 2019	■ Device description: Added UFS 3.0 Gear 4 Rate A support ■ Figure 1-1SM8150 functional block diagram and example application: Updated UFS 2.1 gear 3 to UFS 3.0 Gear 4 Rate A ■ Table 1-1 SM8150/SM8150P features: Updated the External memory via UFS capability to UFS 3.0 Gear 4 Rate A ■ Table 3-19 Supported PCIe standards and exceptions: Updated the feature exception to Link upconfigure capability ■ Table 3-20 Supported UFS standards and exceptions: Updated the applicable standard version to 3.0 and feature exception to Rate B
L	March 2019	■ Table 1-1 SM8150/SM8150P features: □ Added Kryo Gold prime core F_{max} for SM8150 AC variant □ Added GPU F_{max} for SM8150 AB and SM8150 AC variants ■ Table 3-1 Absolute maximum ratings: Added storage temperature parameters and notes ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Added Nominal-L1 mode for VDD_GFX for SM8150 AC ■ Table 3-3 Operating conditions: Removed ambient temperature and associated footnotes ■ Section 4.3.1 Specification-compliant devices: □ Updated the device identification code details □ Added device identification code examples ■ Table 4-4 Device identification details: □ Added Gold prime F_{max} and GPU F_{max} □ Added SM8150 AC variant ES sample
M	April 2019	■ Table 2.2 Bottom pin descriptions – primary pins: Updated pad type of pins N31, M31, M30, P31, and P30 ■ Table 4-4 Device identification details: □ Added SM8150 AC variant ES sample □ Added SM8150P AC variant ES sample

Revision	Date	Description
N	May 2019	■ Table 2-3 Bottom pin descriptions – GPIO pins: □ AL30 pin: PCIE0_RST_N is marked optional and added a footnote indicating that it is a software implementation as bit bang on the same GPIO □ AM30 pin: PCIE1_RST_N is marked optional and added a footnote indicating that it is a software implementation as bit bang on the same GPIO
Revision O was omitted in accordance with QTI document conventions.		
P	October 2019	■ Table 7-1 Silicon reliability results: Updated the silicon reliability results
Revision Q was omitted in accordance with QTI document conventions.		
R	November 2019	■ Table 7-1 *Silicon reliability results*: Updated HBM and CDM from JESD to JS001 and JS002.

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