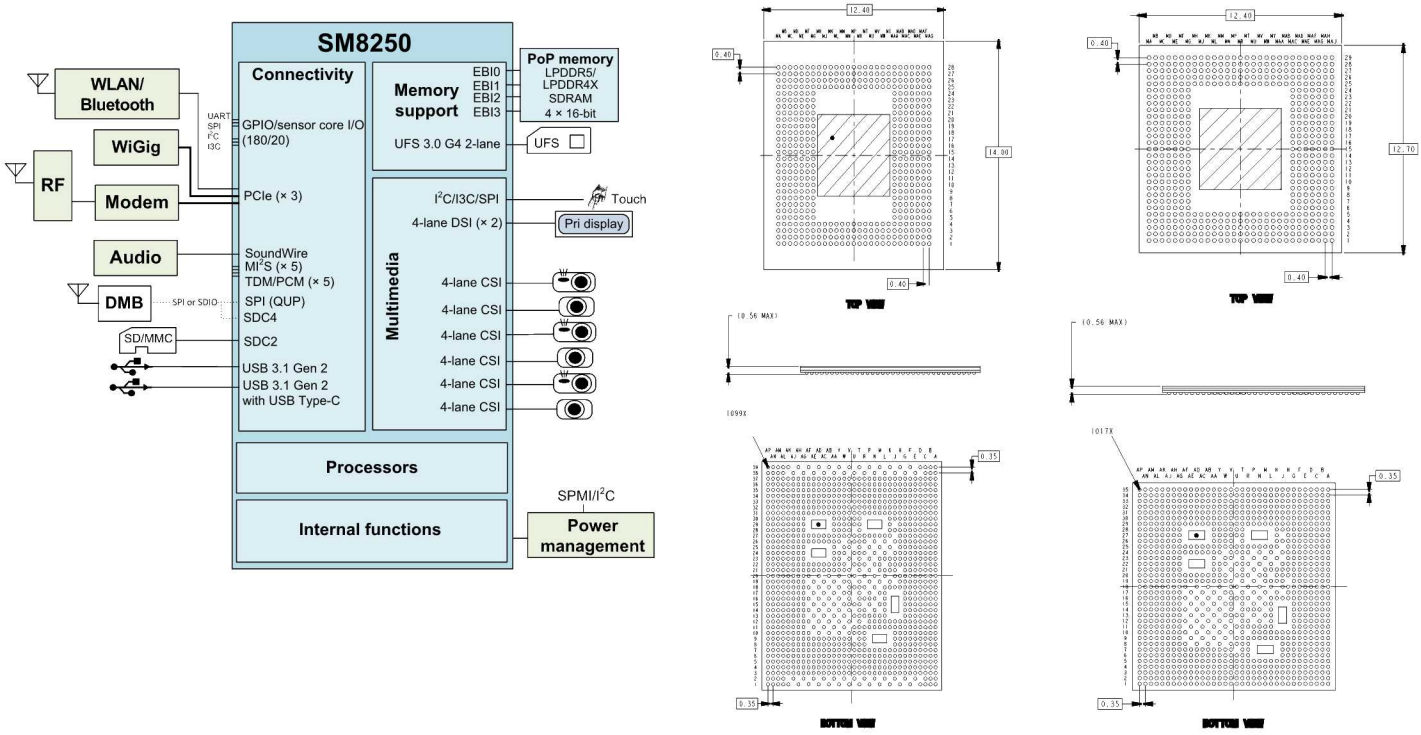
Qualcomm Technologies, Inc.

Device description

SM8250 is the new generation Qualcomm® Snapdragon™ premium-tier processor with external 4G/5G modem (SDX55M). It is designed with the 7 nm process, for superior performance and power efficiency. SM8250 includes the following key components:

- Qualcomm® Kryo™ 585 CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 650 GPU for the highest in graphics performance and power efficiency
- Qualcomm® Hexagon™ DSP with quad Hexagon Vector eXtensions (HVX) processor for vision processing and machine learning
- Qualcomm Spectra™ 480 image processing engine for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 995 DPU for on-device and external ultra HD display support
- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9380/WCD9385 audio codec for low power voice processing and audiophile quality audio playback
- Qualcomm® Sensing Hub for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU240) for advanced secure use cases
- Qualcomm® Neural Processing Unit (NPU230) for high-performance machine learning use cases
- External 802.11ax, 2 × 2 MIMO, and Bluetooth 5.1
- Quad-channel package-on-package (PoP) high-speed LPDDR5/LPDDR4X SDRAM

SM8250 high-level block diagram and 1099 (SM8250–LPDDR5)/1017 (SM8250–LPDDR4X) MPSP drawing



Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

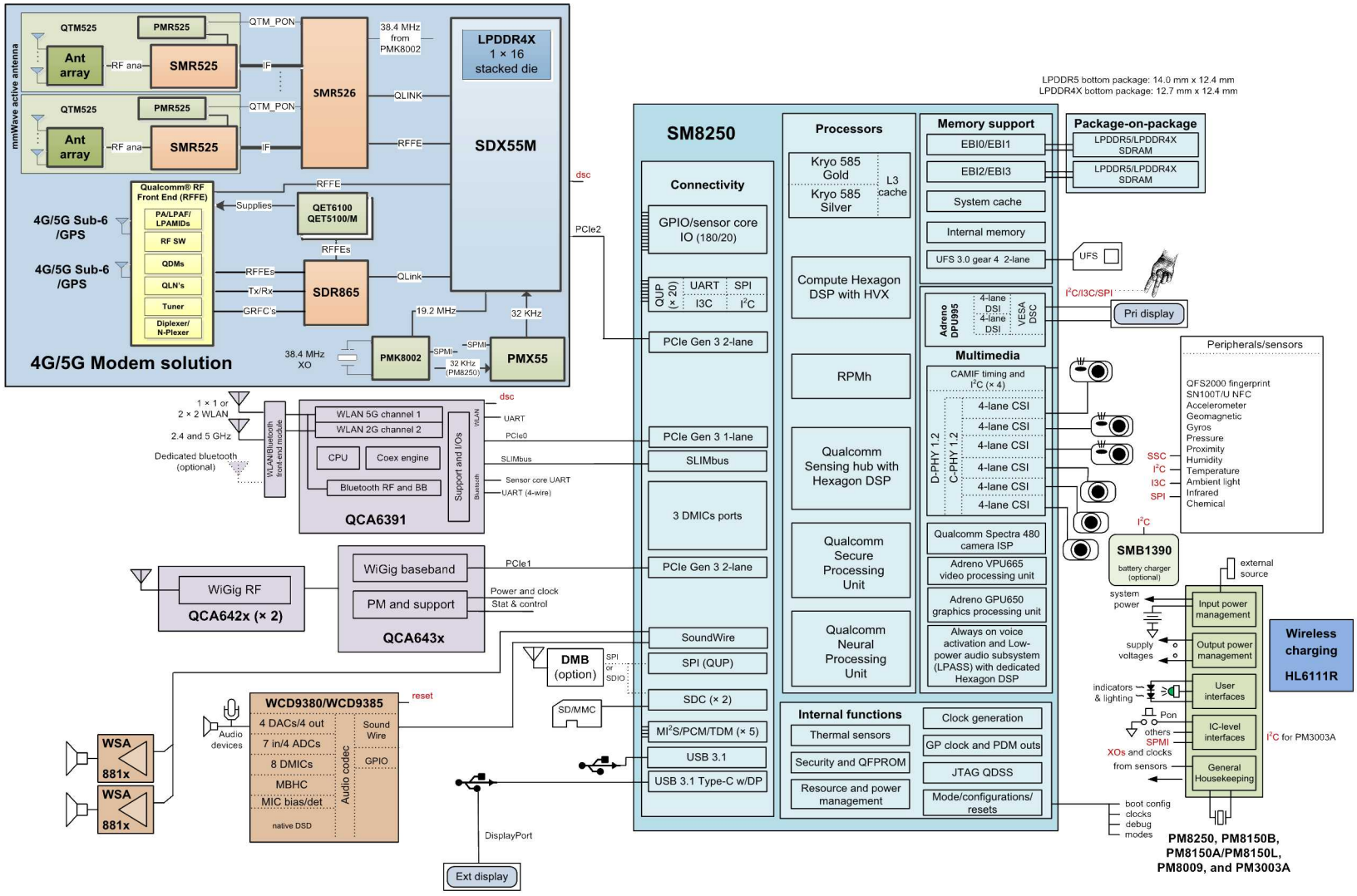


Figure 1-1 SM8250 functional block diagram and example application

1.2 SM8250 features

NOTE: Some of the hardware features integrated within the SM8250 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8250 features.

NOTE: The SM8250 supports LPDDR5 and LPDDR4X in two different package dimensions. The SM8250-LPDDR5 will be sampled first, followed by the SM8250-LPDDR4X two months later for commercial sampling.

Table 1-1 SM8250 features

Feature	SM8250 capability
Processors	
Applications	Kryo 585 – 64-bit applications processor with a 4 MB L3 cache ■ Quad high-performance Kryo Gold cores □ Three Kryo Gold cores with a 256 KB L2 cache per core, Fmax at 2.419 GHz □ One Kryo Gold prime core with a 512 KB L2 cache, Fmax at 2.842 GHz for SM8250 AA variant, Fmax at 3.091 GHz for SM8250 AB variant, and Fmax at 3.1872 GHz for SM8250 AC variant. ■ Quad low-power Kryo Silver cores with a 128 KB L2 cache per core, Fmax at 1.805 GHz.
Digital signal processing	Compute Hexagon DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Coprocessor (Hexagon CP) 2.0 ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The HCP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. Audio Hexagon DSP dedicated to audio subsystem Sensor Hexagon DSP in the Qualcomm Sensing Hub to support always-on, low-power use cases All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Artificial intelligence	Qualcomm NPU230 dedicated neural processing unit for performance and always-on neural network (NN) use cases. It incorporates an NN matrix engine to ensure efficient execution of various neural networks and their parameters. The NPU may be used for typical imaging, video, audio, and data-based NN use cases and will typically be used in conjunction with the compute Hexagon DSP subsystem.
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR5 or LPDDR4X SDRAM (4 × 16-bit) designed for a 2750 MHz (LPDDR5) or 2133 MHz (LPDDR4X) clock and system cache

Table 1-1 SM8250 features (cont.)

Feature	SM8250 capability
External memory	
Via UFS	UFS 3.1 gear 4 – for on-board memory
Via SDC	SD v3.0 4 bit for SD card
Multimedia	
Adreno display processing unit (DPU)	Adreno DPU 995, supports up to three 4K display (one internal display through DSI and two external displays through DisplayPort)
Display interface	Two 4-lane DSI D-PHY 1.2 or two 3-trio C-PHY v1.1 with VESA DSC v1.1 DisplayPort v1.4 at 8.1 Gbps/lane over Type-C with support for MST and VESA DSC v1.1 and FEC (USB3 and USB2 concurrency supported) Miracast – up to 4K60
Display performance	5040 × 2160 [1] at 60 Hz (or 120 Hz in VR mode), up to 30 bpp Two 2560 × 2560 [1] at 120 Hz for dual-panel VR displays, up to 30 bpp 4096 buffer width, and 16 hardware-layer composition
Display processing	Qualcomm® TruPalette™ Display Feature – HDR10+ and HDR10 tone mapping, color gamut mapping, six-zone, memory color, and picture adjust
Pixel processing	Qualcomm® Low-Power Picture Enhancement display – compression [Qualcomm® Universal Bandwidth Compression (UBWC 4.0, DSC v1.1)], CABL, FOSS, Qualcomm Local Tone Mapping, QSync, and destination scaler with DE
Camera support	
Performance	Qualcomm Spectra 480 ISP to support up to 12 cameras by D-PHY and 18 cameras by C-PHY (seven concurrent) ■ Real-time sensor input resolution: 25 + 25 + 2 + 2 + 2 + 2 + 2 ■ 64 MP 30 fps ZSL with a dual ISP ■ Hardware 2PD support and improved face detection ■ Hardware depth map engine and improved zzHDR ■ 4K120 camcorder and improved spatial noise reduction
Camera interface	MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 + 4 + 4 configuration ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port ■ C-PHY v1.2: 10.26 Gbps/trio on three trios per port
Adreno video processing unit (VPU)	■ Adreno VPU 665 – fifth-generation UHD video processing unit ■ Video decode up to 4K240/8K60 ■ Video encode up to 4K120/8K30 ■ Concurrent 4K60 decode and 4K30 encode for wireless display ■ Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs ■ Native encode support for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs ■ Improved encoder with up to 30% reduction in bit rate for same subjective quality video ■ New computer vision processor (CVP) for object detection and tracking
Adreno graphic processing unit (GPU)	■ Adreno GPU 650, Fmax at 587 MHz for SM8250 AA variant and Fmax at 670 MHz for SM8250 AB and AC variants – 4K 60 fps UI or 2X 2K 60 fps UI ■ OpenGL ES 3.2, Vulkan 1.1, DX12 FL 12_1 ■ OpenCL 2.0 full profile

Table 1-1 SM8250 features (cont.)

Feature	SM8250 capability
Audio	
Codec	Integrated within the WCD9380/WCD9385 high fidelity audio codec: ■ Four DACs; four outputs ■ Seven differential analog inputs; four ADCs ■ Eight digital microphones ■ High dynamic range recording ■ HPH load equalization ■ Native DSD, MBHC, and ANC ■ 122 dB dynamic range for HPH ports ■ 32-bit DAC ■ 44.1 kHz family native playback ■ Four GPIOs
Speaker amplifier	Integrated within the WSA8810/WSA8815 class D/G, low noise smart amplifier: ■ 2 W/4 W output power into 8 Ω load ■ Integrated SmartBoost ■ Integrated feedback speaker protection for excursion and temperature control of the transducers ■ Support for receiver assist speaker (RAS) or speaker as receiver (SAR) with handset ANC
Low-power audio subsystem (LPASS)	■ Essential voice communications package ■ Advanced voice communications package ■ Voice UI voice activation package ■ Voice UI speech enhancement package ■ 3D audio capture package
Audio interfaces	SLIMbus: ■ QCA639x SLIMbus SWR: ■ SoundWire interface (two Tx and two Rx data lines; optional configuration of three Tx and one Rx data lines) for codec ■ Dedicated SoundWire interface for smart speaker amplifier Digital Mic: ■ 3 DMIC ports supports up to 6 DMICs MI^{2}S: ■ Five MI2S with 2x data lanes to support full duplex stereo, or up to 4 channel Tx/Rx application ■ One MI2S supports 4 data lanes for up to 8 channels Tx/Rx application TDM/PCM: ■ Up to 32 channels per individual interface ■ Short, long, and one-slot sync mode ■ Maximum clock frequency of 24.576 MHz
Digital mobile broadcast (DMB)	External IC required with SPI or SDIO interface

Table 1-1 SM8250 features (cont.)

Feature	SM8250 capability
Connectivity	
Qualcomm universal peripheral (QUP) ports	20: 7 bits each for four QUPs and 4 bits each for the other QUPs; multiplexed serial interface functions
UART	UART interface available on all QUPs. HS-UART available on GPIO QUP6/QUP7/QUP12/QUP13/QUP18/QUP19/ Qualcomm Sensing Hub
I^2C	I^2C interface available on all QUPs up to 1 Mbps for touch, sensors, near field communicator (NFC), and so on; dedicated controller for each port
I3C	I3C interface available on GPIO QUP0/QUP1/QUP8/QUP14 and Qualcomm Sensing Hub QUP0/QUP1/QUP2. I3C IBI will not be supported.
SPI	SPI interfaces available on all QUPs for cameras, sensors, and so on; dedicated controller for each port
CCI I^2C	Four dedicated I^2C interfaces for camera
USB	Two USB 3.1 ports, support Type-C with DisplayPort v1.4 in one port
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card and DMB
Wireless connectivity	QCA639x 802.11ax RFQCA643x/QCA642x 802.11ad at 60 GHz
Touchscreen support	Capacitive panels via ext IC (I^2C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display. QFS2000/QFS2080/QFS2630 modules.
Configurable GPIOs	
Number of GPIO ports	180 – GPIO_0 to GPIO_179
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	SPU-240 with planned certification enabling Android Strongbox and iUICC, Secure Boot 3.0, Debug security, Key provisioning security, TrustZone, Qualcomm® Trusted Execution Environment v5, hardware-backed KeyStore, combined image signing, image encryption, secure peripherals, Inline Crypto Engine (ICE), File-based Encryption (FBE)
Crypto engines	Crypto engine v5 (CE5), Qualcomm to submit for FIPS certification
TrustZone services	Secure file system, Fast Trusted Storage
DRM support in hardware	PlayReady SL2000/SL3000, Widevine level 1 and level 3, ISDB-T
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sand-boxing
Boot sequence	■ 1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) rest of subsystems ■ Emergency boot over USB 3.1

Table 1-1 SM8250 features (cont.)

Feature	SM8250 capability
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	2-line SPMI; plus other lines, as needed, via GPIOs, I^2C
Wireless connectivity WLAN Bluetooth	 PCIe interface SLIMbus/UART interface
Fabrication technology and package	
Digital die	7 nm process
PoP – small, thermally efficient package Bottom pin array Top pin array Bottom pin array Top pin array	MPSP1099 (SM8250-LPDDR5): 14.0 × 12.4 × 0.56 mm max (without memory device on top) MPSP1017 (SM8250-LPDDR4X): 12.7 × 12.4 × 0.56 mm max (without memory device on top) SM8250-LPDDR5: Bottom: 1099-pin picoscale package (1099 PSP); 0.35 mm pitch Top: 496-pin nanoscale package (496 NSP); 0.4 mm pitch SM8250-LPDDR4X: Bottom: 1017-pin picoscale package (1017 PSP); 0.35 mm pitch Top: 556-pin nanoscale package (556 NSP); 0.4 mm pitch

1. Higher resolution and wider aspect ratio displays can be supported. Exact panel details and timings are required to determine if it can be supported.

2 Pin definitions

The SM8250 is the lower device within a PoP system, as illustrated and explained in Figure 2-1.

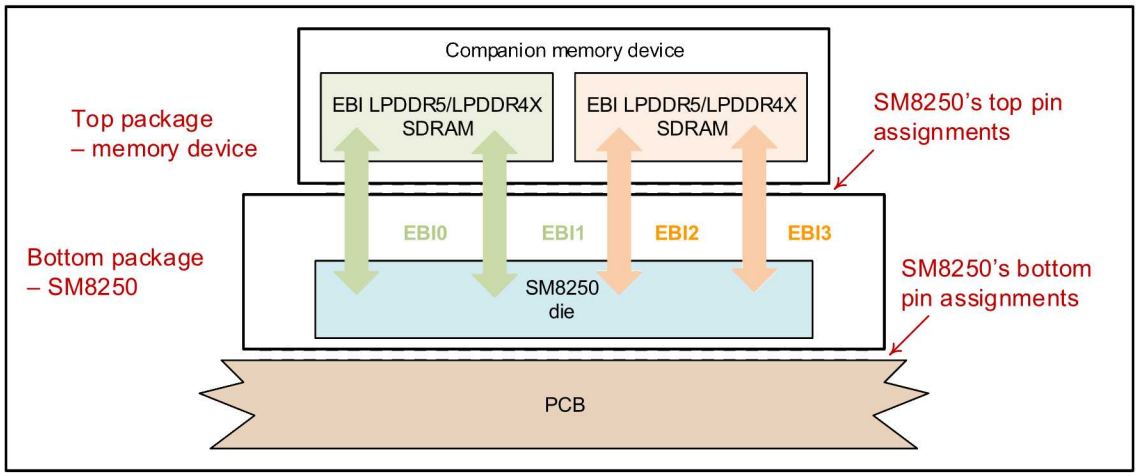


Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8250 bottom pins (Section 2.2)
- SM8250 top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O parameter definitions

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX_0	Pad group 0 (control signals); 1.8 V
PX_2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_10	Pad group 10 (UFS1_REF_CLK and UFS1_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.8 V
PX_13	Pad group 13 (secure processor unit [SPU]); 1.85 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin assignments – bottom

2.2.1 Pin map – bottom

The SM8250 is available in the MPSP1099 (for LPDDR5) or MPSP1017 (for LPDDR4X). Its bottom surface is equivalent to a 1099 PSP (for LPDDR5) or 1017 PSP (for LPDDR4X) that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details and Section 2.3 for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inches × 11 inches hard copy. Other viewing options are available:

- Print that one page on an 11 inches × 17 inches sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.
- Download the *SM8250 Pin Assignment and GPIO Configuration Spreadsheet* (80-PL546-1A) – this Microsoft Excel spreadsheet lists all SM8250 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PL546-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PL546-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

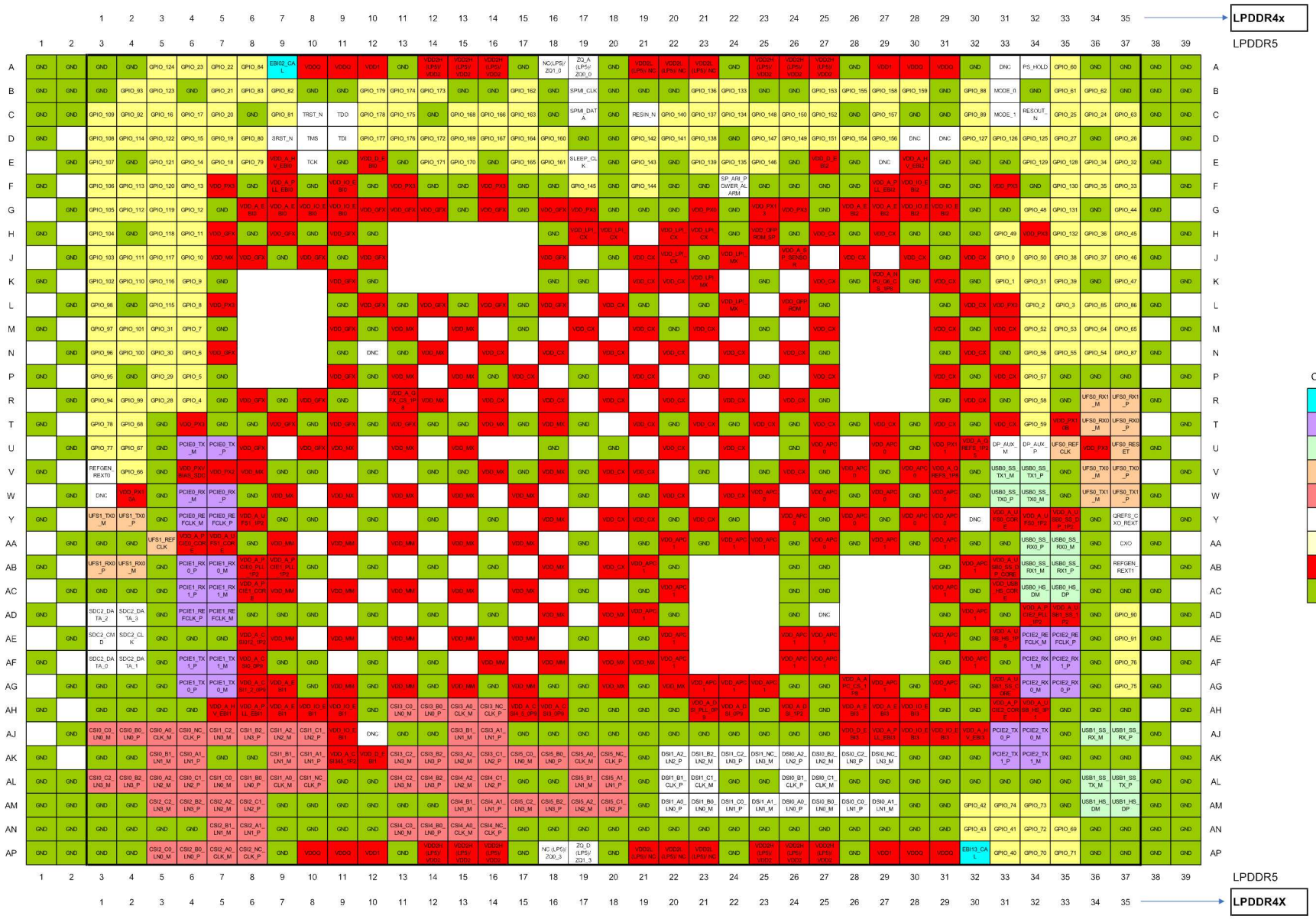


Figure 2-2 SM8250 bottom pin assignments

2.2.2 Pin descriptions – bottom

The bottom pins are described in Table 2-2 through Table 2-4.

Table 2-2 Bottom pin descriptions – general pins

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AJ3	AJ5	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – minus MIPI CSI 0 (CPHY), trio lane 0 – A
AK4	AK6	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – plus MIPI CSI 0 (CPHY), trio lane 1 – A
AL3	AL5	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – minus MIPI CSI 0 (CPHY), trio lane 2 – A
AJ2	AJ4	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – plus MIPI CSI 0 (CPHY), trio lane 0 – B
AK3	AK5	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – minus MIPI CSI 0 (CPHY), trio lane 1 – B
AL2	AL4	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – plus MIPI CSI 0 (CPHY), trio lane 2 – B
AJ1	AJ3	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – minus MIPI CSI 0 (CPHY), trio lane 0 – C
AL4	AL6	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – plus MIPI CSI 0 (CPHY), trio lane 1 – C
AL1	AL3	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – minus MIPI CSI 0 (CPHY), trio lane 2 – C
AJ4	AJ6	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – plus MIPI CSI 0 (CPHY), no connect
AL7	AL9	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – minus MIPI CSI 1 (CPHY), trio lane 0 – A
AK8	AK10	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – plus MIPI CSI 1 (CPHY), trio lane 1 – A
AJ7	AJ9	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – minus MIPI CSI 1 (CPHY), trio lane 2 – A
AL6	AL8	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – plus MIPI CSI 1 (CPHY), trio lane 0 – B
AK7	AK9	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – minus MIPI CSI 1 (CPHY), trio lane 1 – B
AJ6	AJ8	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – plus MIPI CSI 1 (CPHY), trio lane 2 – B
AL5	AL7	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – minus MIPI CSI 1 (CPHY), trio lane 0 – C

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AJ8	AJ10	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – plus MIPI CSI 1 (CPHY), trio lane 1 – C
AJ5	AJ7	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – minus MIPI CSI 1 (CPHY), trio lane 2 – C
AL8	AL10	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – plus MIPI CSI 1 (CPHY), no connect
AP5	AP7	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – minus MIPI CSI 2 (CPHY), trio lane 0 – A
AN6	AN8	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – plus MIPI CSI 2 (CPHY), trio lane 1 – A
AM5	AM7	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – minus MIPI CSI 2 (CPHY), trio lane 2 – A
AP4	AP6	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – plus MIPI CSI 2 (CPHY), trio lane 0 – B
AN5	AN7	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – minus MIPI CSI 2 (CPHY), trio lane 1 – B
AM4	AM6	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – plus MIPI CSI 2 (CPHY), trio lane 2 – B
AP3	AP5	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – minus MIPI CSI 2 (CPHY), trio lane 0 – C
AM6	AM8	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – plus MIPI CSI 2 (CPHY), trio lane 1 – C
AM3	AM5	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – minus MIPI CSI 2 (CPHY), trio lane 2 – C
AP6	AP8	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – plus MIPI CSI 2 (CPHY), no connect
AH13	AH15	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – minus MIPI CSI 3 (CPHY), trio lane 0 – A
AJ14	AJ16	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – plus MIPI CSI 3 (CPHY), trio lane 1 – A
AK13	AK15	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – minus MIPI CSI 3 (CPHY), trio lane 2 – A
AH12	AH14	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – plus MIPI CSI 3 (CPHY), trio lane 0 – B
AJ13	AJ15	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – minus MIPI CSI 3 (CPHY), trio lane 1 – B
AK12	AK14	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – plus MIPI CSI 3 (CPHY), trio lane 2 – B

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AH11	AH13	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – minus MIPI CSI 3 (CPHY), trio lane 0 – C
AK14	AK16	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – plus MIPI CSI 3 (CPHY), trio lane 1 – C
AK11	AK13	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – minus MIPI CSI 3 (CPHY), trio lane 2 – C
AH14	AH16	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – plus MIPI CSI 3 (CPHY), no connect
AN13	AN15	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential clock – minus MIPI CSI 4 (CPHY), trio lane 0 – A
AM14	AM16	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – plus MIPI CSI 4 (CPHY), trio lane 1 – A
AL13	AL15	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – minus MIPI CSI 4 (CPHY), trio lane 2 – A
AN12	AN14	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – plus MIPI CSI 4 (CPHY), trio lane 0 – B
AM13	AM15	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – minus MIPI CSI 4 (CPHY), trio lane 1 – B
AL12	AL14	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – plus MIPI CSI 4 (CPHY), trio lane 2 – B
AN11	AN13	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – minus MIPI CSI 4 (CPHY), trio lane 0 – C
AL14	AL16	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – plus MIPI CSI 4 (CPHY), trio lane 1 – C
AL11	AL13	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – minus MIPI CSI 4 (CPHY), trio lane 2 – C
AN14	AN16	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential clock – plus MIPI CSI 4 (CPHY), no connect
AK17	AK19	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential clock – minus MIPI CSI 5 (CPHY), trio lane 0 – A
AL18	AL20	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – plus MIPI CSI 5 (CPHY), trio lane 1 – A
AM17	AM19	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – minus MIPI CSI 5 (CPHY), trio lane 2 – A
AK16	AK18	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – plus MIPI CSI 5 (CPHY), trio lane 0 – B
AL17	AL19	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – minus MIPI CSI 5 (CPHY), trio lane 1 – B

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AM16	AM18	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – plus MIPI CSI 5 (CPHY), trio lane 2 – B
AK15	AK17	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – minus MIPI CSI 5 (CPHY), trio lane 0 – C
AM18	AM20	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – plus MIPI CSI 5 (CPHY), trio lane 1 – C
AM15	AM17	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – minus MIPI CSI 5 (CPHY), trio lane 2 – C
AK18	AK20	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential clock – plus MIPI CSI 5 (CPHY), no connect
AA35	AA37	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
AM24	AM26	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – plus MIPI DSI 0 (CPHY), trio lane 0 – A
AM27	AM29	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – minus MIPI DSI 0 (CPHY), trio lane 1 – A
AK24	AK26	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – plus MIPI DSI 0 (CPHY), trio lane 2 – A
AM25	AM27	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – minus MIPI DSI 0 (CPHY), trio lane 0 – B
AL24	AL26	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – plus MIPI DSI 0 (CPHY), trio lane 1 – B
AK25	AK27	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – minus MIPI DSI 0 (CPHY), trio lane 2 – B
AM26	AM28	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – plus MIPI DSI 0 (CPHY), trio lane 0 – C
AL25	AL27	DSI0_C1_CLK_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – minus MIPI DSI 0 (CPHY), trio lane 1 – C
AK26	AK28	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – plus MIPI DSI 0 (CPHY), trio lane 2 – C
AK27	AK29	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – minus MIPI DSI 0 (CPHY), no connect
AM20	AM22	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – plus MIPI DSI 1 (CPHY), trio lane 0 – A
AM23	AM25	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – minus MIPI DSI 1 (CPHY), trio lane 1 – A
AK20	AK22	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – plus MIPI DSI 1 (CPHY), trio lane 2 – A

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AM21	AM23	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – minus MIPI DSI 1 (CPHY), trio lane 0 – B
AL20	AL22	DSI1_B1_CLK_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – plus MIPI DSI 1 (CPHY), trio lane 1 – B
AK21	AK23	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – minus MIPI DSI 1 (CPHY), trio lane 2 – B
AM22	AM24	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – plus MIPI DSI 1 (CPHY), trio lane 0 – C
AL21	AL23	DSI1_C1_CLK_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – minus MIPI DSI 1 (CPHY), trio lane 1 – C
AK22	AK24	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – plus MIPI DSI 1 (CPHY), trio lane 2 – C
AK23	AK25	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – minus MIPI DSI 1 (CPHY), no connect
A7	A9	EBI02_CAL	PX_3	AI	EBI0/1 LPDDR5/LPDDR4X calibration resistor
AP30	AP32	EBI13_CAL	PX_3	AI	EBI2/3 LPDDR5/LPDDR4X calibration resistor
U31	U33	DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – minus
U32	U34	DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – plus
B31	B33	MODE_0	PX_0	DI-S PD	Mode control bit 0 – unconnected for native mode
C31	C33	MODE_1	PX_0	DI-S PD	Mode control bit 1 – unconnected for native mode
Y4	Y6	PCIE0_REFCLK_M	–	AO	PCIe 0 Gen 3 reference clock – minus
Y5	Y7	PCIE0_REFCLK_P	–	AO	PCIe 0 Gen 3 reference clock – plus
W4	W6	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – minus
W5	W7	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – plus
U4	U6	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – minus
U5	U7	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – plus
AD5	AD7	PCIE1_REFCLK_M	–	AO	PCIe 1 Gen 3 reference clock – minus
AD4	AD6	PCIE1_REFCLK_P	–	AO	PCIe 1 Gen 3 reference clock – plus
AB5	AB7	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive 0 – minus
AB4	AB6	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive 0 – plus
AC5	AC7	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive 1 – minus
AC4	AC6	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive 1 – plus
AG5	AG7	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit 0 – minus
AG4	AG6	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit 0 – plus
AF5	AF7	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit 1 – minus

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AF4	AF6	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit 1 – plus
AE32	AE34	PCIE2_REFCLK_M	–	AO	PCIe 2 Gen3 reference clock - minus
AE33	AE35	PCIE2_REFCLK_P	–	AO	PCIe 2 Gen3 reference clock - plus
AG32	AG34	PCIE2_RX0_M		AI	PCIe 2 Gen 3 receive 0 - minus
AG33	AG35	PCIE2_RX0_P		AI	PCIe 2 Gen 3 receive 0 - plus
AF32	AF34	PCIE2_RX1_M		AI	PCIe 2 Gen 3 receive 1 - minus
AF33	AF35	PCIE2_RX1_P		AI	PCIe 2 Gen 3 receive 1 - plus
AJ32	AJ34	PCIE2_TX0_M		AO	PCIe 2 Gen 3 transmit 0 - minus
AJ31	AJ33	PCIE2_TX0_P		AO	PCIe 2 Gen 3 transmit 0 - plus
AK32	AK34	PCIE2_TX1_M		AO	PCIe 2 Gen 3 transmit 1 - minus
AK31	AK33	PCIE2_TX1_P		AO	PCIe 2 Gen 3 transmit 1 - plus
A32	A34	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
Y35	Y37	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-die clocking
V1	V3	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
AB35	AB37	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
C19	C21	RESIN_N	PX_0	DI	Reset input
C32	C34	RESOUT_N	PX_3	DO	Reset output
AE2	AE4	SDC2_CLK	PX_2	BH-NP:pdpukp	Secure digital controller 2 clock
AE1	AE3	SDC2_CMD	PX_2	BH-PD:nppukp	Secure digital controller 2 command
AF1	AF3	SDC2_DATA_0	PX_2	BH-PD:nppukp	Secure digital controller 2 data bit 0
AF2	AF4	SDC2_DATA_1	PX_2	BH-PD:nppukp	Secure digital controller 2 data bit 1
AD1	AD3	SDC2_DATA_2	PX_2	BH-PD:nppukp	Secure digital controller 2 data bit 2
AD2	AD4	SDC2_DATA_3	PX_2	BH-PD:nppukp	Secure digital controller 2 data bit 3
E17	E19	SLEEP_CLK	PX_3	DI	Sleep clock
F22	F24	SP_ARI_POWER_ALARM	PX_13	DI	Battery removal alarm for secure processor unit
B17	B19	SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
C17	C19	SPMI_DATA	PX_0	B	Slave and PBUS interface for PMICs – data
D7	D9	SRST_N	PX_3	DI-PU	JTAG reset for debug
E8	E10	TCK	PX_3	DI-PU	JTAG clock input
D9	D11	TDI	PX_3	DI-PU:nppdkp	JTAG data input
C9	C11	TDO	PX_3	DO-Z	JTAG data output
D8	D10	TMS	PX_3	DI-PU:nppdkp	JTAG mode select input
C8	C10	TRST_N	PX_3	DI-PD:nppukp	JTAG reset

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
U33	U35	UFS0_REFCLK	PX_10	DO-Z PD:nppukp	UFS 0 reference clock
U35	U37	UFS0_RESET			UFS 0 reset
T34	T36	UFS0_RX0_M		AI	UFS 0 receive 0 – minus
T35	T37	UFS0_RX0_P		AI	UFS 0 receive 0 – plus
R34	R36	UFS0_RX1_M		AI	UFS 0 receive 1 – minus
R35	R37	UFS0_RX1_P		AI	UFS 0 receive 1 – plus
V34	V36	UFS0_TX0_M		AO	UFS 0 transmit 0 – minus
V35	V37	UFS0_TX0_P		AO	UFS 0 transmit 0 – plus
W34	W36	UFS0_TX1_M		AO	UFS 0 transmit 1 – minus
W35	W37	UFS0_TX1_P		AO	UFS 0 transmit 1 – plus
AA3	AA5	UFS1_REFCLK	PX_10	DO-Z PD:nppukp	UFS 1 reference clock
AB2	AB4	UFS1_RX0_M		AI	UFS 1 receive 0 – minus
AB1	AB3	UFS1_RX0_P		AI	UFS 1 receive 1 – plus
Y1	Y3	UFS1_TX0_M		AO	UFS 1 transmit 0 – minus
Y2	Y4	UFS1_TX0_P		AO	UFS 1 transmit 0 – plus
AC32	AC34	USB0_HS_DM	–	AI, AO	USB high-speed 0 data – minus
AC33	AC35	USB0_HS_DP	–	AI, AO	USB high-speed 0 data – plus
AA33	AA35	USB0_SS_RX0_M		AI	USB super-speed 0 receive 0 – minus
AA32	AA34	USB0_SS_RX0_P		AI	USB super-speed 0 receive 0 – plus
AB32	AB34	USB0_SS_RX1_M		AI	USB super-speed 0 receive 1 – minus
AB33	AB35	USB0_SS_RX1_P		AI	USB super-speed 0 receive 1 – plus
W32	W34	USB0_SS_TX0_M		AO	USB super-speed 0 transmit 0 – minus
W31	W33	USB0_SS_TX0_P		AO	USB super-speed 0 transmit 0 – plus
V31	V33	USB0_SS_TX1_M		AO	USB super-speed 0 transmit 1 – minus
V32	V34	USB0_SS_TX1_P		AO	USB super-speed 0 transmit 1 – plus
AM34	AM36	USB1_HS_DM	–	AI, AO	USB high-speed 1 data – minus
AM35	AM37	USB1_HS_DP	–	AI, AO	USB high-speed 1 data – plus
AJ34	AJ36	USB1_SS_RX_M	–	AI	USB super-speed 1 receive – minus
AJ35	AJ37	USB1_SS_RX_P	–	AI	USB super-speed 1 receive – plus
AL34	AL36	USB1_SS_TX_M	–	AO	USB super-speed 1 transmit – minus
AL35	AL37	USB1_SS_TX_P	–	AO	USB super-speed 1 transmit – plus
–	A19	ZQ_A		AI	LPDDR5 ZQ calibration for channels A and C

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
–	AP19	ZQ_D		AI	LPDDR5 ZQ calibration for channels B and D
A17		ZQ0_0	PX_3	AI	LPDDR4X ZQ calibration for rank 0 in channels A and B
AP16	–	ZQ0_3	PX_3	AI	LPDDR4X ZQ calibration for rank 0 in channels C and D
A16	–	ZQ1_0	PX_3	AI	LPDDR4X ZQ calibration for rank 1 in channels A and B
AP17		ZQ1_3	PX_3	AI	LPDDR4X ZQ calibration for rank 1 in channels C and D

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function–carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SM8250 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the *SM8250 Pin Assignment and GPIO Configuration Spreadsheet* (80-PL546-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PL546-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Table 2-3 Bottom pin descriptions – general-purpose input/output ports

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
B10	B12	GPIO_179	Y	SSC_19	3	PD:nppukp	Configurable I/O SSC I/O 19
C10	C12	GPIO_178	–	SSC_18	3	PD:nppukp	Configurable I/O SSC I/O 18
D10	D12	GPIO_177	Y	SSC_17 QDSS_GPIO_TRACEDATA_LOCA[15]	3	PD:nppukp	Configurable I/O SSC I/O 17 QDSS trace data 15 A
D11	D13	GPIO_176	–	SSC_16 QDSS_GPIO_TRACEDATA_LOCA[14]	3	PD:nppukp	Configurable I/O SSC I/O 16 QDSS trace data 14 A
C11	C13	GPIO_175	Y	SSC_15 QDSS_GPIO_TRACEDATA_LOCA[13]	3	PD:nppukp	Configurable I/O SSC I/O 15 QDSS trace data 13 A
B11	B13	GPIO_174	–	SSC_14 QDSS_GPIO_TRACEDATA_LOCA[12]	3	PD:nppukp	Configurable I/O SSC I/O 14 QDSS trace data 12 A
B12	B14	GPIO_173	–	SSC_13 QDSS_GPIO_TRACEDATA_LOCA[11]	3	PD:nppukp	Configurable I/O SSC I/O 13 QDSS trace data 11 A
D12	D14	GPIO_172	–	SSC_12 QDSS_GPIO_TRACEDATA_LOCA[10]	3	PD:nppukp	Configurable I/O SSC I/O 12 QDSS trace data 10 A
E12	E14	GPIO_171	–	SSC_11 QDSS_GPIO_TRACEDATA_LOCA[9]	3	PD:nppukp	Configurable I/O SSC I/O 11 QDSS trace data 9 A
E13	E15	GPIO_170	–	SSC_10 QDSS_GPIO_TRACECLK_LOCA	3	PD:nppukp	Configurable I/O SSC I/O 10 QDSS trace clock A
D13	D15	GPIO_169	–	SSC_9 QDSS_GPIO_TRACECTL_LOCA	3	PD:nppukp	Configurable I/O SSC I/O 9 QDSS trace control A
C13	C15	GPIO_168	–	SSC_8 QDSS_GPIO_TRACEDATA_LOCA[8]	3	PD:nppukp	Configurable I/O SSC I/O 8 QDSS trace data 8 A
D14	D16	GPIO_167	Y	SSC_7 QDSS_GPIO_TRACEDATA_LOCA[7]	3	PD:nppukp	Configurable I/O SSC I/O 7 QDSS trace data 7 A
C14	C16	GPIO_166	Y	SSC_6 QDSS_GPIO_TRACEDATA_LOCA[6]	3	PD:nppukp	Configurable I/O SSC I/O 6 QDSS trace data 6 A
E15	E17	GPIO_165	–	SSC_5 QDSS_GPIO_TRACEDATA_LOCA[5]	3	PD:nppukp	Configurable I/O SSC I/O 5 QDSS trace data 5 A
D15	D17	GPIO_164	Y	SSC_4 QDSS_GPIO_TRACEDATA_LOCA[4]	3	PD:nppukp	Configurable I/O SSC I/O 4 QDSS trace data 4 A

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
C15	C17	GPIO_163	–	SSC_3 QDSS_GPIO_TRACEDATA_LOCA[3]	3	PD:nppukp	Configurable I/O SSC I/O 3 QDSS trace data 3 A
B15	B17	GPIO_162	Y	SSC_2 QDSS_GPIO_TRACEDATA_LOCA[2]	3	PD:nppukp	Configurable I/O SSC I/O 2 QDSS trace data 2 A
E16	E18	GPIO_161	–	SSC_1 QDSS_GPIO_TRACEDATA_LOCA[1]	3	PD:nppukp	Configurable I/O SSC I/O 1 QDSS trace data 1 A
D16	D18	GPIO_160	Y	SSC_0 QDSS_GPIO_TRACEDATA_LOCA[0]	3	PD:nppukp	Configurable I/O SSC I/O 0 QDSS trace data 0 A
B28	B30	GPIO_159	–	LPASS_13 LPI_DMIC3_DATA LPI_MI2S2_DATA1 EXT_MCLK1	3	PD:nppukp	Configurable I/O LPASS I/O 13 DMIC3 data LPI MI2S2 serial data channel 1 External MCLK1
B27	B29	GPIO_158	Y	LPASS_12 LPI_DMIC3_CLK LPI_MI2S2_DATA0	3	PD:nppukp	Configurable I/O LPASS I/O 12 DMIC 3 clock LPI MI2S2 serial data channel 0
C27	C29	GPIO_157	Y	LPASS_11 LPI_MI2S2_WS WSA_SWR_DATA	3	PD:nppukp	Configurable I/O LPASS I/O 11 LPI MI2S2 serial data word select SoundWire data for WSA
D27	D29	GPIO_156	–	LPASS_10 LPI_MI2S2_CLK WSA_SWR_CLK	3	PD:nppukp	Configurable I/O LPASS I/O 10 LPI MI2S2 clock SoundWire clock for WSA
B26	B28	GPIO_155	–	LPASS_9 LPI_DMIC2_DATA LPI_MI2S1_DATA1 EXT_MCLK2	3	PD:nppukp	Configurable I/O LPASS I/O 9 DMIC2 data LPI MI2S1 serial data channel 1 External MCLK2
D26	D28	GPIO_154	–	LPASS_8 LPI_DMIC2_CLK LPI_MI2S1_DATA0	3	PD:nppukp	Configurable I/O LPASS I/O 8 DMIC2 clock LPI MI2S1 serial data channel 0
B25	B27	GPIO_153	–	LPASS_7 LPI_DMIC1_DATA LPI_MI2S1_WS	3	PD:nppukp	Configurable I/O LPASS I/O 7 DMIC1 data LPI MI2S1 serial data word select
C25	C27	GPIO_152	–	LPASS_6 LPI_DMIC1_CLK LPI_MI2S1_CLK	3	PD:nppukp	Configurable I/O LPASS I/O 6 DMIC1 clock LPI MI2S1 clock
D25	D27	GPIO_151	–	LPASS_5 SWR_RX_DATA1 SWR_TX_DATA2 LPI_MI2S0_DATA3	3	PD:nppukp	Configurable I/O LPASS I/O 5 SoundWire receive data 1 SoundWire transmit data 2 LPI MI2S0 serial data channel 3

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
C24	C26	GPIO_150	Y	LPASS_4 SWR_RX_DATA0 LPI_MI2S0_DATA2	3	PD:nppukp	Configurable I/O LPASS I/O 4 SoundWire receive data 0 LPI MI2S0 serial data channel 2
D24	D26	GPIO_149	–	LPASS_3 SWR_RX_CLK LPI_MI2S0_DATA1	3	PD:nppukp	Configurable I/O LPASS I/O 3 SoundWire receive clock LPI MI2S0 serial data channel 1
C23	C25	GPIO_148	–	LPASS_2 SWR_TX_DATA1 LPI_MI2S0_DATA0	3	PD:nppukp	Configurable I/O LPASS I/O 2 SoundWire transmit data 1 LPI MI2S0 serial data channel 0
D23	D25	GPIO_147	Y	LPASS_1 SWR_TX_DATA0 LPI_MI2S0_WS	3	PD:nppukp	Configurable I/O LPASS I/O 1 SoundWire transmit data 0 LPI MI2S0 serial data word select
E23	E25	GPIO_146	–	LPASS_0 SWR_TX_CLK LPI_MI2S0_SCK	3	PD:nppukp	Configurable I/O LPASS I/O 0 SoundWire transmit clock LPI MI2S0 clock
F17	F19	GPIO_145	–	LPASS_SLIMBUS_DATA2 MI2S1_WS	3	PD:nppukp	Configurable I/O Low-power audio SLIMbus data 2 MI2S1 serial data word select
F19	F21	GPIO_144	–	LPASS_SLIMBUS_DATA1 MI2S1_DATA1	3	PD:nppukp	Configurable I/O Low-power audio SLIMbus data 1 MI2S1 serial data channel 1
E19	E21	GPIO_143	Y	LPASS_SLIMBUS_DATA0 MI2S1_DATA0	3	PD:nppukp	Configurable I/O Low-power audio SLIMbus data 0 MI2S1 serial data channel 0
D19	D21	GPIO_142	Y	LPASS_SLIMBUS_CLK MI2S1_SCK	3	PD:nppukp	Configurable I/O Low-power audio SLIMbus clock MI2S1 clock
D20	D22	GPIO_141	–	MI2S0_WS GP_PDM_MIRA[2]	3	PD:nppukp	Configurable I/O MI2S0 serial data word select General-purpose PDM output 2 A
C20	C22	GPIO_140	–	MI2S0_DATA1	3	PD:nppukp	Configurable I/O MI2S0 serial data channel 1
E21	E23	GPIO_139	–	MI2S0_DATA0	3	PD:nppukp	Configurable I/O MI2S0 serial data channel 0
D21	D23	GPIO_138	Y	MI2S0_SCK GCC_GP3_CLK_MIRA	3	PD:nppukp	Configurable I/O MI2S0 clock General-purpose Clock 3 A
C21	C23	GPIO_137	Y	MI2S1_MCLK AUDIO_REF_CLK MI2S2_DATA1 GCC_GP2_CLK_MIRA	3	PD:nppukp	Configurable I/O MI2S1 master clock Audio reference clock MI2S2 serial data channel 1 General-purpose Clock 2 A
B21	B23	GPIO_136	Y	MI2S0_MCLK GCC_GP1_CLK_MIRA	3	PD:nppukp	Configurable I/O MI2S0 master clock General-purpose Clock 1 A

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
E22	E24	GPIO_135	–	MI2S2_WS	3	PD:nppukp	Configurable I/O MI2S2 serial data word select
C22	C24	GPIO_134	Y	MI2S2_DATA0	3	PD:nppukp	Configurable I/O MI2S2 serial data channel 0
B22	B24	GPIO_133	Y	MI2S2_SCK	3	PD:nppukp	Configurable I/O MI2S2 clock
H33	H35	GPIO_132	Y	QUP_L3(10) FORCED_USB_BOOT	3	PD:nppukp	Configurable I/O QUP 10, lane 3: SPI_CS_0 Forced USB boot [2]
G33	G35	GPIO_131	–	QUP_L2(10)	3	PD:nppukp	Configurable I/O QUP 10, lane 2: SPI_SCLK/UART_TX
F33	F35	GPIO_130	–	QUP_L1(10)	3	PD:nppukp	Configurable I/O QUP 10, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
E32	E34	GPIO_129	Y	QUP_L0(10)	3	PD:nppukp	Configurable I/O QUP 10, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
E33	E35	GPIO_128	Y	QUP_L3(9) BOOT_CONFIG(0)	3	PD:nppukp	Configurable I/O QUP 9, lane 3: SPI_CS_0 Boot configuration bit 0 [2]
D30	D32	GPIO_127	–	QUP_L2(9)	3	PD:nppukp	Configurable I/O QUP 9, lane 2: SPI_SCLK/UART_TX
D31	D33	GPIO_126	Y	QUP_L1(9)	3	PD:nppukp	Configurable I/O QUP 9, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
D32	D34	GPIO_125	–	QUP_L0(9)	3	PD:nppukp	Configurable I/O QUP 9, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
A3	A5	GPIO_124	Y	QUP_L5_4_CS MDP_VSYNC_P_MIRB	3	PD:nppukp	Configurable I/O QUP 4, lane 5: SPI_CS_2 MDP vertical sync – primary B
B3	B5	GPIO_123	Y	QUP_L4_4_CS	3	PD:nppukp	Configurable I/O QUP 4, lane 4: SPI_CS_1
D3	D5	GPIO_122	Y	QUP_L3(3) MDP_VSYNC_S_MIRB	3	PD:nppukp	Configurable I/O QUP 3, lane 3: SPI_CS_0 MDP vertical sync – secondary B
E3	E5	GPIO_121	Y	QUP_L2(3)	3	PD:nppukp	Configurable I/O QUP 3, lane 2: SPI_SCLK/UART_TX
F3	F5	GPIO_120	–	QUP_L1(3)	3	PD:nppukp	Configurable I/O QUP 3, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
G3	G5	GPIO_119	–	QUP_L0(3)	3	PD:nppukp	Configurable I/O QUP 3, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
H3	H5	GPIO_118	Y	QUP_L3(2)	3	PD:nppukp	Configurable I/O QUP 2, lane 3: SPI_CS_0
J3	J5	GPIO_117	–	QUP_L2(2)	3	PD:nppukp	Configurable I/O QUP 2, lane 2: SPI_SCLK/UART_TX

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
K3	K5	GPIO_116	–	QUP_L1(2)	3	PD:nppukp	Configurable I/O QUP 2, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
L3	L5	GPIO_115	–	QUP_L0(2)	3	PD:nppukp	Configurable I/O QUP 2, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
D2	D4	GPIO_114	–	CCI_ASYNC_IN0	3	PD:nppukp	Configurable I/O Camera control interface async 0
F2	F4	GPIO_113	Y	CCI_TIMER4 CCI_ASYNC_IN2	3	PD:nppukp	Configurable I/O Camera control interface timer 4 Camera control interface async 2
G2	G4	GPIO_112	Y	CCI_TIMER3 CCI_ASYNC_IN1	3	PD:nppukp	Configurable I/O Camera control interface timer 3 Camera control interface async 1
J2	J4	GPIO_111	Y	CCI_TIMER2 QDSS_GPIO_TRACEDATA_LOCB[15]	3	PD:nppukp	Configurable I/O Camera control interface timer 2 QDSS trace data 15 B
K2	K4	GPIO_110	Y	CCI_TIMER1 QDSS_GPIO_TRACEDATA_LOCB[14]	3	PD:nppukp	Configurable I/O Camera control interface timer 1 QDSS trace data 14 B
C1	C3	GPIO_109	Y	CCI_TIMER0 QDSS_GPIO_TRACEDATA_LOCB[13]	3	PD:nppukp	Configurable I/O Camera control interface timer 0 QDSS trace data 13 B
D1	D3	GPIO_108	Y	CCI_I2C_SCL3 QDSS_GPIO_TRACEDATA_LOCB[12] GCC_GP3_CLK_MIRB	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 3 clock QDSS trace data 12 B General-purpose Clock 3 B
E1	E3	GPIO_107	–	CCI_I2C_SDA3 QDSS_GPIO_TRACEDATA_LOCB[11] GCC_GP2_CLK_MIRB	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 3 serial data QDSS trace data 11 B General-purpose Clock 2 B
F1	F3	GPIO_106	–	CCI_I2C_SCL2 QDSS_GPIO_TRACEDATA_LOCB[10] GCC_GP1_CLK_MIRB	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 2 clock QDSS trace data 10 B General-purpose Clock 1 B
G1	G3	GPIO_105	–	CCI_I2C_SDA2 QDSS_GPIO_TRACEDATA_LOCB[9]	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 2 serial data QDSS trace data 9 B
H1	H3	GPIO_104	Y	CCI_I2C_SCL1 QDSS_GPIO_TRACECTL_LOCB	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 clock QDSS trace control B
J1	J3	GPIO_103	Y	CCI_I2C_SDA1 QDSS_GPIO_TRACECLK_LOCB	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 1 serial data QDSS trace clock B
K1	K3	GPIO_102	–	CCI_I2C_SCL0 QDSS_GPIO_TRACEDATA_LOCB[8]	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 clock QDSS trace data 8 B

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
M2	M4	GPIO_101	–	CCI_I2C_SDA0 QDSS_GPIO_TRACEDATA_LOCB[7]	3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C 0 serial data QDSS trace data 7 B
N2	N4	GPIO_100	Y	CAM_MCLK6 QDSS_GPIO_TRACEDATA_LOCB[6]	3	PD:nppukp	Configurable I/O Camera master clock 6 QDSS trace data 6 B
R2	R4	GPIO_99	–	CAM_MCLK5 QDSS_GPIO_TRACEDATA_LOCB[5]	3	PD:nppukp	Configurable I/O Camera master clock 5 QDSS trace data 5 B
L1	L3	GPIO_98	–	CAM_MCLK4 QDSS_GPIO_TRACEDATA_LOCB[4]	3	PD:nppukp	Configurable I/O Camera master clock 4 QDSS trace data 4 B
M1	M3	GPIO_97	–	CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB[3]	3	PD:nppukp	Configurable I/O Camera master clock 3 QDSS trace data 3 B
N1	N3	GPIO_96	–	CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB[2]	3	PD:nppukp	Configurable I/O Camera master clock 2 QDSS trace data 2 B
P1	P3	GPIO_95	–	CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB[1]	3	PD:nppukp	Configurable I/O Camera master clock 1 QDSS trace data 1 B
R1	R3	GPIO_94	–	CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB[0]	3	PD:nppukp	Configurable I/O Camera master clock 0 QDSS trace data 0 B
B2	B4	GPIO_93	Y	QUP_L6_2_CS QDSS_CTI_TRIG1_IN_MIRA	3	PD:nppukp	Configurable I/O QUP 2, lane 6: SPI_CS_3 QDSS trigger input 0 A
C2	C4	GPIO_92	Y	QUP_L6_4_CS QDSS_CTI_TRIG1_OUT_MIRA	3	PD:nppukp	Configurable I/O QUP 4, lane 6: SPI_CS_3 QDSS trigger output 0 A
AE35	AE37	GPIO_91	–		3	PD:nppukp	Configurable I/O
AD35	AD37	GPIO_90	–	BOOT_CONFIG(4)	3	PD:nppukp	Configurable I/O Boot configuration bit 4 [2]
C30	C32	GPIO_89	Y	GP_PDM_MIRA[0]	3	PD:nppukp	Configurable I/O General-purpose PDM output 0 A
B30	B32	GPIO_88	Y	GP_PDM_MIRA[1]	3	PD:nppukp	Configurable I/O General-purpose PDM output 1 A
N35	N37	GPIO_87	Y		3	PD:nppukp	Configurable I/O
L35	L37	GPIO_86	Y	PCI_E2_CLKREQN	3	PU:nppdkp	Configurable I/O PCIe2 clock request
L34	L36	GPIO_85	–	PCI_E2_RST_N	3	PD:nppukp	Configurable I/O PCIe2 reset
A6	A8	GPIO_84	Y		3	PD:nppukp	Configurable I/O
B6	B8	GPIO_83	Y	PCI_E1_CLKREQN	3	PU:nppdkp	Configurable I/O PCI1 clock request

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
B7	B9	GPIO_82	–	PCI_E1_RST_N	3	PD:nppukp	Configurable I/O PCIe1 reset
C7	C9	GPIO_81	Y		3	PD:nppukp	Configurable I/O
D6	D8	GPIO_80	Y	PCI_E0_CLKREQN	3	PU:nppdkp	Configurable I/O PCI0 clock request
E6	E8	GPIO_79	–	PCI_E0_RST_N	3	PD:nppukp	Configurable I/O PCI0 reset
T1	T3	GPIO_78	–	SD_WRITE_PROTECT	3	PD:nppukp	Configurable I/O Secure digital card write protection
U1	U3	GPIO_77	Y	QUP_L6_0_CS	3	PD:nppukp	Configurable I/O QUP 0, lane 6: SPI_CS3
AF35	AF37	GPIO_76	–	SDC4_DATA(0) BOOT_CONFIG(3)	3	PD:nppukp	Configurable I/O Secure digital controller 4 data bit 0 Boot configuration bit 3 [2]
AG35	AG37	GPIO_75	–	QSPI_CS_N_1 SDC4_DATA(1)	3	PD:nppukp	Configurable I/O Quad-SPI chip select 1 Secure digital controller 4 clock data bit 1
AM31	AM33	GPIO_74	–	QSPI_DATA(3) SDC4_DATA(2)	3	PD:nppukp	Configurable I/O Quad-SPI data bit 3 Secure digital controller 4 clock data bit 2
AM32	AM34	GPIO_73	–	QSPI_CLK SDC4_CLK	3	PD:nppukp	Configurable I/O Quad-SPI clock Secure digital controller 4 clock
AN32	AN34	GPIO_72	–	QSPI_DATA(2) SDC4_DATA(3)	3	PD:nppukp	Configurable I/O Quad-SPI data bit 2 Secure digital controller 4 clock data bit 3
AP33	AP35	GPIO_71	–	QSPI_DATA(1) SDC4_CMD	3	PD:nppukp	Configurable I/O Quad-SPI data bit 1 Secure digital controller 4 command
AP32	AP34	GPIO_70	Y	QSPI_DATA(0)	3	PD:nppukp	Configurable I/O Quad-SPI data bit 0
AN33	AN35	GPIO_69	–	QSPI_CS_N_0	3	PD:nppukp	Configurable I/O Quad-SPI chip select 0
T2	T4	GPIO_68	Y	MDP_VSYNC_E DP_HOT_PLUG_DETECT	3	PD:nppukp	Configurable I/O MDP vertical sync – external DisplayPort hot plug detect
U2	U4	GPIO_67	Y	MDP_VSYNC_S_MIRA	3	PD:nppukp	Configurable I/O MDP vertical sync – secondary A
V2	V4	GPIO_66	Y	MDP_VSYNC_P_MIRA	3	PD:nppukp	Configurable I/O MDP vertical sync – primary A
M35	M37	GPIO_65	Y	USB_PHY_PS	3	PD:nppukp	Configurable I/O USB PHY port select
M34	M36	GPIO_64	Y	QUP_L6_14_CS	3	PD:nppukp	Configurable I/O QUP 14, lane 6: SPI_CS_3

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
C35	C37	GPIO_63	Y	QUP_L3(11)	3	PD:nppukp	Configurable I/O QUP 11, lane 3: SPI_CS_0
B34	B36	GPIO_62	–	QUP_L2(11)	3	PD:nppukp	Configurable I/O QUP 11, lane 2: SPI_SCLK/UART_TX
B33	B35	GPIO_61	–	QUP_L1(11)	3	PD:nppukp	Configurable I/O QUP 11, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
A33	A35	GPIO_60	–	QUP_L0(11)	3	PD:nppukp	Configurable I/O QUP 11, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
T32	T34	GPIO_59	Y	QUP_L3(18)	3	PD:nppukp	Configurable I/O QUP 18, lane 3: SPI_CS_0
R32	R34	GPIO_58	–	QUP_L2(18)	3	PD:nppukp	Configurable I/O QUP 18, lane 2: SPI_SCLK/UART_TX
P32	P34	GPIO_57	–	QUP_L1(18)	3	PD:nppukp	Configurable I/O QUP 18, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
N32	N34	GPIO_56	–	QUP_L0(18)	3	PD:nppukp	Configurable I/O QUP 18, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
N33	N35	GPIO_55	Y	QUP_L3(17)	3	PD:nppukp	Configurable I/O QUP 17, lane 3: SPI_CS_0
N34	N36	GPIO_54	–	QUP_L2(17)	3	PD:nppukp	Configurable I/O QUP 17, lane 2: SPI_SCLK/UART_TX
M33	M35	GPIO_53	–	QUP_L1(17)	3	PD:nppukp	Configurable I/O QUP 17, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
M32	M34	GPIO_52	–	QUP_L0(17)	3	PD:nppukp	Configurable I/O QUP 17, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
K32	K34	GPIO_51	Y	QUP_L3(16)	3	PD:nppukp	Configurable I/O QUP 16, lane 3: SPI_CS_0
J32	J34	GPIO_50	–	QUP_L2(16)	3	PD:nppukp	Configurable I/O QUP 16, lane 2: SPI_SCLK/UART_TX
H31	H33	GPIO_49	–	QUP_L1(16)	3	PD:nppukp	Configurable I/O QUP 16, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
G32	G34	GPIO_48	–	QUP_L0(16)	3	PD:nppukp	Configurable I/O QUP 16, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
K35	K37	GPIO_47	Y	QUP_L3(15) QUP_L5_14_CS BOOT_CONFIG(2)	3	PD:nppukp	Configurable I/O QUP 15, lane 3: SPI_CS_0 QUP 14, lane 5: SPI_CS_2 Boot configuration bit 2 [2]
J35	J37	GPIO_46	–	QUP_L2(15) QUP_L4_14_CS QDSS_CTI_TRIG0_OUT_MIRA	3	PD:nppukp	Configurable I/O QUP 15, lane 2: SPI_SCLK/UART_TX QUP 14, lane 4: SPI_CS_1 QDSS trigger output 0 A

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
H35	H37	GPIO_45	Y	QUP_L1(15) QDSS_CTI_TRIG0_IN_MIRB	3	PD:nppukp	Configurable I/O QUP 15, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL QDSS trigger input 0 B
G35	G37	GPIO_44	–	QUP_L0(15) QDSS_CTI_TRIG0_OUT_MIRB	3	PD:nppukp	Configurable I/O QUP 15, lane 0: SPI_MISO/UART_CTS/ I2C_SDA QDSS trigger output 0 B
AN30	AN32	GPIO_43	Y	QUP_L3(14)	3	PD:nppukp	Configurable I/O QUP 14, lane 3: SPI_CS_0
AM30	AM32	GPIO_42	–	QUP_L2(14)	3	PD:nppukp	Configurable I/O QUP 14, lane 2: SPI_SCLK/UART_TX
AN31	AN33	GPIO_41	–	QUP_L1(14) IBI_I3C_QUP14_SCL	3	PD:nppukp	Configurable I/O QUP 14, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL QUP14 In-Band interrupt I3C SCL
AP31	AP33	GPIO_40	Y	QUP_L0(14) IBI_I3C_QUP14_SDA	3	PD:nppukp	Configurable I/O QUP 14, lane 0: SPI_MISO/UART_CTS/ I2C_SDA QUP14 In-Band interrupt I3C SDA
K33	K35	GPIO_39	Y	QUP_L3(13)	3	PD:nppukp	Configurable I/O QUP 13, lane 3: SPI_CS_0
J33	J35	GPIO_38	–	QUP_L2(13)	3	PD:nppukp	Configurable I/O QUP 13, lane 2: SPI_SCLK/UART_TX
J34	J36	GPIO_37	–	QUP_L1(13)	3	PD:nppukp	Configurable I/O QUP 13, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
H34	H36	GPIO_36	–	QUP_L0(13)	3	PD:nppukp	Configurable I/O QUP 13, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
F34	F36	GPIO_35	Y	QUP_L3(12)	3	PD:nppukp	Configurable I/O QUP 12, lane 3: SPI_CS_0
E34	E36	GPIO_34	–	QUP_L2(12)	3	PD:nppukp	Configurable I/O QUP 12, lane 2: SPI_SCLK/UART_TX
F35	F37	GPIO_33	–	QUP_L1(12)	3	PD:nppukp	Configurable I/O QUP 12, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
E35	E37	GPIO_32	–	QUP_L0(12) GP_MN	3	PD:nppukp	Configurable I/O QUP 12, lane 0: SPI_MISO/UART_CTS/ I2C_SDA General-purpose M/N:D counter output
M3	M5	GPIO_31	Y	QUP_L3(0)	3	PD:nppukp	Configurable I/O QUP 0, lane 3: SPI_CS_0
N3	N5	GPIO_30	–	QUP_L2(0) GP_PDM_MIRB[0]	3	PD:nppukp	Configurable I/O QUP 0, lane 2: SPI_SCLK/UART_TX General-purpose PDM output 0 B

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
P3	P5	GPIO_29	–	QUP_L1(0) GP_PDM_MIRB[1] IBI_I3C_QUP0_SCL	3	PD:nppukp	Configurable I/O QUP 0, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL General-purpose PDM output 1 B QUP0 In-Band interrupt I3C SCL
R3	R5	GPIO_28	Y	QUP_L0(0) GP_PDM_MIRB[2] IBI_I3C_QUP0_SDA	3	PD:nppukp	Configurable I/O QUP 0, lane 0: SPI_MISO/UART_CTS/ I2C_SDA General-purpose PDM output 2 B QUP0 In-Band interrupt I3C SDA
D33	D35	GPIO_27	Y	QUP_L3(8) BOOT_CONFIG(1)	3	PD:nppukp	Configurable I/O QUP 8, lane 3: SPI_CS_0 Boot configuration bit 1 [2]
D35	D37	GPIO_26	–	QUP_L2(8)	3	PD:nppukp	Configurable I/O QUP 8, lane 2: SPI_SCLK/UART_TX
C33	C35	GPIO_25	–	QUP_L1(8) IBI_I3C_QUP8_SCL	3	PD:nppukp	Configurable I/O QUP 8, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL QUP8 In-Band interrupt I3C SCL
C34	C36	GPIO_24	Y	QUP_L0(8) IBI_I3C_QUP8_SDA	3	PD:nppukp	Configurable I/O QUP 8, lane 0: SPI_MISO/UART_CTS/ I2C_SDA QUP8 In-Band interrupt I3C SDA
A4	A6	GPIO_23	Y	QUP_L3(7)	3	PD:nppukp	Configurable I/O QUP 7, lane 3: SPI_CS_0
A5	A7	GPIO_22	–	QUP_L2(7)	3	PD:nppukp	Configurable I/O QUP 7, lane 2: SPI_SCLK/UART_TX
B5	B7	GPIO_21	–	QUP_L1(7)	3	PD:nppukp	Configurable I/O QUP 7, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
C5	C7	GPIO_20	–	QUP_L0(7)	3	PD:nppukp	Configurable I/O QUP 7, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
D5	D7	GPIO_19	Y	QUP_L3(6)	3	PD:nppukp	Configurable I/O QUP 6, lane 3: SPI_CS_0
E5	E7	GPIO_18	–	QUP_L2(6)	3	PU:nppdkp	Configurable I/O QUP 6, lane 2: SPI_SCLK/UART_TX
C4	C6	GPIO_17	–	QUP_L1(6)	3	PD:nppukp	Configurable I/O QUP 6, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
C3	C5	GPIO_16	–	QUP_L0(6)	3	PD:nppukp	Configurable I/O QUP 6, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
D4	D6	GPIO_15	Y	QUP_L3(5) QUP_L5_2_CS	3	PD:nppukp	Configurable I/O QUP 5, lane 3: SPI_CS_0 QUP 2, lane 5: SPI_CS_2
E4	E6	GPIO_14	Y	QUP_L2(5) QUP_L4_2_CS	3	PD:nppukp	Configurable I/O QUP 5, lane 2: SPI_SCLK/UART_TX QUP 2, lane 4: SPI_CS_1

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #		Pad name	Wake-up function	Configurable function	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5				Voltage	Type	
F4	F6	GPIO_13	–	QUP_L1(5)	3	PD:nppukp	Configurable I/O QUP 5, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
G4	G6	GPIO_12	–	QUP_L0(5)	3	PD:nppukp	Configurable I/O QUP 5, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
H4	H6	GPIO_11	Y	QUP_L3(4)	3	PD:nppukp	Configurable I/O QUP 4, lane 3: SPI_CS_0
J4	J6	GPIO_10	–	QUP_L2(4)	3	PD:nppukp	Configurable I/O QUP 4, lane 2: SPI_SCLK/UART_TX
K4	K6	GPIO_9	–	QUP_L1(4)	3	PD:nppukp	Configurable I/O QUP 4, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
L4	L6	GPIO_8	–	QUP_L0(4)	3	PD:nppukp	Configurable I/O QUP 4, lane 0: SPI_MISO/UART_CTS/ I2C_SDA
M4	M6	GPIO_7	Y	QUP_L3(1) QUP_L5_0_CS	3	PD:nppukp	Configurable I/O QUP 1, lane 3: SPI_CS_0 QUP 0, lane 5: SPI_CS_2
N4	N6	GPIO_6	–	QUP_L2(1) QUP_L4_0_CS	3	PD:nppukp	Configurable I/O QUP 1, lane 2: SPI_SCLK/UART_TX QUP 0, lane 4: SPI_CS_1
P4	P6	GPIO_5	–	QUP_L1(1) IBI_I3C_QUP1_SCL	3	PD:nppukp	Configurable I/O QUP 1, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL QUP1 In-Band interrupt I3C SCL
R4	R6	GPIO_4	Y	QUP_L0(1) IBI_I3C_QUP1_SDA	3	PD:nppukp	Configurable I/O QUP 1, lane 0: SPI_MISO/UART_CTS/ I2C_SDA QUP1 In-Band interrupt I3C SDA
L33	L35	GPIO_3	Y	QUP_L3(19)	3	PD:nppukp	Configurable I/O QUP 19, lane 3: SPI_CS_0
L32	L34	GPIO_2	Y	QUP_L2(19) QDSS_CTI_TRIG1_OUT_MIRB QDSS_CTI_TRIG0_IN_MIRA	3	PD:nppukp	Configurable I/O QUP 19, lane 2: SPI_SCLK/UART_TX QDSS trigger output 1 B QDSS trigger input 0 A
K31	K33	GPIO_1	Y	QUP_L1(19)	3	PD:nppukp	Configurable I/O QUP 19, lane 1: SPI_MOSI/UART_RFR/ I2C_SCL
J31	J33	GPIO_0	Y	QUP_L0(19) QDSS_CTI_TRIG1_IN_MIRB	3	PD:nppukp	Configurable I/O QUP 19, lane 0: SPI_MISO/UART_CTS/ I2C_SDA QDSS trigger input 1 B

1. See Table 2-1 for the parameter and acronym definitions.
2. The boot configuration function of this GPIO is only active at the time of boot, before RESOUT_N is deasserted.

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #		Pad name	Functional description
LPDDR4X	LPDDR5		
A31, AD25, AJ10, D28, D29, E27, N10, W1, Y30	A33, AD27, AJ12, D30, D31, E29, N12, W3, Y32	DNC	Do not connect; connected internally, do not connect externally
A1, A11, A15, A18, A2, A22, A26, A30, A34, A35, AA1, AA17, AA19, AA2, AA21, AA24, AA26, AA28, AA30, AA31, AA34, AA6, AB10, AB12, AB14, AB20, AB24, AB25, AB29, AB3, AB34, AB8, AC1, AC17, AC19, AC2, AC24, AC25, AC3, AC30, AC34, AC35, AD10, AD12, AD14, AD20, AD24, AD29, AD3, AD31, AD34, AD6, AD7, AD8, AE17, AE19, AE3, AE30, AE34, AE4, AE5, AF10, AF12, AF29, AF3, AF31, AF34, AF7, AF8, AG1, AG10, AG12, AG14, AG16, AG17, AG19, AG2, AG24, AG25, AG28, AG3, AG30, AG34, AG8, AH1, AH10, AH17, AH18, AH19, AH2, AH20, AH23, AH25, AH29, AH3, AH30, AH33, AH34, AH35, AH4, AJ11, AJ12, AJ15, AJ16, AJ17, AJ18, AJ19, AJ20, AJ21, AJ22, AJ23, AJ24, AJ25, AJ33, AK1, AK19, AK2, AK28, AK29, AK30, AK33, AK34, AK35, AK5, AK6, AL10, AL15, AL16, AL19, AL22, AL23, AL26, AL27, AL28, AL29, AL30, AL31, AL32, AL33, AL9, AM1, AM10, AM11, AM12, AM19, AM2, AM28, AM29, AM33, AM7, AM8, AM9, AN1, AN10, AN15, AN16, AN17, AN18, AN19, AN2, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN3, AN34, AN35, AN4, AN7, AN8, AN9, AP1, AP11, AP15, AP18, AP2, AP22, AP26, AP34, AP35, AP7, B1, B13, B14, B16, B18, B19, B20, B23, B24, B29, B32, B35, B4, B8, B9, C12, C16, C18, C26, C28, C29, C6, D17, D18, D22, D34, E11, E14, E18, E2, E20, E24, E26, E29, E30, E31, E9, F10, F12, F13, F15, F16, F18, F20, F21, F23, F24, F25, F26, F29, F30, F32, F6, F8, G13, G15, G18, G19, G20, G22, G25, G30, G31, G34, G5, H10, H16, H2, H22, H24, H26, H28, H29, H30, H6, H8, J18, J21, J29, J7, J9, K10, K16, K17, K23, K26, K28, K30, K34, K5, L11, L13, L15, L19, L2, L21, L25, L29, L9, M10, M15, M20, M23, M30, M5, N11, N25, N29, N31, N9, P10, P14, P17, P2, P21, P23, P30, P33, P34, P35, P5, R25, R29, R31, R33, R5, R7, R9, T10, T12, T13, T15, T17, T20, T22, T24, T26, T28, T3, T30, T5, T6, T8, U16, U18, U24, U28, U3, V10, V12, V13, V15, V17, V21, V23, V25, V27, V3, V30, V33, V7, V8, W17, W19, W26, W28, W3, W30, W33, W6, Y10, Y12, Y14, Y20, Y22, Y25, Y27, Y3, Y34, Y7, Y8	A1, A13, A17, A2, A20, A24, A28, A3, A32, A36, A37, A38, A39, A4, AA19, AA2, AA21, AA23, AA26, AA28, AA3, AA30, AA32, AA33, AA36, AA38, AA4, AA8, AB1, AB10, AB12, AB14, AB16, AB22, AB26, AB27, AB31, AB36, AB39, AB5, AC19, AC2, AC21, AC26, AC27, AC3, AC32, AC36, AC37, AC38, AC4, AC5, AD1, AD10, AD12, AD14, AD16, AD22, AD26, AD31, AD33, AD36, AD39, AD5, AD8, AD9, AE19, AE2, AE21, AE32, AE36, AE38, AE5, AE6, AE7, AF1, AF10, AF12, AF14, AF31, AF33, AF36, AF39, AF5, AF9, AG10, AG12, AG14, AG16, AG18, AG19, AG2, AG21, AG26, AG27, AG3, AG30, AG32, AG36, AG38, AG4, AG5, AH1, AH12, AH19, AH20, AH21, AH22, AH25, AH27, AH3, AH31, AH32, AH35, AH36, AH37, AH39, AH4, AH5, AH6, AJ13, AJ14, AJ17, AJ18, AJ19, AJ2, AJ20, AJ21, AJ22, AJ23, AJ24, AJ25, AJ26, AJ27, AJ35, AJ38, AK1, AK21, AK3, AK30, AK31, AK32, AK35, AK36, AK37, AK39, AK4, AK7, AK8, AL1, AL11, AL12, AL17, AL18, AL2, AL21, AL24, AL25, AL28, AL29, AL30, AL31, AL32, AL33, AL34, AL35, AL38, AL39, AM1, AM10, AM11, AM12, AM13, AM14, AM2, AM21, AM3, AM30, AM31, AM35, AM38, AM39, AM4, AM9, AN1, AN10, AN11, AN12, AN17, AN18, AN19, AN2, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN3, AN30, AN31, AN36, AN37, AN38, AN39, AN4, AN5, AN6, AN9, AP1, AP13, AP17, AP2, AP20, AP24, AP28, AP3, AP36, AP37, AP38, AP39, AP4, AP9, B1, B10, B11, B15, B16, B18, B2, B20, B21, B22, B25, B26, B3, B31, B34, B37, B38, B39, B6, C1, C14, C18, C2, C20, C28, C30, C31, C38, C39, C8, D1, D19, D20, D24, D36, D39, E11, E13, E16, E2, E20, E22, E26, E28, E31, E32, E33, E38, E4, F1, F10, F12, F14, F15, F17, F18, F20, F22, F23, F25, F26, F27, F28, F31, F32, F34, F39, F8, G15, G17, G2, G20, G21, G22, G24, G27, G32, G33, G36, G38, G7, H1, H10, H12, H18, H24, H26, H28, H30, H31, H32, H39, H4, H8, J11, J2, J20, J23, J31, J38, J9, K1, K12, K18, K19, K25, K28, K30, K32, K36, K39, K7, L11, L13, L15, L17, L2, L21, L23, L27, L31, L38, L4, M1, M12, M17, M22, M25, M32, M39, M7, N11, N13, N2, N27, N31, N33, N38, P1, P12, P16, P19, P23, P25, P32, P35, P36, P37, P39, P4, P7, R11, R2, R27, R31, R33, R35, R38, R7, R9, T1, T10, T12, T14, T15, T17, T19, T22, T24, T26, T28, T30, T32, T39, T5, T7, T8, U18, U2, U20, U26, U30, U38, U5, V1, V10, V12, V14, V15, V17, V19, V23, V25, V27, V29, V32, V35, V39, V5, V9, W19, W2, W21, W28, W30, W32, W35, W38, W5, W8, Y1, Y5, Y9, Y10, Y12, Y14, Y16, Y22, Y24, Y27, Y29, Y36, Y39	GND	Ground

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #		Pad name	Functional description
LPDDR4X	LPDDR5		
A19, A20, A21, AP19, AP20, AP21	A18, AP18	NC	No connect; not connected internally
AA25, U25, U27, V26, V28, W23, W25, W27, W29, Y24, Y26, Y28, Y29	AA27, U27, U29, V28, V30, W25, W27, W29, W31, Y26, Y28, Y30, Y31	VDD_APC0	Power for Kryo Silver application processor
AA20, AA22, AA23, AA27, AA29, AB19, AB30, AC20, AC29, AD19, AD30, AE20, AE24, AE25, AE29, AF20, AF24, AF25, AF30, AG21, AG22, AG23, AG27, AG29	AA22, AA24, AA25, AA29, AA31, AB21, AB32, AC22, AC31, AD21, AD32, AE22, AE26, AE27, AE31, AF22, AF26, AF27, AF32, AG23, AG24, AG25, AG29, AG31	VDD_APC1	Power for Kryo Gold application processor
AB18, H25, H27, J19, J26, J28, J30, K19, K20, K25, K29, L18, L30, M17, M19, M21, M25, M29, M31, N14, N16, N18, N20, N22, N24, N30, P15, P19, P25, P29, P31, R14, R16, R18, R20, R22, R24, R30, T19, T21, T23, T25, T27, T29, T31, U20, U22, V18, V19, V24, W20, W22, Y18, Y19, Y21	AB20, H27, H29, J21, J28, J30, J32, K21, K22, K27, K31, L20, L32, M19, M21, M23, M27, M31, M33, N16, N18, N20, N22, N24, N26, N32, P17, P21, P27, P31, P33, R16, R18, R20, R22, R24, R26, R32, T21, T23, T25, T27, T29, T31, T33, U22, U24, V20, V21, V26, W22, W24, Y20, Y21, Y23	VDD_CX	Power for digital core circuits
G10, G11, G12, G14, G16, H5, H7, H9, J10, J16, J6, J8, K9, L10, L12, L14, L16, M9, N5, P9, R6, R8, T11, T7, T9, U6, U8	G12, G13, G14, G16, G18, H7, H9, H11, J8, J10, J12, J18, K11, L12, L14, L16, L18, M11, N7, P11, R8, R10, T9, T11, T13, U8, U10	VDD_GFX	Power for graphics
H17, H18, H20, H21, J20	H19, H20, H22, H23, J22	VDD_LPI_CX	Power for low-power island core circuits
K21, L22, J22	J24, K23, L24	VDD_LPI_MX	Power for low-power island memory circuits
AA11, AA7, AA9, AC11, AC7, AC9, AE11, AE13, AE15, AE7, AE9, AF14, AF16, AG11, AG13, AG9, AG15	AA11, AA13, AA9, AC11, AC9, AC13, AE11, AE13, AE15, AE17, AE9, AF16, AF18, AG11, AG13, AG15, AG17	VDD_MM	Power for multimedia subsystem circuits
AA13, AA15, AB16, AC13, AC15, AD16, AD18, AF18, AF19, AG18, AG20, J5, M11, M13, N12, P11, P13, R12, T14, T16, U11, U13, U9, V14, V16, V6, W11, W13, W15, W7, W9, Y16	AA15, AA17, AB18, AC15, AC17, AD18, AD20, AF20, AF21, AG20, AG22, J7, M13, M15, N14, P13, P15, R14, T16, T18, U11, U13, U15, V16, V18, V8, W11, W13, W15, W17, W9, Y18	VDD_MX	Power for on-chip memory
G21	G23	VDD_PX0	Power for pad group 0 – control signals
W2	W4	VDD_PX10A	Power for pad group 10 – UFS
T33	T35	VDD_PX10B	Power for pad group 10 – UFS
U29	U31	VDD_PX11	Power for pad group 11 – CXO pad
G23	G25	VDD_PX13	Power for pad group 13 – secure processor unit (SPU)

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #		Pad name	Functional description
LPDDR4X	LPDDR5		
V5	V7	VDD_PX2	Power for pad group 2 – SDC2 pads
F11, F14, F31, F5, G17, G24, H32, L31, L5, T4, U34	F13, F16, F33, F7, G19, G26, H34, L33, L7, T6, U36	VDD_PX3	Power for pad group 3 – most I/O pads
V4	V6	VDD_PXVBIAS_SDC	Reference voltage for SDC
L24	L26	VDD_QFPROM	Power for programming the QFPROM
H23	H25	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit
AC31	AC33	VDD_USB_HS_CORE	Power for USB high-speed (HS) core circuits
A10, A27, AP10, AP27	A12, A29, AP12, AP29	VDD1	Power for PoP DDR memory core – 1.8 V (top VDD1)
A12, A13, A14, A23, A24, A25, AP12, AP13, AP14, AP23, AP24, AP25	–	VDD2	Power for PoP LPDDR4X memory core – 1.1 V (top VDD2)
–	A14, A15, A16, A25, A26, A27, AP14, AP15, AP16, AP25, AP26, AP27	VDD2H	Power for PoP LPDDR5 memory core – 1.05 V (top VDD2H)
–	A21, A22, A23, AP21, AP22, AP23	VDD2L	Power for PoP LPDDR5 memory core – 0.9 V (top VDD2L)
A28, A29, A8, A9, AP28, AP29, AP8, AP9	A10, A11, A30, A31, AP10, AP11, AP30, AP31	VDDQ	Power for PoP DDR pads (top VDDQ)
AG26	AG28	VDD_A_APC_CS_1P8	Power for application processor current-sensor 1.8 V circuits
AF6	AF8	VDD_A_CSI0_0P9	Power for MIPI CSI0 0.9 V circuits
AE6	AE8	VDD_A_CSI012_1P2	Power for MIPI CSI0/CSI1/ CSI2 1.2 V circuits
AG6	AG8	VDD_A_CSI1_2_0P9	Power for MIPI CSI1/CSI2 0.9 V circuits
AH16	AH18	VDD_A_CSI3_0P9	Power for MIPI CSI3 0.9 V circuits
AK9	AK11	VDD_A_CSI345_1P2	Power for MIPI CSI3/CSI4/CSI5 1.2 V circuits
AH15	AH17	VDD_A_CSI4_5_0P9	Power for MIPI CSI4/CSI5 0.9 V circuits
AH22	AH24	VDD_A_DSI_0P9	Power for MIPI DSI0 0.9 V circuits

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #		Pad name	Functional description
LPDDR4X	LPDDR5		
AH24	AH26	VDD_A_DSI_1P2	Power for MIPI DSI0 1.2 V circuits
AH21	AH23	VDD_A_DSI_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V circuits
G6, G7	G8, G9	VDD_A_EBI0	Power for EBI0 PHY circuits
AG7, AH7	AG9, AH9	VDD_A_EBI1	Power for EBI1 PHY circuits
G26, G27	G28, G29	VDD_A_EBI2	Power for EBI2 PHY circuits
AH26, AH27	AH28, AH29	VDD_A_EBI3	Power for EBI3 PHY circuits
R11	R13	VDD_A_GFX_CS_1P8	Power for graphics current sensor 1.8 V circuits
E7	E9	VDD_A_HV_EBI0	Power for EBI0 PHY high-voltage circuits
AH5	AH7	VDD_A_HV_EBI1	Power for EBI1 PHY high-voltage circuits
E28	E30	VDD_A_HV_EBI2	Power for EBI2 PHY high-voltage circuits
AJ30	AJ32	VDD_A_HV_EBI3	Power for EBI3 PHY high-voltage circuits
K27	K29	VDD_A_NPU_Q6_CS_1P8	Power for NPU/Q6 current sensor 1.8 V circuits
AA4	AA6	VDD_A_PCIE0_CORE	Power for PCIE0 (1-lane) core circuits
AB6	AB8	VDD_A_PCIE0_PLL_1P2	Power for PCIE0 (1-lane) PLL 1.2 V circuits
AC6	AC8	VDD_A_PCIE1_CORE	Power for PCIE1 (2-lane) core circuits
AB7	AB9	VDD_A_PCIE1_PLL_1P2	Power for PCIE1 (2-lane) PLL 1.2 V circuits
AH31	AH33	VDD_A_PCIE2_CORE	Power for PCIE2 (2-lane) core circuits
AD32	AD34	VDD_A_PCIE2_PLL_1P2	Power for PCIE2 (1-lane) PLL 1.2 V circuits
F7	F9	VDD_A_PLL_EBI0	Power for EBI0 PLL circuits
AH6	AH8	VDD_A_PLL_EBI1	Power for EBI1 PLL circuits
F27	F29	VDD_A_PLL_EBI2	Power for EBI2 PLL circuits
AJ27	AJ29	VDD_A_PLL_EBI3	Power for EBI3 PLL circuits
U30	U32	VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits

Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins

Pad #		Pad name	Functional description
LPDDR4X	LPDDR5		
V29	V31	VDD_A_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits
J24	J26	VDD_A_SP_SENSOR	Power for SP sensor circuit
Y32	Y34	VDD_A_UFS0_1P2	Power for UFS0 1.2 V circuits
Y31	Y33	VDD_A_UFS0_CORE	Power for UFS0 core circuits
Y6	Y8	VDD_A_UFS1_1P2	Power for UFS1 1.2 V circuits
AA5	AA7	VDD_A_UFS1_CORE	Power for UFS1 core circuits
AE31	AE33	VDD_A_USB_HS_1P8	Power for USB HS 1.8 V circuits
AH32	AH34	VDD_A_USB_HS_3P1	Power for USB HS 3.1 V circuits
Y33	Y35	VDD_A_USB0_SS_DP_1P2	Power for USB0 SS and DisplayPort 1.2 V circuits
AB31	AB33	VDD_A_USB0_SS_DP_CORE	Power for USB0 SS core circuits
AD33	AD35	VDD_A_USB1_SS_1P2	Power for USB1 SS 1.2 V circuits
AG31	AG33	VDD_A_USB1_SS_CORE	Power for USB1 SS core circuits
E10	E12	VDD_D_EBI0	Power for EBI0 digital circuits
AK10	AK12	VDD_D_EBI1	Power for EBI1 digital circuits
E25	E27	VDD_D_EBI2	Power for EBI2 digital circuits
AJ26	AJ28	VDD_D_EBI3	Power for EBI3 digital circuits
F9, G8, G9	F11, G10, G11	VDD_IO_EBI0	Power for EBI0 I/O circuits
AH8, AH9, AJ9	AH10, AH11, AJ11	VDD_IO_EBI1	Power for EBI1 I/O circuits
F28, G28, G29	F30, G30, G31	VDD_IO_EBI2	Power for EBI2 I/O circuits
AH28, AJ28, AJ29	AH30, AJ30, AJ31	VDD_IO_EBI3	Power for EBI3 I/O circuits

2.3 Pin assignments – top

2.3.1 Pin map – top

The SM8250 is available in the MPSP1099 (for LPDDR5) or MPSP1017 (for LPDDR4X); its top surface is similar to a 496 PSP (LPDDR5) or 556 PSP (LPDDR4X). See Chapter 4 for package details and Section 2.2 for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3 (for LPDDR5) and Figure 2-4 (for LPDDR4X).

The text within Figure 2-3 (for LPDDR5) and Figure 2-4 (for LPDDR4X) is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available and defined in Section 2.2.1.

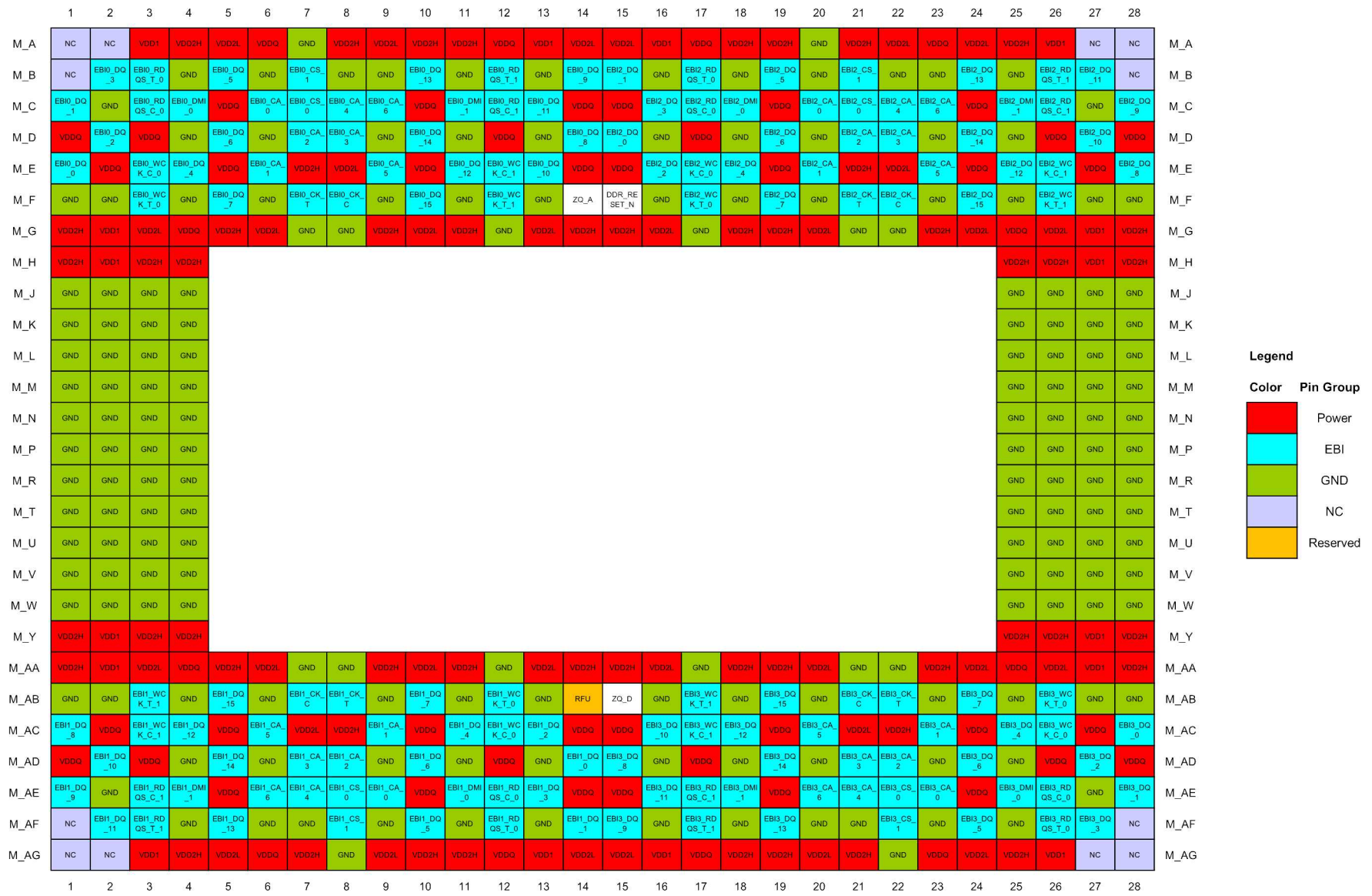


Figure 2-3 LPDDR5 top pin assignments

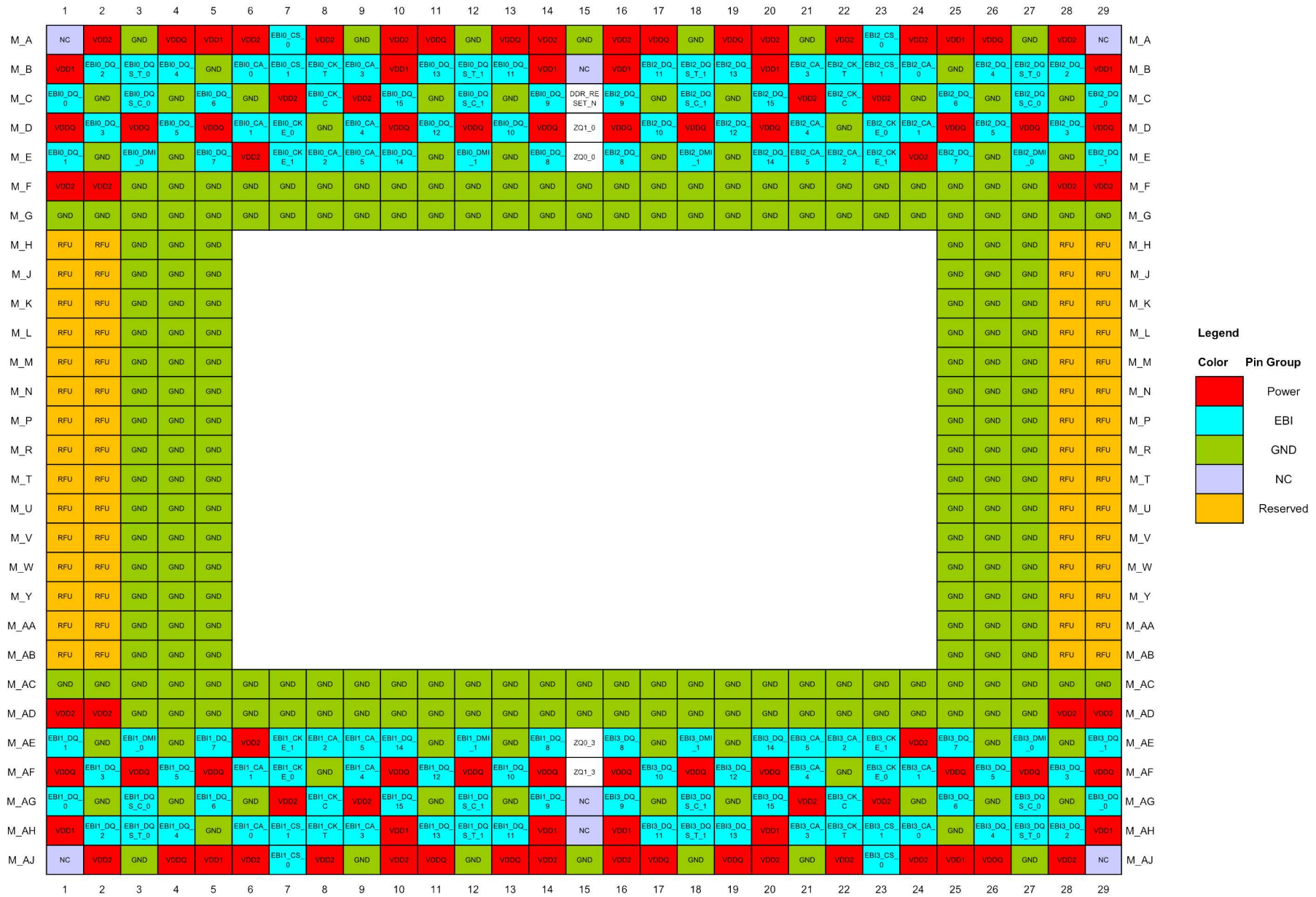


Figure 2-4 LPDDR4X top pin assignments

2.3.2 Pin descriptions – top

Descriptions of top pins are presented in Table 2-5 and Table 2-6.

Table 2-5 Top pin descriptions – general pins

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
M_C15	M_F15	DDR_RESET_N	EBI	DO	LPDDR5/LPDDR4X reset (shared by EBIs)
M_B6	M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 0
M_D6	M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 1
M_E8	M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 2
M_B9	M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 3
M_D9	M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 4
M_E9	M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5/LPDDR4X command/address bit 5
–	M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_C8	M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5/LPDDR4X differential clock (C)
M_B8	M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5/LPDDR4X differential clock (T)
M_D7	–	EBI0_CKE_0	EBI	DO	EBI0 LPDDR4X clock enable 0
M_E7	–	EBI0_CKE_1	EBI	DO	EBI0 LPDDR4X clock enable 1
M_A7	M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5/LPDDR4X chip select 0
M_B7	M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5/LPDDR4X chip select 1
M_E3	M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5/LPDDR4X data mask for byte 0
M_E12	M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5/LPDDR4X data mask for byte 1
M_C1	M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 0
M_E1	M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 1
M_D13	M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 10
M_B13	M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 11
M_D11	M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 12
M_B11	M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 13
M_E10	M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 14
M_C10	M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 15
M_B2	M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 2
M_D2	M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 3
M_B4	M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 4
M_D4	M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 5
M_C5	M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 6
M_E5	M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 7

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
M_E14	M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 8
M_C14	M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5/LPDDR4X data bit 9
M_C3	–	EBI0_DQS_C_0	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 (C)
M_C12	–	EBI0_DQS_C_1	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 (C)
M_B3	–	EBI0_DQS_T_0	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 (T)
M_B12	–	EBI0_DQS_T_1	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 (T)
–	M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 (C)
–	M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 (C)
–	M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 (T)
–	M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 (T)
–	M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (C)
–	M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (C)
–	M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 (T)
–	M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 (T)
M_AH6	M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 0
M_AF6	M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 1
M_AE8	M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 2
M_AH9	M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 3
M_AF9	M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 4
M_AE9	M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5/LPDDR4X command/address bit 5
–	M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_AG8	M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5/LPDDR4X differential clock (C)
M_AH8	M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5/LPDDR4X differential clock (T)
M_AF7	–	EBI1_CKE_0	EBI	DO	EBI1 LPDDR4X clock enable 0
M_AE7	–	EBI1_CKE_1	EBI	DO	EBI1 LPDDR4X clock enable 1
M_AJ7	M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5/LPDDR4X chip select 0
M_AH7	M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5/LPDDR4X chip select 1
M_AE3	M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR5/LPDDR4X data mask for byte 0
M_AE12	M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR5/LPDDR4X data mask for byte 1
M_AG1	M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 0
M_AE1	M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 1
M_AF13	M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 10
M_AH13	M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 11

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
M_AF11	M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 12
M_AH11	M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 13
M_AE10	M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 14
M_AG10	M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 15
M_AH2	M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 2
M_AF2	M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 3
M_AH4	M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 4
M_AF4	M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 5
M_AG5	M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 6
M_AE5	M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 7
M_AE14	M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 8
M_AG14	M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5/LPDDR4X data bit 9
M_AG3	–	EBI1_DQS_C_0	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 (C)
M_AG12	–	EBI1_DQS_C_1	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 (C)
M_AH3	–	EBI1_DQS_T_0	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 (T)
M_AH12	–	EBI1_DQS_T_1	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 (T)
–	M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 (C)
–	M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 (C)
–	M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 (T)
–	M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 (T)
–	M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (C)
–	M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (C)
–	M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 (T)
–	M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 (T)
M_B24	M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 0
M_D24	M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 1
M_E22	M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 2
M_B21	M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 3
M_D21	M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 4
M_E21	M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5/LPDDR4X command/address bit 5
–	M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_C22	M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5/LPDDR4X differential clock (C)
M_B22	M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5/LPDDR4X differential clock (T)

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
M_D23	–	EBI2_CKE_0	EBI	DO	EBI2 LPDDR4X clock enable 0
M_E23	–	EBI2_CKE_1	EBI	DO	EBI2 LPDDR4X clock enable 1
M_A23	M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5/LPDDR4X chip select 0
M_B23	M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5/LPDDR4X chip select 1
M_E27	M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR5/LPDDR4X data mask for byte 0
M_E18	M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR5/LPDDR4X data mask for byte 1
M_C29	M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 0
M_E29	M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 1
M_D17	M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 10
M_B17	M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 11
M_D19	M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 12
M_B19	M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 13
M_E20	M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 14
M_C20	M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 15
M_B28	M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 2
M_D28	M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 3
M_B26	M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 4
M_D26	M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 5
M_C25	M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 6
M_E25	M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 7
M_E16	M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 8
M_C16	M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5/LPDDR4X data bit 9
M_C27	–	EBI2_DQS_C_0	EBI	B	EBI2 LPDDR4X differential data strobe for byte 0 (C)
M_C18	–	EBI2_DQS_C_1	EBI	B	EBI2 LPDDR4X differential data strobe for byte 1 (C)
M_B27	–	EBI2_DQS_T_0	EBI	B	EBI2 LPDDR4X differential data strobe for byte 0 (T)
M_B18	–	EBI2_DQS_T_1	EBI	B	EBI2 LPDDR4X differential data strobe for byte 1 (T)
–	M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 (C)
–	M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 (C)
–	M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 (T)
–	M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 (T)
–	M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (C)
–	M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (C)
–	M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 (T)

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
–	M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 (T)
M_AH24	M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 0
M_AF24	M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 1
M_AE22	M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 2
M_AH21	M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 3
M_AF21	M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 4
M_AE21	M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5/LPDDR4X command/address bit 5
–	M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_AG22	M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5/LPDDR4X differential clock (C)
M_AH22	M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5/LPDDR4X differential clock (T)
M_AF23	–	EBI3_CKE_0	EBI	DO	EBI3 LPDDR4X clock enable 0
M_AE23	–	EBI3_CKE_1	EBI	DO	EBI3 LPDDR4X clock enable 1
M_AJ23	M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5/LPDDR4X chip select 0
M_AH23	M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5/LPDDR4X chip select 1
M_AE27	M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR5/LPDDR4X data mask for byte 0
M_AE18	M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR5/LPDDR4X data mask for byte 1
M_AG29	M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 0
M_AE29	M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 1
M_AF17	M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 10
M_AH17	M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 11
M_AF19	M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 12
M_AH19	M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 13
M_AE20	M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 14
M_AG20	M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 15
M_AH28	M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 2
M_AF28	M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 3
M_AH26	M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 4
M_AF26	M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 5
M_AG25	M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 6
M_AE25	M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 7
M_AE16	M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 8
M_AG16	M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5/LPDDR4X data bit 9
M_AG27	–	EBI3_DQS_C_0	EBI	B	EBI3 LPDDR4X differential data strobe for byte 0 (C)

Table 2-5 Top pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
M_AG18	–	EBI3_DQS_C_1	EBI	B	EBI3 LPDDR4X differential data strobe for byte 1 (C)
M_AH27	–	EBI3_DQS_T_0	EBI	B	EBI3 LPDDR4X differential data strobe for byte 0 (T)
M_AH18	–	EBI3_DQS_T_1	EBI	B	EBI3 LPDDR4X differential data strobe for byte 1 (T)
–	M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 (C)
–	M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 (C)
–	M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 (T)
–	M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 (T)
–	M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (C)
–	M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (C)
–	M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 (T)
–	M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 (T)
M_E15	–	ZQ0_0	–	Reference	LPDDR4X ZQ calibration for rank 0 in channels A and B (shared by EBIs)
M_AE15	–	ZQ0_3	–	Reference	LPDDR4X ZQ calibration for rank 0 in channels C and D (shared by EBIs)
M_D15	–	ZQ1_0	–	Reference	LPDDR4X ZQ calibration for rank 1 in channels A and B (shared by EBIs)
M_AF15	–	ZQ1_3	–	Reference	LPDDR4X ZQ calibration for rank 1 in channels C and D (shared by EBIs)
–	M_F14	ZQ_A	–	Reference	LPDDR5 ZQ resistor for upper two x16 memories (channels A and C)
–	M_AB15	ZQ_D	–	Reference	LPDDR5 ZQ resistor for lower two x16 memories (channels B and D)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Top pin descriptions – ground, NC, and power-supply pins

Pin #		Pad name	Functional description
LPDDR4X	LPDDR5		
M_A12, M_A15, M_A18, M_A21, M_A27, M_A3, M_A9, M_AA25, M_AA26, M_AA27, M_AA3, M_AA4, M_AA5, M_AB25, M_AB26, M_AB27, M_AB3, M_AB4, M_AB5, M_AC1, M_AC10, M_AC11, M_AC12, M_AC13, M_AC14, M_AC15, M_AC16, M_AC17, M_AC18, M_AC19, M_AC2, M_AC20, M_AC21, M_AC22, M_AC23, M_AC24, M_AC25, M_AC26, M_AC27, M_AC28, M_AC29, M_AC3, M_AC4, M_AC5, M_AC6, M_AC7, M_AC8, M_AC9, M_AD10, M_AD11, M_AD12, M_AD13, M_AD14, M_AD15, M_AD16, M_AD17, M_AD18, M_AD19, M_AD20, M_AD21, M_AD22, M_AD23, M_AD24, M_AD25, M_AD26, M_AD27, M_AD3, M_AD4, M_AD5, M_AD6, M_AD7, M_AD8, M_AD9, M_AE11, M_AE13, M_AE17, M_AE19, M_AE2, M_AE26, M_AE28, M_AE4, M_AF22, M_AF8, M_AG11, M_AG13, M_AG17, M_AG19, M_AG2, M_AG24, M_AG26, M_AG28, M_AG4, M_AG6, M_AH25, M_AH5, M_AJ12, M_AJ15, M_AJ18, M_AJ21, M_AJ27, M_AJ3, M_AJ9, M_B25, M_B5, M_C11, M_C13, M_C17, M_C19, M_C2, M_C24, M_C26, M_C28, M_C4, M_C6, M_D22, M_D8, M_E11, M_E13, M_E17, M_E19, M_E2, M_E26, M_E28, M_E4, M_F10, M_F11, M_F12, M_F13, M_F14, M_F15, M_F16, M_F17, M_F18, M_F19, M_F20, M_F21, M_F22, M_F23, M_F24, M_F25, M_F26, M_F27, M_F3, M_F4, M_F5, M_F6, M_F7, M_F8, M_F9, M_G1, M_G10, M_G11, M_G12, M_G13, M_G14, M_G15, M_G16, M_G17, M_G18, M_G19, M_G2, M_G20, M_G21, M_G22, M_G23, M_G24, M_G25, M_G26, M_G27, M_G28, M_G29, M_G3, M_G4, M_G5, M_G6, M_G7, M_G8, M_G9, M_H25, M_H26, M_H27, M_H3, M_H4, M_H5, M_J25, M_J26, M_J27, M_J3, M_J4, M_J5, M_K25, M_K26, M_K27, M_K3, M_K4, M_K5, M_L25, M_L26, M_L27, M_L3, M_L4, M_L5, M_M25, M_M26, M_M27, M_M3, M_M4, M_M5, M_N25, M_N26, M_N27, M_N3, M_N4, M_N5, M_P25, M_P26, M_P27, M_P3, M_P4, M_P5, M_R25, M_R26, M_R27, M_R3, M_R4, M_R5, M_T25, M_T26, M_T27, M_T3, M_T4, M_T5, M_U25, M_U26, M_U27, M_U3, M_U4, M_U5, M_V25, M_V26, M_V27, M_V3, M_V4, M_V5, M_W25, M_W26, M_W27, M_W3, M_W4, M_W5, M_Y3, M_Y4, M_Y5, M_Y25, M_Y26, M_Y27,	M_A20, M_A7, M_AA12, M_AA17, M_AA21, M_AA22, M_AA7, M_AA8, M_AB1, M_AB11, M_AB13, M_AB16, M_AB18, M_AB2, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AB4, M_AB6, M_AB9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AD4, M_AD6, M_AD9, M_AE2, M_AE27, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AF4, M_AF6, M_AF7, M_AF9, M_AG22, M_AG8, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_B4, M_B6, M_B8, M_B9, M_C2, M_C27, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_D4, M_D6, M_D9, M_F1, M_F11, M_F13, M_F16, M_F18, M_F2, M_F20, M_F23, M_F25, M_F27, M_F28, M_F4, M_F6, M_F9, M_G12, M_G17, M_G21, M_G22, M_G7, M_G8, M_J1, M_J2, M_J25, M_J26, M_J27, M_J28, M_J3, M_J4, M_K1, M_K2, M_K25, M_K26, M_K27, M_K28, M_K3, M_K4, M_L1, M_L2, M_L25, M_L26, M_L27, M_L28, M_L3, M_L4, M_M1, M_M2, M_M25, M_M26, M_M27, M_M28, M_M3, M_M4, M_N1, M_N2, M_N25, M_N26, M_N27, M_N28, M_N3, M_N4, M_P1, M_P2, M_P25, M_P26, M_P27, M_P28, M_P3, M_P4, M_R1, M_R2, M_R25, M_R26, M_R27, M_R28, M_R3, M_R4, M_T1, M_T2, M_T25, M_T26, M_T27, M_T28, M_T3, M_T4, M_U1, M_U2, M_U25, M_U26, M_U27, M_U28, M_U3, M_U4, M_V1, M_V2, M_V25, M_V26, M_V27, M_V28, M_V3, M_V4, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28,	GND	Ground
M_A1, M_A29, M_AG15, M_AH15, M_AJ1, M_AJ29, M_B15	M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27, M_AG28, M_B1, M_B28	NC	No connect; not connected internally
M_AA1, M_AA2, M_AA28, M_AA29, M_AB1, M_AB2, M_AB28, M_AB29, M_H1, M_H2, M_H28, M_H29, M_J1, M_J2, M_J28, M_J29, M_K1, M_K2, M_K28, M_K29, M_L1, M_L2, M_L28, M_L29, M_M1, M_M2, M_M28, M_M29, M_N1, M_N2, M_N28, M_N29, M_P1, M_P2, M_P28, M_P29, M_R1, M_R2, M_R28, M_R29, M_T1, M_T2, M_T28, M_T29, M_U1, M_U2, M_U28, M_U29, M_V1, M_V2, M_V28, M_V29, M_W1, M_W2, M_W28, M_W29, M_Y1, M_Y2, M_Y28, M_Y29	M_AB14	RFU	Reserved pins
M_A5, M_A25, M_AH1, M_AH10, M_AH14, M_AH16, M_AH20, M_AH29, M_AJ5, M_AJ25, M_B1, M_B10, M_B14, M_B16, M_B20, M_B29	M_A13, M_A16, M_A26, M_A3, M_AA2, M_AA27, M_AG13, M_AG16, M_AG26, M_AG3, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27	VDD1	Power for memory core (bottom VDD1)

Table 2-6 Top pin descriptions – ground, NC, and power-supply pins (cont.)

Pin #		Pad name	Functional description
LPDDR4X	LPDDR5		
M_A10, M_A14, M_A16, M_A2, M_A20, M_A22, M_A24, M_A28, M_A6, M_A8, M_AD1, M_AD2, M_AD28, M_AD29, M_AE24, M_AE6, M_AG21, M_AG23, M_AG7, M_AG9, M_AJ10, M_AJ14, M_AJ16, M_AJ2, M_AJ20, M_AJ22, M_AJ24, M_AJ28, M_AJ6, M_AJ8, M_C21, M_C23, M_C7, M_C9, M_E24, M_E6, M_F1, M_F2, M_F28, M_F29	M_A10, M_A11, M_A18, M_A19, M_A21, M_A25, M_A4, M_A8, M_AA1, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AA5, M_AA9, M_AC22, M_AC8, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_AG4, M_AG7, M_E21, M_E7, M_G1, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_G28, M_G5, M_G9, M_H1, M_H25, M_H26, M_H28, M_H3, M_H4, M_Y1, M_Y25, M_Y26, M_Y28, M_Y3, M_Y4	VDD2 (LPDDR4X) VDD2H (LPDDR5)	Power for memory core (bottom VDD2 or VDD2H)
–	M_A14, M_A15, M_A22, M_A24, M_A5, M_A9, M_AA10, M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AA3, M_AA6, M_AC21, M_AC7, M_AG14, M_AG15, M_AG20, M_AG24, M_AG5, M_AG9, M_E22, M_E8, M_G10, M_G13, M_G16, M_G20, M_G24, M_G26, M_G3, M_G6	VDD2L (LPDDR5)	Power for memory core (bottom VDD2L)
M_A11, M_A13, M_A17, M_A19, M_A26, M_A4, M_AF1, M_AF10, M_AF12, M_AF14, M_AF16, M_AF18, M_AF20, M_AF25, M_AF27, M_AF29, M_AF3, M_AF5, M_AJ11, M_AJ13, M_AJ17, M_AJ19, M_AJ26, M_AJ4, M_D1, M_D10, M_D12, M_D14, M_D16, M_D18, M_D20, M_D25, M_D27, M_D29, M_D3, M_D5	M_A12, M_A17, M_A23, M_A6, M_AA25, M_AA4, M_AC10, M_AC14, M_AC15, M_AC19, M_AC2, M_AC24, M_AC27, M_AC5, M_AD1, M_AD12, M_AD17, M_AD26, M_AD28, M_AD3, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AE5, M_AG12, M_AG17, M_AG23, M_AG6, M_C10, M_C14, M_C15, M_C19, M_C24, M_C5, M_D1, M_D12, M_D17, M_D26, M_D28, M_D3, M_E10, M_E14, M_E15, M_E19, M_E2, M_E24, M_E27, M_E5, M_G25, M_G4	VDDQ	Power for memory I/O (bottom VDDQ)

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor	-0.3	1.133	V
VDD_APC1	Qualcomm Kryo Gold application processor	-0.3	1.2485	V
VDD_GFX	Graphics	-0.3	0.9746	V
VDD_CX VDD_D_EBI0 VDD_D_EBI1 VDD_D_EBI2 VDD_D_EBI3	Digital core circuits EBI0 PHY digital circuits EBI1 PHY digital circuits EBI2 PHY digital circuits EBI3 PHY digital circuits	-0.3	1.133	V
VDD_MX	On-chip memory	-0.3	1.133	V
VDD_MM	Multimedia subsystem circuits	-0.3	1.133	V
VDD_LPI_CX	Low power island core	-0.3	1.133	V
VDD_LPI_MX	Low power island memory	-0.3	1.133	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDDA_SP_SENSOR	Secure processing unit sensors	-0.3	1.023	V
VDDA_CSI0_0P9	MIPI CSI0 0.9 V circuits			
VDD_A_CSI1_2_0P9	MIPI CSI1, CSI2 0.9 V circuits			
VDDA_CSI3_0P9	MIPI CSI3 0.9 V circuits			
VDD_A_CSI4_5_0P9	MIPI CSI4, CSI5 0.9 V circuits			
VDD_A_DSI_0P9	MIPI DSI 0.9 V circuits			
VDD_A_DSI_PLL_0P9	MIPI DSI PLL 0.9 V circuits			
VDD_A_PCIE0_CORE	PCIe0 core circuits			
VDD_A_PCIE1_CORE	PCIe1 core circuits			
VDD_A_PCIE2_CORE	PCIe2 core circuits			
VDD_A_UFS0_CORE	UFS0 core circuits			
VDD_A_UFS1_CORE	UFS1 core circuits			
VDD_USB_HS_CORE	USB HS core circuits			
VDD_A_EBI0	EBI0 PHY circuits	-0.3	1.133	V
VDD_A_EBI1	EBI1 PHY circuits			
VDD_A_EBI2	EBI2 PHY circuits			
VDD_A_EBI3	EBI3 PHY circuits			
VDD_A_PLL_EBI0	EBI0 PLL circuits			
VDD_A_PLL_EBI1	EBI1 PLL circuits			
VDD_A_PLL_EBI2	EBI2 PLL circuits			
VDD_A_PLL_EBI3	EBI3 PLL circuits			
VDD_A_USB0_SS_DP_CORE	USB0 SS and DisplayPort core circuits	-0.3	1.056	V
VDD_A_USB1_SS_CORE	USB1 SS core circuits			
VDD_A_CSI012_1P2	MIPI CSI0, CSI1, CSI2 1.2 V circuits	-0.3	1.375	V
VDD_A_CSI345_1P2	MIPI CSI3, CSI4, CSI5 1.2 V circuits			
VDD_A_DSI_1P2	MIPI DSI 1.2 V circuits			
VDD_A_HV_EBI0	EBI0 PHY high-voltage circuits			
VDD_A_HV_EBI1	EBI1 PHY high-voltage circuits			
VDD_A_HV_EBI2	EBI2 PHY high-voltage circuits			
VDD_A_HV_EBI3	EBI3 PHY high-voltage circuits			
VDD_A_PCIE0_PLL_1P2	PCIe0 PLL 1.2 V circuits			
VDD_A_PCIE1_PLL_1P2	PCIe1 PLL 1.2 V circuits			
VDD_A_PCIE2_PLL_1P2	PCIe2 PLL 1.2 V circuits			
VDD_A_UFS0_1P2	UFS0 1.2 V circuits			
VDD_A_UFS1_1P2	UFS1 1.2 V circuits			
VDD_A_USB0_SS_DP_1P2	USB0 SS and DisplayPort 1.2 V circuits			
VDD_A_USB1_SS_1P2	USB1 SS 1.2 V circuits			
VDD_A_USB_HS_3P1	USB HS 3.1 V circuits	-0.3	3.52	V
VDD_PX0	Digital pad circuits - control signals	-0.3	2.112	V
VDD_PX2	Digital pad circuits - SDC2	-0.3	2.09 3.333	V
VDD_PX3	Digital pad circuits - most I/Os	-0.3	2.112	V
VDD1	POP DDR memory core - 1.8 V [1]			

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_PX10A VDD_PX10B	Digital pad circuits - UFS clock	-0.3	1.408	V
VDD_PX13	Digital pad circuits - SPU	-0.3	2.09	V
VDD_PX11 VDD_A_QREFS_1P8 VDD_QFPROM VDD_QFPROM_SP VDD_A_APC_CS_1P8 VDD_A_GFX_CS_1P8 VDD_A_NPU_Q6_CS_1P8 VDD_A_USB_HS_1P8	Digital pad circuits - CXO Reference voltage for QREFS 1.8 V circuits Programming QFPROM Programming QFPROM, SPU Application processor current sensor 1.8 V circuit Graphics current sensor 1.8 V circuit NPU_Q6 current sensor 1.8 V circuit USB HS 1.8 V circuit	-0.3	2.09	V
VDD_A_QREFS_1P25 VDD_PXVBIAS_SDC	Reference voltage for QREFS 1.25 V circuits Reference voltage for SDC	-0.3	1.485	V
VDD_IO_EBI0 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI1 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI2 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI3 (LPDDR5, freq <=1555 MHz) VDDQ (LPDDR5, freq <=1555 MHz)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR5 pads [1]	-0.3	0.407	V
VDD_IO_EBI0 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI1 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI2 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI3 (LPDDR5, freq > 1555 MHz) VDDQ (LPDDR5, freq > 1555 MHz)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR5 pads [1]	-0.3	0.627	V
VDD_IO_EBI0 (LPDDR4X) VDD_IO_EBI1 (LPDDR4X) VDD_IO_EBI2 (LPDDR4X) VDD_IO_EBI3 (LPDDR4X) VDDQ (LPDDR4X)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR4X pads [1]	-0.3	0.715	V
VDD2H (VDD2 for LPDDR4X)	POP DDR pads [1]	–	–	V
VDD2L	POP LPDDR5 pads [1]	–	–	V
T_S	Storage temperature [2] [3]	-55	+150	°C
ESD protection – see Section 7.1.				
Thermal conditions – see Section 4.5.				

1. See the LPDDR5 and LPDDR4X data sheets for VDD2H/VDD2L (for LPDDR5) and VDD2 (for LPDDR4X), and VDD1, VDDQ (for both standards) absolute maximum DC ratings for minimum and maximum voltages.
2. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
3. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-4). The SM8250 device meets all performance specifications listed in Section 3.6 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor			
	Turbo_L1	0.740	1.030	V
	Turbo	0.740	0.962	
	Nominal_L1	0.640	0.930	
	Nominal	0.605	0.898	
	SVS_L1	0.560	0.854	
	SVS	0.515	0.790	
	Low_SVS	0.470	0.730	
VDD_APC1	Qualcomm Kryo Gold application processor			
	Turbo_L3	0.796	1.135	V
	Turbo_L2	0.764	1.087	
	Turbo_L1	0.764	1.031	
	Turbo	0.764	0.963	
	Nominal_L1	0.660	0.931	
	Nominal	0.624	0.899	
	SVS_L1	0.576	0.859	
	SVS	0.532	0.791	
	Low_SVS	0.484	0.731	
VDD_GFX	Graphics			
	Nominal_L1 [2]	0.640	0.930	V
	Nominal	0.605	0.898	
	SVS_L2	0.580	0.886	
	SVS_L1	0.560	0.854	
	SVS_L0	0.545	0.838	
	SVS	0.515	0.790	
	Low_SVS	0.470	0.730	
VDD_CX	Digital core and EBI PHY digitial circuits			
VDD_D_EBI0	Turbo_L1	0.700	1.030	V
VDD_D_EBI1	Turbo	0.660	0.962	
VDD_D_EBI2	Nominal_L1	0.640	0.930	
VDD_D_EBI3	Nominal	0.605	0.898	
	SVS_L1	0.560	0.854	
	SVS	0.515	0.790	
	Low_SVS	0.470	0.730	
	Retention [3]	0.352	0.480	

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDD_MX	On-chip memory			
	Turbo_L1	0.740	1.030	V
	Turbo	0.740	0.998	
	Nominal_L1	0.695	0.998	
	Nominal	0.695	0.966	
	SVS_L2	0.695	0.954	
	SVS_L1	0.695	0.922	
	SVS	0.695	0.878	
	Retention [3]	0.512	0.668	
VDD_MM	Multimedia subsystem circuits			
	Turbo	0.660	1.030	V
	Nominal	0.605	0.966	
	SVS_L1	0.560	0.922	
	SVS	0.515	0.858	
	Low_SVS	0.470	0.798	
VDD_LPI_CX	Low power island core			
	Turbo	0.660	1.030	V
	Nominal	0.605	0.966	
	SVS	0.515	0.862	
	Low_SVS	0.470	0.798	
	Min_SVS	0.455	0.734	
VDD_LPI_MX	Low power island memory			
	Turbo	0.740	1.030	V
	Nominal	0.695	0.998	
	SVS	0.695	0.910	
VDD_A_EBI0	EBI PHY and PLL circuits			
VDD_A_EBI1				
VDD_A_EBI2	Turbo_L1	0.820	1.030	V
VDD_A_EBI3	Turbo	0.820	1.030	
VDD_A_PLL_EBI0	Nominal	0.820	1.030	
VDD_A_PLL_EBI1	SVS_L1	0.820	1.030	
VDD_A_PLL_EBI2	SVS	0.640	0.906	
VDD_A_PLL_EBI3	Low_SVS	0.640	0.906	

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Nominal_L1 of VDD_GFX is associated with SM8250-AB only.
3. The voltage setting at the PMIC for this mode in this power domain is a static setting. There is no scaling.

Table 3-3 Operating conditions

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A_SP_SENSOR	Secure processing unit sensors	0.83	0.88	0.93	V
VDD_A_CSI0_0P9	MIPI CSI0 0.9 V circuits				
VDD_A_CSI1_2_0P9	MIPI CSI1, CSI2 0.9 V circuits				
VDD_A_CSI3_0P9	MIPI CSI3 0.9 V circuits				
VDD_A_CSI4_5_0P9	MIPI CSI4, CSI5 0.9 V circuits				
VDD_A_DSI_0P9	MIPI DSI 0.9 V circuits				
VDD_A_DSI_PLL_0P9	MIPI DSI PLL 0.9 V circuits				
VDD_A_PCIE0_CORE	PCIe0 core circuits				
VDD_A_PCIE1_CORE	PCIe1 core circuits				
VDD_A_PCIE2_CORE	PCIe2 core circuits				
VDD_A_UFS0_CORE	UFS0 core circuits				
VDD_A_UFS1_CORE	UFS1 core circuits				
VDD_USB_HS_CORE	USB HS core circuits				
VDD_A_USB0_SS_DP_CORE	USB0 SS and DisplayPort core circuits	0.85	0.92	0.96	V
VDD_A_USB1_SS_CORE	USB1 SS core circuits				
VDD_A_CSI012_1P2	MIPI CSI0, CSI1, CSI2 1.2 V circuits	1.15	1.2	1.25	V
VDD_A_CSI345_1P2	MIPI CSI3, CSI4, CSI5 1.2 V circuits				
VDD_A_DSI_1P2	MIPI DSI 1.2 V circuits				
VDD_A_HV_EBI0	EBI0 PHY high-voltage circuits				
VDD_A_HV_EBI1	EBI1 PHY high-voltage circuits				
VDD_A_HV_EBI2	EBI2 PHY high-voltage circuits				
VDD_A_HV_EBI3	EBI3 PHY high-voltage circuits				
VDD_A_PCIE0_PLL_1P2	PCIe0 PLL 1.2 V circuits				
VDD_A_PCIE1_PLL_1P2	PCIe1 PLL 1.2 V circuits				
VDD_A_PCIE2_PLL_1P2	PCIe2 PLL 1.2 V circuits				
VDD_A_UFS0_1P2	UFS0 1.2 V circuits				
VDD_A_UFS1_1P2	UFS1 1.2 V circuits				
VDD_A_USB0_SS_DP_1P2	USB0 SS and DisplayPort 1.2 V circuits				
VDD_A_USB1_SS_1P2	USB1 SS 1.2 V circuits				
VDD_A_USB_HS_3P1	USB HS 3.1 V circuits	2.97	3.072	3.2	V
VDD_PX0	Digital pad circuits - control signals	1.7	1.8	1.92	V
VDD_PX2	Digital pad circuits - SDC2	1.7 2.72	1.8 2.96	1.9 3.03	V
VDD_PX3 VDD1	Digital pad circuits - most I/Os POP DDR memory core - 1.8 V [3]	1.7	1.8	1.92	V
VDD_PX10A VDD_PX10B	Digital pad circuits - UFS clock	1.12	1.2	1.28	V
VDD_PX13	Digital pad circuits - SPU	1.7	1.856	1.9	V

Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_PX11 VDD_A_QREFS_1P8 VDD_QFPROM VDD_QFPROM_SP VDD_A_APC_CS_1P8 VDD_A_GFX_CS_1P8 VDD_A_NPU_Q6_CS_1P8 VDD_A_USB_HS_1P8	Digital pad circuits - CXO Reference voltage for QREFS 1.8 V circuits Programming QFPROM Programming QFPROM, SPU Application processor current sensor 1.8 V circuit Graphics current sensor 1.8 V circuit NPU_Q6 current sensor 1.8 V circuit USB HS 1.8 V circuit	1.7	1.8	1.9	V
VDD_A_QREFS_1P25 VDD_PXVBIAS_SDC	Reference voltage for QREFS 1.25 V circuits Reference voltage for SDC	1.125	1.25	1.35	V
VDD_IO_EBI0 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI1 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI2 (LPDDR5, freq <=1555 MHz) VDD_IO_EBI3 (LPDDR5, freq <=1555 MHz) VDDQ (LPDDR5, freq <=1555 MHz)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR5 pads [3]	0.27	0.3	0.37	V
VDD_IO_EBI0 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI1 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI2 (LPDDR5, freq > 1555 MHz) VDD_IO_EBI3 (LPDDR5, freq > 1555 MHz) VDDQ (LPDDR5, freq > 1555 MHz)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR5 pads [3]	0.47	0.5	0.57	V
VDD_IO_EBI0 (LPDDR4X) VDD_IO_EBI1 (LPDDR4X) VDD_IO_EBI2 (LPDDR4X) VDD_IO_EBI3 (LPDDR4X) VDDQ (LPDDR4X)	EBI0 I/O memory circuits EBI1 I/O memory circuits EBI2 I/O memory circuits EBI3 I/O memory circuits POP LPDDR4X pads [3]	0.57	0.6	0.65	V
VDD2H (VDD2 for LPDDR4X)	POP DDR pads	– [3]	– [3]	– [3]	V
VDD2L	POP LPDDR5 pads	– [3]	– [3]	– [3]	V
Thermal conditions					
T_J	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. See the LPDDR5 and LPDDR4X data sheets for the recommended DC operating conditions (min/typ/max voltages) of VDD2H/VDD2L (for LPDDR5) and VDD2 (for LPDDR4X) and VDD1, VDDQ (for both standards).

3.3 Power distribution network

The following subsections contain the maximum impedance specifications for the power delivery network (PDN).

NOTE: Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, contact QTI for assistance (https://createpoint.qti.qualcomm.com).

Table 3-4 PDN specifications (for LPDDR5 package)

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_APC0	5	22	130	1	AA27, U27, U29, V28, V30, W25, W27, W31, Y26, Y28, Y30, Y31	AA26, AA28, AA30, AA32, AB27, T26, T28, T30, U26, U30, V25, V27, V29, V32, W28, W32, Y27, Y29
VDD_APC1	2	13	80	1	AA24, AA25, AA29, AA31, AB21, AB32, AC22, AC31, AD21, AD32, AE22, AE26, AE27, AE31, AF22, AF26, AF27, AF32, AG23, AG24, AG25, AG29, AG31	AA23, AA26, AA28, AA30, AA32, AA33, AB22, AB26, AB27, AB31, AC21, AC26, AC27, AC32, AD22, AD26, AD31, AD33, AE21, AE32, AF31, AF33, AG21, AG26, AG27, AG30, AG32, AH22, AH25, AH31, AH32, Y22, Y24
VDD_GFX	3	17	110	1	G12, G13, G14, G16, G18, H11, H7, H9, J10, J12, J18, J8, K11, L14, L16, L18, M11, N7, P11, R10, R8, T11, T13, T9, U10, U8	F12, F14, F15, F17, F18, G15, G17, G7, H10, H12, H18, H8, J11, J9, K12, K18, K19, K7, L11, L13, L15, L17, M12, M17, M7, N11, P12, P7, R11, R7, R9, T10, T12, T14, T7, T8, V10, V9
VDD_MM	5	30	170	1	AA11, AA13, AA9, AC11, AC9, AE11, AE13, AE15, AE17, AE9, AF16, AF18, AG11, AG13, AG15, AG17	AA8, AB10, AB12, AB14, AD10, AD12, AD14, AD16, AD8, AD9, AE19, AF10, AF12, AF14, AF9, AG10, AG12, AG14, AG16, AG18, AG19, AH12, AJ13, AJ17, Y10, Y12, Y14, Y9
VDD_CX	3	20	100	1	AB20, H27, H29, J21, J28, J30, J32, K21, K22, K27, K31, L20, L32, M19, M21, M23, M27, M31, M33, N16, N18, N20, N22, N24, N26, N32, P17, P21, P27, P31, R16, R18, R20, R22, R24, R26, R32, T21, T23, T25, T27, T29, T31, T33, U22, U24, V20, V21, V26, W22, W24, Y20, Y21, Y23	AA19, AA23, AC19, AC21, G27, H26, H28, H30, H31, H32, J20, J31, K19, K28, K30, K32, L21, L23, L27, L31, M17, M22, M25, M32, N27, N31, N33, P16, P19, P23, P25, P32, R27, R31, R33, T15, T17, T19, T22, T24, T26, T28, T30, T32, U18, U20, U26, U30, V19, V23, V25, V27, W19, W21, Y22, Y24
VDDMX	70	90	600	1	J7	H8, K7
	5	24	130	2	AA15, AA17, AB18, AC15, AC17, AD18, AD20, AF20, AF21, AG20, AG22, M13, M15, N14, P13, P15, R14, T16, T18, U11, U13, U15, V16, V18, V8, W11, W13, W15, W17, W9, Y18	AA19, AB14, AB16, AC19, AC21, AD14, AD16, AE19, AE21, AG19, AG21, AH19, AH20, AH21, AH22, H8, K7, L13, L15, M12, M17, P12, P16, T10, T12, T14, T15, T17, T19, T8, U18, V10, V12, V14, V15, V17, V19, V9, W19, W8, Y10, Y12, Y14, Y16, Y9
VDD_LPI_CX	70	83	500	1	H19, H20, H22, H23	G20, G21, G22, G24, H18, H24, J20, K19
VDD_LPI_MX	100	170	1000	1	J24, K23, L24	H24, K25, L23, M25

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

Table 3-5 PDN specifications (for LPDDR4X package)

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_APC0	5	22	130	1	AA25, U25, U27, V26, V28, W23, W25, W29, Y24, Y26, Y28, Y29	AA24, AA26, AA28, AA30, AB25, T24, T26, T28, U24, U28, V23, V25, V27, V30, W26, W30, Y25, Y27
VDD_APC1	2	13	80	1	AA22, AA23, AA27, AA29, AB19, AB30, AC20, AC29, AD19, AD30, AE20, AE24, AE25, AE29, AF20, AF24, AF25, AF30, AG21, AG22, AG23, AG27, AG29	AA21, AA24, AA26, AA28, AA30, AA31, AB20, AB24, AB25, AB29, AC19, AC24, AC25, AC30, AD20, AD24, AD29, AD31, AE19, AE30, AF29, AF31, AG19, AG24, AG25, AG28, AG30, AH20, AH23, AH29, AH30, Y20, Y22
VDD_GFX	3	17	110	1	G10, G11, G12, G14, G16, H5, H7, H9, J10, J16, J6, J8, K9, L12, L14, L16, M9, N5, P9, R6, R8, T11, T7, T9, U6, U8	F10, F12, F13, F15, F16, G13, G15, G5, H8, H10, H16, H6, J9, J7, K10, K16, K17, K5, L9, L11, L13, L15, M10, M15, M5, N9, P10, P5, R9, R5, R7, T8, T10, T12, T5, T6, V8, V7
VDD_MM	5	30	170	1	AA11, AA7, AA9, AC7, AC9, AE11, AE13, AE15, AE7, AE9, AF14, AF16, AG11, AG13, AG9, AG15	AA6, AB8, AB10, AB12, AD8, AD10, AD12, AD14, AD6, AD7, AE17, AF8, AF10, AF12, AF7, AG8, AG10, AG12, AG14, AG16, AG17, AH10, AJ11, AJ15, Y8, Y10, Y12, Y7
VDD_CX	3	20	100	1	AB18, H25, H27, J19, J26, J28, J30, K19, K20, K25, K29, L18, L30, M17, M19, M21, M25, M29, M31, N14, N16, N18, N20, N22, N24, N30, P15, P19, P25, P29, R14, R16, R18, R20, R22, R24, R30, T19, T21, T23, T25, T27, T29, T31, U20, U22, V18, V19, V24, W20, W22, Y18, Y19, Y21	AA17, AA21, AC17, AC19, G25, H24, H26, H28, H29, H30, J18, J29, K17, K26, K28, K30, L19, L21, L25, L29, M15, M20, M23, M30, N25, N29, N31, P14, P17, P21, P23, P30, R25, R29, R31, T13, T15, T17, T20, T22, T24, T26, T28, T30, U16, U18, U24, U28, V17, V21, V23, V25, W17, W19, Y20, Y22
VDDMX	70	90	600	1	J5	H6, K5
	5	24	130	2	AA13, AA15, AB16, AC13, AC15, AD16, AD18, AF18, AF19, AG18, AG20, M11, M13, N12, P11, P13, R12, T14, T16, U11, U13, U9, V14, V16, V6, W11, W13, W15, W7, W9, Y16	AA17, AB12, AB14, AC17, AC19, AD12, AD14, AE17, AE19, AG17, AG19, AH17, AH18, AH19, AH20, H6, K5, L11, L13, M10, M15, P10, P14, T8, T10, T12, T13, T15, T17, T6, U16, V8, V10, V12, V13, V15, V17, V7, W17, W6, Y8, Y10, Y12, Y14, Y7
VDD_LPI_CX	70	83	500	1	H17, H18, H20, H21	G18, G19, G20, G22, H16, H22, J18, K17
VDD_LPI_MX	100	170	1000	1	J22, K21, L22	H22, K23, L21, M23

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 to 200 MHz.

   $Z_{specification}$ =

Table 3-6 PDN specifications–DDR rails (for LPDDR5 package)

Power domain	DC resistance (mΩ)	Maximum effective impedance Zspecification 1 (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		Rmid_freq (mΩ)	L (pH)			
VDD_D_EBI0	25	50	550	1	E12	F12, E11, E13
VDD_D_EBI2	25	50	550	2	E27	F26, E26, F28, F27, E28
VDD_D_EBI3	25	50	550	3	AJ28	AJ27, AH27
VDD_D_EBI1	25	50	550	4	AK12	AL12, AL11, AJ13
VDD_A_(PLL)_EBI0	26	120	1000	1	G9, G8, F9	F8, G7, H10, H8, F10, E11
VDD_A_(PLL)_EBI1	26	120	1000	2	AH9, AH8, AG9	AF10, AF9, AG10
VDD_A_(PLL)_EBI2	26	120	1000	3	G29, G28, F29	H28, G27, F27, F28, E28
VDD_A_(PLL)_EBI3	26	120	1000	4	AJ29, AH29, AH28	AJ27, AH27, AG27, AG30, AK30
VDD_IO_EBI0	27	53	1100	1	G11, G10, F11	H12, H10, F12, E11, F10
VDD_IO_EBI1	27	53	1100	2	AJ11, AH11, AH10	AG12, AG10, AH12
VDD_IO_EBI2	27	53	1100	3	G31, G30, F30	H32, H31, H30, G32, F32, F31, E31
VDD_IO_EBI3	27	53	1100	4	AJ31, AJ30, AH30	AH32, AH31, AG30, AK32, AK31, AK30

1. The PDN AC effective impedance specification (mask) is obtained by plotting Zspecification using Rmid_freq and AC inductance (L) values. Zspecification is the maximum impedance allowed from 1 to 200 MHz.

   Zspecification =

Table 3-7 PDN specifications–DDR rails (for LPDDR4X package)

Power domain	DC resistance (mΩ)	Maximum effective impedance Zspecification 1 (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		Rmid_freq (mΩ)	L (pH)			
VDD_D_EBI0	25	50	550	1	E10	F10, E9, E11
VDD_D_EBI2	25	50	550	2	E25	F24, E24, F26, F25, E26
VDD_D_EBI3	25	50	550	3	AJ26	AJ25, AH25
VDD_D_EBI1	25	50	550	4	AK10	AL10, AL9, AJ11
VDD_A_(PLL)_EBI0	26	120	1000	1	G7, G6, F7	F6, G5, H8, H6, F8, E9
VDD_A_(PLL)_EBI1	26	120	1000	2	AH7, AH6, AG7	AF8, AF7, AG8
VDD_A_(PLL)_EBI2	26	120	1000	3	G27, G26, F27	H26, G25, F25, F26, E26
VDD_A_(PLL)_EBI3	26	120	1000	4	AJ27, AH27, AH26	AJ25, AH25, AG25, AG28, AK28
VDD_IO_EBI0	27	53	1100	1	G9, G8, F9	H10, H8, F10, E9, F8
VDD_IO_EBI1	27	53	1100	2	AJ9, AH9, AH8	AG10, AG8, AH10
VDD_IO_EBI2	27	53	1100	3	G29, G28, F28	H30, H29, H28, G30, F30, F29, E29
VDD_IO_EBI3	27	53	1100	4	AJ29, AJ28, AH28	AH30, AH29, AG28, AK30, AK29, AK28

1. The PDN AC effective impedance specification (mask) is obtained by plotting Zspecification using Rmid_freq and AC inductance (L) values. Zspecification is the maximum impedance allowed from 1 to 200 MHz.

   Zspecification =

Table 3-8 PDN specifications–SerDes rails (for LPDDR5 package)

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_A_CSI0_0P9	84	177	1125	1	AF8	AE7, AF9
VDD_A_CSI1_2_0P9	84	88	563	2	AG8	AE7, AF9
VDD_A_CSI3_0P9	84	177	1125	3	AH18	AJ19, AJ18, AJ17, AH19, AG16, AG19, AG18
VDD_A_CSI_4_5_0P9	84	88	563	4	AH17	AJ19, AJ18, AJ17, AH19, AG16, AG19, AG18
VDD_A_PCIE0_CORE	89	118	750	5	AA6	AB5, Y5
VDD_A_PCIE1_CORE	89	98	625	6	AC8	AD9, AD8
VDD_A_UFS1_CORE	101	177	1125	7	AA7	AA8
VDD_A_UFS0_CORE	98	119	760	8	Y33	AA33, AA32, W32
VDD_A_PCIE2_CORE	89	98	625	9	AH33	AH32, AG32
VDD_A_DSI_0P9	119	85	540	10	AH24	AJ22, AH22, AJ25, AH25, AJ24, AJ23
VDD_A_DSI_PLL_0P9	458	85	540	11	AH23	AJ22, AH22, AJ25, AH25, AJ24, AJ23
VDD_A_USB0_SS_DP_CORE	73	98	625	1	AB33	AA33, AA32, AC32
VDD_A_USB1_SS_CORE	192	138	880	2	AG33	AF33, AH32, AG32
VDD_A_CSI345_1P2	204	86	550	1	AK11	AL12, AL11
VDD_A_PCIE0_PLL_1P2	480	236	1500	2	AB8	AA8
VDD_A_PCIE1_PLL_1P2	480	236	1500	3	AB9	AB10
VDD_A_CSI012_1P2	204	79	500	4	AE8	AE7, AD9, AD8, AF9
VDD_A_UFS1_1P2	656	236	1500	5	Y8	Y9, W8
VDD_A_DSI_1P2	225	79	500	6	AH26	AJ27, AH27, AG27, AJ25, AH25, AJ26, AG26
VDD_A_PCIE2_PLL_1P2	480	236	1500	7	AD34	AD33
VDD_A_USB1_SS_1P2	800	236	1500	8	AD35	AE36, AD36, AC36
VDD_A_UFS0_1P2	638	236	1500	9	Y34	AA33, W35
VDD_A_USB0_SS_DP_1P2	364	236	1500	10	Y35	W35, AA36, Y36
VDD_PXVBIAS_SDC	–	157	1000	1	V6	W5, V5, U5

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC Inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 to 200 MHz.

   $Z_{specification}$ =

Table 3-9 PDN specifications–SerDes rails (for LPDDR4X package)

Power domain	DC resistance (mΩ)	Maximum impedance $Z_{specification}$ [1] (1-200 MHz)		Port number	Pin number of positive ports	Pin number of negative ports
		R_{mid_freq} (mΩ)	L (pH)			
VDD_A_CSI0_0P9	84	177	1125	1	AF6	AE5, AF7
VDD_A_CSI1_2_0P9	84	88	563	2	AG6	AE5, AF7
VDD_A_CSI3_0P9	84	177	1125	3	AH16	AJ17, AJ16, AJ15, AH17, AG14, AG17, AG16
VDD_A_CSI_4_5_0P9	84	88	563	4	AH15	AJ17, AJ16, AJ15, AH17, AG14, AG17, AG16
VDD_A_PCIE0_CORE	89	118	750	5	AA4	AB3, Y3
VDD_A_PCIE1_CORE	89	98	625	6	AC6	AD7, AD6
VDD_A_UFS1_CORE	101	177	1125	7	AA5	AA6
VDD_A_UFS0_CORE	98	119	760	8	Y31	AA31, AA30, W30
VDD_A_PCIE2_CORE	89	98	625	9	AH31	AH30, AG30
VDD_A_DSI_0P9	119	85	540	10	AH22	AJ20, AH20, AJ23, AH23, AJ22, AJ21
VDD_A_DSI_PLL_0P9	458	85	540	11	AH21	AJ20, AH20, AJ23, AH23, AJ22, AJ21
VDD_A_USB0_SS_DP_CORE	73	98	625	1	AB31	AA31, AA30, AC30
VDD_A_USB1_SS_CORE	192	138	880	2	AG31	AF31, AH30, AG30
VDD_A_CSI345_1P2	204	86	550	1	AK9	AL10, AL9
VDD_A_PCIE0_PLL_1P2	480	236	1500	2	AB6	AA6
VDD_A_PCIE1_PLL_1P2	480	236	1500	3	AB7	AB8
VDD_A_CSI012_1P2	204	79	500	4	AE6	AE5, AD7, AD6, AF7
VDD_A_UFS1_1P2	656	236	1500	5	Y6	Y7, W6
VDD_A_DSI_1P2	225	79	500	6	AH24	AJ25, AH25, AG25, AJ23, AH23, AJ24, AG24
VDD_A_PCIE2_PLL_1P2	480	236	1500	7	AD32	AD31
VDD_A_USB1_SS_1P2	800	236	1500	8	AD33	AE34, AD34, AC34
VDD_A_UFS0_1P2	638	236	1500	9	Y32	AA31, W33
VDD_A_USB0_SS_DP_1P2	364	236	1500	10	Y33	W33, AA34, Y34
VDD_PXVBIAS_SDC	–	157	1000	1	V4	W3, V3, U3

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC Inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 to 200 MHz.

   $Z_{specification}$ =

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8250 + SDX55M Linux Android Current Consumption Data* (80-PL546-7).

3.5 Dhrystone and rock bottom maximum power

Table 3-10 Dhrystone and rock bottom maximum power

SDM version	Kryo octa-core Dhrystone (W) [1, 2, 3]	Rock bottom (mW) [4]
SM8250 (BB/feature code = AA)	7	7
SM8250 (BB/feature code = AB)	8	7
SM8250 (BB/feature code = AC)	9	7

1. This Kryo octa-core Dhrystone specification applies to SM8250 CS devices that run Kryo Gold prime core at 2.842 GHz for the AA variant, 3.091 GHz for the AB variant, and 3.1872 GHz for the AC variant; and the other three Kryo Gold cores at 2.419 GHz and Kryo quad Silver cores at 1.805 GHz at $T_{junction}$ = 85°C.
2. Dhrystone power should be measured on the VDD_APC0 and VDD_APC1 rails, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).
4. Rock bottom power (VDD_CX and VDD_MX) should be measured at the VDD_CX and VDD_MX rails. See AIR1 in Table 3-1 (Test definitions) of *SM8250+SDX55M Linux Android Current Consumption Data* (80-PL546-7) for the test setup.

3.6 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM8250 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-11 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDD_PX3	V

Table 3-11 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDD_PX3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	1.0	µA
I_{IL}	Input low leakage current [1]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [1]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage	VDD_PX3 - 0.45	VDD_PX3	V
V_{OL}	Low-level output voltage	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
2. Pin voltage = VDD_PX3 maximum. For keeper pins, pin voltage = VDD_PX3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDD_PX3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_PX3 maximum.

Table 3-12 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA

Table 3-12 SDC 3 V mode DC specifications (cont.)

Parameter	Description	Min	Typ	Max	Units
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_PX2	–	VDD_PX2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDD_PX2	V

Table 3-13 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 Digital I/O characteristics for VDD_PX10A/VDD_PX10B (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDD_PX10	V
V_{OH}	Output high-level voltage	0.75 × VDD_PX10	VDD_PX10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE: All SM8250 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described in more detail in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-1.

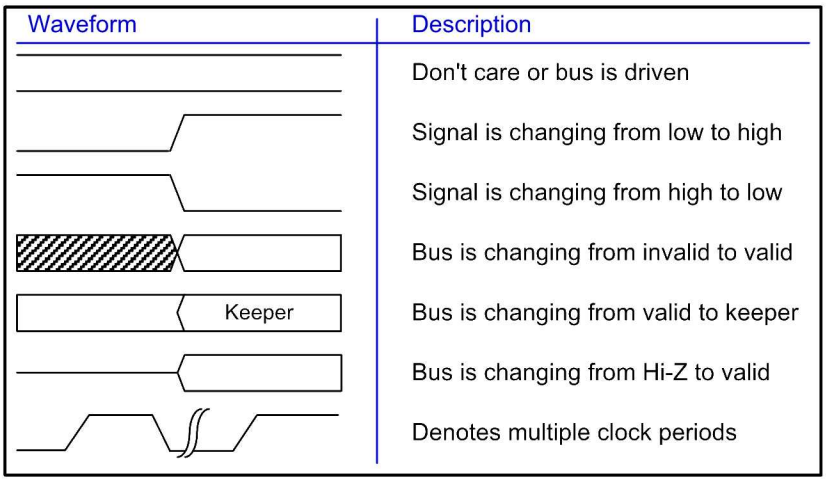


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.7.2 Rise and fall time specifications

The testers that characterize SM8250 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-2.

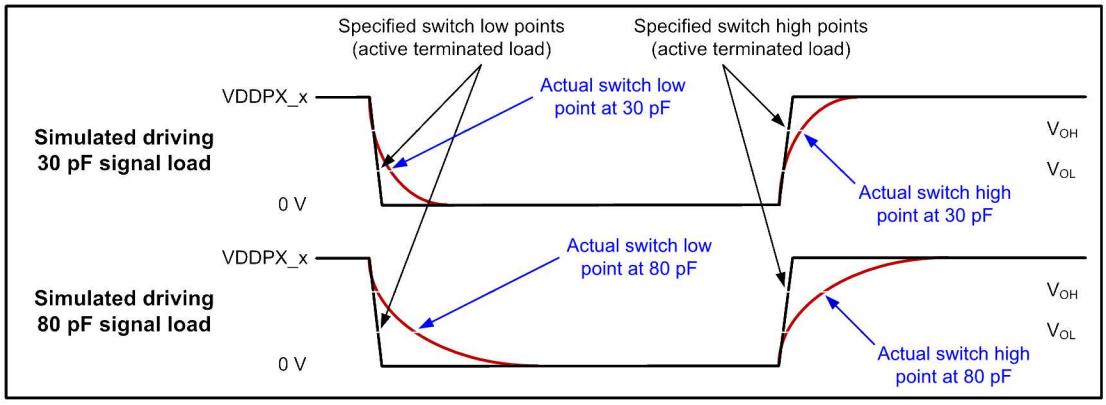


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8250 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The SM8250 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

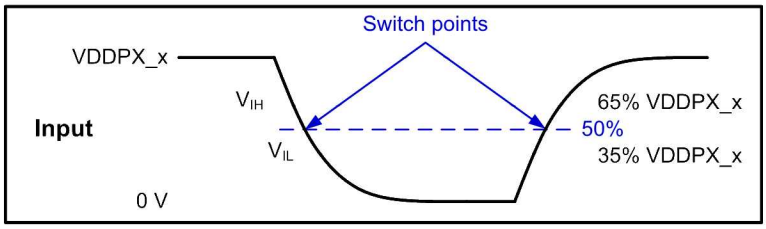


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX_x} - 50 mV or more
- V_{OL} ~ 50 mV or less

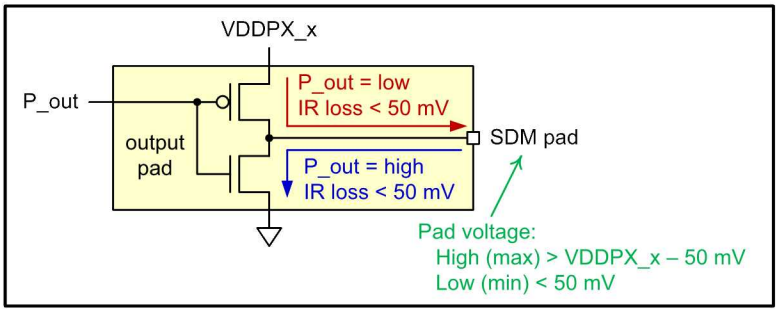


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5/LPDDR4X SDRAM memory that is attached to the top of the SM8250 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8250 Recommendations* (80-VP300-16).

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SM8250 device supports up to six D-PHY or C-PHY camera interfaces.

Table 3-15 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v2.0	RAW7 is not supported; DPCM is not supported.
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.2	None

3.9.2 Audio support

The SM8250 supports the WCD9380/WCD9385 audio codec IC to provide the system's audio functions. SM8250 audio-related interface options with the WCD include:

- Digital microphone: Section 3.10.6
- SWR: Section 3.10.7
- SLIMbus: Section 3.10.8
- I^2S: Section 3.10.9
- PCM/TDM: Section 3.10.10
- I^2C/I3C: Section 3.10.12

See the *WCD9380/WCD9385 Audio Codec Device Specification* (80-PL335-1) for performance characteristics.

3.9.3 Display support

The SM8250 device supports up to two D-PHY or C-PHY displays.

Table 3-16 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

3.9.4 DMB support

The SM8250 supports an external DMB solution using the following interface options:

- SPI: Section 3.10.13
- SD: Section 3.10.1

3.10 Connectivity

The connectivity functions supported by the SM8250 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- Digital microphone PDM interface
- SoundWire (SWR) interface
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Touchscreen connections
- Through proper configuration of the 20 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - I3C

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

Table 3-17 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

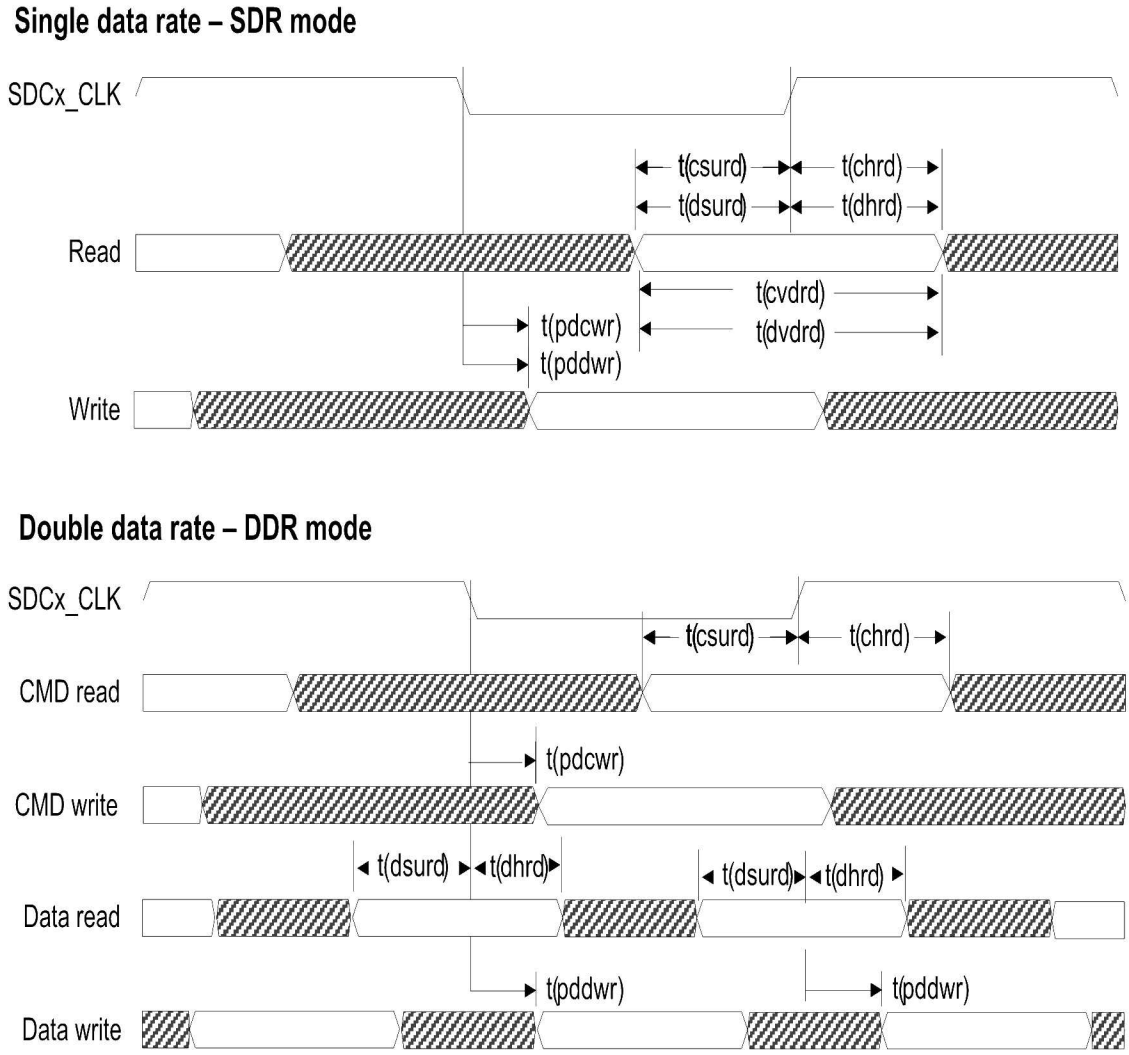


Figure 3-5 SD interface timing

3.10.2 USB interfaces

Table 3-18 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	None
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.10.3 DisplayPort

Table 3-19 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.10.4 PCIe interface

Table 3-20 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link upconfigure capability

3.10.5 UFS interface

Table 3-21 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	Rate B
Universal Flash Storage (UFS), Version 2.1	None

3.10.6 Digital microphone PDM interface

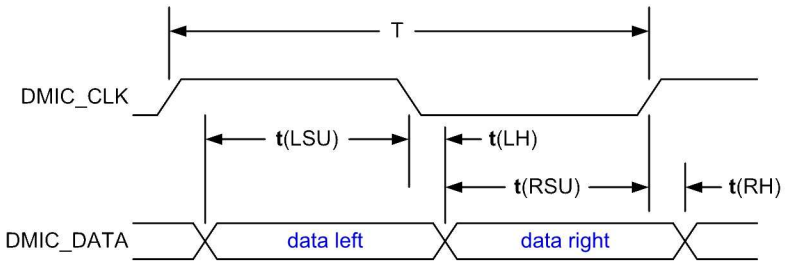


Figure 3-6 Digital microphone PDM interface timing

Table 3-22 Digital microphone timing

Parameter		Min	Typ	Max	Units
1/T	DMIC clock frequency	0.6	–	6.144	MHz
	DMIC clock duty cycle	45	–	55	%

Table 3-22 Digital microphone timing (cont.)

t(LSU)	Data left setup time to clock falling edge	10	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	ns

3.10.7 SoundWire (SWR) interface

SM8250 SoundWire PHY timing parameters, as specified in Table 3-23, are compliant to clock and data specifications, as specified in the *MIPI Alliance Specification for SoundWire Version 0.8, Revision 04.* See Figure 3-7 and Figure 3-8.

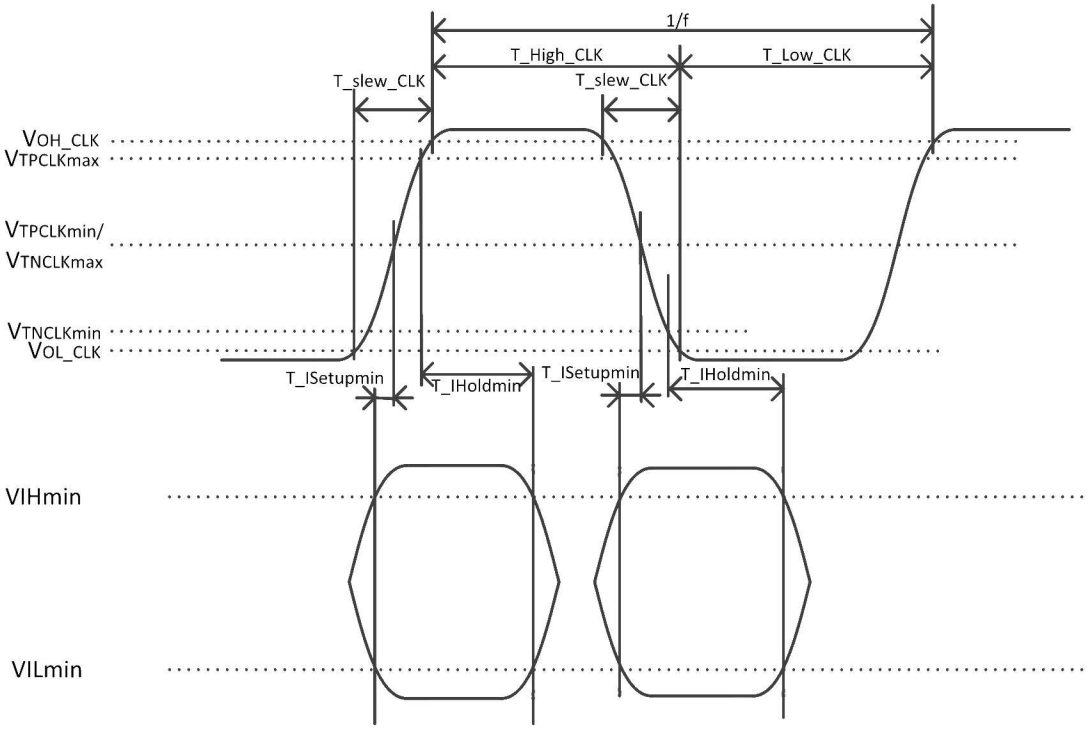


Figure 3-7 PHY timing – clock output/input and data input

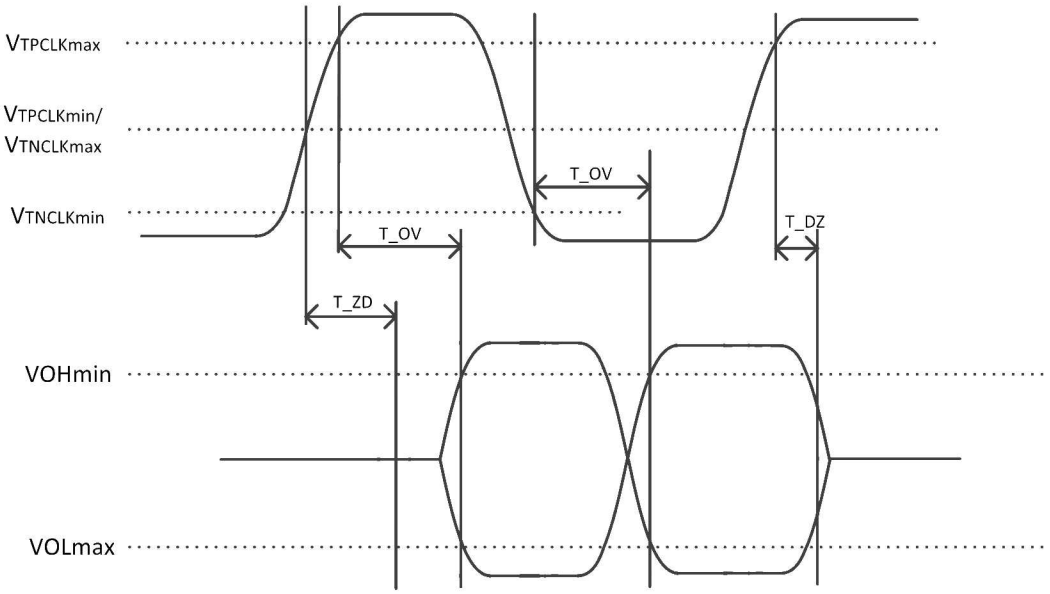


Figure 3-8 PHY timing – clock output and data output

Table 3-23 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Units
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	ns
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	4	–	ns
t_IHold_min_Data_1V8	Input hold time	–	5	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.10.8 SLIMbus interface

Table 3-24 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.10.9 I²S interfaces

There are two I²S interface types supported by the SM8250:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI²S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-25 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

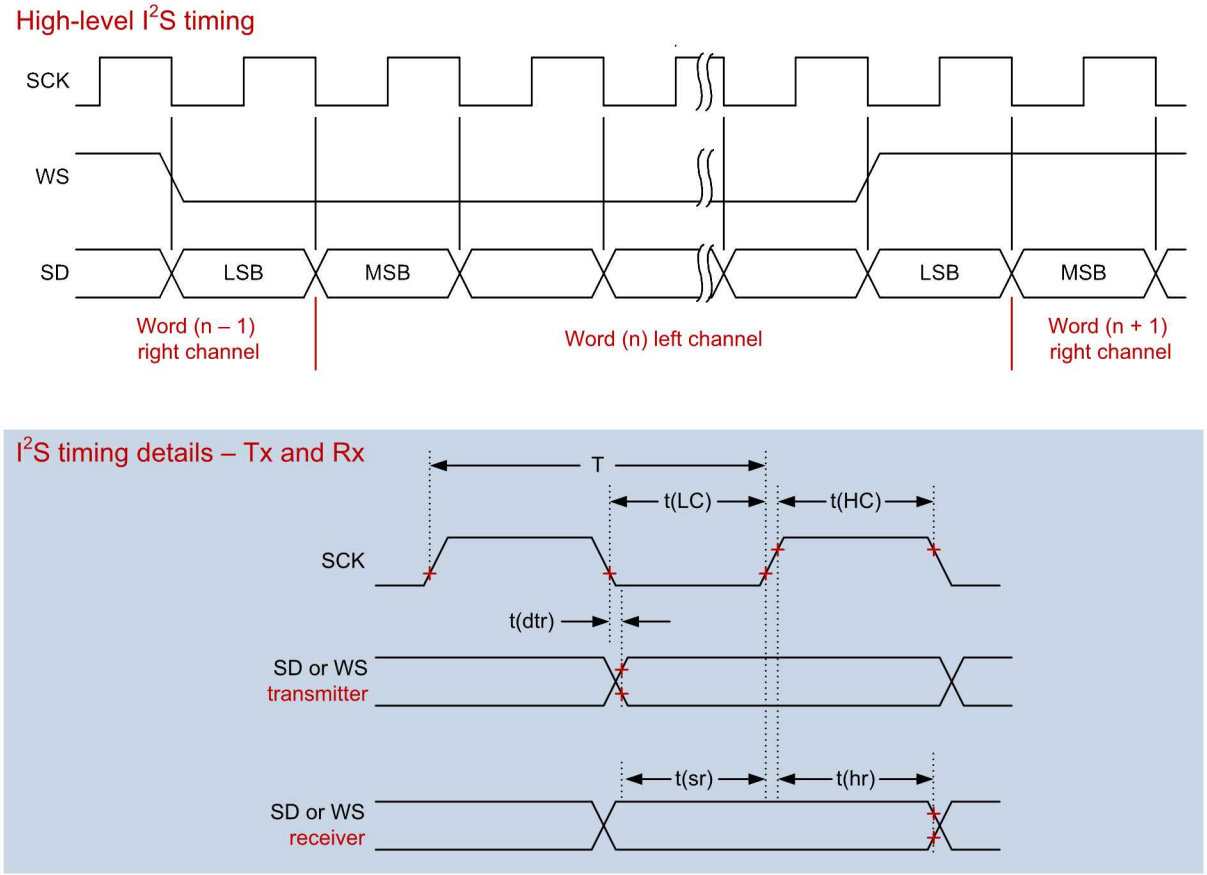


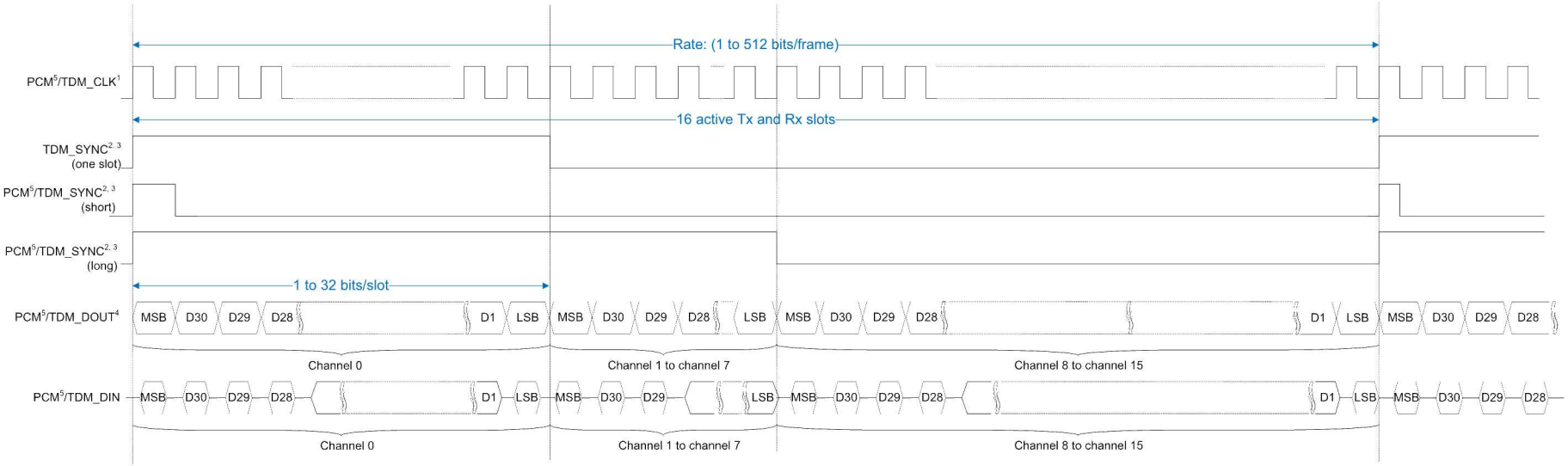
Figure 3-9 I²S timing diagram

Table 3-26 I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60 × T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

1. Load capacitance is between 10 pF and 40 pF.

3.10.10 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-10 PCM/TDM audio format with different sync modes

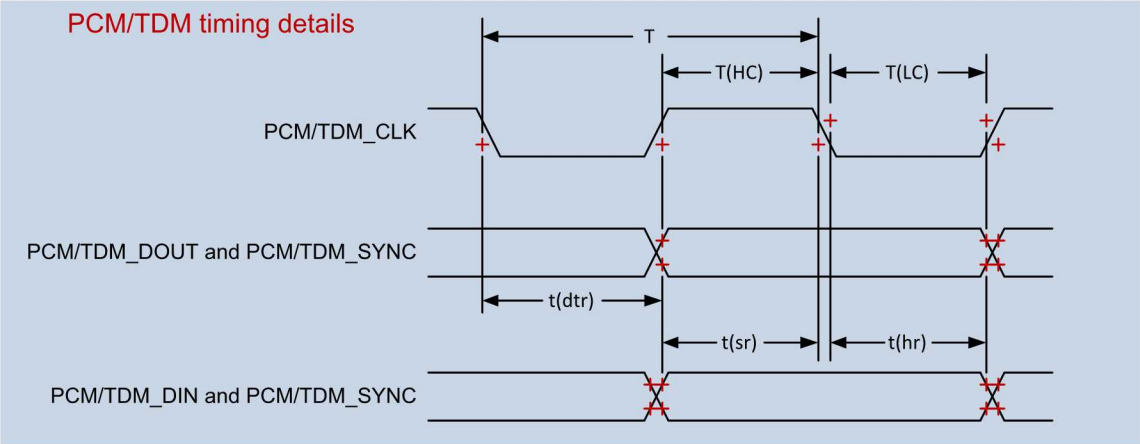


Figure 3-11 PCM/TDM timing diagram

Table 3-27 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns
Slave mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.40 × T	0.60 × T	ns
t(LC)	Clock low		0.40 × T	0.60 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns

1. Load capacitance is between 10 pF to 40 pF.
2. End-to-end testing for the TDM clock is completed up to 12.288 MHz.

3.10.11 Touchscreen connections

Touchscreen panels are supported using I^2C buses (Section 3.10.12) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.12 I²C/I3C interface

Table 3-28 Supported I²C/I3C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.10.13 Serial peripheral interface

The SM8250 supports SPI as a master only. Any one of the 20 QUP ports can be configured as an SPI master.

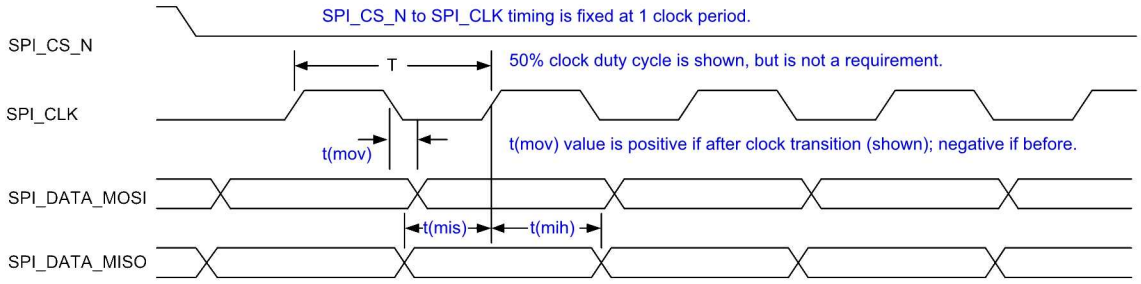


Figure 3-12 SPI master timing diagram

Table 3-29 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz CXO input

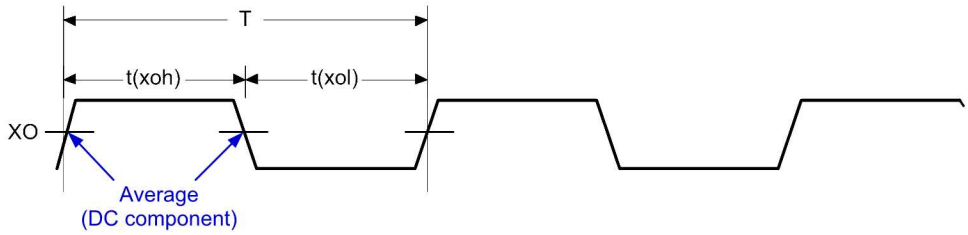


Figure 3-13 XO timing parameters

Table 3-30 CXO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *38.4 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-NJ458-19) document for more information.

3.11.1.2 Sleep clock

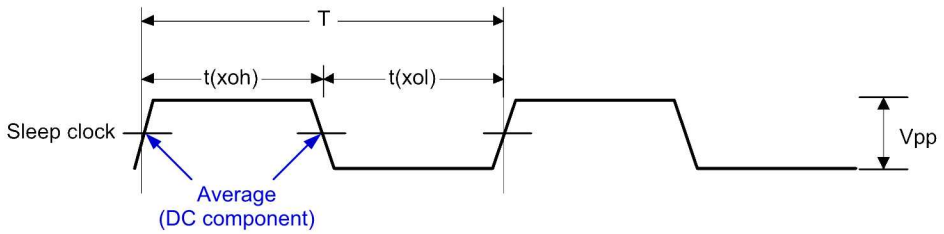


Figure 3-14 Sleep-clock timing parameters

Table 3-31 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.521	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

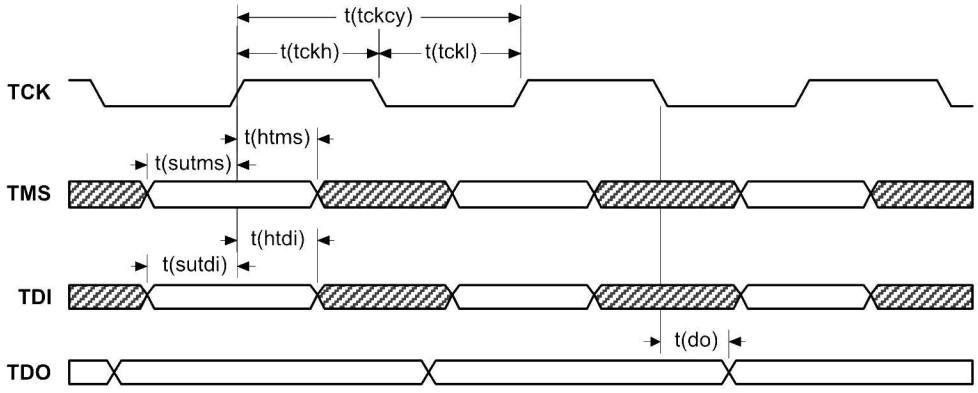


Figure 3-15 JTAG interface timing diagram

Table 3-32 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.11.4 SWD

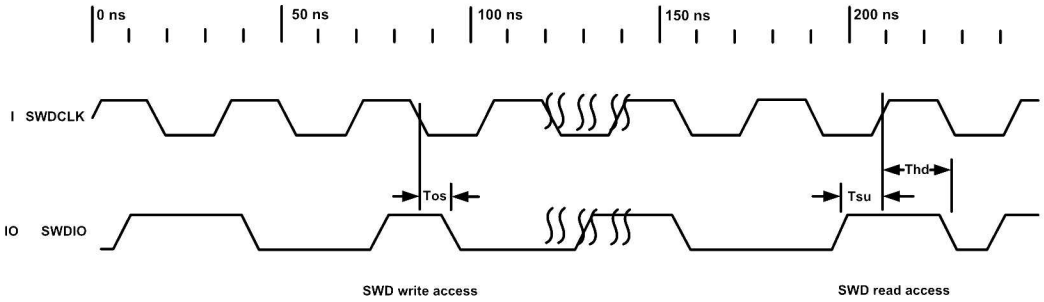


Figure 3-16 SWD write and read AC timing diagram

Table 3-33 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

Note: SWDCLK runs at 20 MHz or lower.

3.12 Power management interface

The digital I/Os must meet the logic-level requirements specified in Section 3.6.

3.12.1 System power management interface (SPMI)

Table 3-34 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM8250 device is available in the MPSP1099 (for LPDDR5) or MPSP1017 (for LPDDR4X), a PoP system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 1099 or 1017 PSP, and it accepts memory modules from above that are equivalent to a 496 (LPDDR5) or 556 (LPDDR4X) NSP. The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawings are shown in Figure 4-1 and Figure 4-2.

NOTE: Click the following links to download *Package Outline Drawing, MPSP1099, 12.4 × 14.0 × 0.56 mm, ST94, M147, SB136, PB 496NSP, PL1, MEP (NT90-VV027-2)* from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-VV027-2

After successfully logging on, the document is downloaded.

NOTE: Click the following links to download *Package Outline Drawing, MPSP1017, 12.4 × 12.7 × 0.56 mm, ST94, M147, SB136, PB 556NSP, PL1, MEP (NT90-VV026-3)* from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-VV026-3

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the **Related Files** line that is located directly underneath the PDF link.

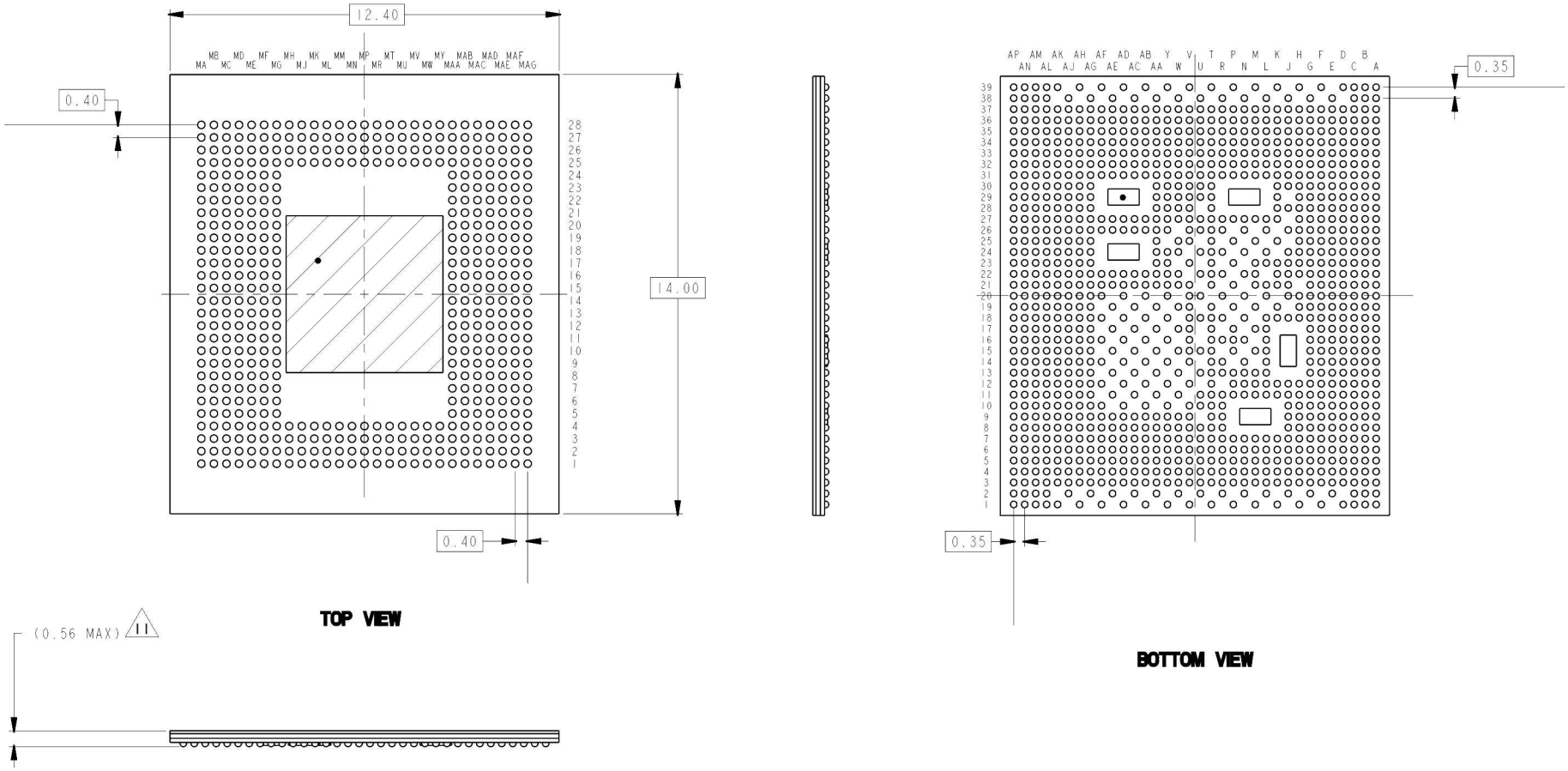


Figure 4-1 MPSP1099 outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

NOTE: The coplanarity specification for the SM8250 bottom package is 100 µm.

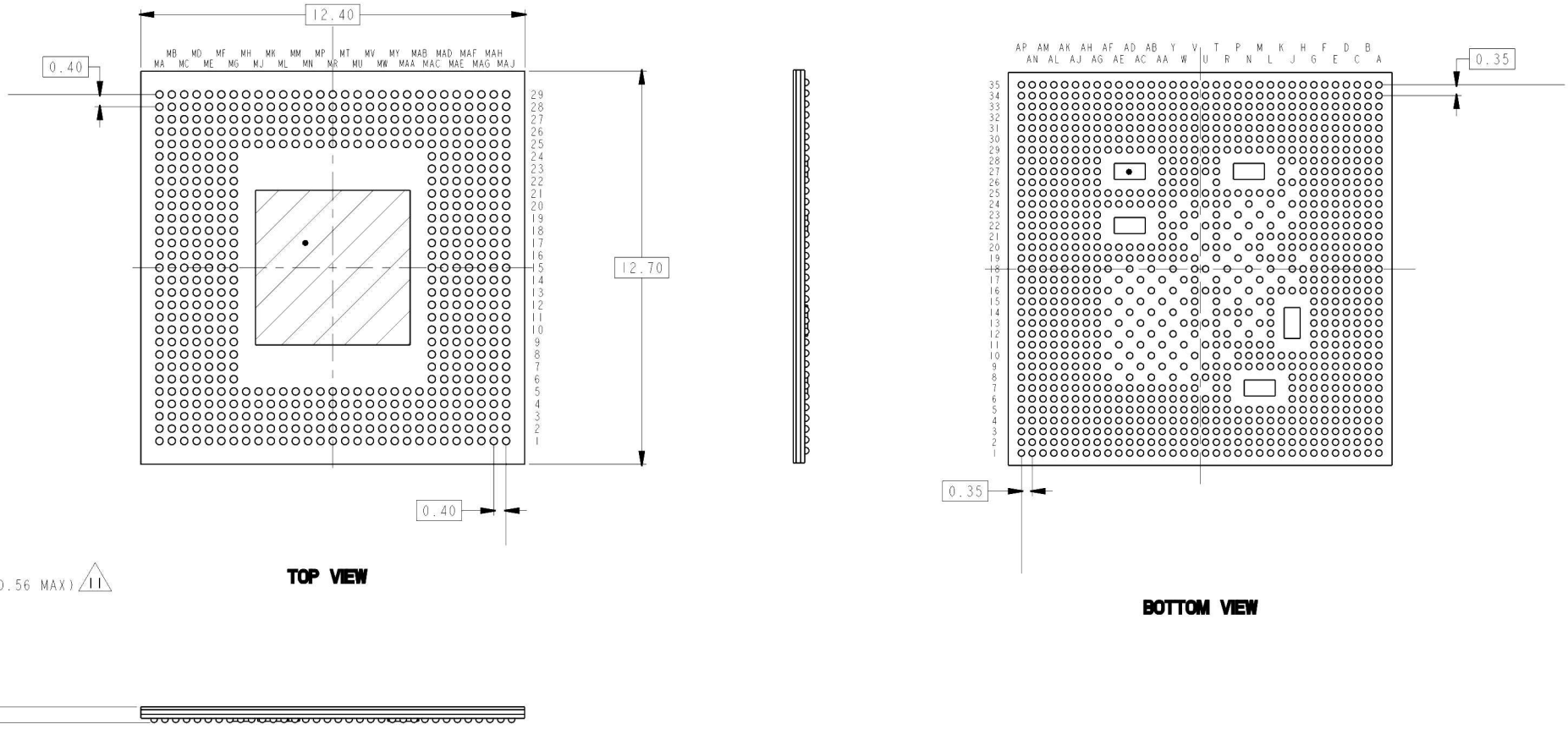


Figure 4-2 MPSP1017 outline drawing

NOTE: This is a simplified outline drawing. Click the link on the first page of this chapter to download the complete, up-to-date package outline drawing.

NOTE: The coplanarity specification for the SM8250 bottom package is 100 µm.

4.2 Part marking

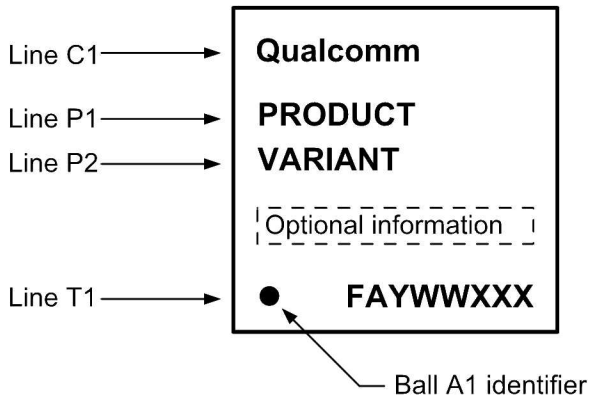


Figure 4-3 SM8250 device marking (top view, not to scale) for both LPDDR5 and LPDDR4X packages

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	QTI product name ■ SM8250
P2	VARIANT	PRR-BB ■ See Table 4-4 for the assigned values.
	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ■ F = F (TSMC) A = assembly site code ■ A = C (Amkor, Korea) ■ A = X (Amkor, Japan) Y = single/last digit of year WW = two digit work week of current year XXX = serial number
	●	Ball A1 indicator

NOTE: For complete marking definitions of all SM8250 variants and revisions, see the *SM8250 Device Revision Guide* (80-PL546-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 Related register (0x00780198)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining the feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example 1	SM-8250	-1	-MPSP	1017			-TR	-00	-0	-AA
Example 2	SM-8250	-0	-MPSP	1099			-TR	-00	-0	-AA

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8250-1-MPSP1017-TR-00-0-AA
- Example 2: SM-8250-0-MPSP1099-TR-00-0-AA

Notes:

- The shipping package is either TR (tape and reel) or MT (matrix tray).

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Hardware revision	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	Hardware revision number	FEATURE_ID [2]	S value	Comments	Sample date
SM8250	ES1	v1.0	000-AA	0x0 00C3 0E1	0x0	0	SM8250 (000-0-AA), MPSP1099, BASE AP, LPDDR5	04/30/2019
SM8250	ES1	v1.0	100-AA	0x0 00C3 0E1	0x4	0	SM8250 (100-0-AA), MPSP1017, BASE AP, LPDDR4X	04/30/2019
SM8250	ES2	v2.0	001-AA	0x1 00C3 0E1	0x5	0	SM8250 (001-0-AA), MPSP1099, BASE AP, LPDDR5	7/31/2019
SM8250	ES2	v2.0	101-AA	0x1 00C3 0E1	0x3	0	SM8250 (101-0-AA), MPSP1017, BASE AP, LPDDR4X	7/31/2019
SM8250	CS	v2.1	002-AA	0x2 00C3 0E1	0x3	0	SM8250 (002-0-AA), MPSP1099, BASE AP, LPDDR5	9/30/2019
SM8250	ES3	v2.1	102-AA	0x2 00C3 0E1	0x0	0	SM8250 (102-0-AA), MPSP1017, BASE AP, LPDDR4X, YWW < 944	9/30/2019
SM8250	CS	v2.1	102-AA	0x2 00C3 0E1	0x0	0	SM8250 (102-0-AA), MPSP1017, BASE AP, LPDDR4X, YWW ≥ 944	11/30/2019
SM8250	ES	v2.1	002-AB	0x2 00C3 0E1	0x9	0	SM8250 (002-0-AB), MPSP1099, BASE AP, LPDDR5, Gold Prime at 3.091 GHz GPU at 670 MHz	4/30/2020
SM8250	CS	v2.1	002-AB CS date code is as follows ■ Amkor: 027	0x2 00C3 0E1	0x9	0	SM8250 (002-0-AB), MPSP1099, BASE AP, LPDDR5, Gold Prime at 3.091 GHz, GPU at 670 MHz	6/30/2020
SM8250	ES	v2.1	002-AC	0x2 00C3 0E1	0xE	0	SM8250 (002-0-AC), MPSP1099, BASE AP, LPDDR5, Gold Prime at 3.1872 GHz	10/30/2020
SM8250	CS	v2.1	002-AC CS date code is as follows ■ Amkor: 049	0x2 00C3 0E1	0xE	0	SM8250 (002-0-AC), MPSP1099, BASE AP, LPDDR5, Gold Prime at 3.1872 GHz	12/1/2020

Table 4-4 Device identification details (cont.)

Device	Sample type	Hardware revision	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	Hardware revision number	FEATURE_ID [2]	S value	Comments	Sample date
SM8250	ES	v2.1	102-AC	0x2 00C3 0E1	0x10	0	SM8250 (102-0-AC), MPSP1017, BASE AP, LPDDR4X, Gold Prime at 3.1872 GHz	10/30/2020
SM8250	CS	v2.1	102-AC CS date code is as follows ■ Amkor: 049	0x2 00C3 0E1	0x10	0	SM8250 (102-0-AC), MPSP1017, BASE AP, LPDDR4X, Gold Prime at 3.1872 GHz	12/1/2020

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.

4.3.2 Daisy chain devices

The SM8250 daisy chain ordering part numbers are TP-MPSP1017-1 (LPDDR4X) and TP-MPSP1099-1 (LPDDR5).

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-5.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SM8250 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8250 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the
SM8250 LPDDR5 8GB PACKAGE THERMAL MODEL ICEPAK (HS11-PL546-5HW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PL546-5HW
SM8250 LPDDR5 8GB PACKAGE THERMAL MODEL FLOTHERM (HS11-PL546-6HW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PL546-6HW
SM8250 LPDDR5 6GB PACKAGE THERMAL MODEL ICEPAK (HS11-PL546-5AHW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PL546-5AHW
SM8250 LPDDR5 6GB PACKAGE THERMAL MODEL FLOTHERM (HS11-PL546-6AHW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PL546-6AHW

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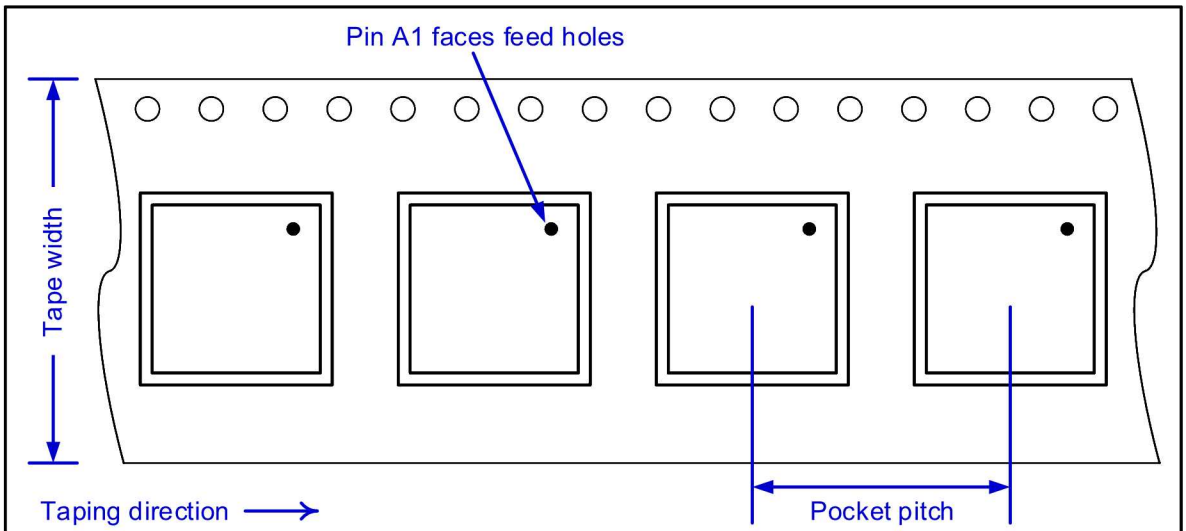
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8250 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

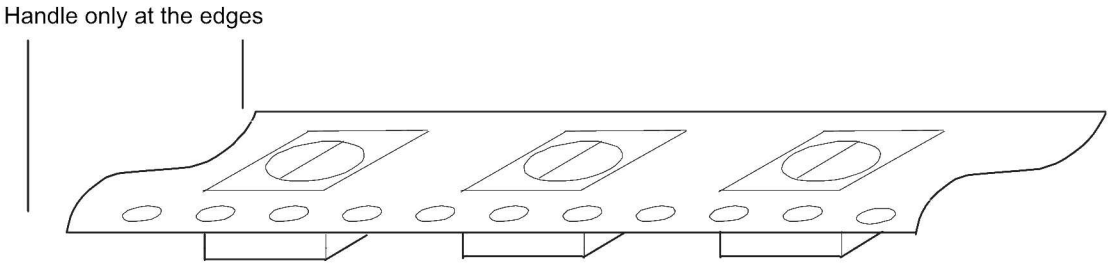


Figure 5-2 Tape handling

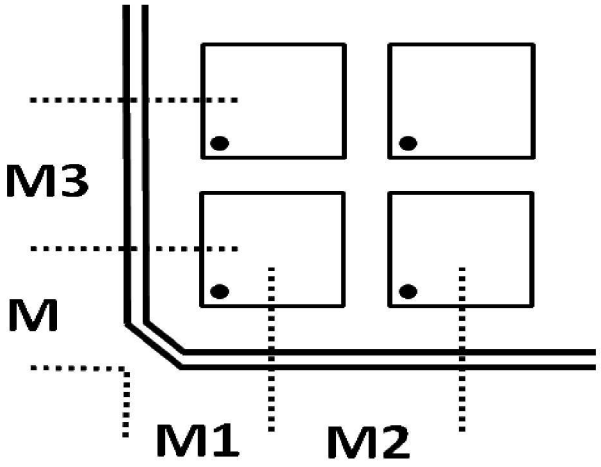
5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

For LPDDR5 package, each tray of the SM8250 contains up to 108 devices. Production orders of the SM8250 that are shipped in matrix tray carriers will be in [10 + 1] tray stacks of [1080] units. The stacking configuration and quantity for sample orders will vary.

See Figure 5-3 for matrix-tray key attributes and dimensions (for LPDDR5 package).



Key dimensions	
Array	6 x 18 (108)
M	20.45 mm
M1	13.00 mm
M2	17.00 mm
M3	19.00 mm

Figure 5-3 Matrix-tray key attributes and dimensions (for LPDDR5 package)

For LPDDR4X package, each tray of the SM8250 contains up to 126 devices. Production orders of the SM8250 that are shipped in matrix tray carriers will be in [10 + 1] tray stacks of [1260] units. The stacking configuration and quantity for sample orders will vary.

See Figure 5-4 for matrix-tray key attributes and dimensions (for LPDDR4X package).

Key dimensions	
Array	7 x 18 (126)
M	14.85 mm
M1	13.00 mm
M2	17.00 mm
M3	17.70 mm

Figure 5-4 Matrix-tray key attributes and dimensions (for LPDDR4X package)

5.2 Storage

5.2.1 Bagged storage conditions

SM8250 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM8250 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SM8250 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

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6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy-chain components.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the following links to download *Daisy Chain Interconnect, MPSP1099, 12.4 × 14.0 mm,* (DS90-VV027-1 for LPDDR5) and *Daisy Chain Interconnect, MPSP1017, 12.7 × 12.4 mm,* (DS90-VV026-1 for LPDDR4X) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-VV027-1

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-VV026-1

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7 Part reliability

7.1 Reliability qualification summary

SM8250 reliability evaluation report for SM8250-LPDDR4X MPSP 1019 12.7 × 12.4 mm and SM8250-LPDDR5 1099 MPSP 14.0 × 12.4 mm device.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from multiple fab lots)	767	DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from multiple fab lots)	710	Pass FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from multiple fab lots)	710	> 20 [1]
ESD ─ Human body model (HBM) rating JS001 (Total samples from one fab lot)	24	1000 V
ESD ─ Charged device model (CDM) rating JS002 (Total samples from one fab lot)	6	250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 95°C (Total samples from one fab lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 95°C (Total samples from one fab lot)	6	Pass

1. The cumulative DPPM/FITs from multiple products manufactured at TSMC fab.

Table 7-2 SM8250-LPDDR5 1099 MPSP 14.0 × 12.4 mm package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Amkor Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning**: JESD22-A113-F MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500/ 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

Table 7-3 SM8250-LPDDR4X 1019 MPSP 12.7 × 12.4 mm package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Amkor Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning**: JESD22-A113-F MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots **Note**: * BHAST result is bridged from MPSP1099 package qualification data	231	231	Pass *
High-temperature storage life: JESD22-A103 Temperature 150°C, 500/ 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

7.2 Device characteristics

Table 7-4 Device characteristics

Device name	SM8250
Package type	1099 MPSP (for LPDDR5) 1017 MPSP (for LPDDR4X)
Package body size	12.4 mm × 14.0 mm × 0.56 mm (for LPDDR5) 12.4 mm × 12.7 mm × 0.56 mm (for LPDDR4X)
Lead count	1099 (for LPDDR5) 1017 (for LPDDR4X)
Lead composition	SAC125/Ni
Fab process	7 nm
Fab sites	TSMC
Assembly sites	■ Amkor, Korea ■ Amkor, Japan
Solder ball pitch	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	December 2018	Initial release
B	February 2019	■ Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins: Updated the VDD_LPI_MX description ■ Section 3.3 Power distribution network: Added this section for the PDN specifications ■ Section 4.3.2 Daisy chain devices: Added this section ■ Section 4.4 Device moisture sensitivity level: Added this section ■ Section 4.5 Thermal characteristics: Added this section ■ Chapter 5 Carrier, handling, and storage information: Added this chapter ■ Chapter 6 PCB mounting guidelines: Added this chapter ■ Section 7.2 Device characteristics: Added this section

Revision	Date	Description
C	April 2019	■ Global: Added WCD9385 in addition to WCD9380 throughput the document ■ Table 1-1 SM8250 features: Updated the fingerprint support ■ Table 2-2 Bottom pin descriptions – general pins: Updated the pad types ■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: □ Updated the configurable function and functional description for GPIO_77 □ Deleted the BOOT_CONFIG functions ■ Section 3.1 Absolute maximum ratings: Added this section ■ Section 3.2 Operating conditions: Added this section ■ Section 3.4 Average operating current: Added this section ■ Section 3.5 Dhrystone and rock bottom maximum power: Added this section ■ Section 3.6 Digital logic characteristics: Added this section ■ Section 3.7 Timing diagram conventions: Added this section ■ Section 3.8 Memory support: Added this section ■ Section 3.9 Multimedia: Added this section ■ Section 3.10 Connectivity: Added this section ■ Section 3.11 Internal functions: Added this section ■ Section 3.12 Power management interface: Added this section ■ Table 3-8 PDN specifications–SerDes rails (for LPDDR5 package): Added the details for VDD_PXVBIAS_SDC ■ Table 3-9 PDN specifications–SerDes rails (for LPDDR4X package): Added the details for VDD_PXVBIAS_SDC ■ Section 4.2 Part marking: Added this section ■ Section 4.3 Device ordering information: Added this section ■ Section 4.5 Thermal characteristics: Updated the document references for thermal models
D	July 2019	■ Cover page: Updated the high level block diagram ■ Table 1-1 SM8250 features: Updated the I3C IBI feature ■ Table 3-3 Operating conditions: Updated the device operating temperature ■ Table 4-4 Device identification details: Updated the device identification details for ES2 samples

Revision	Date	Description
E	September 2019	■ Cover page: Updated TSIF to SPI in the high level block diagram ■ Figure 1-1 SM8250 functional block diagram and example application: Updated TSIF to SPI and added connections ■ Table 1-1 SM8250 features: □ Removed TSIF from digital mobile broadcast feature □ Updated QFS2500 to QFS2580 □ Updated QFPROM feature ■ Table 2-2 Bottom pin descriptions – general pins: Updated the ZQ calibration pin descriptions for LPDDR4X ■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: Removed references to TSIF ■ Table 2-5 Top pin descriptions – general pins: Updated ZQ calibration pin descriptions for LPDDR4X ■ Table 3-1 Absolute maximum ratings: Updated the specification values ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Updated the specification values ■ Table 3-3 Operating conditions: Updated the specification values ■ Table 3-5 PDN specifications (for LPDDR4X package): Updated the ground pin for VDD_CX ■ Table 3-10 Dhrystone and rock bottom maximum power: Updated the table ■ Table 3-31 Sleep-clock timing parameters: Updated the typical value of sleep clock period and sleep clock frequency parameter ■ Section 3.9.1 Camera interfaces: Updated this section ■ Section 3.9.4 DMB support: Updated the SPI support ■ Section 3.10.7 SoundWire (SWR) interface: Added this section ■ Table 4-4 Device identification details: Updated the device identification details for ES3 and CS samples
F	October 2019	■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: □ Updated the operating conditions for VDD_GFX □ Added a note for Retention ■ Section 4.1 Device physical dimensions: Added a note for downloading the package coordinate file
G	November 12, 2019	■ Section 7.1 Reliability qualification summary: Added this section
H	November 26, 2019	■ Table 3-3 Operating conditions: Updated the typical voltage value for LPDDR4X ■ Table 4-4 Device identification details: Updated the CS date code
Revision I was omitted in accordance with QTI document conventions		
J	December 11, 2019	■ Global: □ Removed UFS card (UFS port 1) support □ Updated UFS 3.1 support ■ Table 4-4 Device identification details: Added date code for ES3 samples and updated the device identification details for CS samples
K	December 13, 2019	■ Table 1-1 SM8250 features: Updated the application processor capability and Adreno GPU Fmax value

Revision	Date	Description
L	February 2020	■ Table 1-1 *SM8250 features*: □ Added the Kryo Gold prime frequency for AB variant □ Added the GPU frequency for AB variant ■ Table 3-10 *Dhrystone and rock bottom maximum power*: Updated the power values for AB variant ■ Table 4-4 *Device identification details*: Updated the ES and CS device identification details for AB variants
M	March 9, 2020	Table 3-2 Operating conditions for voltage rails with AVS Type-1: Added Nominal_L1 specification for VDD_GFX
N	March 16, 2020	■ Figure 1-1 SM8250 functional block diagram and example application: Removed 38.4 MHz connection and PA sense connection ■ Table 2-4 Bottom pin descriptions – DNC, ground, and power-supply pins: Updated the voltage value of VDD2 pin ■ Section 4.1 Device physical dimensions: Updated the package outline drawing document number and download link
Revision O was omitted in accordance with QTI document conventions		
P	June 2020	■ Global: Replaced Qualcomm Always Aware with Qualcomm Sensing Hub across the document ■ Table 1-1 SM8250 features: Removed QFS2580 and replaced QFS2530 with QFS2630 ■ Section 3.6 Digital logic characteristics: Removed timing characteristics figure and discussion ■ Table 3-30 CXO timing parameters: Updated the reference document ■ Table 4-4 Device identification details: Added the date code for CS samples
Revision Q was omitted in accordance with QTI document conventions		
R	October 2020	■ Table 1-1 *SM8250 features*: Updated the Kryo Gold prime frequency and GPU for AC variant ■ Table 3-10 *Dhrystone and rock bottom maximum power*: Added the Dhrystone and rock bottom power of AC variant. Updated the Kryo Gold prime frequency for AC variant ■ Table 4-4 *Device identification details*: Updated the device identification details for AC variant

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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