Qualcomm Technologies, Inc.

Device description

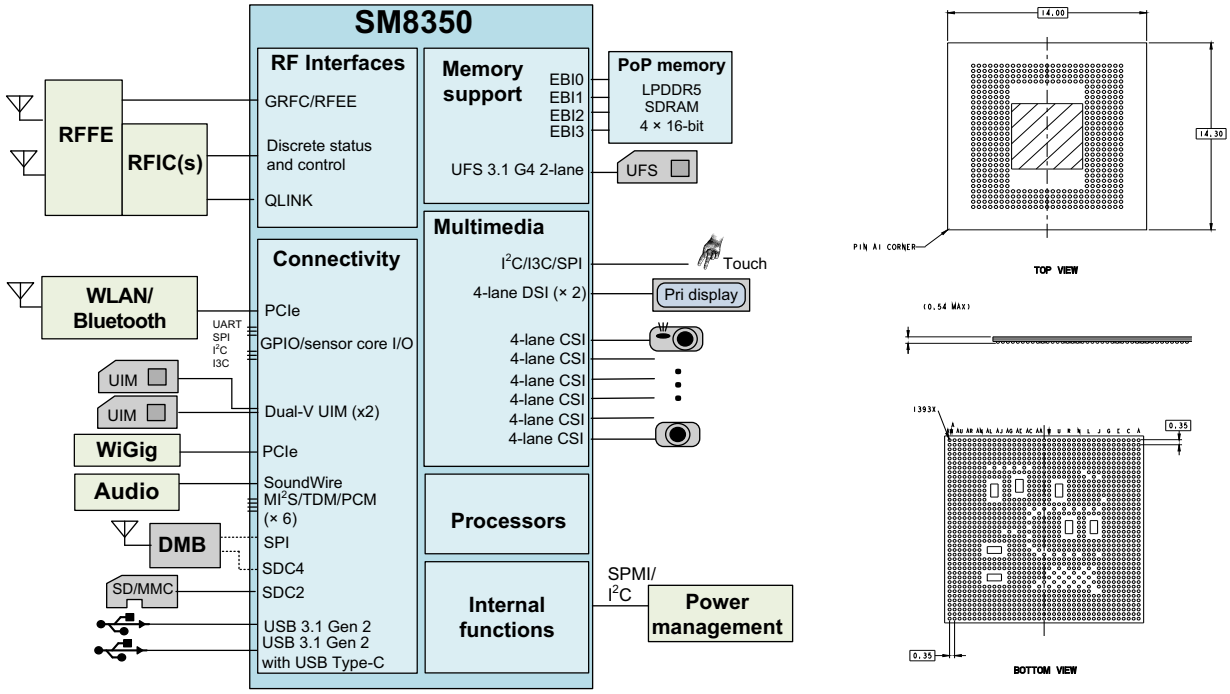
The SM8350 device is the new generation Qualcomm® Snapdragon™ premium-tier 5G SoC that has the integrated modem. It is designed with the 5 nm process, for superior performance and power efficiency. SM8350/SM8350P includes the following key components:

- Qualcomm® Kryo™ 680 CPU built on Arm v8 Cortex technology
- Qualcomm® Adreno™ 660 GPU for the highest in graphics performance and power efficiency
- Qualcomm Spectra™ 580 image processing engine for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 1095 DPU for on-device and external ultra HD display support
- 3G/4G/5G modem – mmWave and sub-6 GHz bands (Rel 15 integrated modem)

Key features (see Section 1.2 for details)

- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9380/WCD9385 audio codec for low-power voice processing and audiophile quality audio playback
- Qualcomm® Snapdragon Sensors Core Technology for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU250) for advanced secure use cases
- Compute Qualcomm® Hexagon™ DSP with Hexagon Vector eXtensions (HVX) and Hexagon Tensor Accelerator
- External 802.11ax, 2 × 2 MIMO, and Bluetooth Milan
- Quad-channel package-on-package (PoP) high-speed LPDDR5 SDRAM
- 14.3 × 14.0 mm MPSP1393 PoP

SM8350/SM8350P high-level block diagram and MPSP1393 outline drawing



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Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

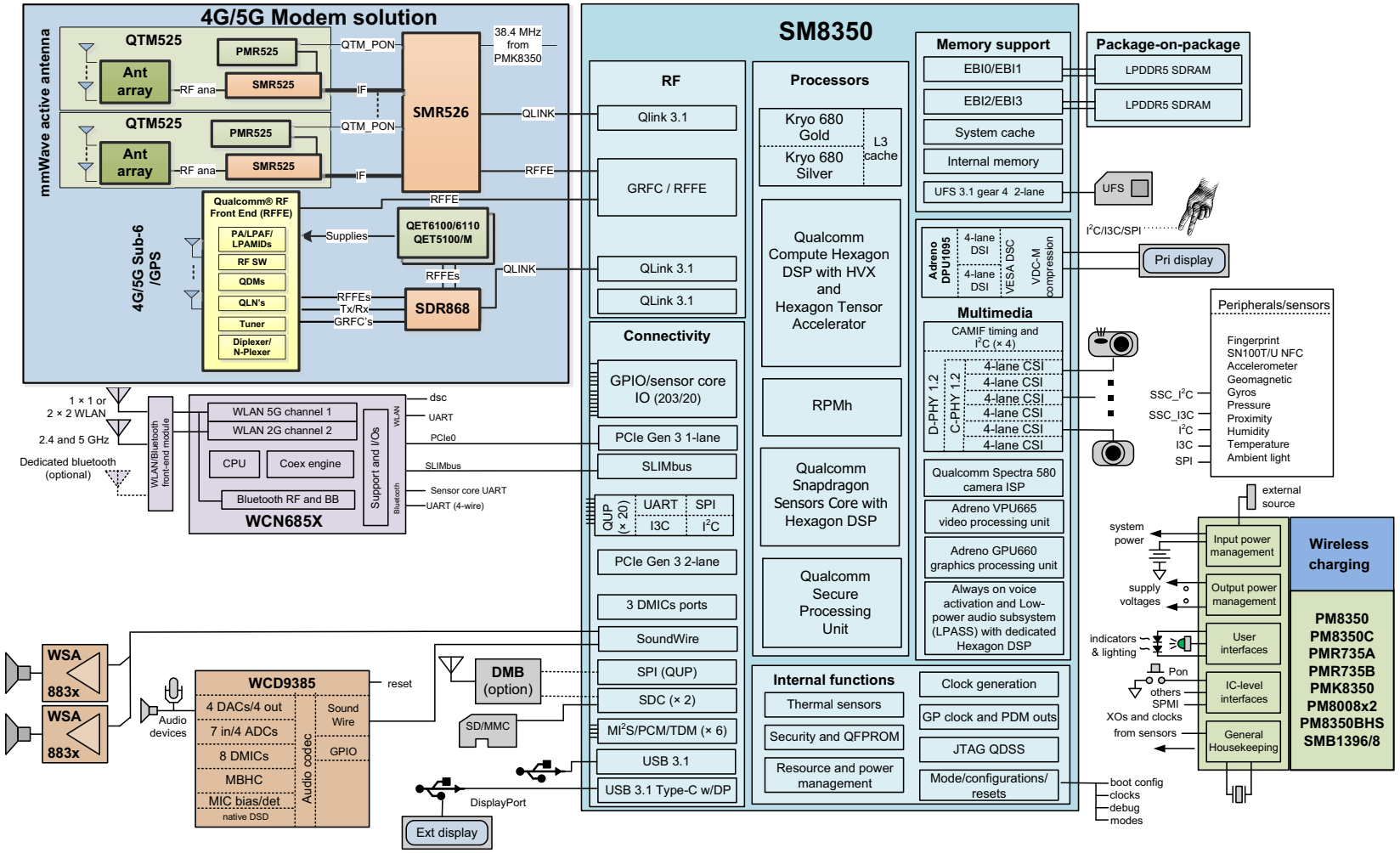

Figure 1-1 SM8350/SM8350P (SDR868) functional block diagram and example application

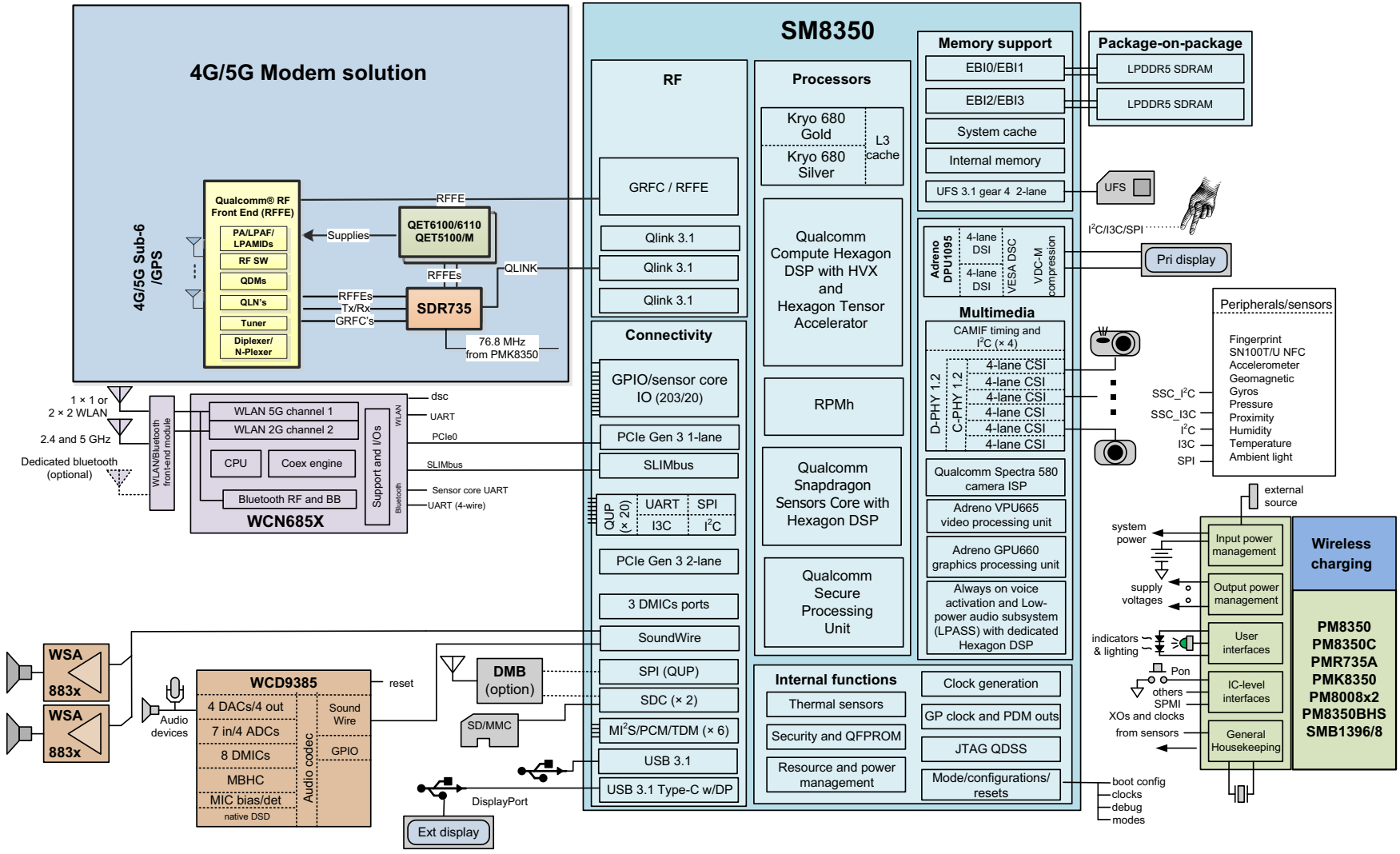

Figure 1-2 SM8350/SM8350P (SDR735) functional block diagram and example application

1.2 SM8350/SM8350P features

NOTE: Some of the hardware features integrated within the SM8350/SM8350P must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SM8350/SM8350P features.

Table 1-1 SM8350/SM8350P features

<table>
<tr><th>Feature</th><th>SM8350/SM8350P capability</th></tr>
<tr><td colspan="2">Processors</td></tr>
<tr><td>Applications</td><td>Kryo 680 CPU subsystem
■ Quad high-performance Kryo Gold cores
■ Quad low-power Kryo Silver cores

<table>
<tr><th>Cores (SM8350 AB variant)</th><th>Fmax</th><th>Cache per core</th></tr>
<tr><td>1 - Kryo Gold Prime</td><td>2.842 GHz</td><td>1 MB L2</td></tr>
<tr><td>3 - Kryo Gold</td><td>2.419 GHz</td><td>512 KB L2</td></tr>
<tr><td>4 - Kryo Silver</td><td>1.805 GHz</td><td>128 KB L2</td></tr>
</table>

<table>
<tr><th>Cores (SM8350 AC variant)</th><th>Fmax</th><th>Cache per core</th></tr>
<tr><td>1 - Kryo Gold Prime</td><td>2.995 GHz</td><td>1 MB L2</td></tr>
<tr><td>3 - Kryo Gold</td><td>2.419 GHz</td><td>512 KB L2</td></tr>
<tr><td>4 - Kryo Silver</td><td>1.805 GHz</td><td>128 KB L2</td></tr>
</table>
</td></tr>
</table>

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Table 1-1 SM8350/SM8350P features (cont.)

Feature	SM8350/SM8350P capability
Digital signal processing and artificial intelligence	Compute Hexagon DSP with quad HVX and Hexagon Coprocessor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator ■ Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on ■ The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. **SM8350 AB variant** / **SM8350 AC variant** INT8: 18 TOPS / 24 TOPS **Note**: TOPS – Trillion operations per second The audio Hexagon DSP is dedicated to the audio subsystem with support for always-on low-power use cases. A dedicated audio-Hexagon Tensor Accelerator offload engine improves performance and power consumption of always-on audio neural network use cases. The sensor Hexagon DSP in the Snapdragon Sensors Core Technology supports always-on, low-power use cases. All Hexagon DSP are cache-based processors with full access to DDR memory for large memory requirements. Hexagon Tensor Accelerator dedicated neural processing unit for performance and always-on neural network (NN) use cases. It incorporates an NN matrix engine to ensure efficient execution of various neural networks and their parameters. The Hexagon Tensor Accelerator may be used for typical imaging, video, audio, and data-based NN use cases and will typically be used in conjunction with the compute Hexagon DSP subsystem.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Snapdragon Sensors Core LPI	Hexagon v66 DSP – 860 MHz normal; 1.2 GHz turbo Two hardware threads L1 16I/16D Data acquisition engine (DAE) Sensor data conditioner (SDC) 1.5 MB island memory Eight dedicated buses (one I3C/I^{2}C, one I3C/I^{2}C, two SPI, two I^{2}C, two UART) 20 sensor IOs
Modem Location	3G/4G/5G – mmWave and sub-6 GHz bands (Rel 15) 5.5 Gbps DL, 2.5 Gbps UL, 800 MHz mmW, 200 MHz sub-6 Gen 9 VT v4
Memory support	
System memory via PoP and EBI	Four-channel PoP high-speed memory – LPDDR5 SDRAM (4 × 16-bit) designed for a 3200 MHz (LPDDR5) clock and 3 MB system cache

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Table 1-1 SM8350/SM8350P features (cont.)

Feature	SM8350/SM8350P capability
External memory	
Via UFS	UFS 3.1 gear 4, 1x 2-lane
Via SDC	SD v3.0 4 bit for SD card
Multimedia	
Display	DPU 1095: ■ Maximum resolution for internal panel: UHD + 60/QHD + 120 Hz 10-bit (phone) ■ External panel support: DisplayPort v1.4 with MST (2x 4K60 10-bit or 1x 8K30 with DSC) ■ Compression support: VDC-M for internal panel and DSC v1.2 ■ Processing: rounded corner, Demura engine and SPR ■ Power-saving: panel self-refresh using LLC
Camera support	Qualcomm Spectra 580: 64MP30/3x28MP30 ZSL, 4K120/720p960 Qualcomm Spectra 580 ISP supports connectivity to multiple cameras due to six included CPHY/DPHY interfaces. Furthermore, up to five cameras may operate concurrently due to the Qualcomm Spectra 580's 3 IFEs and 2 IFE-lites ■ Real-time sensor input resolution: 36 + 36 + 36 + 2 + 2 ■ ZSL: 64 MP at 30 fps, (64 + 25) at 30 fps, (28 + 28 + 28) at 30 fps, (36 + 16 + 12) at 30 fps ■ MFHDR hardware for snapshot, video, preview ■ Staggered HDR for snapshot, video, preview ■ 12 MP, 120 fps over one ISP (16 MP, 120 fps over two ISPs) ■ Slow-Mo 720p960 MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 + 4 + 4 configuration ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port ■ C-PHY v1.2: 10.26 Gbps/trio on three trios per port
Adreno video processing unit (VPU)	Adreno VPU 665 – fifth-generation UHD video processing unit Video decode up to 4K240/8K60 Video encode up to 4K120/8K30 Concurrent 4K60 decode and 4K60 encode for wireless display Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs Native encode support for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs
Adreno graphic processing unit (GPU)	Adreno GPU 660, Fmax at 840 MHz – 4K 60 fps UI or 2X 2K 60 fps UI OpenGL ES 3.2, Vulkan 1.2 OpenCL 2.0 full profile Adreno ML (Machine Learning)

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Table 1-1 SM8350/SM8350P features (cont.)

Feature	SM8350/SM8350P capability
Audio	LPI, improved voice UI concurrencies, ML HW accelerator; V66M, 16/16/1 MB L2/1 MB TCM 1.5 GHz, LPI
Codec	Integrated within the WCD9380/WCD9385 high fidelity audio codec
Speaker amplifier	Integrated within the WSA8830/WSA8835 class-H, low noise smart amplifier
Low-power audio subsystem (LPASS)	Essential voice communications package Advanced voice communications package Voice UI voice activation package Voice UI speech enhancement package 3D audio capture package
Audio interfaces	SLIMbus for WCN685x SoundWire interface (two Tx and two Rx data for codec Dedicated SoundWire interface for smart speaker amplifier Three DMIC ports support up to six DMICs Five MI^{2}S with 2x data lanes to support full duplex stereo, or up to four channel Tx/Rx application One MI^{2}S supports four data lanes for up to eight channels Tx/Rx application TDM/PCM: Up to 32 channels per individual interface
Connectivity	
Qualcomm universal peripheral (QUP) ports	20: Seven lanes each for four QUPs and four lanes each for the other QUPs; multiplexed serial interface functions
USB PCIe	Two USB 3.1 ports: gen2 10 Gbps (DP + data), support Type-C with DisplayPort v1.4 in one port 2 + 1-lane gen3
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MMC card and DMB
Touchscreen support	Capacitive panels via ext IC (I^{2}C, I3C, SPI, and interrupts)
Fingerprint support	Ultrasonic Qualcomm® Fingerprint Sensors for under glass, under metal, or under OLED display QFS2608 and QFS2630 modules
DMB support	Via external DMB device (SDC or SPI)
Configurable GPIOs	
Number of GPIO ports	203 – GPIO_0 to GPIO_202

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Table 1-1 SM8350/SM8350P features (cont.)

Feature	SM8350/SM8350P capability
Internal functions	
Security	
Crypto	AES-GCM, "HW ECC & RSA" (Elliptic-Curve Cryptography), ICE Crypto engine v5 (CE5), FIPS/CAVP certifiable
QFPROM	Fuse bits available for OEM use
Access Control	Programmable security domain protection and sand-boxing
Secure boot and tools	Secure Boot with Sec Tools 2.0; easy to use tool set
User data encryption	File based encryption (FBE)
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.3)
DRM	Widevine V16 L1, HDCP v2.3
QTEE services	ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
SPU	SPU250
Boot sequence	1) Applications PBL; 2) XBL; 3) SHRM; 4) AOP 5) HLOS; 6) rest of subsystems Emergency boot over USB 3.1
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD), embedded USB debug (EUD), and ETM
Chipset interface features	
Power management	2-line SPMI; plus other lines, as needed, via GPIOs, I^2C
Wireless connectivity	
WLAN	PCIe interface
Bluetooth	SLIMbus/UART interface
Fabrication technology and package	
Digital die	5 nm process
PoP – small, thermally efficient package	14.3 × 14.0 × 0.54 mm
WLAN/BT/FM	WCN685x
RF	SDR868/SDR735, SMR526/QTM525 (mmW)
PMIC	PM8350, PM8350B, PM8350C, PMK8350, PM8008x2, PMR735A, PMR735B
Codec	WSA883x, WCD938x

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2 Pin definitions

The SM8350 is the lower device within a PoP system, as shown and explained in Figure 2-1.

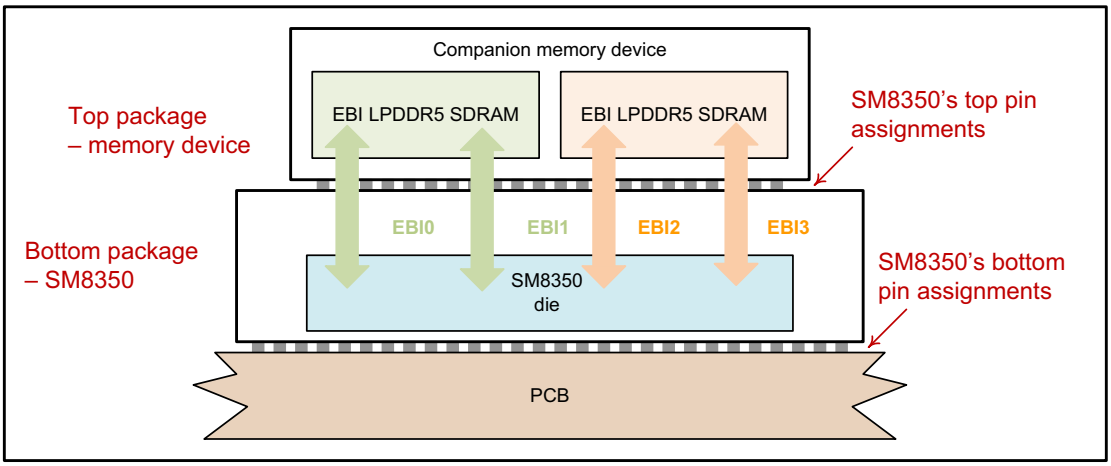

Figure 2-1 PoP system pin assignments

Two sets of pin assignment details are presented in this chapter:

- SM8350 bottom pins (Section 2.2)
- SM8350 top pins (Section 2.3)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
EBI1 pads	Pads for EBI1 are tailored for 1.2 V interfaces and are source terminated. See Chapter 3 for more details.
3.0 V (H) pads	Programmable drive strength, 2–8 mA, in 2 mA steps
Others [1]	Programmable drive strength, 2–16 mA, in 2 mA steps

1. Digital pads other than EBI1 pads or high-voltage tolerant pads.

2.2 Pin assignments: bottom

2.2.1 Pin map: bottom

The SM8350 is available in the MPSP1393 package. Its bottom surface is equivalent to an MPSP1393 that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details and Section 2.3 for information about the top pin assignments.

A high-level view of the bottom pin assignments is shown in Figure 2-2.

The text within Figure 2-2 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inch × 17 inch sheet.
- View the graphic's PDF soft copy and zoom in — the resolution is sufficient for comfortable reading.
- Download the *SM8350 Pin Assignment and GPIO Configuration Spreadsheet* (80-PN145-1A). This Microsoft Excel spreadsheet lists all SM8350/SM8350P pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the *SM8350 Pin Assignment and GPIO Configuration Spreadsheet* (80-PN145-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PN145-1A

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

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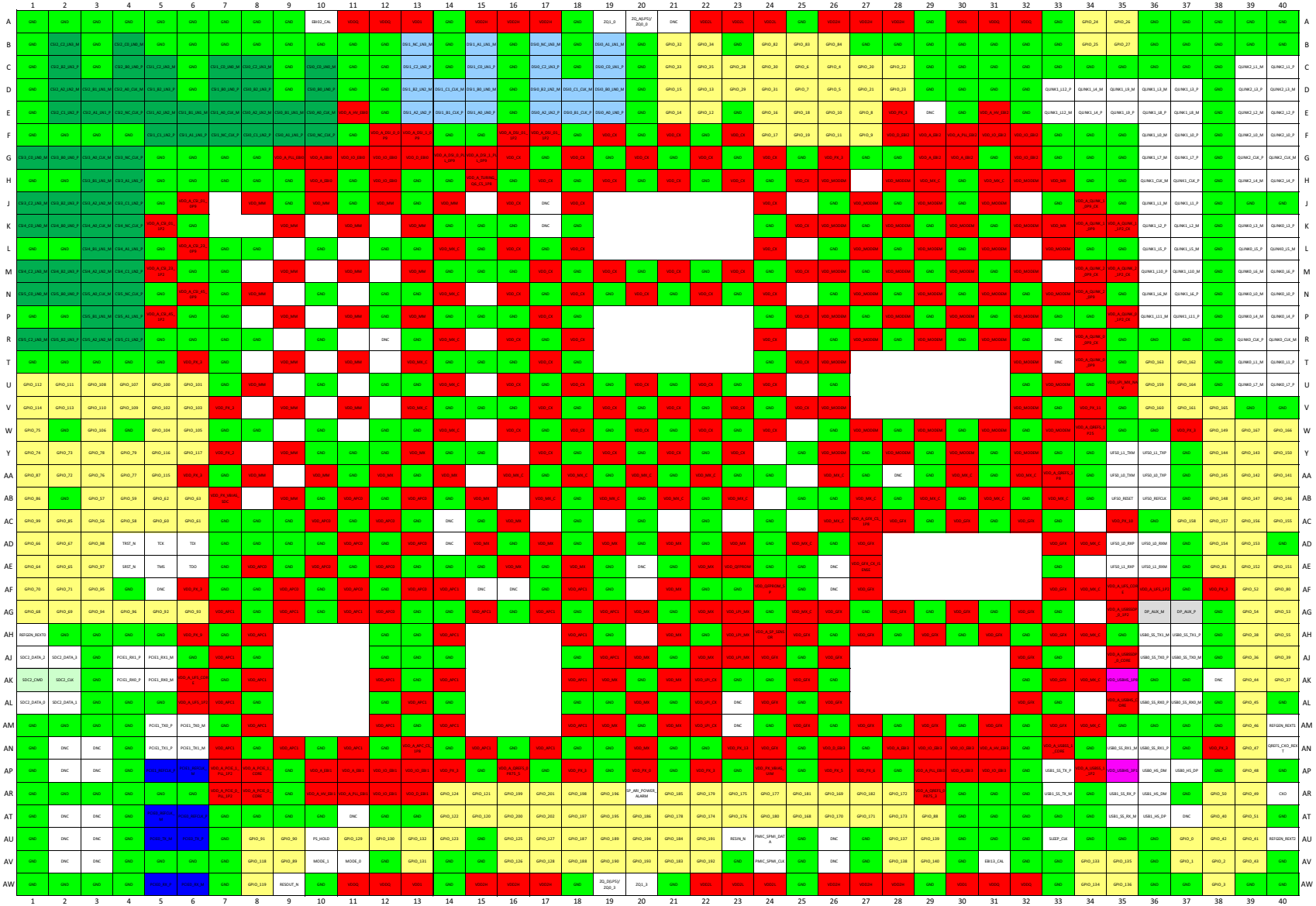

Figure 2-2 SM8350 bottom pin assignments

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2.2.2 Pin descriptions: bottom

The bottom pins are described in Table 2-2 through Table 2-6.

Table 2-2 Bottom pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
E10	CSI0_A0_CLK_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – negative MIPI CSI 0 (CPHY), trio lane 0 – A
F9	CSI0_A1_LN1_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – positive MIPI CSI 0 (CPHY), trio lane 1 – A
E8	CSI0_A2_LN2_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – negative MIPI CSI 0 (CPHY), trio lane 2 – A
D10	CSI0_B0_LN0_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – positive MIPI CSI 0 (CPHY), trio lane 0 – B
E9	CSI0_B1_LN1_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – negative MIPI CSI 0 (CPHY), trio lane 1 – B
D8	CSI0_B2_LN3_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – positive MIPI CSI 0 (CPHY), trio lane 2 – B
C10	CSI0_C0_LN0_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – negative MIPI CSI 0 (CPHY), trio lane 0 – C
F8	CSI0_C1_LN2_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – positive MIPI CSI 0 (CPHY), trio lane 1 – C
C8	CSI0_C2_LN3_M	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – negative MIPI CSI 0 (CPHY), trio lane 2 – C
F10	CSI0_NC_CLK_P	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – positive MIPI CSI 0 (CPHY), no connect
E7	CSI1_A0_CLK_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – negative MIPI CSI 1 (CPHY), trio lane 0 – A
F6	CSI1_A1_LN1_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – positive MIPI CSI 1 (CPHY), trio lane 1 – A
E5	CSI1_A2_LN2_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – negative MIPI CSI 1 (CPHY), trio lane 2 – A
D7	CSI1_B0_LN0_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – positive MIPI CSI 1 (CPHY), trio lane 0 – B
E6	CSI1_B1_LN1_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – negative MIPI CSI 1 (CPHY), trio lane 1 – B
D5	CSI1_B2_LN3_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – positive MIPI CSI 1 (CPHY), trio lane 2 – B
C7	CSI1_C0_LN0_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – negative MIPI CSI 1 (CPHY), trio lane 0 – C
F5	CSI1_C1_LN2_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – positive MIPI CSI 1 (CPHY), trio lane 1 – C
C5	CSI1_C2_LN3_M	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – negative MIPI CSI 1 (CPHY), trio lane 2 – C
F7	CSI1_NC_CLK_P	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – positive MIPI CSI 1 (CPHY), no connect

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
D4	CSI2_A0_CLK_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – negative MIPI CSI 2 (CPHY), trio lane 0 – A
E3	CSI2_A1_LN1_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – positive MIPI CSI 2 (CPHY), trio lane 1 – A
D2	CSI2_A2_LN2_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – negative MIPI CSI 2 (CPHY), trio lane 2 – A
C4	CSI2_B0_LN0_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – positive MIPI CSI 2 (CPHY), trio lane 0 – B
D3	CSI2_B1_LN1_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – negative MIPI CSI 2 (CPHY), trio lane 1 – B
C2	CSI2_B2_LN3_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – positive MIPI CSI 2 (CPHY), trio lane 2 – B
B4	CSI2_C0_LN0_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – negative MIPI CSI 2 (CPHY), trio lane 0 – C
E2	CSI2_C1_LN2_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – positive MIPI CSI 2 (CPHY), trio lane 1 – C
B2	CSI2_C2_LN3_M	CSI	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – negative MIPI CSI 2 (CPHY), trio lane 2 – C
E4	CSI2_NC_CLK_P	CSI	AI, AO	MIPI CSI 2 (DPHY), differential clock – positive MIPI CSI 2 (CPHY), no connect
G3	CSI3_A0_CLK_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – negative MIPI CSI 3 (CPHY), trio lane 0 – A
H4	CSI3_A1_LN1_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – positive MIPI CSI 3 (CPHY), trio lane 1 – A
J3	CSI3_A2_LN2_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – negative MIPI CSI 3 (CPHY), trio lane 2 – A
G2	CSI3_B0_LN0_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – positive MIPI CSI 3 (CPHY), trio lane 0 – B
H3	CSI3_B1_LN1_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – negative MIPI CSI 3 (CPHY), trio lane 1 – B
J2	CSI3_B2_LN3_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – positive MIPI CSI 3 (CPHY), trio lane 2 – B
G1	CSI3_C0_LN0_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – negative MIPI CSI 3 (CPHY), trio lane 0 – C
J4	CSI3_C1_LN2_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – positive MIPI CSI 3 (CPHY), trio lane 1 – C
J1	CSI3_C2_LN3_M	CSI	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – negative MIPI CSI 3 (CPHY), trio lane 2 – C
G4	CSI3_NC_CLK_P	CSI	AI, AO	MIPI CSI 3 (DPHY), differential clock – positive MIPI CSI 3 (CPHY), no connect
K3	CSI4_A0_CLK_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential clock – negative MIPI CSI 4 (CPHY), trio lane 0 – A
L4	CSI4_A1_LN1_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – positive MIPI CSI 4 (CPHY), trio lane 1 – A

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M3	CSI4_A2_LN2_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – negative MIPI CSI 4 (CPHY), trio lane 2 – A
K2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – positive MIPI CSI 4 (CPHY), trio lane 0 – B
L3	CSI4_B1_LN1_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – negative MIPI CSI 4 (CPHY), trio lane 1 – B
M2	CSI4_B2_LN3_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – positive MIPI CSI 4 (CPHY), trio lane 2 – B
K1	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – negative MIPI CSI 4 (CPHY), trio lane 0 – C
M4	CSI4_C1_LN2_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – positive MIPI CSI 4 (CPHY), trio lane 1 – C
M1	CSI4_C2_LN3_M	CSI	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – negative MIPI CSI 4 (CPHY), trio lane 2 – C
K4	CSI4_NC_CLK_P	CSI	AI, AO	MIPI CSI 4 (DPHY), differential clock – positive MIPI CSI 4 (CPHY), no connect
N3	CSI5_A0_CLK_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential clock – negative MIPI CSI 5 (CPHY), trio lane 0 – A
P4	CSI5_A1_LN1_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – positive MIPI CSI 5 (CPHY), trio lane 1 – A
R3	CSI5_A2_LN2_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – negative MIPI CSI 5 (CPHY), trio lane 2 – A
N2	CSI5_B0_LN0_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – positive MIPI CSI 5 (CPHY), trio lane 0 – B
P3	CSI5_B1_LN1_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – negative MIPI CSI 5 (CPHY), trio lane 1 – B
R2	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – positive MIPI CSI 5 (CPHY), trio lane 2 – B
N1	CSI5_C0_LN0_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – negative MIPI CSI 5 (CPHY), trio lane 0 – C
R4	CSI5_C1_LN2_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – positive MIPI CSI 5 (CPHY), trio lane 1 – C
R1	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – negative MIPI CSI 5 (CPHY), trio lane 2 – C
N4	CSI5_NC_CLK_P	CSI	AI, AO	MIPI CSI 5 (DPHY), differential clock – positive MIPI CSI 5 (CPHY), no connect
AR40	CXO	PX11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
AG36	DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – minus
AG37	DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – plus
E19	DSI0_A0_LN0_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – positive MIPI DSI 0 (CPHY), trio lane 0 – A
B19	DSI0_A1_LN1_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – negative MIPI DSI 0 (CPHY), trio lane 1 – A

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
E17	DSI0_A2_LN2_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – positive MIPI DSI 0 (CPHY), trio lane 2 – A
D19	DSI0_B0_LN0_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – negative MIPI DSI 0 (CPHY), trio lane 0 – B
E18	DSI0_B1_CLK_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – positive MIPI DSI 0 (CPHY), trio lane 1 – B
D17	DSI0_B2_LN2_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – negative MIPI DSI 0 (CPHY), trio lane 2 – B
C19	DSI0_C0_LN1_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – positive MIPI DSI 0 (CPHY), trio lane 0 – C
D18	DSI0_C1_CLK_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential clock – negative MIPI DSI 0 (CPHY), trio lane 1 – C
C17	DSI0_C2_LN3_P	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – positive MIPI DSI 0 (CPHY), trio lane 2 – C
B17	DSI0_NC_LN3_M	DSI	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – negative MIPI DSI 0 (CPHY), no connect
E15	DSI1_A0_LN0_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – positive MIPI DSI 1 (CPHY), trio lane 0 – A
B15	DSI1_A1_LN1_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – negative MIPI DSI 1 (CPHY), trio lane 1 – A
E13	DSI1_A2_LN2_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – positive MIPI DSI 1 (CPHY), trio lane 2 – A
D15	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – negative MIPI DSI 1 (CPHY), trio lane 0 – B
E14	DSI1_B1_CLK_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – positive MIPI DSI 1 (CPHY), trio lane 1 – B
D13	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – negative MIPI DSI 1 (CPHY), trio lane 2 – B
C15	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – positive MIPI DSI 1 (CPHY), trio lane 0 – C
D14	DSI1_C1_CLK_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – negative MIPI DSI 1 (CPHY), trio lane 1 – C
C13	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – positive MIPI DSI 1 (CPHY), trio lane 2 – C
B13	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – negative MIPI DSI 1 (CPHY), no connect
A10	EBI02_CAL	EBI	DO	EBI0/2 LPDDR5 calibration resistor
AV31	EBI13_CAL	EBI	DO	EBI1/3 LPDDR5 calibration resistor
AV11	MODE_0	PX_3	DI-PD:nppukp	Mode control bit 0 – unconnected for native mode
AV10	MODE_1	PX_3	DI-PD:nppukp	Mode control bit 1 – unconnected for native mode
AT5	PCIE0_REFCLK_M	–	AI, AO	PCIe 0 Gen 3 reference clock – minus
AT6	PCIE0_REFCLK_P	–	AI, AO	PCIe 0 Gen 3 reference clock – plus
AW6	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – minus

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
AW5	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – plus
AU5	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – minus
AU6	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – plus
AP6	PCIE1_REFCLK_M	–	AI, AO	PCIe 1 Gen 3 reference clock – minus
AP5	PCIE1_REFCLK_P	–	AI, AO	PCIe 1 Gen 3 reference clock – plus
AK5	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive 0 – minus
AK4	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive 0 – plus
AJ5	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive 1 – minus
AJ4	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive 1 – plus
AM6	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit 0 – minus
AM5	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit 0 – plus
AN6	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit 1 – minus
AN5	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit 1 – plus
AV24	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
AU24	PMIC_SPMI_DATA	PX_0	BH-PD:nppukp	Slave and PBUS interface for PMICs – data
AU10	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
R40	QLINK0_CLK_M	–	AI, AO	QLink0 clock – negative
R39	QLINK0_CLK_P	–	AI, AO	QLink0 clock – positive
P39	QLINK0_L4_M	–	AI, AO	QLink0 lane 4 – negative
P40	QLINK0_L4_P	–	AI, AO	QLink0 lane 4 – positive
L40	QLINK0_L5_M	–	AI, AO	QLink0 lane 5 – negative
L39	QLINK0_L5_P	–	AI, AO	QLink0 lane 5 – positive
T39	QLINK0_L1_M	–	AI, AO	QLink0 lane 1 – negative
T40	QLINK0_L1_P	–	AI, AO	QLink0 lane 1 – positive
U39	QLINK0_L7_M	–	AI, AO	QLink0 lane 7 – negative
U40	QLINK0_L7_P	–	AI, AO	QLink0 lane 7 – positive
M39	QLINK0_L6_M	–	AI, AO	QLink0 lane 6 – negative
M40	QLINK0_L6_P	–	AI, AO	QLink0 lane 6 – positive
N39	QLINK0_L0_M	–	AI, AO	QLink0 lane 0 – negative
N40	QLINK0_L0_P	–	AI, AO	QLink0 lane 0 – positive
K39	QLINK0_L3_M	–	AI, AO	QLink0 lane 3 – negative
K40	QLINK0_L3_P	–	AI, AO	QLink0 lane 3 – positive
H36	QLINK1_CLK_M	–	AI, AO	QLink1 clock – negative
H37	QLINK1_CLK_P	–	AI, AO	QLink1 clock – positive
G36	QLINK1_L7_M	–	AI, AO	QLink1 lane 7 – negative
G37	QLINK1_L7_P	–	AI, AO	QLink1 lane 7 – positive
E37	QLINK1_L8_M	–	AI, AO	QLink1 lane 8 – negative
E36	QLINK1_L8_P	–	AI, AO	QLink1 lane 8 – positive

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
D35	QLINK1_L9_M	–	AI, AO	QLink1 lane 9 – negative
E35	QLINK1_L9_P	–	AI, AO	QLink1 lane 9 – positive
M37	QLINK1_L10_M	–	AI, AO	QLink1 lane 10 – negative
M36	QLINK1_L10_P	–	AI, AO	QLink1 lane 10 – positive
P36	QLINK1_L11_M	–	AI, AO	QLink1 lane 11 – negative
P37	QLINK1_L11_P	–	AI, AO	QLink1 lane 11 – positive
E33	QLINK1_L12_M	–	AI, AO	QLink1 lane 12 – negative
D33	QLINK1_L12_P	–	AI, AO	QLink1 lane 12 – positive
J36	QLINK1_L1_M	–	AI, AO	QLink1 lane 1 – negative
J37	QLINK1_L1_P	–	AI, AO	QLink1 lane 1 – positive
K37	QLINK1_L2_M	–	AI, AO	QLink1 lane 2 – negative
K36	QLINK1_L2_P	–	AI, AO	QLink1 lane 2 – positive
F36	QLINK1_L0_M	–	AI, AO	QLink1 lane 0 – negative
F37	QLINK1_L0_P	–	AI, AO	QLink1 lane 0 – positive
D36	QLINK1_L3_M	–	AI, AO	QLink1 lane 3 – negative
D37	QLINK1_L3_P	–	AI, AO	QLink1 lane 3 – positive
D34	QLINK1_L4_M	–	AI, AO	QLink1 lane 4 – negative
E34	QLINK1_L4_P	–	AI, AO	QLink1 lane 4 – positive
L37	QLINK1_L5_M	–	AI, AO	QLink1 lane 5 – negative
L36	QLINK1_L5_P	–	AI, AO	QLink1 lane 5 – positive
N36	QLINK1_L6_M	–	AI, AO	QLink1 lane 6 – negative
N37	QLINK1_L6_P	–	AI, AO	QLink1 lane 6 – positive
G40	QLINK2_CLK_M	–	AI, AO	QLink2 clock – negative
G39	QLINK2_CLK_P	–	AI, AO	QLink2 clock – positive
E39	QLINK2_L2_M	–	AI, AO	QLink2 lane 2 – negative
E40	QLINK2_L2_P	–	AI, AO	QLink2 lane 2 – positive
D40	QLINK2_L3_M	–	AI, AO	QLink2 lane 3 – negative
D39	QLINK2_L3_P	–	AI, AO	QLink2 lane 3 – positive
H39	QLINK2_L4_M	–	AI, AO	QLink2 lane 4 – negative
H40	QLINK2_L4_P	–	AI, AO	QLink2 lane 4 – positive
F39	QLINK2_L0_M	–	AI, AO	QLink2 lane 0 – negative
F40	QLINK2_L0_P	–	AI, AO	QLink2 lane 0 – positive
C39	QLINK2_L1_M	–	AI, AO	QLink2 lane 1 – negative
C40	QLINK2_L1_P	–	AI, AO	QLink2 lane 1 – positive
AN40	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-die clocking
AH1	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
AM40	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
AU40	REFGEN_REXT2	PX_3	AI, AO	West-side high-speed interface – external resistor

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
AU23	RESIN_N	PX_0	DI	Reset input
AW9	RESOUT_N	PX_3	DO	Reset output
AK2	SDC2_CLK	PX_2	BH-NP:pdpukp	Secure digital controller 2 clock
AK1	SDC2_CMD	PX_2	BH-PD:nppukp	Secure digital controller 2 command
AL1	SDC2_DATA_0	PX_2	BH-PD:nppukp	Secure digital controller 0 data
AL2	SDC2_DATA_1	PX_2	BH-PD:nppukp	Secure digital controller 1 data
AJ1	SDC2_DATA_2	PX_2	BH-PD:nppukp	Secure digital controller 2 data
AJ2	SDC2_DATA_3	PX_2	BH-PD:nppukp	Secure digital controller 3 data
AU33	SLEEP_CLK	PX_3	DI	Sleep clock
AR20	SP_ARI_POWER_ALARM	PX_13	DI	Power alarm
AE4	SRST_N	PX_3	DI-PU	JTAG reset for debug
AD5	TCK	PX_3	DI-PU	JTAG clock input
AD6	TDI	PX_3	DI-PU:nppdkp	JTAG data input
AE6	TDO	PX_3	DO-Z	JTAG data output
AE5	TMS	PX_3	DI-PU:nppdkp	JTAG mode select input
AD4	TRST_N	PX_3	DI-PD:nppukp	JTAG reset
AD36	UFS0_L0_RXM	–	AI	UFS0 lane 0 receiver – minus
AD35	UFS0_L0_RXP	–	AI	UFS0 lane 0 receiver – plus
AA35	UFS0_L0_TXM	–	AO	UFS0 lane 0 transmit – minus
AA36	UFS0_L0_TXP	–	AO	UFS0 lane 0 transmit – plus
AE36	UFS0_L1_RXM	–	AI	UFS0 lane 1 receiver – minus
AE35	UFS0_L1_RXP	–	AI	UFS0 lane 1 receiver – plus
Y35	UFS0_L1_TXM	–	AO	UFS0 lane 1 transmit – minus
Y36	UFS0_L1_TXP	–	AO	UFS0 lane 1 transmit – plus
AB36	UFS0_REFCLK	PX_10	DO-Z:PD:nppukp	UFS 0 reference clock
AB35	UFS0_RESET	PX_10	DO-Z:PD:nppukp	UFS reset
AP36	USB0_HS_DM	–	AI, AO	USB 2.0 high-speed data – minus
AP37	USB0_HS_DP	–	AI, AO	USB 2.0 high-speed data – plus
AL37	USB0_SS_RX0_M	–	AI	USB 3.0 Type C PHY receiver 0 – minus
AL36	USB0_SS_RX0_P	–	AI	USB 3.0 Type C PHY receiver 0 – plus
AN35	USB0_SS_RX1_M	–	AI	USB 3.0 Type C PHY receiver 1 – minus
AN36	USB0_SS_RX1_P	–	AI	USB 3.0 Type C PHY receiver 1 – plus
AJ37	USB0_SS_TX0_M	–	AO	USB 3.0 Type C PHY transmit 0 – minus
AJ36	USB0_SS_TX0_P	–	AO	USB 3.0 Type C PHY transmit 0 – plus
AH36	USB0_SS_TX1_M	–	AO	USB 3.0 Type C PHY transmit 1 – minus
AH37	USB0_SS_TX1_P	–	AO	USB 3.0 Type C PHY transmit 1 – plus
AR36	USB1_HS_DM	–	AI, AO	USB 2.0 high-speed data – minus
AT36	USB1_HS_DP	–	AI, AO	USB 2.0 high-speed data – plus

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Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
AT35	USB1_SS_RX_M	–	AI	USB 3.0 Type C PHY receiver – minus
AR35	USB1_SS_RX_P	–	AI	USB 3.0 Type C PHY receiver – plus
AR33	USB1_SS_TX_M	–	AO	USB 3.0 Type C PHY receiver – minus
AP33	USB1_SS_TX_P	–	AO	USB 3.0 Type C PHY receiver – plus
A20	ZQ_A(LP5)/ZQ0_0	–	AI	LPDDR5 ZQ calibration for channels A and C
AW19	ZQ_D(LP5)/ZQ0_3	–	AI	LPDDR5 ZQ calibration for channels B and D
A19	ZQ1_0	–	AI	Unused. Can be left floating.
AW20	ZQ1_3	–	AI	Unused. Can be left floating.

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that includes a worksheet for all SM8350/SM8350P GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the *SM8350 Pin Assignment and GPIO Configuration Spreadsheet* (80-PN145-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PN145-1A

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Table 2-3 Bottom pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AU37	GPIO_0	QUP_L0[13]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AV37	GPIO_1	QUP_L1[13]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AV38	GPIO_2	QUP_L3[13] QUP_L4_12_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AW38	GPIO_3	QUP_L2[13] QUP_L5_12_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
C26	GPIO_4	QUP_L0[0]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
D26	GPIO_5	QUP_L1[0]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
C25	GPIO_6	QUP_L2[0] QUP_L4_6_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
D25	GPIO_7	QUP_L3[0] QUP_L5_6_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
E27	GPIO_8	QUP_L0[1]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
F27	GPIO_9	QUP_L1[1]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N

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Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
E26	GPIO_10	QUP_L2[1] QUP_L6_6_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
F26	GPIO_11	QUP_L3[1]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
E22	GPIO_12	QUP_L0[2]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
D22	GPIO_13	QUP_L1[2]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
E21	GPIO_14	QUP_L2[2] QDSS_CTI_TRIG0_OUT_MIRB	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QDSS trigger output 0 B	Y
D21	GPIO_15	QUP_L3[2] MDP_VSYNC_P_MIRB BOOT_CONFIG[11]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 MDP vertical sync – primary B Boot configuration bit	Y
E24	GPIO_16	QUP_L0[3]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
F24	GPIO_17	QUP_L1[3]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
E25	GPIO_18	QUP_L2[3]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
F25	GPIO_19	QUP_L3[3]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
C27	GPIO_20	QUP_L0[4] GP_PDM_MIRB[2]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 General-purpose PDM output	N
D27	GPIO_21	QUP_L1[4] GP_PDM_MIRB[1]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 General-purpose PDM output	N

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
C28	GPIO_22	QUP_L2[4] GP_PDM_MIRB[0]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 General-purpose PDM output	N
D28	GPIO_23	QUP_L3[4]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
A34	GPIO_24	QUP_L0[5]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
B34	GPIO_25	QUP_L1[5]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
A35	GPIO_26	QUP_L2[5] MDP_VSYNC_S_MIRB	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 MDP vertical sync – secondary	Y
B35	GPIO_27	QUP_L3[5] QDSS_CTI_TRIG1_OUT_MIRB	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QDSS trigger output 1 B	Y
C23	GPIO_28	QUP_L0[6]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
D23	GPIO_29	QUP_L1[6]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
C24	GPIO_30	QUP_L2[6]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
D24	GPIO_31	QUP_L3[6]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
B21	GPIO_32	QUP_L0[7]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
C21	GPIO_33	QUP_L1[7]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
B22	GPIO_34	QUP_L2[7]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
C22	GPIO_35	QUP_L3[7] BOOT_CONFIG[8]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Boot configuration bit	Y
AJ39	GPIO_36	QUP_L0[8] IBI_I3C_QUP8_SDA	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP8 in-band interrupt I^3C SDA	Y
AK40	GPIO_37	QUP_L1[8] IBI_I3C_QUP8_SCL	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP8 in-band interrupt I^3C SCL	N
AH39	GPIO_38	QUP_L2[8]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AJ40	GPIO_39	QUP_L3[8] USB2PHY_AC_EN2	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 USB AC coupling control	Y
AT38	GPIO_40	QUP_L0[9]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AU39	GPIO_41	QUP_L1[9]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AU38	GPIO_42	QUP_L2[9] QUP_L6_12_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AV39	GPIO_43	QUP_L3[9] FORCED_USB_BOOT	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Forced USB boot (2)	Y

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AK39	GPIO_44	QUP_L0[10] QSPI_DATA[0] SDC4_DATA[0]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI data Secure digital controller data	Y
AL39	GPIO_45	QUP_L1[10] QSPI_DATA[1] SDC4_DATA[1]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI data Secure digital controller data	N
AM39	GPIO_46	QUP_L2[10]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AN39	GPIO_47	QUP_L3[10] QSPI_CS_N_0 BOOT_CONFIG[9]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI chip select Boot configuration bit	Y
AP39	GPIO_48	QUP_L0[11] QSPI_DATA[2] SDC4_DATA[2]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI data Secure digital controller data	N
AR39	GPIO_49	QUP_L1[11] QSPI_DATA[3] SDC4_DATA[3]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI data Secure digital controller data	N
AR38	GPIO_50	QUP_L2[11] QSPI_CLK SDC4_CLK	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI clock Secure digital controller clock	Y
AT39	GPIO_51	QUP_L3[11] QSPI_CS_N_1 SDC4_CMD	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 Quad SPI chip select Secure digital controller command	Y
AF39	GPIO_52	QUP_L0[12]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N

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Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AG40	GPIO_53	QUP_L1[12] GP_MN	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 General-purpose M/N:D counter output	N
AG39	GPIO_54	QUP_L2[12]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AH40	GPIO_55	QUP_L3[12]	PX_3	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AC3	GPIO_56	QUP_L0[14] IBI_I3C_QUP14_SDA	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP in-band interrupt I^3C SDA	Y
AB3	GPIO_57	QUP_L1[14] IBI_I3C_QUP14_SCL	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP in-band interrupt I^3C SCL	N
AC4	GPIO_58	QUP_L2[14] QUP_L4_18_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AB4	GPIO_59	QUP_L3[14] QUP_L5_18_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AC5	GPIO_60	QUP_L0[15] IBI_I3C_QUP15_SDA	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP in-band interrupt I3C SDA	Y
AC6	GPIO_61	QUP_L1[15] IBI_I3C_QUP15_SCL	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 QUP in-band interrupt I3C SCL	N
AB5	GPIO_62	QUP_L2[15] QUP_L6_18_CS	PX_3	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AB6	GPIO_63	QUP_L3[15] QUP_L4_19_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AE1	GPIO_64	QUP_L0[16]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AE2	GPIO_65	QUP_L1[16]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AD1	GPIO_66	QUP_L2[16] QUP_L5_19_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AD2	GPIO_67	QUP_L3[16] QUP_L6_19_CS	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5 For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AG1	GPIO_68	QUP_L0[18]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AG2	GPIO_69	QUP_L1[18]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AF1	GPIO_70	QUP_L2[18]	PX_3	PU:nppdkp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AF2	GPIO_71	QUP_L3[18]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AA2	GPIO_72	QUP_L0[17]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
Y2	GPIO_73	QUP_L1[17]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
Y1	GPIO_74	QUP_L2[17]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
W1	GPIO_75	QUP_L3[17]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AA3	GPIO_76	QUP_L0[19]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
AA4	GPIO_77	QUP_L1[19]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
Y3	GPIO_78	QUP_L2[19]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	N
Y4	GPIO_79	QUP_L3[19]	PX_3	PD:nppukp	Configurable I/O For QUP assignment/mapping information, see Table 2-4 and Table 2-5	Y
AF40	GPIO_80		PX_3	PD:nppukp	Configurable I/O	Y
AE38	GPIO_81	USB_PHY_PS	PX_3	PD:nppukp	Configurable I/O USB PHY port select	Y
B24	GPIO_82	MDP_VSYNC_P_MIRA	PX_3	PD:nppukp	Configurable I/O MDP vertical sync – primary	Y
B25	GPIO_83	MDP_VSYNC_S_MIRA	PX_3	PD:nppukp	Configurable I/O MDP vertical sync – secondary	Y
B26	GPIO_84	MDP_VSYNC_E	PX_3	PD:nppukp	Configurable I/O MDP vertical sync – external	Y
AC2	GPIO_85		PX_3	PD:nppukp	Configurable I/O	Y
AB1	GPIO_86		PX_3	PD:nppukp	Configurable I/O	Y
AA1	GPIO_87	DP_HOT_PLUG_DETECT QDSS_CTI_TRIG0_IN_MIRB	PX_3	PD:nppukp	Configurable I/O DisplayPort hot plug detect QDSS trigger input 0 B	Y
AT29	GPIO_88	QDSS_CTI_TRIG0_OUT_MIRA	PX_3	PD:nppukp	Configurable I/O QDSS trigger output 0 A	Y
AV9	GPIO_89	QDSS_CTI_TRIG1_OUT_MIRA	PX_3	PD:nppukp	Configurable I/O QDSS trigger output 1 A	Y
AU9	GPIO_90	QDSS_CTI_TRIG1_IN_MIRA	PX_3	PD:nppukp	Configurable I/O QDSS trigger input 1 A	Y
AU8	GPIO_91	QDSS_CTI_TRIG0_IN_MIRA	PX_3	PD:nppukp	Configurable I/O QDSS trigger input 0 A	Y
AG5	GPIO_92	QDSS_CTI_TRIG1_IN_MIRB SD_CARD_DET_N	PX_3	PD:nppukp	Configurable I/O QDSS trigger input 1 B Secure digital card detect	Y

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AG6	GPIO_93	SD_WRITE_PROTECT	PX_3	PD:nppukp	Configurable I/O Secure digital card write protection	N
AG3	GPIO_94	PCIE0_RESET_N	PX_3	PD:nppukp	Configurable I/O PCIe reset	N
AF3	GPIO_95	PCIE0_CLKREQ_N	PX_3	PU:nppdkp	Configurable I/O PCIe clock request	Y
AG4	GPIO_96	PCIE0_WAKE_N	PX_3	PD:nppukp	Configurable I/O PCIe wake up	Y
AE3	GPIO_97	PCIE1_RESET_N	PX_3	PD:nppukp	Configurable I/O PCIe reset	N
AD3	GPIO_98	PCIE1_CLKREQ_N	PX_3	PU:nppdkp	Configurable I/O PCIe clock request	Y
AC1	GPIO_99	PCIE1_WAKE_N	PX_3	PD:nppukp	Configurable I/O PCIe wake up	Y
U5	GPIO_100	CAM_MCLK0 QDSS_GPIO_TRACEDATA_LOCB[0]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
U6	GPIO_101	CAM_MCLK1 QDSS_GPIO_TRACEDATA_LOCB[1]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
V5	GPIO_102	CAM_MCLK2 QDSS_GPIO_TRACEDATA_LOCB[2]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
V6	GPIO_103	CAM_MCLK3 QDSS_GPIO_TRACEDATA_LOCB[3]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
W5	GPIO_104	CAM_MCLK4 QDSS_GPIO_TRACEDATA_LOCB[4]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
W6	GPIO_105	CAM_MCLK5 QDSS_GPIO_TRACEDATA_LOCB[5]	PX_3	PD:nppukp	Configurable I/O Camera master clock QDSS trace data	N
W3	GPIO_106	CCI_ASYNC_IN0 QDSS_GPIO_TRACEDATA_LOCB[6]	PX_3	PD:nppukp	Configurable I/O Camera control interface async QDSS trace data	N
U4	GPIO_107	CCI_I2C_SDA0 QDSS_GPIO_TRACEDATA_LOCB[7]	PX_3	PD:nppukp	Configurable I/O Dedicated camera control interface I^2C serial data QDSS trace data	N

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
U3	GPIO_108		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Dedicated camera control interface I2C clock	
		QDSS_GPIO_TRACEDATA_LOCB[8]			QDSS trace data	
V4	GPIO_109		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Dedicated camera control interface I2C serial data	
		QDSS_GPIO_TRACECLK_LOCB			QDSS trace clock B	
V3	GPIO_110		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Dedicated camera control interface I2C clock	
		QDSS_GPIO_TRACECTL_LOCB			QDSS trace control B	
U2	GPIO_111		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Dedicated camera control interface I2C serial data	
		QDSS_GPIO_TRACEDATA_LOCB[9]			QDSS trace data	
U1	GPIO_112		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Dedicated camera control interface I2C clock	
		QDSS_GPIO_TRACEDATA_LOCB[10]			QDSS trace data	
V2	GPIO_113		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA3			Dedicated camera control interface I2C serial data	
		QDSS_GPIO_TRACEDATA_LOCB[11]			QDSS trace data	
V1	GPIO_114		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL3			Dedicated camera control interface I2C clock	
		QDSS_GPIO_TRACEDATA_LOCB[12]			QDSS trace data	
AA5	GPIO_115		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER0			Camera control interface timer	
		GCC_GP1_CLK_MIRB			General-purpose clock	
		QDSS_GPIO_TRACEDATA_LOCB[13]			QDSS trace data	
Y5	GPIO_116		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER1			Camera control interface timer	
		GCC_GP2_CLK_MIRB			General-purpose clock	
		QDSS_GPIO_TRACEDATA_LOCB[14]			QDSS trace data	
Y6	GPIO_117		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER2			Camera control interface timer	
		GCC_GP3_CLK_MIRB			General-purpose clock	
		QDSS_GPIO_TRACEDATA_LOCB[15]			QDSS trace data	
AV8	GPIO_118		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3			Camera control interface timer	
		CCI_ASYNC_IN1			Camera control interface async	

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AW8	GPIO_119	CCI_TIMER4 CCI_ASYNC_IN2	PX_3	PD:nppukp	Configurable I/O Camera control interface timer Camera control interface async	Y
AT15	GPIO_120	MI2S2_SCK	PX_3	PD:nppukp	Configurable I/O MI^{2}S clock	N
AR15	GPIO_121	MI2S2_DATA0	PX_3	PD:nppukp	Configurable I/O MI^{2}S serial data channel	N
AT14	GPIO_122	MI2S2_WS	PX_3	PD:nppukp	Configurable I/O MI^{2}S serial data word select	N
AU14	GPIO_123	PRI_MI2S_MCLK	PX_3	PD:nppukp	Configurable I/O Primary MI^{2}S master clock	N
AR14	GPIO_124	SEC_MI2S_MCLK AUDIO_REF_CLK MI2S2_DATA1	PX_3	PD:nppukp	Configurable I/O Secondary MI^{2}S master clock Audio reference clock MI^{2}S serial data channel	N
AU16	GPIO_125	MI2S0_SCK	PX_3	PD:nppukp	Configurable I/O MI^{2}S clock	N
AV16	GPIO_126	MI2S0_DATA0 GP_PDM_MIRA[0]	PX_3	PD:nppukp	Configurable I/O MI^{2}S serial data channel General-purpose PDM output	N
AU17	GPIO_127	MI2S0_DATA1 GP_PDM_MIRA[1]	PX_3	PD:nppukp	Configurable I/O MI^{2}S serial data channel General-purpose PDM output	N
AV17	GPIO_128	MI2S0_WS GP_PDM_MIRA[2]	PX_3	PD:nppukp	Configurable I/O MI^{2}S serial data word select General-purpose PDM output	N
AU11	GPIO_129	LPASS_SLIMBUS_CLK MI2S1_SCK GCC_GP1_CLK_MIRA	PX_3	PD:nppukp	Configurable I/O Low-power audio SLIMbus clock MI^{2}S clock General-purpose clock	N
AU12	GPIO_130	LPASS_SLIMBUS_DATA0 MI2S1_DATA0 GCC_GP2_CLK_MIRA	PX_3	PD:nppukp	Configurable I/O Low-power audio SLIMbus data MI^{2}S serial data channel General-purpose clock	Y

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AV13	GPIO_131		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_DATA1			MI^{2}S serial data channel	
		GCC_GP3_CLK_MIRA			General-purpose clock	
AU13	GPIO_132		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_WS			MI^{2}S serial data word select	
AV34	GPIO_133		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_DATA			UIM data	
AW34	GPIO_134		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_CLK			UIM clock	
AV35	GPIO_135		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_RESET			UIM reset	
AW35	GPIO_136		PX_3	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT			UIM presence detection	
AU28	GPIO_137		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_DATA			UIM data	
AV28	GPIO_138		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_CLK			UIM clock	
AU29	GPIO_139		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_RESET			UIM reset	
AV29	GPIO_140		PX_3	PD:nppukp	Configurable I/O	Y
		UIM0_PRESENT			UIM presence detection	
AA40	GPIO_141		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front end interface clock	
		GRFC0			Generic RF controller bit	
AA39	GPIO_142		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front end interface data	
		GRFC1			Generic RF controller bit	
		BOOT_CONFIG[0]			Boot configuration bit	
Y39	GPIO_143		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front end interface clock	
		GRFC2			Generic RF controller bit	
Y38	GPIO_144		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front end interface data	
		GRFC3			Generic RF controller bit	
		BOOT_CONFIG[1]			Boot configuration bit	
AA38	GPIO_145		PX_3	PD:nppukp	Configurable I/O	N
		RFFE2_CLK			RF front end interface clock	
		GRFC4			Generic RF controller bit	

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Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AB40	GPIO_146		PX_3	PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front end interface data	
		GRFC5			Generic RF controller bit	
		BOOT_CONFIG[2]			Boot configuration bit	
AB39	GPIO_147		PX_3	PD:nppukp	Configurable I/O	N
		RFFE3_CLK			RF front end interface clock	
		GRFC6			Generic RF controller bit	
AB38	GPIO_148		PX_3	PD:nppukp	Configurable I/O	N
		RFFE3_DATA			RF front end interface data	
		GRFC7			Generic RF controller bit	
		BOOT_CONFIG[3]			Boot configuration bit	
W38	GPIO_149		PX_3	PD:nppukp	Configurable I/O	N
		RFFE4_CLK			RF front end interface clock	
		GRFC8			Generic RF controller bit	
Y40	GPIO_150		PX_3	PD:nppukp	Configurable I/O	N
		RFFE4_DATA			RF front end interface data	
		GRFC9			Generic RF controller bit	
		BOOT_CONFIG[4]			Boot configuration bit	
AE40	GPIO_151		PX_3	PD:nppukp	Configurable I/O	Y
		WLAN_COEX_UART1_RX			Interface between WCN685x and SM8350	
AE39	GPIO_152		PX_3	PD:nppukp	Configurable I/O	N
		WLAN_COEX_UART1_TX			Interface between WCN685x and SM8350	
		BOOT_CONFIG[10]			Boot configuration bit	
AD39	GPIO_153		PX_3	PD:nppukp	Configurable I/O	Y
		HST_SW_CTRL			SW control for WCN685x	
AD38	GPIO_154		PX_3	PD:nppukp	Configurable I/O	N
		GRFC11			Generic RF controller bit	
AC40	GPIO_155		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_0			GPS control signal [PPS signal/EXT Blanking/TX AGGR]	
AC39	GPIO_156		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_1			GPS control signal [PPS signal/EXT Blanking/TX AGGR]	
		BOOT_CONFIG[7]			Boot configuration bit	

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
AC38	GPIO_157		PX_3	PD:nppukp	Configurable I/O	Y
		GRFC12			Generic RF controller bit	
		PA_INDICATOR_1_OR_2			PA transmit indicator	
		NAV_GPIO_2			GPS control signal [PPS signal/EXT Blanking/TX AGGR]	
		BOOT_CONFIG[5]			Boot configuration bit	
AC37	GPIO_158		PX_3	PD:nppukp	Configurable I/O	N
		GRFC0_MIRA			Generic RF controller bit	
		BOOT_CONFIG[6]			Boot configuration bit	
U36	GPIO_159		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK0_REQUEST			QLink request	
V36	GPIO_160		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_ENABLE			QLink enable	
V37	GPIO_161		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_WMSS_RESET_N			SDR modem subsystem reset output	
T37	GPIO_162		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK1_REQUEST			QLink request	
T36	GPIO_163		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_ENABLE			QLink enable	
U37	GPIO_164		PX_3	PD:nppukp	Configurable I/O	N
		QLINK1_WMSS_RESET_N			SMR modem subsystem reset output	
V38	GPIO_165		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK2_REQUEST			QLink request	
W40	GPIO_166		PX_3	PD:nppukp	Configurable I/O	N
		QLINK2_ENABLE			QLink enable	
W39	GPIO_167		PX_3	PD:nppukp	Configurable I/O	N
		QLINK2_WMSS_RESET_N			SDR modem subsystem reset output	
AT25	GPIO_168		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_0			LPASS I/O	
		SWR_TX_CLK			SoundWire transmit clock	
		LPI_QUA_MI2S_SCK			LPI MI^{2}S clock	
AR26	GPIO_169		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_1			LPASS I/O	
		SWR_TX_DATA0			SoundWire transmit data	
		LPI_QUA_MI2S_WS			LPI MI2S serial data word select	
AT26	GPIO_170		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_2			LPASS I/O	
		SWR_TX_DATA1			SoundWire transmit data	

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		LPI_QUA_MI2S_DATA0			LPI MI2S serial data channel	
AT27	GPIO_171		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_3			LPASS I/O	
		SWR_RX_CLK			SoundWire receive clock	
		LPI_QUA_MI2S_DATA1			LPI MI2S serial data channel	
AR28	GPIO_172		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_4			LPASS I/O	
		SWR_RX_DATA0			SoundWire receive data	
		LPI_QUA_MI2S_DATA2			LPI MI2S serial data channel	
AT28	GPIO_173		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_5			LPASS I/O	
		SWR_RX_DATA1			SoundWire receive data	
		EXT_MCLK1_C			External MCLK	
		LPI_QUA_MI2S_DATA3			LPI MI2S serial data channel	
AT22	GPIO_174		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_6			LPASS I/O	
		LPI_DMIC1_CLK			DMIC clock	
		LPI_I2S1_CLK			LPI MI2S clock	
AR23	GPIO_175		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_7			LPASS I/O	
		LPI_DMIC1_DATA			DMIC data	
		LPI_I2S1_WS			LPI MI2S serial data word select	
AT23	GPIO_176		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_8			LPASS I/O	
		LPI_DMIC2_CLK			DMIC clock	
		LPI_I2S1_DATA0			LPI MI^{2}S serial data channel	
AR24	GPIO_177		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_9			LPASS I/O	
		LPI_DMIC2_DATA			DMIC data	
		LPI_I2S1_DATA1			LPI MI^{2}S serial data channel	
		EXT_MCLK1_B			External MCLK	
AT21	GPIO_178		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_10			LPASS I/O	
		LPI_I2S2_CLK			LPI MI^{2}S clock	
		WSA_SWR_CLK			SoundWire clock for WSA	
AR22	GPIO_179		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_11			LPASS I/O	
		LPI_I2S2_WS			LPI MI^{2}S serial data word select	

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		WSA_SWR_DATA			SoundWire data for WSA	
AT24	GPIO_180	LPASS_12 LPI_DMIC3_CLK LPI_I2S2_DATA0	PX_3	PD:nppukp	Configurable I/O LPASS I/O DMIC clock LPI MI^{2}S serial data channel	Y
AR25	GPIO_181	LPASS_13 LPI_DMIC3_DATA LPI_I2S2_DATA1 EXT_MCLK1_A	PX_3	PD:nppukp	Configurable I/O LPASS I/O DMIC data LPI MI^{2}S serial data channel External MCLK	N
AR27	GPIO_182	LPASS_14 SWR_TX_DATA2	PX_3	PD:nppukp	Configurable I/O LPASS I/O SoundWire transmit data	N
AV21	GPIO_183	QDSS_GPIO_TRACEDATA_LOCA[0] SSC_0	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AU21	GPIO_184	QDSS_GPIO_TRACEDATA_LOCA[1] SSC_1	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AR21	GPIO_185	QDSS_GPIO_TRACEDATA_LOCA[2] SSC_2	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AT20	GPIO_186	QDSS_GPIO_TRACEDATA_LOCA[3] SSC_3	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AU18	GPIO_187	QDSS_GPIO_TRACEDATA_LOCA[4] SSC_4	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AV18	GPIO_188	QDSS_GPIO_TRACEDATA_LOCA[5] SSC_5	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AU19	GPIO_189	QDSS_GPIO_TRACEDATA_LOCA[6] SSC_6	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AV19	GPIO_190	QDSS_GPIO_TRACEDATA_LOCA[7] SSC_7	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AU22	GPIO_191		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Bottom pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description	Wake-up function? (yes/no)
			Voltage	Type		
		QDSS_GPIO_TRACECTL_LOCA SSC_8			QDSS trace control A SSC I/O	
AV22	GPIO_192	QDSS_GPIO_TRACECLK_LOCA SSC_9	PX_3	PD:nppukp	Configurable I/O QDSS trace clock A SSC I/O	N
AV20	GPIO_193	QDSS_GPIO_TRACEDATA_LOCA[8] SSC_10	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AU20	GPIO_194	QDSS_GPIO_TRACEDATA_LOCA[9] SSC_11	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AT19	GPIO_195	QDSS_GPIO_TRACEDATA_LOCA[10] SSC_12	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AR19	GPIO_196	QDSS_GPIO_TRACEDATA_LOCA[11] SSC_13	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AT18	GPIO_197	QDSS_GPIO_TRACEDATA_LOCA[12] SSC_14	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AR18	GPIO_198	QDSS_GPIO_TRACEDATA_LOCA[13] SSC_15	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AR16	GPIO_199	QDSS_GPIO_TRACEDATA_LOCA[14] SSC_16	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	N
AT16	GPIO_200	QDSS_GPIO_TRACEDATA_LOCA[15] SSC_17	PX_3	PD:nppukp	Configurable I/O QDSS trace data SSC I/O	Y
AR17	GPIO_201	SSC_18	PX_3	PD:nppukp	Configurable I/O SSC I/O	N
AT17	GPIO_202	SSC_19	PX_3	PD:nppukp	Configurable I/O SSC I/O	Y

1. See Table 2-1 for the parameter and acronym definitions.

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Table 2-4 QUP lane to function mapping

Interface	Lane						
	L0	L1	L2	L3	L4	L5	L6
UART	CTS	RFR	Tx	Rx			
HS UART	CTS	RFR	Tx	Rx			
I^2C	SDA	SCL					
I3C	SDA	SCL					
SPI	MISO	MOSI	SCLK	CS_0	CS_1	CS_2	CS_3

Table 2-5 QUP engine to function mapping

QUP engine	GPIO numbers	UART	HS-UART	I^2C	I3C	SPI
QUP_0	4–7	Yes		Yes		Yes
QUP_1	8–11	Yes		Yes		Yes
QUP_2	12–15	Yes		Yes		Yes
QUP_3	16–19	Yes		Yes		Yes
QUP_4	20–23	Yes		Yes		Yes
QUP_5	24–27	Yes		Yes		Yes
QUP_6	28–31		Yes	Yes		Yes
QUP_7	32–35		Yes	Yes		Yes
QUP_8	36–39	Yes		Yes	Yes	Yes
QUP_9	40–43	Yes		Yes		Yes
QUP_10	44–47	Yes		Yes		Yes
QUP_11	48–51	Yes		Yes		Yes
QUP_12	52–55		Yes	Yes		Yes
QUP_13	0–3		Yes	Yes		Yes
QUP_14	56–59	Yes		Yes	Yes	Yes
QUP_15	60–63	Yes		Yes	Yes	Yes
QUP_16	64–67	Yes		Yes		Yes
QUP_17	72–75	Yes		Yes		Yes
QUP_18	68–71		Yes	Yes		Yes
QUP_19	76–79		Yes	Yes		Yes

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Table 2-6 Bottom pin descriptions: ground, DNC, and power-supply pins

Pad #	Pad name	Functional description
A1, A2, A3, A4, A5, A6, A7, A8, A9, A14, A18, A25, A29, A33, A36, A37, A38, A39, A40, AA7, AA11, AA13, AA17, AA19, AA21, AA23, AA24, AA27, AA29, AA31, AA34, AA37, AB2, AB10, AB12, AB14, AB18, AB20, AB22, AB25, AB26, AB28, AB30, AB32, AB34, AB37, AC7, AC8, AC9, AC11, AC13, AC15, AC18, AC20, AC22, AC24, AC29, AC31, AC33, AC36, AD7, AD8, AD9, AD10, AD12, AD16, AD18, AD20, AD22, AD24, AD26, AD37, AD40, AE7, AE9, AE11, AE13, AE14, AE15, AE17, AE19, AE21, AE24, AE25, AE33, AE37, AF4, AF7, AF8, AF10, AF12, AF17, AF19, AF22, AF23, AF25, AF37, AG8, AG10, AG13, AG14, AG16, AG18, AG21, AG24, AG27, AG29, AG31, AG33, AG38, AH2, AH3, AH4, AH5, AH7, AH12, AH13, AH19, AH22, AH26, AH28, AH30, AH32, AH35, AH38, AJ3, AJ6, AJ8, AJ12, AJ13, AJ14, AJ18, AJ21, AJ25, AJ33, AJ38, AK3, AK7, AK13, AK20, AK23, AK24, AK26, AK32, AK36, AK37, AL3, AL4, AL5, AL8, AL12, AL14, AL18, AL19, AL21, AL25, AL33, AL38, AL40, AM1, AM2, AM3, AM4, AM7, AM13, AM20, AM24, AM26, AM28, AM30, AM32, AM35, AM36, AM37, AM38, AN1, AN4, AN8, AN10, AN12, AN14, AN16, AN18, AN19, AN21, AN22, AN25, AN27, AN32, AN34, AN37, AP1, AP4, AP9, AP15, AP17, AP19, AP21, AP23, AP25, AP28, AP32, AP38, AP40, AR1, AR2, AR3, AR4, AR5, AR6, AR9, AR30, AR31, AR32, AR34, AR37, AT1, AT4, AT7, AT8, AT9, AT10, AT12, AT13, AT30, AT31, AT32, AT33, AT34, AT40, AU1, AU4, AU7, AU15, AU25, AU27, AU30, AU31, AU32, AU34, AU35, AU36, AV1, AV4, AV5, AV6, AV7, AV12, AV14, AV15, AV23, AV25, AV27, AV30, AV32, AV33, AV36, AV40, AW1, AW2, AW3, AW4, AW7, AW10, AW14, AW18, AW21, AW25, AW29, AW33, AW36, AW37, AW39, AW40, B1, B3, B5, B6, B7, B8, B9, B10, B11, B12, B14, B16, B18, B20, B23, B27, B28, B29, B30, B31, B32, B33, B36, B37, B38, B39, B40, C1, C3, C6, C9, C11, C12, C14, C16, C18, C20, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, D1, D6, D9, D11, D12, D16, D20, D29, D30, D31, D32, D38, E1, E12, E16, E20, E23, E30, E32, E38, F1, F2, F3, F4, F11, F14, F15, F18, F20, F22, F33, F34, F35, F38, G5, G6, G7, G8, G17, G19, G21, G23, G25, G27, G28, G31, G33, G34, G35, G38, H1, H2, H5, H6, H7, H8, H9, H11, H13, H14, H16, H18, H20, H22, H24, H30, H34, H35, H38, J5, J9, J11, J13, J26, J28, J30, J33, J35, J38, J39, J40, K6, K14, K15, K16, K18, K24, K27, K29, K31, K38, L1, L2, L5, L7, L8, L10, L12, L13, L15, L17, L26, L28, L30, L34, L35, L38, M6, M7, M14, M15, M16, M18, M20, M22, M24, M27, M29, M31, M38, N5, N7, N10, N12, N13, N17, N19, N21, N23, N26, N28, N30, N32, N35, N38, P1, P2, P6, P7, P12, P14, P15, P16, P18, P24, P27, P29, P31, P33, P34, P38, R5, R6, R7, R8, R10, R13, R17, R26, R28, R30, R32, R35, R36, R37, R38, T1, T2, T3, T4, T5, T7, T14, T15, T16, T18, T24, T35, T38, U7, U10, U12, U13, U17, U19, U21, U23, U26, U32, U34, U38, V14, V15, V16, V18, V20, V22, V24, V33, V35, V39, V40, W2, W4, W7, W8, W10, W12, W13, W17, W19, W21, W23, W26, W28, W30, W32, W35, W36, Y10, Y11, Y12, Y14, Y15, Y18, Y20, Y22, Y25, Y27, Y29, Y31, Y33, Y34, Y37	GND	Ground
A21, AA28, AC14, AD14, AE20, AE26, AF15, AF16, AF26, AF5, AK38, AL23, AM23, AN2, AN3, AP2, AP3, AT11, AT2, AT3, AT37, AU2, AU26, AU3, AV2, AV26, AV3, E29, J17, K17, R12, R33, T33	DNC	Do not connect; connected internally, do not connect externally.
A13, A30, AW13, AW30	VDD1	Power for memory core (bottom VDDx)
A15, A16, A17, A26, A27, A28, AW15, AW16, AW17, AW26, AW27, AW28	VDD2H	Power for memory core (bottom VDDx)
A22, A23, A24, AW22, AW23, AW24	VDD2L	Power for memory core (bottom VDDx)
AN13	VDD_A_APC_CS_1P8	Power for application processor current-sensor circuits
G10, H10	VDD_A_EBI0	Power for EBI PHY circuits
AP10, AP11	VDD_A_EBI1	Power for EBI PHY circuits
F29, G29, G30	VDD_A_EBI2	Power for EBI PHY circuits
AN28, AP30	VDD_A_EBI3	Power for EBI PHY circuits

Table 2-6 Bottom pin descriptions: ground, DNC, and power-supply pins (cont.)

Pad #	Pad name	Functional description
AC27	VDD_A_GFX_CS_1P8	Power for graphics current sensor circuits
E11	VDD_A_HV_EBI0	Power for EBI PHY high-voltage circuits
AR10	VDD_A_HV_EBI1	Power for EBI PHY high-voltage circuits
E31	VDD_A_HV_EBI2	Power for EBI PHY high-voltage circuits
AN31	VDD_A_HV_EBI3	Power for EBI PHY high-voltage circuits
G9	VDD_A_PLL_EBI0	Power for EBI PLL circuits
AR11	VDD_A_PLL_EBI1	Power for EBI PLL circuits
F30	VDD_A_PLL_EBI2	Power for EBI PLL circuits
AP29	VDD_A_PLL_EBI3	Power for EBI PLL circuits
AH24	VDD_A_SP_SENSOR	Power for SP sensor circuit
H15	VDD_A_TURING_Q6_CS_1P8	Power for Q6 current sensor 1.8 V circuits
F19, F21, F23, G16, G18, G20, G22, G24, H17, H19, H21, H23, H25, J16, J18, J24, K25, L16, L18, L24, M17, M19, M21, M23, U18, P17, P25, V25, V23, V21, V19, R16, R18, R24, V17, U16, U24, T17, T25, U22, U20, W16, W18, W20, N20, N16, N18, Y17, N22, N24, Y19, W24, W22, Y21, Y23, M25	VDD_CX	Power for digital core circuits
G13	VDD_D_EBI0	Power for EBI0 digital circuits
AR13	VDD_D_EBI1	Power for EBI1 digital circuits
F28	VDD_D_EBI2	Power for EBI2 digital circuits
AN26	VDD_D_EBI3	Power for EBI3 digital circuits
G11, G12, H12	VDD_IO_EBI0	Power for EBI0 I/O circuits
AP12, AP13, AR12	VDD_IO_EBI1	Power for EBI1 I/O circuits
F31, F32, G32	VDD_IO_EBI2	Power for EBI2 I/O circuits
AN29, AN30, AP31	VDD_IO_EBI3	Power for EBI3 I/O circuits
AA8, AA10, AB9, J8, J10, J12, J14, K9, K11, K13, M9, M11, M13, T11, T9, U8, V11, Y9, V9, N8, P9, P11, P13	VDD_MM	Power for multimedia subsystem
Y13, AA12, AA14, AB15, AC16, AD15, AD17, AD19, AD21, AD23, AE16, AE18, AE22, AF21, AG20, AG22, AH21, AJ20, AJ22, AK19, AK21, AL20, AM19, AM21, AN20, H33, K33	VDD_MX	Power for on-chip memory
AA16, AA18, AA20, AA22, AA26, AA30, AA32, AB17, AB19, AB21, AB23, AB27, AB29, AB31, AB33, AC26, AD25, AD34, AF34, AG25, AH34, AK34, AM34, H29, H31, L14, U14, W14, V13, T13, R14, N14	VDD_MX_C	Power for on-chip memory
AP20	VDD_PX_0	Power for pad group 0 – control signals
AC35	VDD_PX_10	Power for pad group 10 – UFS
V34	VDD_PX_11	Power for pad group 11 – CXO pad
AN23	VDD_PX_13	Power for pad group 13 – secure processor unit (SPU)
Y7	VDD_PX_2	Power for pad group 2 – SDC2 pads

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Table 2-6 Bottom pin descriptions: ground, DNC, and power-supply pins (cont.)

Pad #	Pad name	Functional description
V7, W37, T6, AA6, AF6, AF38, AN38, AP14, AP18, AP22, E28, G26	VDD_PX_3	Power for pad group 3 – most I/O pads
AP26	VDD_PX_5	Power for pad group 5 – UIM1 pads
AP27	VDD_PX_6	Power for pad group 5 – UIM2 pads
AH6	VDD_PX_9	Power for pad group 9 – UFS
AB7	VDD_PX_VBIAS_SDC	Reference voltage for SDC
AP24	VDD_PX_VBIAS_UIM	Reference voltage for UIM
A11, A12, A31, A32, AW11, AW12, AW31, AW32	VDDQ	Power for PoP DDR pads (top VDDQ)
AB11, AB13, AC10, AC12, AD11, AD13, AE8, AE10, AE12, AF9, AF11, AF13, AG12	VDD_APC0	Power for the Kryo Silver application processor
AF14, AF18, AG7, AG9, AG11, AG15, AG17, AG19, AH8, AH14, AH18, AJ7, AJ19, AK8, AK12, AK14, AK18, AL7, AL13, AM8, AM12, AM14, AM18, AN7, AN9, AN11, AN15, AN17	VDD_APC1	Power for the Kryo Gold application processor
J6	VDD_A_CSI_01_0P9	Power for MIPI CSI
K5	VDD_A_CSI_01_1P2	Power for MIPI CSI
L6	VDD_A_CSI_23_0P9	Power for MIPI CSI
M5	VDD_A_CSI_23_1P2	Power for MIPI CSI
N6	VDD_A_CSI_45_0P9	Power for MIPI CSI
P5	VDD_A_CSI_45_1P2	Power for MIPI CSI
F12	VDD_A_DSI_0_0P9	Power for MIPI DSI
F16, F17	VDD_A_DSI_01_1P2	Power for MIPI DSI
G14	VDD_A_DSI_0_PLL_0P9	Power for MIPI DSI
F13	VDD_A_DSI_1_0P9	Power for MIPI DSI
G15	VDD_A_DSI_1_PLL_0P9	Power for MIPI DSI
AR8	VDD_A_PCIE_0_CORE	Power for PCIe
AR7	VDD_A_PCIE_0_PLL_1P2	Power for PCIe
AP8	VDD_A_PCIE_1_CORE	Power for PCIe
AP7	VDD_A_PCIE_1_PLL_1P2	Power for PCIe
T34	VDD_A_QLINK_0_0P9	Power for QLink
R34	VDD_A_QLINK_0_0P9_CK	Power for QLink clock circuits
P35	VDD_A_QLINK_0_1P2_CK	Power for QLink clock circuits
K34	VDD_A_QLINK_1_0P9	Power for QLink
J34	VDD_A_QLINK_1_0P9_CK	Power for QLink clock circuits
K35	VDD_A_QLINK_1_1P2_CK	Power for QLink clock circuits
N34	VDD_A_QLINK_2_0P9	Power for QLink
M34	VDD_A_QLINK_2_0P9_CK	Power for QLink clock circuits
M35	VDD_A_QLINK_2_1P2_CK	Power for QLink clock circuits
AR29	VDD_A_QREFS_0P875_3	Reference voltage for QREFS
AP16	VDD_A_QREFS_0P875_5	Reference voltage for QREFS

Table 2-6 Bottom pin descriptions: ground, DNC, and power-supply pins (cont.)

Pad #	Pad name	Functional description
W34	VDD_A_QREFS_1P25	Reference voltage for QREFS
AA33	VDD_A_QREFS_1P8	Reference voltage for the QREFS
AF36, AL6	VDD_A_UFS_1P2	Power for UFS
AF35, AK6	VDD_A_UFS_CORE	Power for UFS
AK35	VDD_A_USBHS_1P8	Power for the USB high-speed circuits
AP35	VDD_A_USBHS_3P1	Power for the USB high speed circuits
AL35	VDD_A_USBHS_CORE	Power for USB HS
AG35	VDD_A_USBSSDP_0_1P2	Power for USB SS & DP
AJ35	VDD_A_USBSSDP_0_CORE	Power for USB SS & DP
AP34	VDD_A_USBSS_1_1P2	Power for USB SS
AN33	VDD_A_USBSS_1_CORE	Power for USB SS
AC28, AC30, AC32, AD27, AD33, AF27, AF33, AG26, AG28, AG30, AG32, AH25, AH27, AH29, AH31, AH33, AJ24, AJ26, AJ32, AK25, AK33, AL24, AL26, AL32, AM25, AM27, AM29, AM31, AM33, AN24	VDD_GFX	Power for graphics
AE27	VDD_GFX_CX_ISENSE	Power for graphics
AK22, AL22, AM22	VDD_LPI_CX	Power for LPI digital core circuits
AG23, AH23, AJ23	VDD_LPI_MX	Power for low-power island memory circuits
U35	VDD_LPI_MX_NAV	Power for low-power island memory circuits
W33, W31, T32, M32, M30, M28, M26, Y26, Y28, Y30, Y32, W29, W27, U33, R27, R31, R29, P32, P30, P28, V26, V32, P26, N33, N31, N29, N27, T26, H26, H28, H32, J27, J29, J31, K26, K28, K30, K32, L27, L29, L31, L33	VDD_MODEM	Power for modem circuits
AE23	VDD_QFPROM	Power for programming the QFPROM
AF24	VDD_QFPROM_SP	Power for programming the QFPROM; secure processor unit

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2.3 Pin assignments: top

2.3.1 Pin map: top

The SM8350 is available in the MPSP1393. See Chapter 4 for package details and Section 2.2 for information about the bottom pin assignments.

A high-level view of the top pin assignments is shown in Figure 2-3 for LPDDR5.

The text within Figure 2-3 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available; these options are defined in Section 2.2.1.

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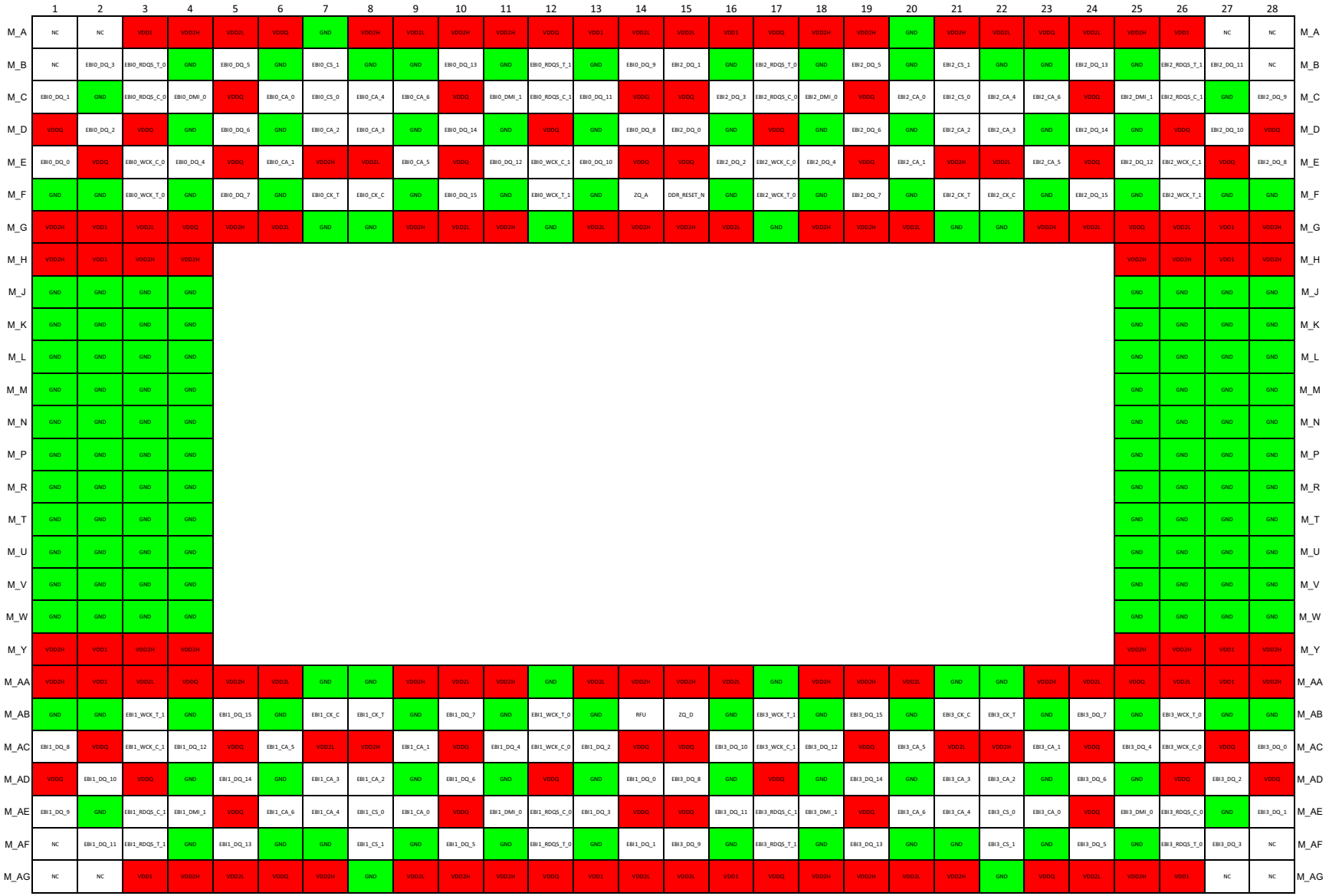

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
M_A	NC	NC	VDD1	VDD2H	VDD2L	VDDQ	GND	VDD2H	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD1	VDDQ	VDD2H	VDD2H	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD2H	VDD1	NC	NC	M_A
M_B	NC	EBI0_DQ_3	EBI0_RDQS_T_0	GND	EBI0_DQ_5	GND	EBI0_CS_1	GND	GND	EBI0_DQ_13	GND	EBI0_RDQS_T_1	GND	EBI0_DQ_9	EBI2_DQ_1	GND	EBI2_RDQS_T_0	GND	EBI2_DQ_5	GND	EBI2_CS_1	GND	GND	EBI2_DQ_13	GND	EBI2_RDQS_T_1	EBI2_DQ_11	NC	M_B
M_C	EBI0_DQ_1	GND	EBI0_RDQS_C_0	EBI0_DMI_0	VDDQ	EBI0_CA_0	EBI0_CS_0	EBI0_CA_4	EBI0_CA_6	VDDQ	EBI0_DMI_1	EBI0_RDQS_C_1	EBI0_DQ_11	VDDQ	VDDQ	EBI2_DQ_3	EBI2_RDQS_C_0	EBI2_DMI_0	VDDQ	EBI2_CA_0	EBI2_CS_0	EBI2_CA_4	EBI2_CA_6	VDDQ	EBI2_DMI_1	EBI2_RDQS_C_1	GND	EBI2_DQ_9	M_C
M_D	VDDQ	EBI0_DQ_2	VDDQ	GND	EBI0_DQ_6	GND	EBI0_CA_2	EBI0_CA_3	GND	EBI0_DQ_14	GND	VDDQ	GND	EBI0_DQ_8	EBI2_DQ_0	GND	VDDQ	GND	EBI2_DQ_6	GND	EBI2_CA_2	EBI2_CA_3	GND	EBI2_DQ_14	GND	VDDQ	EBI2_DQ_10	VDDQ	M_D
M_E	EBI0_DQ_0	VDDQ	EBI0_WCK_C_0	EBI0_DQ_4	VDDQ	EBI0_CA_1	VDD2H	VDD2L	EBI0_CA_5	VDDQ	EBI0_DQ_12	EBI0_WCK_C_1	EBI0_DQ_10	VDDQ	VDDQ	EBI2_DQ_2	EBI2_WCK_C_0	EBI2_DQ_4	VDDQ	EBI2_CA_1	VDD2H	VDD2L	EBI2_CA_5	VDDQ	EBI2_DQ_12	EBI2_WCK_C_1	VDDQ	EBI2_DQ_8	M_E
M_F	GND	GND	EBI0_WCK_T_0	GND	EBI0_DQ_7	GND	EBI0_CK_T	EBI0_CK_C	GND	EBI0_DQ_15	GND	EBI0_WCK_T_1	GND	ZQ_A	DDR_RESET_N	GND	EBI2_WCK_T_0	GND	EBI2_DQ_7	GND	EBI2_CK_T	EBI2_CK_C	GND	EBI2_DQ_15	GND	EBI2_WCK_T_1	GND	GND	M_F
M_G	VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDD2L	GND	VDD2H	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	M_G
M_H	VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	M_H
M_J	GND	GND	GND	GND																					GND	GND	GND	GND	M_J
M_K	GND	GND	GND	GND																					GND	GND	GND	GND	M_K
M_L	GND	GND	GND	GND																					GND	GND	GND	GND	M_L
M_M	GND	GND	GND	GND																					GND	GND	GND	GND	M_M
M_N	GND	GND	GND	GND																					GND	GND	GND	GND	M_N
M_P	GND	GND	GND	GND																					GND	GND	GND	GND	M_P
M_R	GND	GND	GND	GND																					GND	GND	GND	GND	M_R
M_T	GND	GND	GND	GND																					GND	GND	GND	GND	M_T
M_U	GND	GND	GND	GND																					GND	GND	GND	GND	M_U
M_V	GND	GND	GND	GND																					GND	GND	GND	GND	M_V
M_W	GND	GND	GND	GND																					GND	GND	GND	GND	M_W
M_Y	VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	M_Y
M_AA	VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDD2L	GND	VDD2H	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	M_AA
M_AB	GND	GND	EBI1_WCK_T_1	GND	EBI1_DQ_15	GND	EBI1_CK_C	EBI1_CK_T	GND	EBI1_DQ_7	GND	EBI1_WCK_T_0	GND	RFU	ZQ_D	GND	EBI3_WCK_T_1	GND	EBI3_DQ_15	GND	EBI3_CK_C	EBI3_CK_T	GND	EBI3_DQ_7	GND	EBI3_WCK_T_0	GND	GND	M_AB
M_AC	EBI1_DQ_8	VDDQ	EBI1_WCK_C_1	EBI1_DQ_12	VDDQ	EBI1_CA_5	VDD2L	VDD2H	EBI1_CA_1	VDDQ	EBI1_DQ_4	EBI1_WCK_C_0	EBI1_DQ_2	VDDQ	VDDQ	EBI3_DQ_10	EBI3_WCK_C_1	EBI3_DQ_12	VDDQ	EBI3_CA_5	VDD2L	VDD2H	EBI3_CA_1	VDDQ	EBI3_DQ_4	EBI3_WCK_C_0	VDDQ	EBI3_DQ_0	M_AC
M_AD	VDDQ	EBI1_DQ_10	VDDQ	GND	EBI1_DQ_14	GND	EBI1_CA_3	EBI1_CA_2	GND	EBI1_DQ_6	GND	VDDQ	GND	EBI1_DQ_0	EBI3_DQ_8	GND	VDDQ	GND	EBI3_DQ_14	GND	EBI3_CA_3	EBI3_CA_2	GND	EBI3_DQ_6	GND	VDDQ	EBI3_DQ_2	VDDQ	M_AD
M_AE	EBI1_DQ_9	GND	EBI1_RDQS_C_1	EBI1_DMI_1	VDDQ	EBI1_CA_6	EBI1_CA_4	EBI1_CS_0	EBI1_CA_0	VDDQ	EBI1_DMI_0	EBI1_RDQS_C_0	EBI1_DQ_3	VDDQ	VDDQ	EBI3_DQ_11	EBI3_RDQS_C_1	EBI3_DMI_1	VDDQ	EBI3_CA_6	EBI3_CA_4	EBI3_CS_0	EBI3_CA_0	VDDQ	EBI3_DMI_0	EBI3_RDQS_C_0	GND	EBI3_DQ_1	M_AE
M_AF	NC	EBI1_DQ_11	EBI1_RDQS_T_1	GND	EBI1_DQ_13	GND	GND	EBI1_CS_1	GND	EBI1_DQ_5	GND	EBI1_RDQS_T_0	GND	EBI1_DQ_1	EBI3_DQ_9	GND	EBI3_RDQS_T_1	GND	EBI3_DQ_13	GND	GND	EBI3_CS_1	GND	EBI3_DQ_5	GND	EBI3_RDQS_T_0	EBI3_DQ_3	NC	M_AF
M_AG	NC	NC	VDD1	VDD2H	VDD2L	VDDQ	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD1	VDDQ	VDD2H	VDD2H	VDD2L	VDD2H	GND	VDDQ	VDD2L	VDD2H	VDD1	NC	NC	M_AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Figure 2-3 SM8350 LPDDR5 top pin assignments

2.3.2 Pin descriptions: top

Descriptions of top pins are presented in Section 2.3.2.1 for LPDDR5 pins.

2.3.2.1 LPDDR5 top pins

Table 2-7 Top pin descriptions – LPDDR5 general pins

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0
M_C20	EBI2_CA_0	EBI	DO	EBI2 LPDDR5 command/address bit 0
M_AE23	EBI3_CA_0	EBI	DO	EBI3 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_AC9	EBI1_CA_1	EBI	DO	EBI1 LPDDR5 command/address bit 1
M_E20	EBI2_CA_1	EBI	DO	EBI2 LPDDR5 command/address bit 1
M_AC23	EBI3_CA_1	EBI	DO	EBI3 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_AD8	EBI1_CA_2	EBI	DO	EBI1 LPDDR5 command/address bit 2
M_D21	EBI2_CA_2	EBI	DO	EBI2 LPDDR5 command/address bit 2
M_AD22	EBI3_CA_2	EBI	DO	EBI3 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_AD7	EBI1_CA_3	EBI	DO	EBI1 LPDDR5 command/address bit 3
M_D22	EBI2_CA_3	EBI	DO	EBI2 LPDDR5 command/address bit 3
M_AD21	EBI3_CA_3	EBI	DO	EBI3 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_AE7	EBI1_CA_4	EBI	DO	EBI1 LPDDR5 command/address bit 4
M_C22	EBI2_CA_4	EBI	DO	EBI2 LPDDR5 command/address bit 4
M_AE21	EBI3_CA_4	EBI	DO	EBI3 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_AC6	EBI1_CA_5	EBI	DO	EBI1 LPDDR5 command/address bit 5
M_E23	EBI2_CA_5	EBI	DO	EBI2 LPDDR5 command/address bit 5
M_AC20	EBI3_CA_5	EBI	DO	EBI3 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_AE6	EBI1_CA_6	EBI	DO	EBI1 LPDDR5 command/address bit 6
M_C23	EBI2_CA_6	EBI	DO	EBI2 LPDDR5 command/address bit 6
M_AE20	EBI3_CA_6	EBI	DO	EBI3 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock – negative
M_AB7	EBI1_CK_C	EBI	DO	EBI1 LPDDR5 differential clock – negative
M_F22	EBI2_CK_C	EBI	DO	EBI2 LPDDR5 differential clock – negative
M_AB21	EBI3_CK_C	EBI	DO	EBI3 LPDDR5 differential clock – negative
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock – positive

Table 2-7 Top pin descriptions – LPDDR5 general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_AB8	EBI1_CK_T	EBI	DO	EBI1 LPDDR5 differential clock – positive
M_F21	EBI2_CK_T	EBI	DO	EBI2 LPDDR5 differential clock – positive
M_AB22	EBI3_CK_T	EBI	DO	EBI3 LPDDR5 differential clock – positive
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_AE8	EBI1_CS_0	EBI	DO	EBI1 LPDDR5 chip select 0
M_C21	EBI2_CS_0	EBI	DO	EBI2 LPDDR5 chip select 0
M_AE22	EBI3_CS_0	EBI	DO	EBI3 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_AF8	EBI1_CS_1	EBI	DO	EBI1 LPDDR5 chip select 1
M_B21	EBI2_CS_1	EBI	DO	EBI2 LPDDR5 chip select 1
M_AF22	EBI3_CS_1	EBI	DO	EBI3 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_AE11	EBI1_DMI_0	EBI	DO	EBI1 LPDDR5 data mask for byte 0
M_C18	EBI2_DMI_0	EBI	DO	EBI2 LPDDR5 data mask for byte 0
M_AE25	EBI3_DMI_0	EBI	DO	EBI3 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_AE4	EBI1_DMI_1	EBI	DO	EBI1 LPDDR5 data mask for byte 1
M_C25	EBI2_DMI_1	EBI	DO	EBI2 LPDDR5 data mask for byte 1
M_AE18	EBI3_DMI_1	EBI	DO	EBI3 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_AD14	EBI1_DQ_0	EBI	B	EBI1 LPDDR5 data bit 0
M_D15	EBI2_DQ_0	EBI	B	EBI2 LPDDR5 data bit 0
M_AC28	EBI3_DQ_0	EBI	B	EBI3 LPDDR5 data bit 0
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_AD2	EBI1_DQ_10	EBI	B	EBI1 LPDDR5 data bit 10
M_D27	EBI2_DQ_10	EBI	B	EBI2 LPDDR5 data bit 10
M_AC16	EBI3_DQ_10	EBI	B	EBI3 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_AF2	EBI1_DQ_11	EBI	B	EBI1 LPDDR5 data bit 11
M_B27	EBI2_DQ_11	EBI	B	EBI2 LPDDR5 data bit 11
M_AE16	EBI3_DQ_11	EBI	B	EBI3 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_AC4	EBI1_DQ_12	EBI	B	EBI1 LPDDR5 data bit 12
M_E25	EBI2_DQ_12	EBI	B	EBI2 LPDDR5 data bit 12
M_AC18	EBI3_DQ_12	EBI	B	EBI3 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_AF5	EBI1_DQ_13	EBI	B	EBI1 LPDDR5 data bit 13
M_B24	EBI2_DQ_13	EBI	B	EBI2 LPDDR5 data bit 13

Table 2-7 Top pin descriptions – LPDDR5 general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_AF19	EBI3_DQ_13	EBI	B	EBI3 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_AD5	EBI1_DQ_14	EBI	B	EBI1 LPDDR5 data bit 14
M_D24	EBI2_DQ_14	EBI	B	EBI2 LPDDR5 data bit 14
M_AD19	EBI3_DQ_14	EBI	B	EBI3 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_AB5	EBI1_DQ_15	EBI	B	EBI1 LPDDR5 data bit 15
M_F24	EBI2_DQ_15	EBI	B	EBI2 LPDDR5 data bit 15
M_AB19	EBI3_DQ_15	EBI	B	EBI3 LPDDR5 data bit 15
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_AF14	EBI1_DQ_1	EBI	B	EBI1 LPDDR5 data bit 1
M_B15	EBI2_DQ_1	EBI	B	EBI2 LPDDR5 data bit 1
M_AE28	EBI3_DQ_1	EBI	B	EBI3 LPDDR5 data bit 1
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2
M_AC13	EBI1_DQ_2	EBI	B	EBI1 LPDDR5 data bit 2
M_E16	EBI2_DQ_2	EBI	B	EBI2 LPDDR5 data bit 2
M_AD27	EBI3_DQ_2	EBI	B	EBI3 LPDDR5 data bit 2
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_AE13	EBI1_DQ_3	EBI	B	EBI1 LPDDR5 data bit 3
M_C16	EBI2_DQ_3	EBI	B	EBI2 LPDDR5 data bit 3
M_AF27	EBI3_DQ_3	EBI	B	EBI3 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_AC11	EBI1_DQ_4	EBI	B	EBI1 LPDDR5 data bit 4
M_E18	EBI2_DQ_4	EBI	B	EBI2 LPDDR5 data bit 4
M_AC25	EBI3_DQ_4	EBI	B	EBI3 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_AF10	EBI1_DQ_5	EBI	B	EBI1 LPDDR5 data bit 5
M_B19	EBI2_DQ_5	EBI	B	EBI2 LPDDR5 data bit 5
M_AF24	EBI3_DQ_5	EBI	B	EBI3 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_AD10	EBI1_DQ_6	EBI	B	EBI1 LPDDR5 data bit 6
M_D19	EBI2_DQ_6	EBI	B	EBI2 LPDDR5 data bit 6
M_AD24	EBI3_DQ_6	EBI	B	EBI3 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_AB10	EBI1_DQ_7	EBI	B	EBI1 LPDDR5 data bit 7
M_F19	EBI2_DQ_7	EBI	B	EBI2 LPDDR5 data bit 7
M_AB24	EBI3_DQ_7	EBI	B	EBI3 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8

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Table 2-7 Top pin descriptions – LPDDR5 general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_AC1	EBI1_DQ_8	EBI	B	EBI1 LPDDR5 data bit 8
M_E28	EBI2_DQ_8	EBI	B	EBI2 LPDDR5 data bit 8
M_AD15	EBI3_DQ_8	EBI	B	EBI3 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9
M_AE1	EBI1_DQ_9	EBI	B	EBI1 LPDDR5 data bit 9
M_C28	EBI2_DQ_9	EBI	B	EBI2 LPDDR5 data bit 9
M_AF15	EBI3_DQ_9	EBI	B	EBI3 LPDDR5 data bit 9
M_C3	EBI0_RDQS_C_0	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 0 – positive
M_AE12	EBI1_RDQS_C_0	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 0 – positive
M_C17	EBI2_RDQS_C_0	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 0 – positive
M_AE26	EBI3_RDQS_C_0	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 0 – positive
M_B3	EBI0_RDQS_T_0	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 0 – negative
M_AF12	EBI1_RDQS_T_0	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 0 – negative
M_B17	EBI2_RDQS_T_0	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 0 – negative
M_AF26	EBI3_RDQS_T_0	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 0 – negative
M_C12	EBI0_RDQS_C_1	EBI	DI	EBI0 LPDDR5 differential read data strobe for byte 1 – positive
M_AE3	EBI1_RDQS_C_1	EBI	DI	EBI1 LPDDR5 differential read data strobe for byte 1 – positive
M_C26	EBI2_RDQS_C_1	EBI	DI	EBI2 LPDDR5 differential read data strobe for byte 1 – positive
M_AE17	EBI3_RDQS_C_1	EBI	DI	EBI3 LPDDR5 differential read data strobe for byte 1 – positive
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 – negative
M_AF3	EBI1_RDQS_T_1	EBI	B	EBI1 LPDDR5 differential read data strobe for byte 1 – negative
M_B26	EBI2_RDQS_T_1	EBI	B	EBI2 LPDDR5 differential read data strobe for byte 1 – negative
M_AF17	EBI3_RDQS_T_1	EBI	B	EBI3 LPDDR5 differential read data strobe for byte 1 – negative
M_F15	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 – positive
M_AC12	EBI1_WCK_C_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 – positive
M_E17	EBI2_WCK_C_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 – positive
M_AC26	EBI3_WCK_C_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 – positive

Table 2-7 Top pin descriptions – LPDDR5 general pins (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 – negative
M_AB12	EBI1_WCK_T_0	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 – negative
M_F17	EBI2_WCK_T_0	EBI	DO	EBI2 LPDDR5 differential data clock for byte 0 – negative
M_AB26	EBI3_WCK_T_0	EBI	DO	EBI3 LPDDR5 differential data clock for byte 0 – negative
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 – positive
M_AC3	EBI1_WCK_C_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 – positive
M_E26	EBI2_WCK_C_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 – positive
M_AC17	EBI3_WCK_C_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 – positive
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 – negative
M_AB3	EBI1_WCK_T_1	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 – negative
M_F26	EBI2_WCK_T_1	EBI	DO	EBI2 LPDDR5 differential data clock for byte 1 – negative
M_AB17	EBI3_WCK_T_1	EBI	DO	EBI3 LPDDR5 differential data clock for byte 1 – negative
M_F14	ZQ_A	–	Reference	LPDDR5 ZQ calibration for channels A and C
M_AB15	ZQ_D	–	Reference	LPDDR5 ZQ calibration for channels B and D

1. See Table 2-1 for parameter and acronym definitions.

Table 2-8 Top pin descriptions – LPDDR5 ground, NC, reserved, and power-supply pins

Pad #	Pad name	Functional description
M_A7, M_A20, M_AA7, M_AA8, M_AA12, M_AA17, M_AA21, M_AA22, M_AB1, M_AB2, M_AB4, M_AB6, M_AB9, M_AB11, M_AB13, M_AB16, M_AB18, M_AB20, M_AB23, M_AB25, M_AB27, M_AB28, M_AD4, M_AD6, M_AD9, M_AD11, M_AD13, M_AD16, M_AD18, M_AD20, M_AD23, M_AD25, M_AE2, M_AE27, M_AF4, M_AF6, M_AF7, M_AF9, M_AF11, M_AF13, M_AF16, M_AF18, M_AF20, M_AF21, M_AF23, M_AF25, M_AG8, M_AG22, M_B4, M_B6, M_B8, M_B9, M_B11, M_B13, M_B16, M_B18, M_B20, M_B22, M_B23, M_B25, M_C2, M_C27, M_D4, M_D6, M_D9, M_D11, M_D13, M_D16, M_D18, M_D20, M_D23, M_D25, M_F1, M_F2, M_F4, M_F6, M_F9, M_F11, M_F13, M_F16, M_F18, M_F20, M_F23, M_F25, M_F27, M_F28, M_G7, M_G8, M_G12, M_G17, M_G21, M_G22, M_J1, M_J2, M_J3, M_J4, M_J25, M_J26, M_J27, M_J28, M_K1, M_K2, M_K3, M_K4, M_K25, M_K26, M_K27, M_K28, M_L1, M_L2, M_L3, M_L4, M_L25, M_L26, M_L27, M_L28, M_M1, M_M2, M_M3, M_M4, M_M25, M_M26, M_M27, M_M28, M_N1, M_N2, M_N3, M_N4, M_N25, M_N26, M_N27, M_N28, M_P1, M_P2, M_P3, M_P4, M_P25, M_P26, M_P27, M_P28, M_R1, M_R2, M_R3, M_R4, M_R25, M_R26, M_R27, M_R28, M_T1, M_T2, M_T3, M_T4, M_T25, M_T26, M_T27, M_T28, M_U1, M_U2, M_U3, M_U4, M_U25, M_U26, M_U27, M_U28, M_V1, M_V2, M_V3, M_V4, M_V25, M_V26, M_V27, M_V28, M_W1, M_W2, M_W3, M_W4, M_W25, M_W26, M_W27, M_W28	GND	Ground
M_AG28, M_B1, M_B28, M_A1, M_A2, M_A27, M_A28, M_AF1, M_AF28, M_AG1, M_AG2, M_AG27	NC	Not connected
M_AB14	RFU	Reserved pins

Table 2-8 Top pin descriptions – LPDDR5 ground, NC, reserved, and power-supply pins (cont.)

Pad #	Pad name	Functional description
M_A3, M_A13, M_A16, M_A26, M_AA2, M_AA27, M_AG3, M_AG13, M_AG16, M_AG26, M_G2, M_G27, M_H2, M_H27, M_Y2, M_Y27	VDD1	Power for memory core (bottom VDDx)
M_A4, M_A8, M_A10, M_A11, M_A18, M_A19, M_A21, M_A25, M_AA1, M_AA5, M_AA9, M_AA11, M_AA14, M_AA15, M_AA18, M_AA19, M_AA23, M_AA28, M_AC8, M_AC22, M_AG4, M_AG7, M_AG10, M_AG11, M_AG18, M_AG19, M_AG21, M_AG25, M_E7, M_E21, M_G1, M_G5, M_G9, M_G11, M_G14, M_G15, M_G18, M_G19, M_G23, M_G28, M_H1, M_H3, M_H4, M_H25, M_H26, M_H28, M_Y1, M_Y3, M_Y4, M_Y25, M_Y26, M_Y28	VDD2H	Power for memory core (bottom VDDx)
M_A5, M_A9, M_A14, M_A15, M_A22, M_A24, M_AA3, M_AA6, M_AA10, M_AA13, M_AA16, M_AA20, M_AA24, M_AA26, M_AC7, M_AC21, M_AG5, M_AG9, M_AG14, M_AG15, M_AG20, M_AG24, M_E8, M_E22, M_G3, M_G6, M_G10, M_G13, M_G16, M_G20, M_G24, M_G26	VDD2L	Power for memory core (bottom VDDx)
M_A6, M_A12, M_A17, M_A23, M_AA4, M_AA25, M_AC2, M_AC5, M_AC10, M_AC14, M_AC15, M_AC19, M_AC24, M_AC27, M_AD1, M_AD3, M_AD12, M_AD17, M_AD26, M_AD28, M_AE5, M_AE10, M_AE14, M_AE15, M_AE19, M_AE24, M_AG6, M_AG12, M_AG17, M_AG23, M_C5, M_C10, M_C14, M_C15, M_C19, M_C24, M_D1, M_D3, M_D12, M_D17, M_D26, M_D28, M_E2, M_E5, M_E10, M_E14, M_E15, M_E19, M_E24, M_E27, M_G4, M_G25	VDDQ	Power for PoP DDR pads (top VDDQ)

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3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor	-0.3	1.133	V
VDD_APC1	Qualcomm Kryo Gold application processor	-0.3	1.249	V
VDD_GFX	Graphics	-0.3	1.133	V
VDD_CX	Digital core and EBI PHY digital circuits	-0.3	1.133	V
VDD_MX/MX_C	On-chip memory	-0.3	0.98	V
VDD_MM	Multimedia subsystem circuits	-0.3	1.133	V
VDD_LPI_CX	Low power island core	-0.3	1.133	V
VDD_LPI_MX	Low power island memory	-0.3	0.98	V
VDD_A_PLL_EBI0/1/2/3	EBI PHY and PLL circuits	-0.3	1.133	V
VDD_MODEM	Modem subsystem	-0.3	1.133	V
VDDA_SP_SENSOR VDD_A_CSI_01/23/45_0P9 VDD_A_DSI_0/1_0P9 VDD_A_DSI_0/1_PLL_0P9 VDD_A_PCIE_0/1_CORE VDD_A_UFS_CORE VDD_A_USBHS_CORE VDD_A_QLINK_0/1/2_0P9 VDD_A_QLINK_0/1/2_0P9_CK VDD_A_QREFS_0P875	Power for SP sensor circuit Power for MIPI CSI 0.9 V circuits Power for MIPI DSI 0.9 V circuits Power for MIPI DSI PLL 0.9 V circuits Power for PCIe core circuits Power for UFS core circuits Power for USB HS core circuits Power for QLink Power for QLink clock circuits Reference voltage for QREFS	-0.3	1.012	V
VDD_A_USBSS_1_CORE VDD_A_USBSSDP_0_CORE	Power for USB SS core circuits Power for USB SS and DisplayPort core circuits	-0.3	1.012	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_CSI_01/23/45_1P2 VDD_A_DSI_01_1P2 VDD_A_PCIE_0/1_PLL_1P2 VDD_A_QLINK_0/1/2_1P2_CK VDD_A_UFS_1P2 VDD_A_USBSS_1_1P2 VDD_A_USBSSDP_0_1P2 VDD_A_HV_EBI	Power for MIPI CSI 1.2 V circuits Power for MIPI DSI 1.2 V circuits Power for PCIe PLL 1.2 V circuits Power for QLink clock circuits Power for UFS Power for USB SS Power for USB SS and Display Port Power for EBI PHY high-voltage circuits	-0.3	1.386	V
VDD_A_USBHS_3P1	Power for USB High Speed circuits	-0.3	3.52	V
VDD_PX_0 VDD_PX_3 VDD1	Power for pad group 0 – control signals Power for pad group 3 – most I/O pads Power for DDR memory core [1]	-0.3	2.09	V
VDD_PX_2 VDD_PX_2	Power for pad group 2 – SDC2 pads Power for pad group 2 – SDC2 pads	-0.3	2.09 3.52	V
VDD_PX_5 VDD_PX_5	Power for pad group 5 – UIM1 pads Power for pad group 5 – UIM1 pads	-0.3	2.09 3.52	V
VDD_PX_6 VDD_PX_6	Power for pad group 5 – UIM2 pads Power for pad group 5 – UIM2 pads	-0.3	2.09 3.52	V
VDD_PX_9	Power for pad group 9 – UFS	-0.3	1.419	V
VDD_PX_10	Power for pad group 10 – UFS	-0.3	1.419	V
VDD_PX_11	Power for pad group 11 – CXO pad	-0.3	1.419	V
VDD_PX_13	Power for pad group 13 – secure processor unit (SPU)	-0.3	2.09	V
VDD_A_QREFS_1P8 VDD_A_TURING_Q6_CS_1P8 VDD_A_USBHS_1P8 VDD_A_APC_CS_1P8 VDD_A_GFX_CS_1P8 VDD_QFPROM VDD_QFPROM_SP	Reference voltage for QREFS 1.8 V circuits Power for Q6 current sensor 1.8 V circuits Power for the USB high-speed circuits Power for application processor current-sensor circuits Power for graphics current sensor circuits Power for programming QFPROM Power for programming QFPROM, SPU	-0.3	2.09	V
VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits	-0.3	1.463	V
VDD_PX_VBIAS_SDC VDD_PX_VBIAS_UIM	Reference voltage for SDC Reference voltage for UIM	-0.3	1.463	V
VDD_IO_EBI VDDQ	EBI I/O memory circuits POP LPDDR5 pads [1]	-0.3	0.627	V
VDD2L	Power for memory core (bottom VDDx)	–	–	V
VDD2H	Power for memory core (bottom VDDx)	–	–	V
T_S	Storage temperature [2] [3]	-55	+150	°C

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
ESD protection – see Section 7.1.				
Thermal conditions – see Section 4.5.				

1. See the LPDDR5 data sheets for VDD2H/VDD2L (for LPDDR5), and VDD1, VDDQ (for both standards) absolute maximum DC ratings for minimum and maximum voltages.
2. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
3. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Qualcomm Kryo Silver application processor Active	0.485	1.030	V
VDD_APC1	Qualcomm Kryo Gold application processor Active	0.500	1.135	V
VDD_GFX	Graphics Active	0.485	1.030	V
VDD_CX VDD_D_EBI	Digital core and EBI PHY digital circuits Active Retention [2]	0.485 0.352	1.030 0.480	V V
VDD_MX/MX_C	On-chip memory Active Retention [2]	0.695 0.540	0.977 0.668	V V
VDD_MM	Multimedia subsystem circuits Active	0.485	1.030	V
VDD_LPI_CX	Low power island core Active	0.485	1.030	V
VDD_LPI_MX VDD_LPI_MX_NAV	Low power island memory Active	0.695	0.977	V
VDD_A_EBI0/1/2/3 VDD_A_PLL_EBI0/1/2/3	EBI PHY and PLL circuits Active	0.640	1.030	V
VDD_MODEM	Modem subsystem Active	0.485	1.030	V

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1. The voltage range shown above covers the entire process range across all the active modes and is a super set of any individual device's operating voltage range. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for this mode in this power domain is a static setting.

Table 3-3 Operating conditions for non AVS voltage rails

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A_SP_SENSOR	Power for SP sensor circuit	0.83	0.875	0.92	V
VDD_A_CSI_01/23/45_0P9	Power for MIPI CSI 0.9 V circuits				
VDD_A_DSI_0/1_0P9	Power for MIPI DSI 0.9 V circuits				
VDD_A_DSI_0/1_PLL_0P9	Power for MIPI DSI PLL 0.9 V circuits				
VDD_A_PCIE_0/1_CORE	Power for PCIe core circuits				
VDD_A_UFS_CORE	Power for UFS core circuits				
VDD_A_USBHS_CORE	Power for USB HS core circuits				
VDD_A_QLINK_0/1/2_0P9	Power for QLink				
VDD_A_QLINK_0/1/2_0P9_CK	Power for QLink clock circuits				
VDD_A_QREFS_0P875	Reference voltage for QREFS				
VDD_A_USBSS_1_CORE	Power for USB SS core circuits	0.83	0.875	0.92	V
VDD_A_USBSSDP_0_CORE	Power for USB SS and DisplayPort core circuits				
VDD_A_CSI_01/23/45_1P2	Power for MIPI CSI 1.2 V circuits	1.15	1.2	1.26	V
VDD_A_DSI_01_1P2	Power for MIPI DSI 1.2 V circuits				
VDD_A_PCIE_0/1_PLL_1P2	Power for PCIe PLL 1.2 V circuits				
VDD_A_QLINK_0/1/2_1P2_CK	Power for QLink clock circuits				
VDD_A_UFS_1P2	Power for UFS				
VDD_A_USBSS_1_1P2	Power for USB SS				
VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort				
VDD_A_HV_EBI	Power for EBI PHY high-voltage circuits				
VDD_A_USBHS_3P1	Power for USB High Speed circuits	2.99	3.072	3.2	V
VDD_PX_0	Power for pad group 0 – control signals	1.7	1.8	1.9	V
VDD_PX_3	Power for pad group 3 – most I/O pads				
VDD1	Power for DDR memory core				
VDD_PX_2	Power for pad group 2 – SDC2 pads	1.7	1.8	1.9	V
VDD_PX_2	Power for pad group 2 – SDC2 pads	2.72	3.0	3.2	
VDD_PX_5	Power for pad group 5 – UIM1 pads	1.7	1.8	1.9	V
VDD_PX_5	Power for pad group 5 – UIM1 pads	2.72	3.0	3.2	
VDD_PX_6	Power for pad group 5 – UIM2 pads	1.7	1.8	1.9	V
VDD_PX_6	Power for pad group 5 – UIM2 pads	2.72	3.0	3.2	
VDD_PX_9	Power for pad group 9 – UFS	1.12	1.2	1.29	V
VDD_PX_10	Power for pad group 10 – UFS	1.12	1.2	1.29	V
VDD_PX_11	Power for pad group 11 – CXO pad	1.12	1.2	1.29	V
VDD_PX_13	Power for pad group 13 – secure processor unit (SPU)	1.7	1.8	1.9	V

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Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDD_A_QREFS_1P8	Reference voltage for QREFS 1.8 V circuits	1.7	1.8	1.9	V
VDD_A_TURING_Q6_CS_1P8	Power for Q6 current sensor 1.8 V circuits				
VDD_A_USBHS_1P8	Power for the USB high-speed circuits				
VDD_A_APC_CS_1P8	Power for application processor current-sensor circuits				
VDD_A_GFX_CS_1P8	Power for graphics current sensor circuits				
VDD_QFPROM	Power for programming QFPROM				
VDD_QFPROM_SP	Power for programming QFPROM, SPU				
VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits	1.15	1.25	1.33	V
VDD_PX_VBIAS_SDC	Reference voltage for SDC	1.15	1.25	1.33	V
VDD_PX_VBIAS_UIM	Reference voltage for UIM				
VDDQ	PoP LPDDR5 pads	0.47	0.5	0.57	V
VDD_IO_EBI	EBI I/O memory circuits				
VDD2L	Power for memory core (bottom VDDx)	_ [3]	_ [3]	_ [3]	V
VDD2H	Power for memory core (bottom VDDx)	_ [3]	_ [3]	_ [3]	V
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. See the LPDDR5 data sheets for the recommended DC operating conditions (min/typ/max voltages) of VDD2H/VDD2L and VDD1, VDDQ.

3.3 Power delivery network specification

Detailed power delivery network specification is available in *SM8350 Chipset Power Delivery Network Specification* (80-PN145-1P) document.

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SM8350 Linux Android Current Consumption Data Application Note* (80-PN145-7).

3.5 Dhrystone and rock bottom maximum power

Table 3-4 Dhrystone and rock bottom maximum power

SDM version	Kryo octa-core Dhrystone (W) [1, 2, 3]	Rock bottom (mW) [4]
SM8350-AB	7	9
SM8350-AC	8	9

1. This Kryo octa-core Dhrystone specification applies to SM8350 CS devices at $T_{junction}$ = 85°C.
2. Dhrystone power should be measured on the VDD_APC0 and VDD_APC1 rails, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).
4. Rock bottom power (VDD_CX and VDD_MX) should be measured at the VDD_CX and VDD_MX rails. See AIR1 in Table 3-1 (Test definitions) of *SM8350 Linux Android Current Consumption Data* (80-PN145-7) for the test setup.

3.6 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SM8350 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-5 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDD_PX3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDD_PX3	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [1]	–	See Table 3-6	µA
I_{IL}	Input low leakage current [1]	See Table 3-6	–	µA

Table 3-5 DC specification of 1.8 V GPIOs

Parameter	Description	Min	Max	Units
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [1]	–	See Table 3-6	µA
I_{OZL}	Low-level, tri-state leakage current [1]	See Table 3-6	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [3]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage	VDD_PX3 - 0.45	VDD_PX3	V
V_{OL}	Low-level output voltage	0.0	0.45	V

1. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on characterization of corner devices over temperature.
2. Pin voltage = VDD_PX3 maximum. For keeper pins, pin voltage = VDD_PX3 maximum - 0.45 V.
3. Pin voltage = GND and supply = VDD_PX3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_PX3 maximum.

Table 3-6 Leakage current

GPIO groups	I_{IL}/I_{OZL} (min) µA	I_{IH}/I_{OZH} (max) µA	GPIO numbers
1.8 V GPIO group 1	-1	3	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 38, 39, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 58, 59, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 131, 132, 136, 140, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 174, 175, 176, 177, 180, 181, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202
1.8 V GPIO group 2	-1	4	36, 37, 56, 57, 60, 61, 107, 108, 109, 110, 111, 112, 113, 114, 183, 184, 185, 186, 187, 188
1.8V GPIO group 3	-5	6.5	141, 142, 143, 144, 145, 146, 147, 148, 149, 150

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Table 3-6 Leakage current

GPIO groups	I_{IL}/I_{OZL} (min) µA	I_{IH}/I_{OZH} (max) µA	GPIO numbers
1.8V GPIO group 4	-3	6.5	129, 130, 168, 169, 170, 171, 172, 173, 178, 179, 182
1.8V GPIO group 5	-10	40	40, 41

Table 3-7 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDD_PX2	–	VDD_PX2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDD_PX2	V

Table 3-8 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

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Table 3-9 UIM 3 V mode DC specifications (VDD_PX_5 and VDD_PX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UIM.
3. UIM specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UIM specifies V_{OL} = 0.2 ×VDDPX_x (RST, CLK) and 0.4 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-10 UIM 1.8 V mode DC specifications (VDD_PX_5 and VDD_PX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

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1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UIM.
3. UIM specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UIM specifies V_{OL} = 0.2 × VDDPX_x (RST, CLK) and 0.3 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-11 Digital I/O characteristics for VDD_PX_9/VDD_PX_10 (UFS)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDD_PX10	V
V_{OH}	Output high-level voltage	0.75 × VDD_PX10	VDD_PX10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SM8350 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.2.

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE: All SM8350 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described in more detail in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-1.

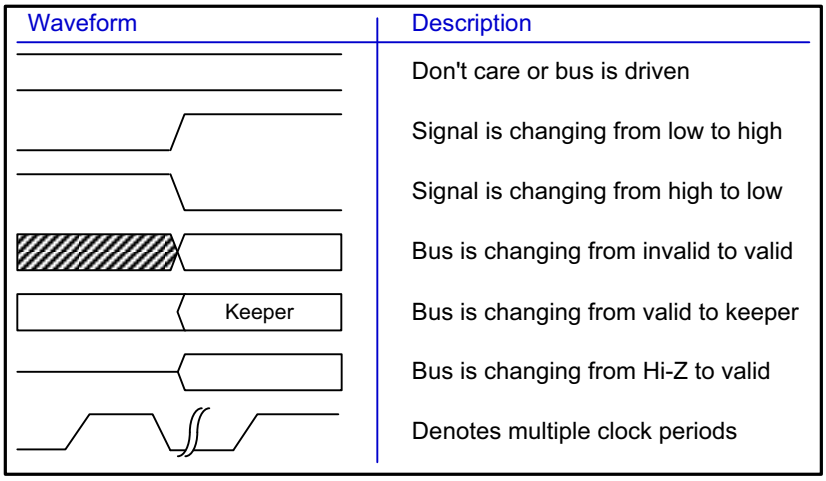

Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.7.2 Rise and fall time specifications

The testers that characterize SM8350 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-2.

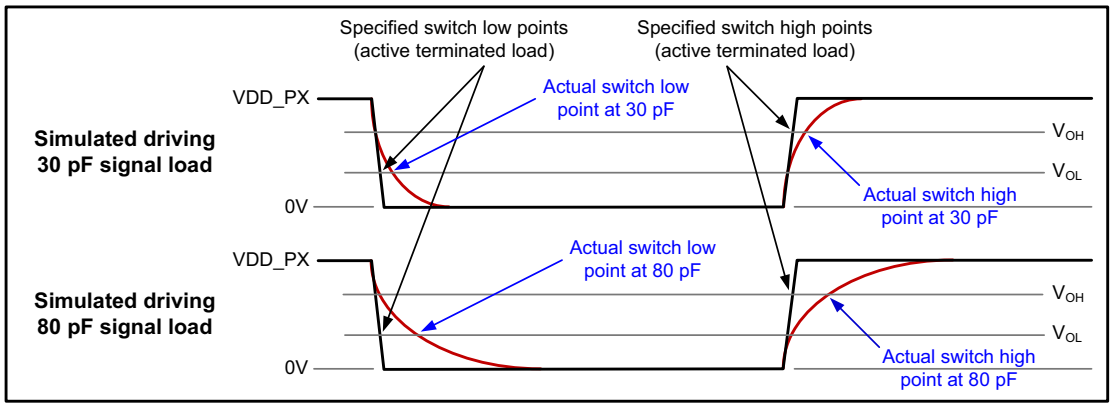

Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SM8350 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The SM8350 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

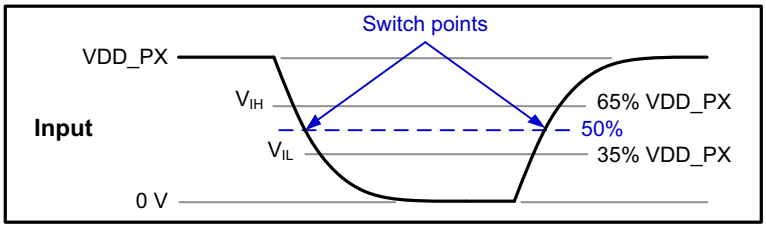

Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DDPX_x} - 50 mV or more
- V_{OL} ~ 50 mV or less

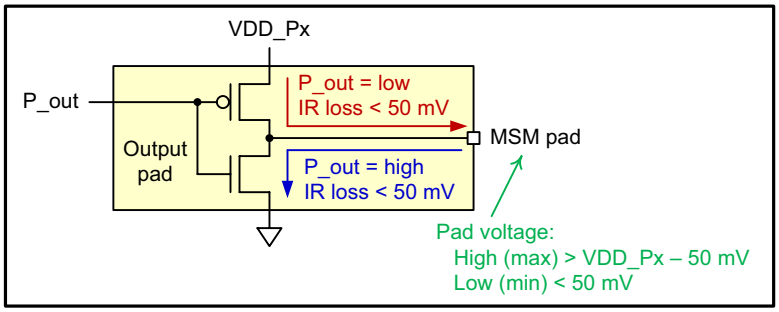

Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR5 SDRAM memory that is attached to the top of the SM8350 chipset. The memory pinout and package requirements are specified in the *PoP Memory for SM8350 Recommendations* (80-VP300-17).

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The SM8350 device supports up to six D-PHY or C-PHY camera interfaces.

Table 3-12 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v2.0	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.2	None

3.9.2 Audio support

The SM8350 supports the WCD9380/WCD9385 audio codec IC to provide the system's audio functions. SM8350 audio-related interface options with the WCD include:

- Digital microphone: Section 3.10.7
- SWR: Section 3.10.8
- SLIMbus: Section 3.10.9
- I^2S: Section 3.10.10
- PCM/TDM: Section 3.10.11
- I^2C/I3C: Section 3.10.13
- SPI: Section 3.10.14

See the *WCD9380/WCD9385 Audio Codec Device Specification* (80-PL335-1) for performance characteristics.

3.9.3 Display support

The SM8350 device supports up to two D-PHY or C-PHY displays.

Table 3-13 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

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3.9.4 DMB support

The SM8350 supports an external DMB solution using the following interface options:

- SPI: Section 3.10.14
- SD: Section 3.10.1

3.10 Connectivity

The connectivity functions supported by the SM8350 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort support over USB Type-C
- Peripheral Component Interconnect Express (PCIe) interfaces
- Digital microphone PDM interface
- SoundWire (SWR) interface
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Touchscreen connections
- Through proper configuration of the 20 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - I3C

Pertinent specifications for these functions are detailed in the following subsections.

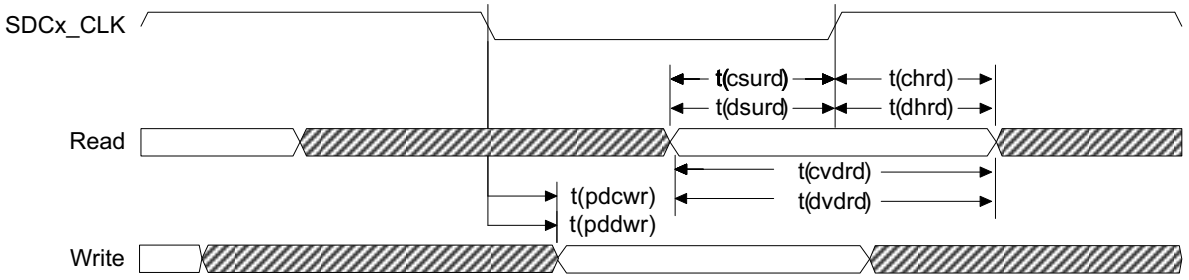
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

Table 3-14 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Single data rate SDR mode



Double data rate DDR mode

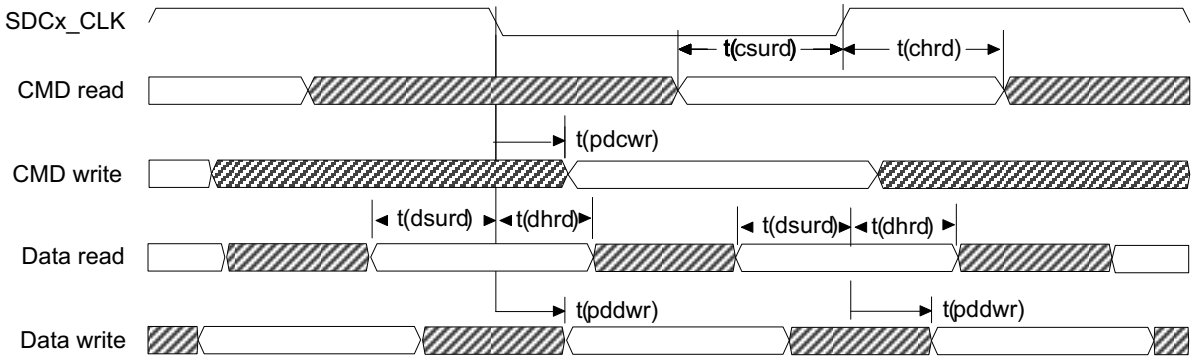


Figure 3-5 SD interface timing

3.10.2 USB interfaces

Table 3-15 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	None
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.10.3 DisplayPort

Table 3-16 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.10.4 PCIe interface

Table 3-17 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link upconfigure capability

3.10.5 UFS interface

Table 3-18 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None
Universal Flash Storage (UFS), Version 2.1	None

3.10.6 UIM interface

Table 3-19 Supported UIM standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.10.7 Digital microphone PDM interface

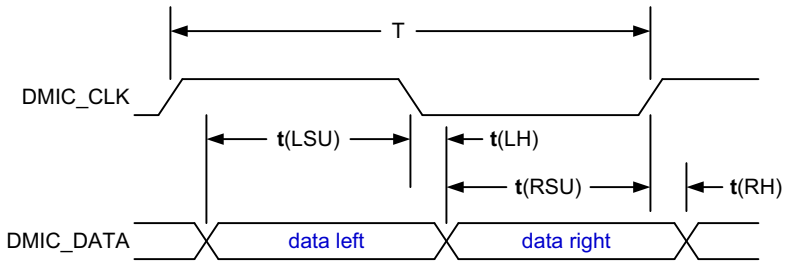


Figure 3-6 Digital microphone PDM interface timing

Table 3-20 Digital microphone timing

Parameter		Min	Typ	Max	Units
1/T	DMIC clock frequency	0.6	–	12.288	MHz
	DMIC clock duty cycle	45	–	55	%

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Table 3-20 Digital microphone timing (cont.)

t(LSU)	Data left setup time to clock falling edge	10	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	ns

3.10.8 SoundWire (SWR) interface

SM8350 SoundWire PHY timing parameters, as specified in Table 3-21, are compliant to clock and data specifications, as specified in the *MIPI Alliance Specification for SoundWire Version 1.2.* See Figure 3-7 and Figure 3-8.

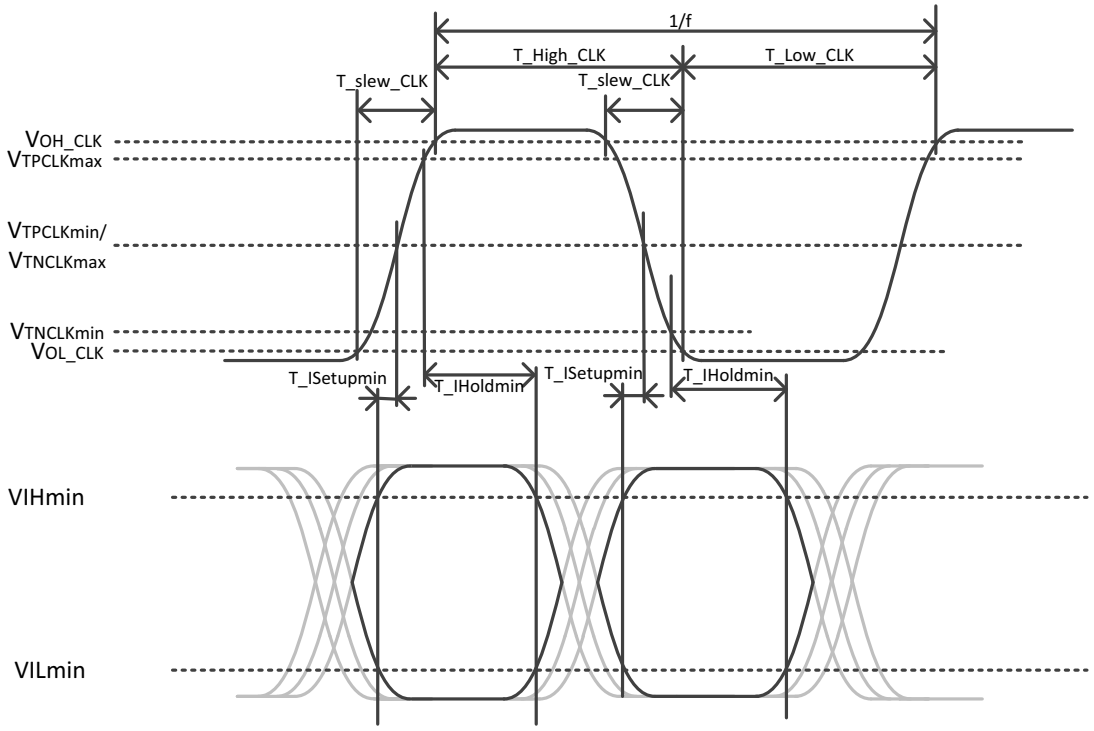

Figure 3-7 PHY timing – clock output/input and data input

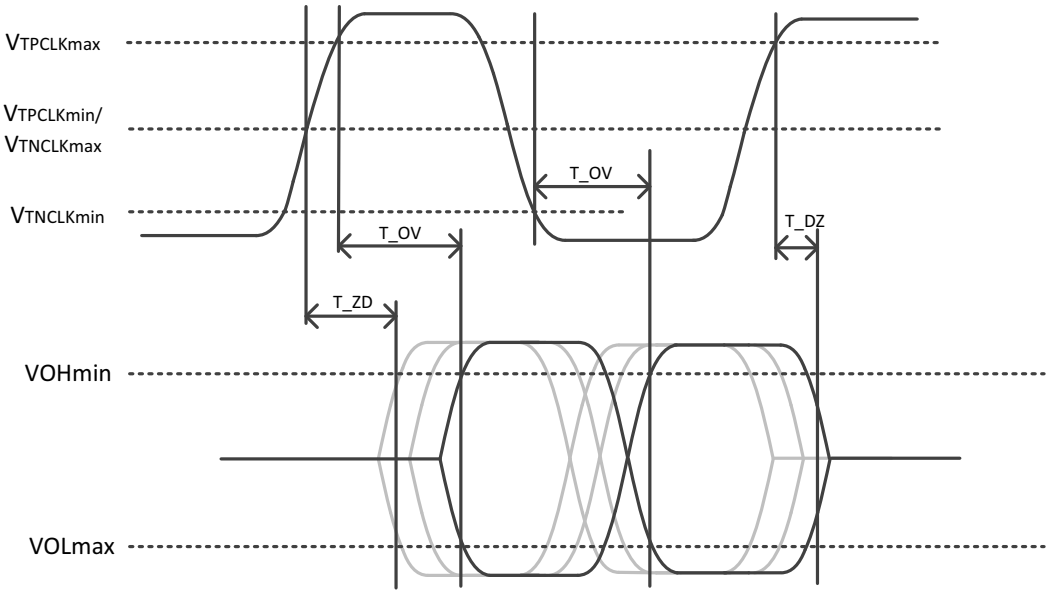

Figure 3-8 PHY timing – clock output and data output

Table 3-21 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Units
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	25.6	ns
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	2	–	ns
t_IHold_min_Data_1V8	Input hold time	–	5	ns
DC_Out_Clock	Duty cycle generated at clock output signal. calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

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3.10.9 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 2.0	None

3.10.10 I²S interfaces

There are two I²S interface types supported by the SM8350:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI²S) interface for microphone and speaker functions

The following information applies to both interface types.

Table 3-23 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

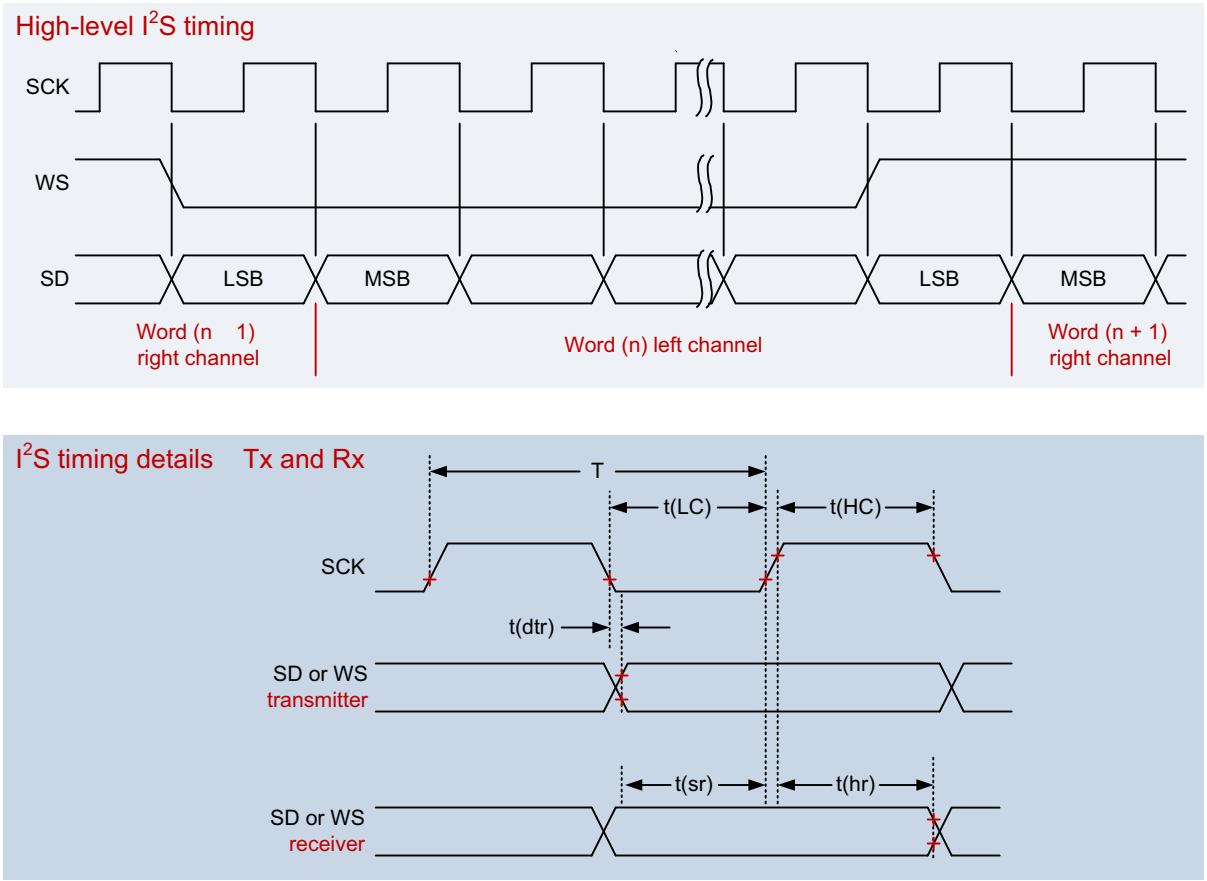

Figure 3-9 I²S timing diagram

Table 3-24 I²S interface timing

Parameter		Comments [1] [2]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

1. Load capacitance is between 10 pF and 40 pF
2. Not all MI²S ports support 24.576 MHz clock frequency. See *Section MI2S/PCM/TDM Interface* in *SM8350 Digital Baseband Design Guidelines/Training Slides* (80-PN145-5) for more information

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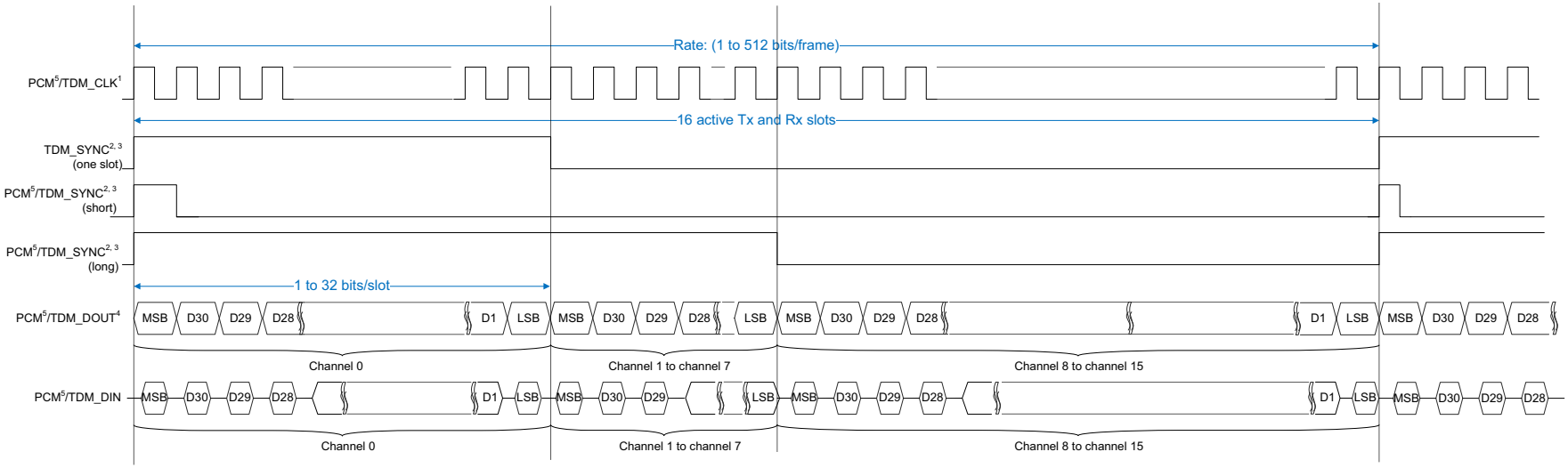
3.10.11 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-10 PCM/TDM audio format with different sync modes

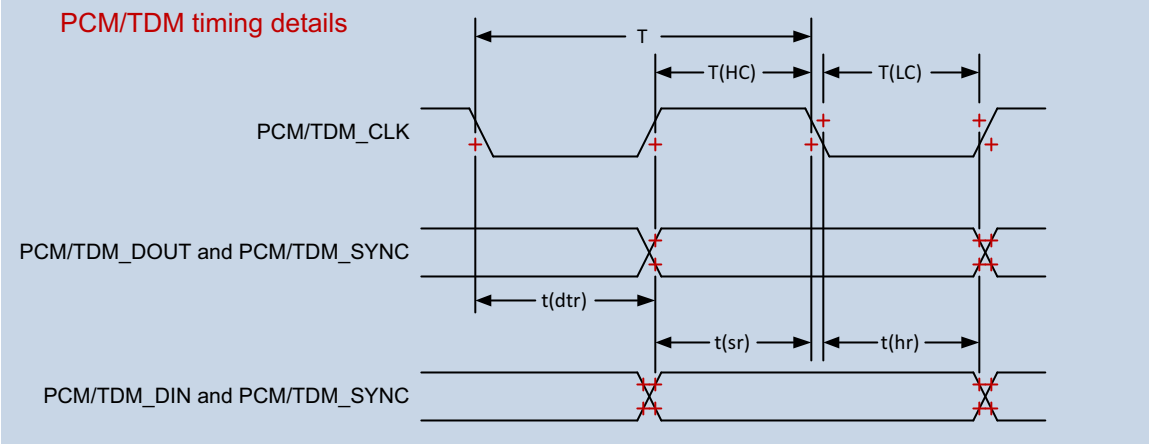


Figure 3-11 PCM/TDM timing diagram

Table 3-25 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns
Slave mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns

1. Load capacitance is between 10 pF to 40 pF.
2. End-to-end testing for the TDM clock is completed up to 12.288 MHz.

3.10.12 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.10.13) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.13 I2C/I3C interface

Table 3-26 Supported I2C/I3C standards and exceptions

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.10.14 Serial peripheral interface

The SM8350 supports SPI as a master only. Any one of the 20 QUP ports can be configured as an SPI master.

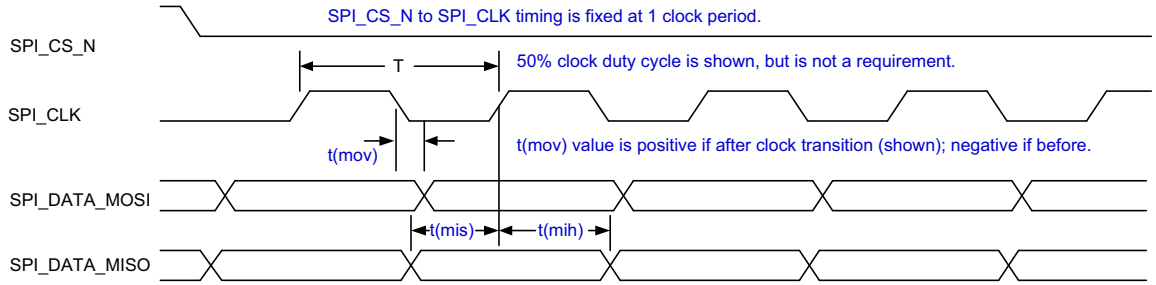


Figure 3-12 SPI master timing diagram

Table 3-27 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz CXO input

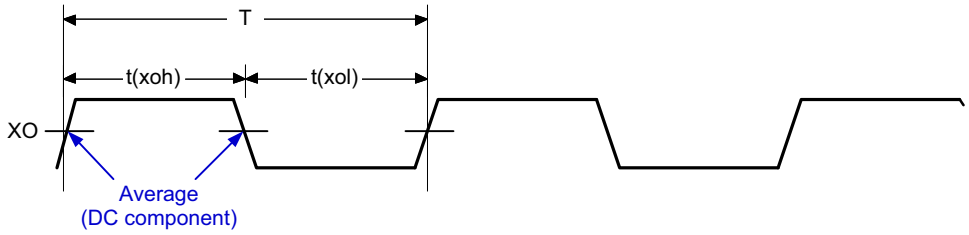


Figure 3-13 XO timing parameters

Table 3-28 CXO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See *Section 3.6.2 38.4 MHz XO crystal requirements* of *PMK8350/PMK65 Data Sheet* (80-PT197-1) for more information.

3.11.1.2 Sleep clock

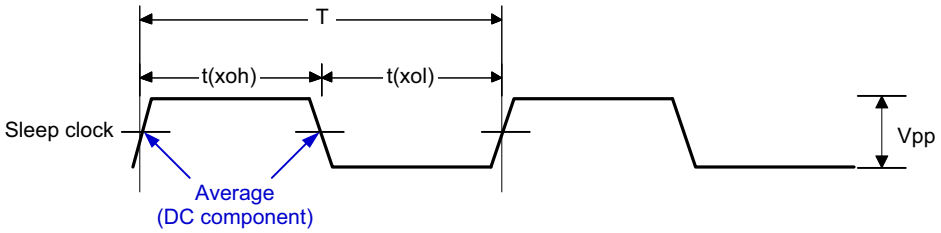


Figure 3-14 Sleep-clock timing parameters

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Table 3-29 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.521	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

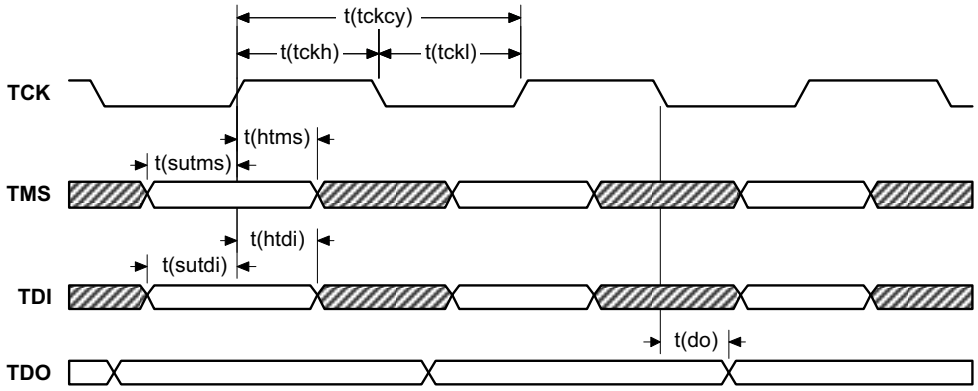

Figure 3-15 JTAG interface timing diagram

Table 3-30 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.11.4 SWD

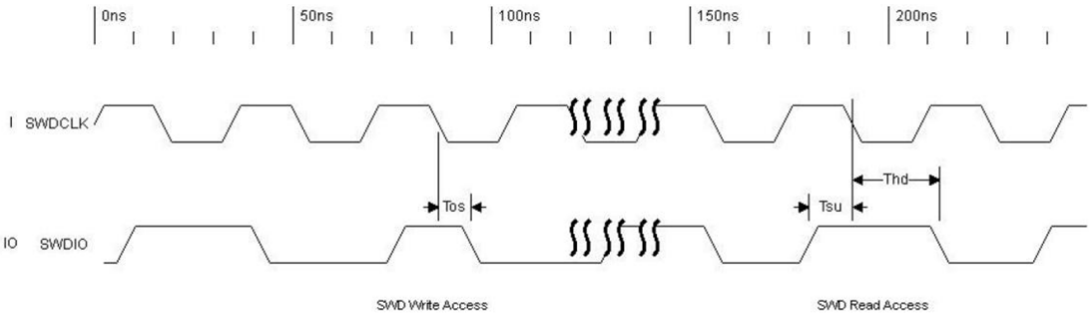

Figure 3-16 SWD write and read AC timing diagram

Table 3-31 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

Note: SWDCLK runs at 20 MHz or lower.

3.12 Power management interface

The digital I/Os must meet the logic-level requirements specified in Section 3.6.

3.12.1 System power management interface (SPMI)

Table 3-32 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SM8350 is available in the MPSP1393 that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The MPSP1393 has a 14.3 mm by 14 mm body, with a maximum height of 0.54 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the MPSP1393 outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download the *Package Outline Drawing, MPSP1393, 14.0 × 14.3 × 0.54 mm, ST90, M147, SB118, PB 496NSP, PL1, MEP* (NT90-PP665-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PP665-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the accurate ball location. To download this text file, search for the NT90 in CreatePoint, and click the appropriate link in the **Related Files** line that is located directly underneath the PDF link.

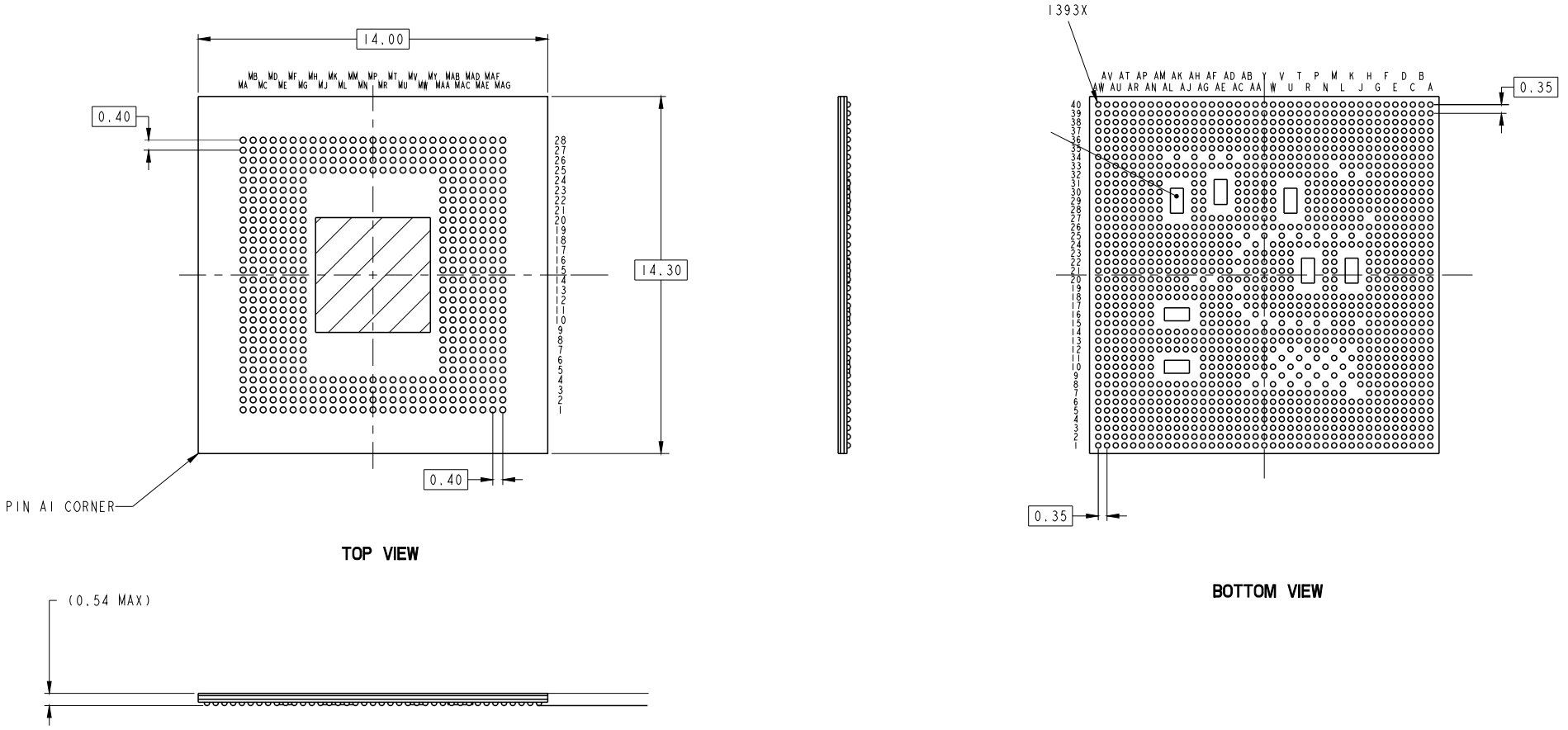

Figure 4-1 MPSP1393 outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

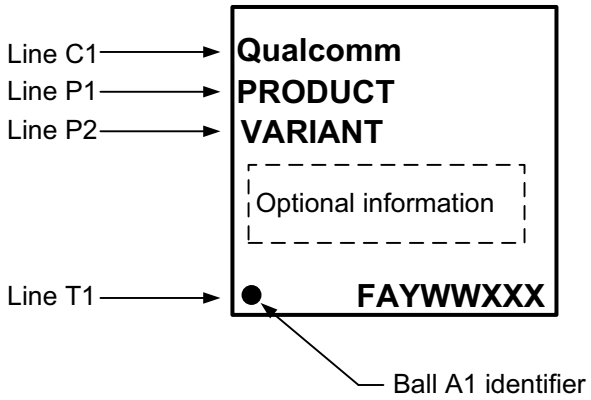

Figure 4-2 SM8350/SM8350P device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm company name
P1	PRODUCT	QTI product name ■ SM8350 ■ SM8350P
P2	VARIANT	PRR-BB ■ See Table 4-4 for the assigned values.
	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ■ F = J (Samsung) A = assembly site code ■ A = C (Amkor, Korea) ■ A = X (Shinko, Japan) Y = single/last digit of year WW = two digit work week of current year XXX = serial number
	●	Ball A1 indicator

NOTE: For complete marking definitions of all SM8350/SM8350P variants and revisions, see the *SM8350/SM8350P Device Revision Guide* (80-PN145-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 Related register (0x00780178)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining the feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example 1	SM-8350	-1	-MPSP	1393			-TR	-00	-0	-AB

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SM-8350-1-MPSP1393-TR-00-0-AB

NOTE: The shipping package is either TR (tape and reel) or MT (matrix tray).

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [1]	FEATURE_ID [2]	Hardware revision number	Source configuration code (S) [3]	Comments	Sample date
SM8350	ES1	100-AB	0x2	0x0 0135 0E1	0	SM8350 (100-0-AB), MPSP1393, LPDDR5, Gold Prime at 2.842 GHz	03/31/2020
SM8350	ES2	101-AB	0x0	0x1 0135 0E1	0	SM8350 (101-0-AB), MPSP1393, LPDDR5, Gold Prime at 2.842 GHz	6/19/2020
SM8350	ES3	103-AB	0x0	0x3 0135 0E1	0	SM8350 (103-0-AB), MPSP1393, LPDDR5, Gold Prime at 2.842 GHz	7/31/2020
SM8350	CS [4]	103-AB CS date codes are as follows: ■ Amkor: 038 ■ Shinko: 038	0x0	0x3 0135 0E1	0	SM8350 (103-0-AB), MPSP1393, LPDDR5, Gold Prime at 2.842 GHz	9/30/2020
SM8350	ES	903-AC	0xF	0x3 0135 0E1	0	SM8350 (903-0-AC), MPSP1393, LPDDR5, Gold Prime at 2.995 GHz	02/26/2021
SM8350	CS [4]	903-AC CS date codes are as follows: ■ Amkor: 121 ■ Shinko: 121	0xF	0x3 0135 0E1	0	SM8350 (903-0-AC), MPSP1393, LPDDR5, Gold Prime at 2.995 GHz	06/15/2021
SM8350P	ES	000-AB	0x0	0x0 0142 0E1	0	SM8350P, MPSP1393, LPDDR5, no modem, Gold Prime at 2.842 GHz	05/29/2020
SM8350P	ES2	003-AB	0x0	0x3 0142 0E1	0	SM8350P (003-0-AB), MPSP1393, LPDDR5, no modem, Gold Prime at 2.842 GHz	7/31/2020
SM8350P	CS [4]	003-AB CS date codes are as follows: ■ Amkor: 037 ■ Shinko: 037	0x0	0x3 0142 0E1	0	SM8350P (003-0-AB), MPSP1393, LPDDR5, no modem, Gold Prime at 2.842 GHz	9/30/2020

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. See Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
3. S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-5.
4. Devices shipped after the CS sample date represent CS quality material. ES material may be shipped post CS sample date upon customer request.

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Table 4-5 Source configuration codes

S value	Die	F value = J
0	Digital	Samsung

4.3.2 Daisy chain devices

The SM8350 daisy chain ordering part numbers are TBD.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SM8350/SM8350P rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SM8350/SM8350P devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the
SM8350 LPDDR5 8GB PACKAGE THERMAL MODEL ICEPAK (HS11-PN145-5HW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PN145-5HW
SM8350 LPDDR5 8GB PACKAGE THERMAL MODEL FLOTHERM (HS11-PN145-6HW)
https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PN145-6HW

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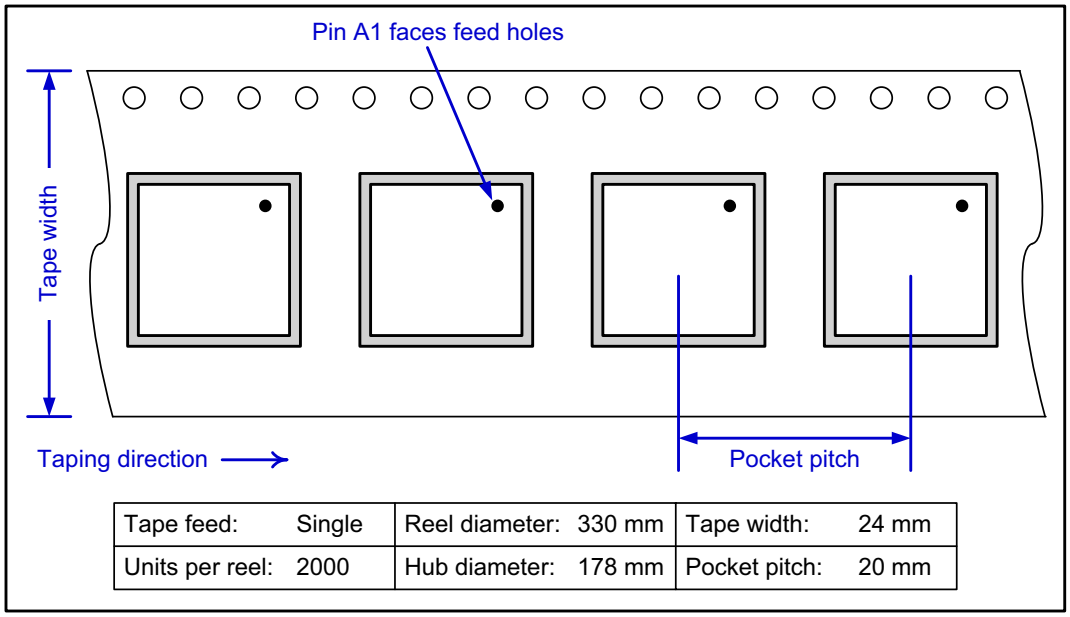
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SM8350 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

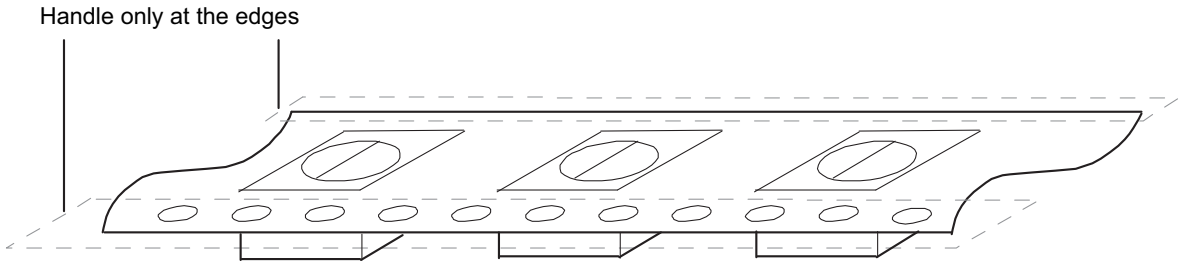


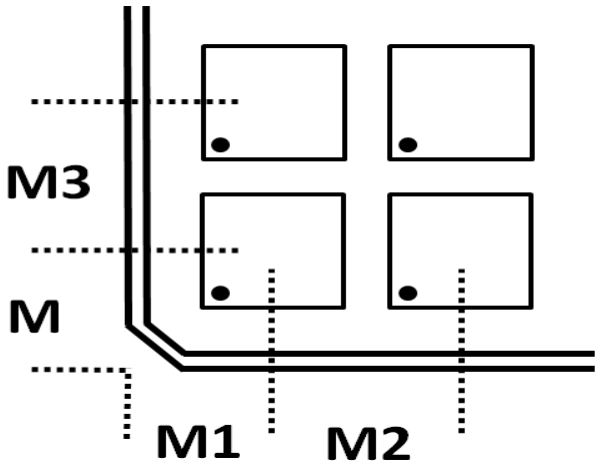
Figure 5-2 Tape handling

5.1.2 Matrix tray information – available for sample material only

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	7 x 17 (119)
M	12.90 mm
M1	12.70 mm
M2	18.10 mm
M3	18.35 mm

Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Storage

5.2.1 Bagged storage conditions

SM8350 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SM8350 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SM3250 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

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6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualification summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	574	Pass
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	312	Pass FIT < 100
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	312	Pass > 10
ESD ─ Human body model (HBM) rating per JS001 (Total samples from one wafer lot)	21	Pass; 1 kV
ESD ─ Charged device model (CDM) rating per C101 (Total samples from one wafer lot) All pins passed +/-250 V except EBI and QLINK_UL passed – 200 V	3	Pass; ± 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 105°C (Total samples from one wafer lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 95°C (Total samples from one wafer lot)	6	Pass

Table 7-2 SM8350-LPDDR5 package reliability results

Tests, standards, and conditions	Amkor Korea sample size	Shinko Japan sample size	Results
Moisture resistance test (MRT): J-STD-020D Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 700 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning**: JESD22-A113-H MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hours duration **Preconditioning:** JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C Total samples from three different assembly lots	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hours duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	See note
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder bump shear (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder ball shear: JESD22-B117 (Total samples from three different assembly lots at each SAT)	15	15	Pass
Internal/external visual (Total samples from three different assembly lots at each SAT)	15	15	Pass

7.2 Device characteristics

Table 7-3 Device characteristics

Device name	SM8350
Package type	MPSP1393
Package body size	14.0 mm × 14.3 mm × 0.54 mm
Lead composition	SAC125/Ni
Fab process	5 nm
Fab sites	Samsung
Assembly sites	■ Amkor, Korea ■ Shinko, Japan
Solder ball pitch	0.35 mm

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8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	September 2019	Initial release
B	November 2019	■ Replaced SDR735 with SDR865 in Figure 1-1 SM8350 functional block diagram and example application and Table 1-1 SM8350 features ■ Updated the cover diagram and Figure 1-1 SM8350 functional block diagram and example application and Table 1-1 SM8350 features to remove the second instance of UFS ■ Updated pin information in the following pin tables and pin maps: □ Figure 2-2 SM8350 bottom pin assignments □ Figure 2-3 SM8350 LPDDR5 top pin assignments □ Figure 2-4 SM8350 LPDDR4X top pin assignments □ Table 2-2 Bottom pin descriptions – general pins □ Table 2-3 Bottom pin descriptions – general-purpose input/output ports □ Table 2-6 Bottom pin descriptions: ground, DNC, and power-supply pins □ Table 2-7 Top pin descriptions – LPDDR5 general pins □ Table 2-8 Top pin descriptions – LPDDR5 ground, NC, reserved, and power-supply pins □ Table 2-9 Top pin descriptions – LPDDR4X general pins □ Table 2-10 Top pin descriptions – LPDDR4X ground, NC, reserved, and power-supply pins ■ Added pin information, inserting Table 2-4 QUP lane to function mapping and Table 2-5 QUP engine to function mapping ■ Added NT90 information and outline drawing in Section 4.1 Device physical dimensions ■ Global: Clarified the package type
C	December 2019	■ Figure 1-1 SM8350 functional block diagram and example application: Added QET6110 and corrected the signal connection to the QET block ■ Table 2-2 Bottom pin descriptions – general pins: Corrected the AW19 pin name ■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: Corrected the alternate function pin names for GPIOs 168 to 181 ■ Table 2-4 QUP lane to function mapping: Corrected the QUP table
D	February 2020	■ Chapter 2 Pin definitions: Updated the document number and document download link of pin assignment and GPIO configuration spreadsheet ■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: Updated the alternate functions for GPIO_92, GPIO_94 to GPIO_99, GPIO_153, and GPIO_154 ■ Table 3-1 PDN specifications for core rails: Added this table ■ Table 3-2 PDN specifications–SerDes rails: Added this table

Revision	Date	Description
E	March 5, 2020	■ Table 2-5 QUP engine to function mapping: Updated QUP_9 for I3C support ■ Table 3-1 PDN specifications for core rails: Updated the table header and added note 2 ■ Table 3-2 PDN specifications–SerDes rails: Updated this table ■ Table 3-3 PDN specifications–DDR rails: Added this table
F	March 10, 2020	■ Global: Removed LPDDR4X related information across the document ■ Table 3-2 PDN specifications–SerDes rails: Updated the power domain
G	April 2020	■ Section 3.1 Absolute maximum ratings: Added this section ■ Section 3.2 Operating conditions: Added this section ■ Table 3-3 PDN specifications for core rails: Updated the positive pin of VDD_LPI_CX and updated the power domain of U335 ■ Table 3-5 PDN specifications–DDR rails: Swapped the positive pins of VDD_A_PLL_EBI2, VDD_A_EBI2 ■ Section 4.2 Part marking: Added this section ■ Section 4.3 Device ordering information: Added this section ■ Section 4.4 Device moisture sensitivity level: Added this section ■ Section 4.5 Thermal characteristics: Added this section ■ Chapter 5 Carrier, storage, and handling information: Added this chapter ■ Chapter 6 PCB mounting guidelines: Added this chapter
H	June 2020	■ Global: Updated the document for SM8350P ■ Table 1-1 SM8350/SM8350P features: □ Updated the memory speed □ Replaced QFS2530 with QFS2630 ■ Figure 1-1 SM8350/SM8350P functional block diagram and example application: Updated the block diagram ■ Table 3-2 Operating conditions for non AVS voltage rails: Updated the USB HS core circuit specification ■ Table 3-6 Battery pack and VBATT PDN specifications: Added this table ■ Table 3-7 VPH_PWR PDN specifications – PM8350: Added this table ■ Table 3-8 VPH_PWR PDN specifications – PM8350C: Added this table ■ Table 3-9 VPH_PWR PDN specifications – PMR735A: Added this table ■ Table 4-4 Device identification details: Updated the device identification details
Revision I was omitted in accordance with QTI document conventions		

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Revision	Date	Description
J	September 2020	■ Table 1-1 SM8350/SM8350P features: Updated the CPU and GPU frequency details. Also updated the WLAN/BT/FM feature. ■ Table 3-2 Operating conditions for voltage rails with AVS Type-1: Updated the specification values ■ Table 3-3 Operating conditions for non AVS voltage rails: Updated the specification values ■ Section 3.3 Power delivery network specification: Updated this section ■ Section 3.4 Average operating current: Added this section ■ Section 3.5 Dhrystone and rock bottom maximum power: Added this section ■ Section 3.6 Digital logic characteristics: Added this section ■ Section 3.7 Timing characteristics: Added this section ■ Section 3.8 Memory support: Added this section ■ Section 3.9 Multimedia: Added this section ■ Section 3.10 Connectivity: Added this section ■ Section 3.11 Internal functions: Added this section ■ Section 3.12 Power management interface: Added this section ■ Table 4-4 Device identification details: Updated the device identification details for CS samples ■ Section 5.1.2 Matrix tray information – available for sample material only: Updated the matrix tray information to clarify that it is available for sample material only. ■ Chapter 7 Part reliability: Added this chapter
K	October 9, 2020	■ Table 3-24 *SPI master timing characteristics*: Updated the minimum and maximum value of t(mis) and t(mih)
L	October 29, 2020	■ Table 4-4 Device identification details: Updated assembly site date codes for CS ■ Table 7-1 Silicon reliability results: Added final qualification results ■ Table 7-2 SM8350-LPDDR5 package reliability results: Added final qualification results
M	November 2020	■ Cover: Updated the Kryo CPU ■ Figure 1-1 SM8350/SM8350P (SDR868) functional block diagram and example application: Updated the figure title and Kryo CPU ■ Figure 1-2 SM8350/SM8350P (SDR735) functional block diagram and example application: Added this figure ■ Table 1-1 SM8350/SM8350P features: □ Updated the Quad low-power Kryo Silver cores for AB variant □ Updated the supported RF
N	December 17, 2020	■ Figure 1-2 SM8350/SM8350P (SDR735) functional block diagram and example application: Updated the Kryo CPU ■ Table 1-1 SM8350/SM8350P features: □ Updated the Kryo cores for SM8350 AC variant □ Updated the GPU frequency for SM8350 AC variant ■ Table 4-4 Device identification details: Updated this table for AC variant
Revision O was omitted in accordance with QTI document conventions		
P	December 22, 2020	■ Table 4-4 Device identification details: Updated the ES date of AC variant to be TBD. For sampling date information, contact QTI business team
Revision Q was omitted in accordance with QTI document conventions		
R	January 11, 2021	■ Table 7-1 Silicon reliability results: Updated the sample size
Revision S was omitted in accordance with QTI document conventions		

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Revision	Date	Description
T	January 25, 2021	■ Table 1-1 SM8350/SM8350P features: Updated the GPU frequency and DSP details ■ Table 4-4 Device identification details: Added the Kryo Gold Prime Fmax values
U	February 2021	■ Table 2-3 Bottom pin descriptions – general-purpose input/output ports: Updated the configurable function for GPS control signal (GPIO_155, GPIO_156, and GPIO_157) ■ Table 3-4 Dhrystone and rock bottom maximum power: Updated this table for AB and AC variants ■ Table 4-4 Device identification details: Updated the device identification details for SM8350 AC variant
V	March 2021	■ Table 3-5 DC specification of 1.8 V GPIOs: Updated the table footnote
W	May 2021	■ Table 1-1 SM8350/SM8350P features: Updated the Kryo Gold Prime frequency for SM8350 AC variant ■ Table 4-4 Device identification details: Updated the device identification details for CS samples of SM8350 AC variant and updated the Kryo Gold Prime frequency for AC variant
Revision X was omitted in accordance with QTI document conventions		
Y	June 2021	■ Table 1-1 *SM8350/SM8350P features*: Updated the Kryo Gold Prime frequency for SM8350 AC variant ■ Table 3-9 *UIM 3 V mode DC specifications (VDD_PX_5 and VDD_PX_6)*: Added this table ■ Table 3-10 *UIM 1.8 V mode DC specifications (VDD_PX_5 and VDD_PX_6)*: Added this table ■ Section 3.10.6 *UIM interface*: Added this section ■ Table 4-4 *Device identification details*: Updated the CS date code and Kryo Gold Prime frequency for AC variant

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For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

Document release date: July 1, 2021

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