PM8350B/PM8350BH/PM8350BHS

Data Sheet

80-PT205-1 Rev. H

Device description

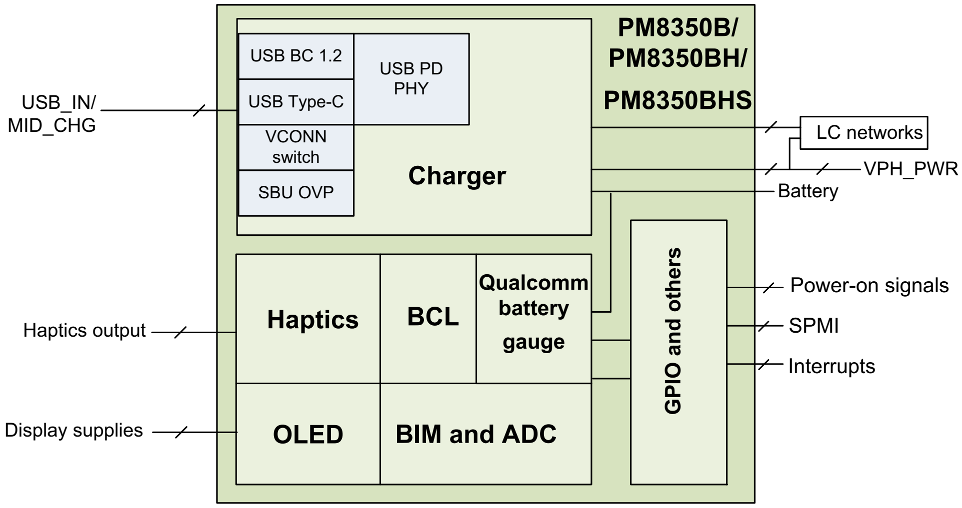
The PM8350B/PM8350BH/PM8350BHS interface PMIC, supplements the master core PM8350 PMIC and the slave core PM8350C PMIC to integrate all wireless handset power management, general housekeeping, and user interface support functions into an integrated three-IC solution.

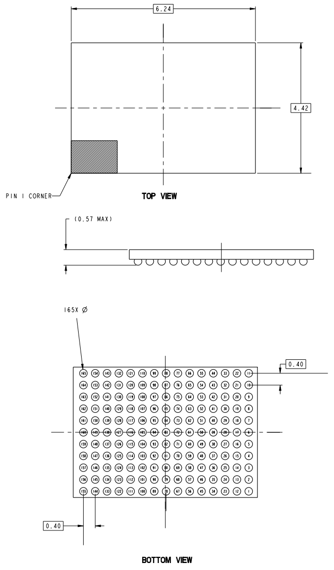
- Best in class high-efficiency 6 A 3-level buck/Div2 charge pump combination architecture Li-ion battery charger (> 97% peak efficiency)
- Dedicated paths for USB and wireless charging with charger operation up to 21.5 V (25 V absolute max)
- Supports up to a 6 A charge current (single path) and a 12 A charge current (dual path using SMB1396/SMB1398 companion ICs)
- Supports *USB Type-C Specification* Rev. 1.4 and *USB Power Delivery Specification* Rev. 3.0
- Supports Qualcomm® Quick Charge™ 2.0, Quick Charge 3.0, and Quick Charge 4.0 technology
- Supports 2S battery with charge balancing (SMB1399 needed). See Section 1.3 for details.
- Simultaneous wireless charging and OTG support using external 5 V boost
- Simultaneous USB charging and reverse wireless charging support using external 5 V boost

Key features (see Section 1.2 for details)

- Qualcomm battery gauge with improved SoC accuracy
- Analog-to-digital converter (ADC) subsystem with analog multiplexer (AMUX) and voltage/current analog-to-digital converter (VADC/IADC)
- Battery interface module (BIM) that includes battery serial interface (BSI) or PMIC serial interface (PSI) and battery missing detection (BMD)
- Battery current limiting (BCL) subsystem that provides both hardware and software alarms, which are used by the system for reducing battery current.
- Triple supply high performance and high efficiency boost regulators for OLED panels
- LDO supply for DDIC digital power
- Full H-bridge haptics driver with dedicated 5 V to 10 V programmable boost for LRA application and SoundWire interface. See Section 1.3 for details.
- SPMI interface
- Eight GPIOs
- 165-pin fan-out wafer-level nanoscale package (165 FOWNSP)

PM8350B/PM8350BH/PM8350BHS high-level block diagram and 165 FOWNSP package drawing





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1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

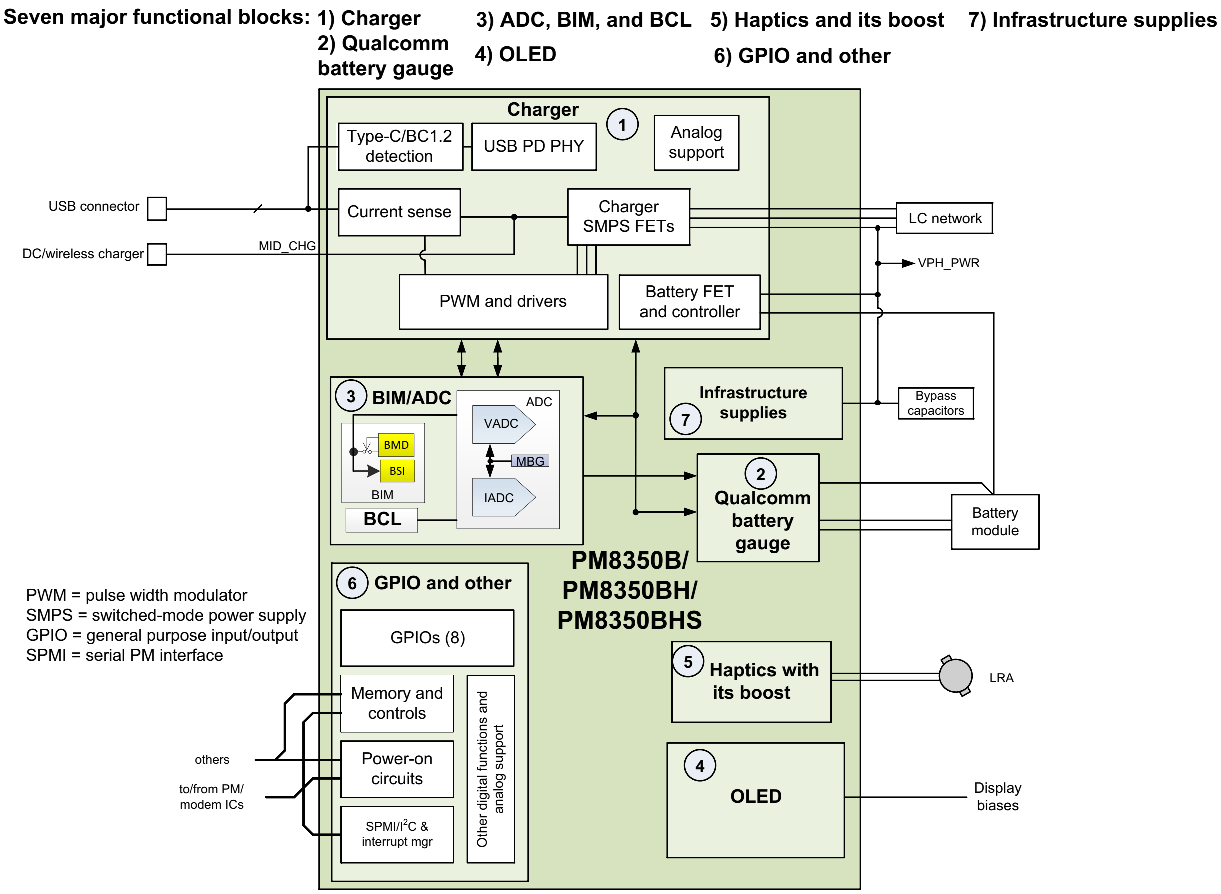


Figure 1-1 PM8350B/PM8350BH/PM8350BHS high-level functional block diagram

1.2 PM8350B/PM8350BH/PM8350BHS features

NOTE: Some hardware features integrated within the PM8350B/PM8350BH/PM8350BHS device must be enabled through the IC software. See the latest revision of the applicable software release notes to identify the enabled PMIC features.

Table 1-1 PM8350B/PM8350BH/PM8350BHS features

Feature	PM8350B/PM8350BH/PM8350BHS capability
Charger	
Battery charger	■ High-efficiency 6 A 3-level buck/ Div2 charge pump combination architecture Li-ion battery charger □ Extremely low Rds(on) MOSFETs minimizing power dissipation during charging □ > 97% peak efficiency ■ Dedicated charging paths for USB and wireless charging with +3.6 V to +21.5 V operating range and absolute maximum voltage of +25 V ■ Automatic USB/wireless input path selection and priority ■ USB charging input path □ 10 mΩ FP FET to minimize power loss during high current charging □ USB Type-C CC logic compliant to the *USB Type-C Specification* Rev. 1.4. □ VCONN switch capable of delivering 1.5 W for DisplayPort alt-mode □ USB power delivery PHY hardware compliant to *USB Power Delivery Specification* Rev. 3.0 □ Quick Charge 2.0 and Quick Charge 3.0 hardware support; Quick Charge 4.0 software support □ Automatic power source detection (APSD) per the *USB Battery Charging Specification* Rev. 1.2 □ Automatic input current limit (AICL) for universal USB adapter compatibility ■ Wireless charging input path □ 20 mΩ FP FET to sense input current □ Automatic input current limit (AICL) to detect input collapse

Table 1-1 PM8350B/PM8350BH/PM8350BHS features (cont.)

Feature	PM8350B/PM8350BH/PM8350BHS capability
Battery charger (continued)	■ 6 A charge current (single path) and 12 A charge current (dual path using SMB1396/SMB1398 companion ICs) ■ Support 2S battery with charge balancing (SMB1399 needed) See Section 1.3 for details. ■ Simultaneous wireless charging and OTG support using external 5 V boost ■ Simultaneous USB charging and reverse wireless charging support using external 5 V boost ■ Battery interface □ 5 mΩ integrated BATFET with soft start for optimal charging efficiency and battery life □ Input/output CurrentPath control allows system operation with deeply discharged/missing battery □ Battery supplemental mode (BSM) to allow battery to supplement system current exceeding what the charger buck can provide □ Differential battery voltage Kelvin sensing to compensate for the IR drop caused by the phone PCB and battery pack protection FETs to prolong CC charging and reduce the total charging time □ JEITA battery temperature management and JISC 8714 support □ Battery-missing detection options (in the battery interface module) □ Ship-mode and AFP mode ■ Intelligent charging control and thermal management □ Hardware autonomous charging □ Trickle charger □ Hardware-controlled thermal loop manages input current limit based on the die temperature
Qualcomm battery gauge	
Qualcomm battery gauge	■ Improved SoC accuracy ■ Qualcomm battery gauge is a hybrid of voltage and current based SoC with optimum linear parameter estimation using extended Kalman filtering ■ 2S battery support, with charge balancing. See Section 1.3 for details. ■ SMB parallel charging current sensing through ICHG pins ■ BAT_THERM IR compensation eliminates variation of BAT_THERM reading with varying charge/discharge currents ■ Simplified hardware architecture with reduced states and easy configurability ■ Online battery ESR and Rslow estimation
BIM and ADC	
BIM	■ BIM module includes the battery serial interface (BSI) or PMIC serial interface (PSI) and battery missing detection (BMD) hardware ■ BSI is a single-wire interface that can communicate with external hardware using the MIPI-BIF protocol. ■ BMD is a hardware that detects battery removal in all modes (on, off, sleep)

Table 1-1 PM8350B/PM8350BH/PM8350BHS features (cont.)

Feature	PM8350B/PM8350BH/PM8350BHS capability
On-chip ADC	■ The ADC subsystem includes signal multiplexing and voltage analog-to-digital converter (VADC) ■ Support for 2S battery - 1/6 divider for higher voltage levels, mid-node monitoring, charge balancing FETs. See Section 1.3 for details. ■ A dedicated internal 1.875 V LDO used to bias the VADC and pull-up resistors ■ Parallel hardware interface to arbitrate ADC requests from multiple clients (Qualcomm battery gauge, charger, and BCL) ■ Qualcomm battery gauge and BCL requires Vbatt and Ibatt ■ Charger requires USB and DC input levels, thermistor values, and Vbatt/Ibatt
OLED	
Display supplies	■ Triple supply high performance and high efficiency boost regulators for OLED panels ■ 4.6 V to 5.2 V ELVDD boost regulator ■ -0.8 V to -6.6 V ELVSS inverting regulator (dual phase) ■ 5.0 V to 8 V OLEDB boost regulator ■ 2x pin controls to change regulator voltages and control features. Fully programmable scheme to map rising edges on control pin to regulator voltage control ■ 1.2 V LDO supply for optimizing DDIC digital power
Haptics	
Haptics boost and driver	■ Full H-bridge haptics driver with dedicated 5 V to 10 V programmable boost for LRA applications. See Section 1.3 for details. ■ SoundWire interface with LPASS ■ 640 sample FIFO for pattern generation ■ Hardware-based arbitration for multiple haptics requests ■ Closed loop braking ■ Off-mode vibration and virtual key support
GPIO and other pins	
IC-level interfaces	
Primary status and control	■ Two-line serial power management interface (MIPI SPMI) ■ Supported by SPMI
Interrupt managers	■ PBS 3.0 with one-time programmable (OTP) memory and user programmable
Programmable boot sequence	■ RAM for customizable power-on, power-off, and reset sequences
Configurable I/Os	
General-purpose input/output (GPIO) pins	■ Eight GPIO pins, configurable as digital inputs or outputs ■ Some GPIOs have primary/alternate functions for IC-level interfacing or required controls for user interface functions if those UI functions are used.
Internal clocks	Internal 19.2 MHz RC clock
Package	
Size	6.24 × 4.42 × 0.57 mm
Pin count and package type	165-pin FOWNSP (0.40 mm pitch)

1.3 PM8350B SKUs

PM8350B has the following three SKUs: PM8350B, PM8350BH, and PM8350BHS.

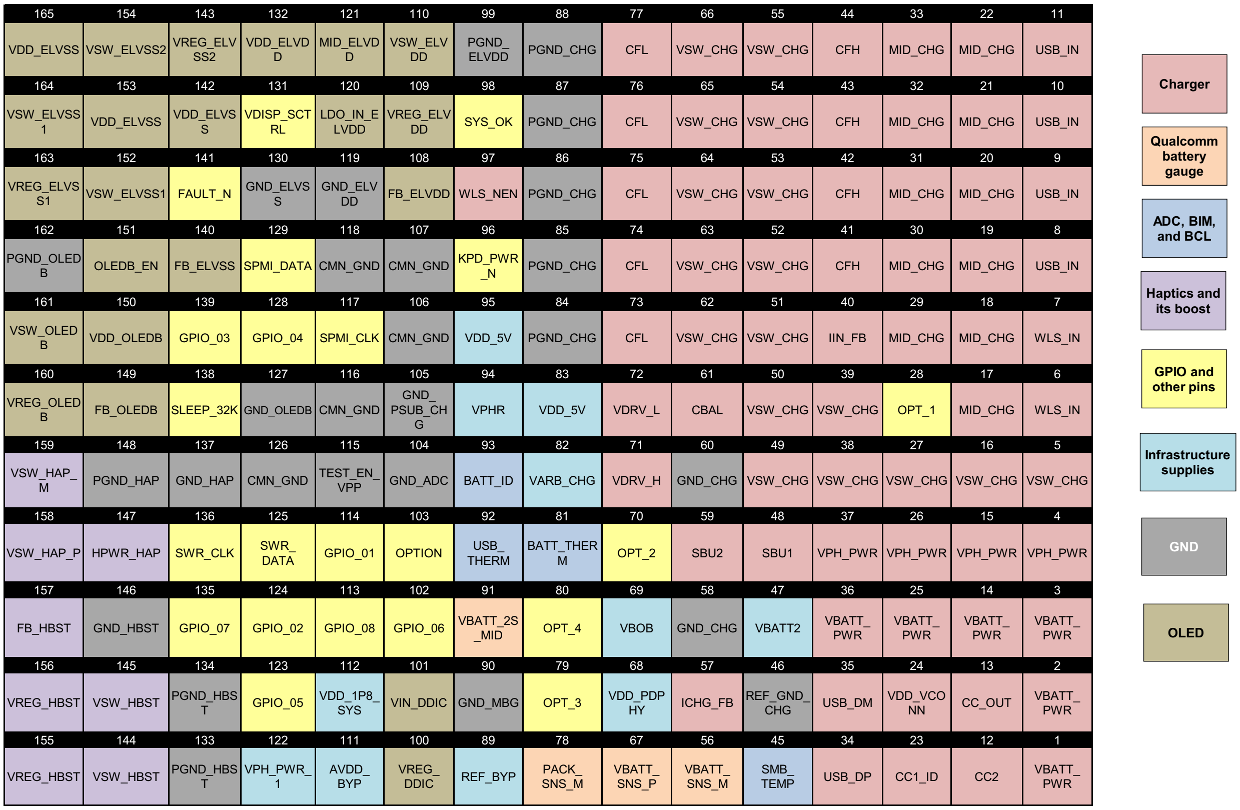
The table below lists the differences between the three SKUs.

SKU	Haptics boost support [1]	Battery charging support
PM8350B	5 V	1S only
PM8350BH	5 V to 10 V	1S only
PM8350BHS [2]	5 V to 10 V	2S only

1. PM8350B uses 2.2 μH inductor for haptics boost. PM8350BH/BHS uses 1 μH inductor for haptics boost.
2. PM8350BHS is not PoR for SM8350 chipset. OEMs can contact QTI if they intend to use PM8350BHS on SM8350 chipset.

2 Pad definitions

The PM8350B/PM8350BH/PM8350BHS is available in the 165 FOWNSP – see Chapter 4 for package details. A high-level view of the pad assignments is shown in Figure 2-1.



165	154	143	132	121	110	99	88	77	66	55	44	33	22	11
VDD_ELVSS	VSW_ELVSS2	VREG_ELVSS2	VDD_ELVDD	MID_ELVDD	VSW_ELVDD	PGND_ELVDD	PGND_CHG	CFL	VSW_CHG	VSW_CHG	CFH	MID_CHG	MID_CHG	USB_IN
164	153	142	131	120	109	98	87	76	65	54	43	32	21	10
VSW_ELVSS1	VDD_ELVSS	VDD_ELVSS	VDISP_SCTRL	LDO_IN_ELVDD	VREG_ELVDD	SYS_OK	PGND_CHG	CFL	VSW_CHG	VSW_CHG	CFH	MID_CHG	MID_CHG	USB_IN
163	152	141	130	119	108	97	86	75	64	53	42	31	20	9
VREG_ELVSS1	VSW_ELVSS1	FAULT_N	GND_ELVSS	GND_ELVDD	FB_ELVDD	WLS_NEN	PGND_CHG	CFL	VSW_CHG	VSW_CHG	CFH	MID_CHG	MID_CHG	USB_IN
162	151	140	129	118	107	96	85	74	63	52	41	30	19	8
PGND_OLEDB	OLEDB_EN	FB_ELVSS	SPMI_DATA	CMN_GND	CMN_GND	KPD_PWR_N	PGND_CHG	CFL	VSW_CHG	VSW_CHG	CFH	MID_CHG	MID_CHG	USB_IN
161	150	139	128	117	106	95	84	73	62	51	40	29	18	7
VSW_OLEDB	VDD_OLEDB	GPIO_03	GPIO_04	SPMI_CLK	CMN_GND	VDD_5V	PGND_CHG	CFL	VSW_CHG	VSW_CHG	IIN_FB	MID_CHG	MID_CHG	WLS_IN
160	149	138	127	116	105	94	83	72	61	50	39	28	17	6
VREG_OLEDB	FB_OLEDB	SLEEP_32K	GND_OLEDB	CMN_GND	GND_PSUB_CHG	VPHR	VDD_5V	VDRV_L	CBAL	VSW_CHG	VSW_CHG	OPT_1	MID_CHG	WLS_IN
159	148	137	126	115	104	93	82	71	60	49	38	27	16	5
VSW_HAP_M	PGND_HAP	GND_HAP	CMN_GND	TEST_EN_VPP	GND_ADC	BATT_ID	VARB_CHG	VDRV_H	GND_CHG	VSW_CHG	VSW_CHG	VSW_CHG	VSW_CHG	VSW_CHG
158	147	136	125	114	103	92	81	70	59	48	37	26	15	4
VSW_HAP_P	HPWR_HAP	SWR_CLK	SWR_DATA	GPIO_01	OPTION	USB_THERM	BATT_THERM	OPT_2	SBU2	SBU1	VPH_PWR	VPH_PWR	VPH_PWR	VPH_PWR
157	146	135	124	113	102	91	80	69	58	47	36	25	14	3
FB_HBST	GND_HBST	GPIO_07	GPIO_02	GPIO_08	GPIO_06	VBATT_2S_MID	OPT_4	VBOB	GND_CHG	VBATT2	VBATT_PWR	VBATT_PWR	VBATT_PWR	VBATT_PWR
156	145	134	123	112	101	90	79	68	57	46	35	24	13	2
VREG_HBST	VSW_HBST	PGND_HBST	GPIO_05	VDD_1P8_SYS	VIN_DDIC	GND_MBG	OPT_3	VDD_PDPHY	ICHG_FB	REF_GND_CHG	USB_DM	VDD_VCONN	CC_OUT	VBATT_PWR
155	144	133	122	111	100	89	78	67	56	45	34	23	12	1
VREG_HBST	VSW_HBST	PGND_HBST	VPH_PWR_1	AVDD_BYP	VREG_DDIC	REF_BYP	PACK_SNS_M	VBATT_SNS_P	VBATT_SNS_M	SMB_TEMP	USB_DP	CC1_ID	CC2	VBATT_PWR

Figure 2-1 PM8350B/PM8350BH/PM8350BHS pad assignments (bottom view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pad that handles 10 mA or more of current flow into the device [1]
PO	Power output; a pad that handles 10 mA or more of current flow out of the device [1]
Z	High-impedance (Hi-Z) output
MV	Medium voltage
LV	Low voltage
GNDP	Power ground; a pad that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pads.
GNDC	Common ground; a pad that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates.
GPIO pins, when configured as outputs, have configurable drive strengths that depend upon the GPIO pad's supply voltage. See the electrical specifications in Chapter 3 for details.	

1. The maximum current levels expected on PI and PO type pads are listed in Chapter 3.

2.2 Pad descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Pad descriptions – charger

Table 2-3 Pad descriptions – Qualcomm battery gauge

Table 2-4 Pad descriptions – ADC, BIM, and BCL

Table 2-5 Pad descriptions – OLED

Table 2-6 Pad descriptions – haptics and its boost

Table 2-7 Pad descriptions – GPIO and other pins

Table 2-8 Pad descriptions – infrastructure supplies

Table 2-9 Pad descriptions – ground pads

Table 2-2 Pad descriptions – charger

Pad #	Pad name	Pad type [1]	Functional description
8, 9, 10, 11	USB_IN	PI, PO	USB power input of the charger. One of two potential charger input power sources or output during USB-OTG operation.
6, 7	WLS_IN	PI, PO	Wireless (DC) power input of the charger. One of two potential charger input power sources or output during reverse wireless operation.
97	WLS_NEN	DO	DC/wireless charging output enable/disable pin. Keeps wireless charger output stage disabled (forward voltage blocking) during USB charging.
17, 18, 19, 20, 21, 22, 29, 30, 31, 32, 33	MID_CHG	PI, PO	Mid joint point of QUSB, QWLS, and charger buck input
41, 42, 43, 44	CFH	PI, PO	Flying capacitor high side node
73, 74, 75, 76, 77	CFL	PI, PO	Flying capacitor low side node
71	VDRV_H	PI, PO	Bootstrap capacitor high-side connection
72	VDRV_L	PI, PO	Bootstrap capacitor low-side connection
61	CBAL	PI, PO	Balance node for flying capacitor
5, 16, 27, 38, 39, 49, 50, 51, 52, 53, 54, 55, 62, 63, 64, 65, 66	VSW_CHG	PI, PO	Charger buck/boost switch node
4, 15, 26, 37	VPH_PWR	PI, PO	System power input/output node
1, 2, 3, 14, 25, 36	VBATT_PWR	PI, PO	Battery power input/output node; connected to pack (+) of battery pack
67	VBATT_SNS_P	AI	Remote sense of the battery cell positive; charger senses battery voltage across VBATT_SNS_P and VBATT_SNS_M
56	VBATT_SNS_M	AI	Remote sense of the battery cell negative; charger senses battery voltage across VBATT_SNS_P and VBATT_SNS_M
40	IIN_FB	AI	Input current feedback signal; input to PMIC charger input current limit control loop
57	ICHG_FB	AI	Charge current feedback signal; input to PMIC charger charge current limit control loop
34	USB_DP	AI, DI, DO	USB D+ signal line for automatic power source detection
35	USB_DM	AI, DI, DO	USB D- signal line for automatic power source detection
23	CC1_ID	AI, DI, DO, PO	USB Type-C CC1 pin
12	CC2	AI, DI, DO, PO	USB Type-C CC2 pin
13	CC_OUT	DO	1.8 V push-pull tri-state output indicating USB Type-C connector orientation (CC1 or CC2 connection)
48	SBU1	AI	USB Type-C SBU1 pin
59	SBU2	AI	USB Type-C SBU2 pin
24	VDD_VCONN	PI	VDD source for VCONN switch; connect to VPH_PWR or VREG_BOB

1. See Table 2-1 for parameter and acronym definitions.

Table 2-3 Pad descriptions – Qualcomm battery gauge

Pad #	Pad name	Pad type [1]	Functional description
67	VBATT_SNS_P	AI	Remote sense of the battery cell positive; Qualcomm battery gauge senses battery voltage across VBATT_SNS_P and PACK_SNS_M
78	PACK_SNS_M	AI	Pack sense minus; connected to pack (-) of battery pack; Qualcomm battery gauge senses battery voltage across VBATT_SNS_P and PACK_SNS_M
91	VBATT_2S_MID	AI	MID of 2S battery pack. Used for cell balancing.

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pad descriptions – ADC, BIM, and BCL

Pad #	Pad name	AMUX channel	Pad type [1]	Functional description
81	BATT_THERM	AMUX_THM1	AI	Battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and battery gauge.
93	BATT_ID	AMUX_THM2	AI	Battery ID input to ADC and MIPI BIF interface. It can be used for missing battery detection.
45	SMB_TEMP	AMUX_THM3	AI	SMB temp sensor (current) signal input
92	USB_THERM	AMUX_THM4	AI	USB Type-C connector temperature sensor
103	OPTION	AMUX_THM5	AI	Reserved pin (must be left floating)
102	GPIO_06	AMUX_THM6	AI	GPIO input to AMUX
114	GPIO_01	AMUX1_GPIO	AI	GPIO input to AMUX
124	GPIO_02	AMUX2_GPIO	AI	GPIO input to AMUX
139	GPIO_03	AMUX3_GPIO	AI	GPIO input to AMUX
128	GPIO_04	AMUX4_GPIO	AI	GPIO input to AMUX

1. See Table 2-1 for parameter and acronym definitions.

Table 2-5 Pad descriptions – OLED

Pad #	Pad name	Pad type [1]	Functional description
Display driver IC			
101	VIN_DDIC	PI	Power input for DDIC LDO; connects to VREG_S12 of core PMIC
100	VREG_DDIC	PO	Power output of DDIC LDO
Display bias positive			
132	VDD_ELVDD	PI	Display bias positive: supply power input for boost circuits
110	VSW_ELVDD	PI	Display bias positive: boost SMPS switch node
121	MID_ELVDD	PO	Display bias positive: boost SMPS regulated output
109	VREG_ELVDD	PO	Display bias positive: LDO supply power output
108	FB_ELVDD	AI	Display bias positive: boost SMPS sense input
120	LDO_IN_ELVDD	PI	Display bias positive: LDO supply power input

Table 2-5 Pad descriptions – OLED (cont.)

Pad #	Pad name	Pad type [1]	Functional description
Display bias negative			
142, 153, 165	VDD_ELVSS	PI	Display bias minus: supply power input for boost circuits
152, 164	VSW_ELVSS1	PO	Display bias minus: boost SMPS switch node 1
154	VSW_ELVSS2	PO	Display bias minus: boost SMPS switch node 2
163	VREG_ELVSS1	PO	Display bias minus: boost SMPS regulated output 1
143	VREG_ELVSS2	PO	Display bias minus: boost SMPS regulated output 2
140	FB_ELVSS	AI	Display bias minus: boost SMPS sense input
OLED bias			
151	OLEDB_EN	DI	Enable for OLEDB boost driver
150	VDD_OLEDB	PI	Power input for OLEDB boost driver
161	VSW_OLEDB	PO	OLEDB boost SMPS switch node
160	VREG_OLEDB	PO	OLEDB boost power output
149	FB_OLEDB	AI	Feedback sense for OLEDB boost output

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Pad descriptions – haptics and its boost

Pad #	Pad name	Pad type [1]	Functional description
147	HPWR_HAP	PI	Power input for haptics driver
158	VSW_HAP_P	PO	Haptics H-bridge driver output plus
159	VSW_HAP_M	PO	Haptics H-bridge driver output minus
144, 145	VSW_HBST	PO	Haptics boost switch node
155, 156	VREG_HBST	PO	Haptics boost power output
157	FB_HBST	AI	Feedback sense for haptics boost output

1. See Table 2-1 for parameter and acronym definitions.

Table 2-7 Pad descriptions – GPIO and other pins

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
Configurable GPIOs [2] [3]				
114	GPIO_01	 VBATT_2S_MID2 AMUX1_GPIO	MV	Configurable; default digital input with 10 μA pull-down MID2 of 2S battery pack. Used for cell balancing. GPIO input to AMUX

Table 2-7 Pad descriptions – GPIO and other pins (cont.)

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
124	GPIO_02		MV	Configurable; default digital input with 10 µA pull-down
		WLS_THERM		Wireless charging thermistor
		BAT2_THERM		Secondary battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and battery gauge.
		AMUX2_GPIO		GPIO input to AMUX
139	GPIO_03		MV	Configurable; default digital input with 10 µA pull-down
		AMUX3_GPIO		GPIO input to AMUX
128	GPIO_04		MV	Configurable; default digital input with 10 µA pull-down
		AMUX4_GPIO		GPIO input to AMUX
123	GPIO_05		LV	Configurable; default digital input with 10 µA pull-down
102	GPIO_06		LV	Configurable; default digital input with 10 µA pull-down
		EXT_BOOST_EN		External haptics boost enable
		AMUX_THM6		GPIO input to AMUX
		HAP_EXT_TRIG		Haptics external trigger
135	GPIO_07		LV	Configurable; default digital input with 10 µA pull-down
		SMB_EN		SMB charger enable
113	GPIO_08		LV	Configurable; default digital input with 10 µA pull-down
		SMB_SHIP		SMB charger ship mode control
Other pins				
96	KPD_PWR_N		DI	Phone power key for exiting ship mode
98	SYS_OK		DO	System OK or charger detection indicator output (user programmable)
28	OPTION_1		AI	Option pin 1
70	OPTION_2		AI	Option pin 2
79	OPTION_3		AI	Low side external sense positive terminal
80	OPTION_4		AI	Low side external sense negative terminal
117	SPMI_CLK		DI	SPMI communication bus clock signal
129	SPMI_DATA		DI, DO	SPMI communication bus data signal
136	SWR_CLK		DI	MIPI SoundWire clock
125	SWR_DATA		DI, DO	MIPI SoundWire data
131	VDISP_SCTRL		DI	Hardware SWIRE interface AMOLED displays

Table 2-7 Pad descriptions – GPIO and other pins (cont.)

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
138	SLEEP_32K		AI	32 kHz clock from PMK8350
141	FAULT_N		DI, DO	Connects to FAULT_N pin of other PMICs. This signal is used to send/receive the fault condition across all PMICs in the chipset. The driver is an open-drain pull-down. There is an internal 200 kΩ resistive pull-up to DVDD (1.5 V) on this pin.

1. See Table 2-1 for the parameter and acronym definitions.
2. GPIOs may be configured for the following use cases:
   User interface functions
   IC-level interface functions
   General housekeeping functions
   To assign a GPIO to a particular function, identify all of your application's requirements and map each GPIO to its function—carefully avoiding assignment conflicts.
3. No GPIOs are connected to the RRADC. Also, there are no free channels available on the RRADC, because they are all accounted for.

Fixed supply for GPIO_05, GPIO_06, GPIO_07, and GPIO_08:

- 0 and 1 = VDD_1P8_SYS (1.8 V)

For GPIO_01, GPIO_02, GPIO_03, and GPIO_04, options include the following:

- 0 = VPH_PWR_1 (3.6 V nominal)
- 1 = VDD_1P8_SYS (1.8 V)

NOTE: Configure unused GPIOs as digital inputs with their internal pull-downs enabled.

Table 2-8 Pad descriptions – infrastructure supplies

Pad #	Pad name	Pad type [1]	Functional description
89	REF_BYP	AO	Bandgap reference
82	VARB_CHG	PO	Power source arbitration circuit output and must not be used for other purposes
47	VBATT2	PI	VBATT2 powers VARB in a 2S battery system. Connect to 2S battery pack plus in 2S battery system. Connect to VBATT_PWR in 1S system.
69	VBOB	PI	BOB output that powers VARB when battery is low
83, 95	VDD_5V	PO	5 V LDO output supply for the boot-strap capacitor
111	AVDD_BYP	AO	Bypass capacitor for dedicated LDO analog infrastructure circuits. This LDO must only be used for analog infrastructure circuits and must not be used as a general LDO output.
112	VDD_1P8_SYS	PI	1.8 V supply from core PMIC to power I/O
94	VPHR	PI	Connects to VPH_PWR. Powers internal PMIC circuits

Table 2-8 Pad descriptions – infrastructure supplies (cont.)

Pad #	Pad name	Pad type [1]	Functional description
122	VPH_PWR_1	PI	Connects to VPH_PWR. Powers internal PMIC circuits
68	VDD_PDPHY	PI	Power input for the USB PD PHY. Connects to the 3.075 V USB LDO on the core PMIC.

1. See Table 2-1 for the parameter and acronym definitions.

Table 2-9 Pad descriptions – ground pads

Pad #	Pad name	Pad type [1]	Functional description
Common grounds			
58, 60	GND_CHG	GNDC	Ground for ESD cell
105	GND_PSUB_CHG	GNDC	Ground for charger substrate
106, 107, 116, 118, 126	CMN_GND	GNDC	Common ground
137	GND_HAP	GNDC	Ground for haptics controller
146	GND_HBST	GNDC	Ground for haptics boost controller
119	GND_ELVDD	GNDC	Ground for ELVDD controller
127	GND_OLEDB	GNDC	Ground for OLEDB boost controller
115	TEST_EN_VPP	GNDC	Pin must be grounded externally
Special grounds [2]			
90	GND_MBG	GNDC	Bandgap reference ground
46	REF_GND_CHG	GNDC	Quiet reference ground
84, 85, 86, 87, 88	PGND_CHG	GNDP	Power ground for the charger
104	GND_ADC	GNDP	ADC controller ground
99	PGND_ELVDD	GNDP	Power ground for display bias positive: LDO power supply.
148	PGND_HAP	GNDP	Power ground for haptics
133, 134	PGND_HSBT	GNDP	Power ground for haptics boost
130	GND_ELVSS	GNDP	Display bias minus ground and PSUB ground
162	PGND_OLEDB	GNDP	Power ground for OLEDB boost

1. See Table 2-1 for the parameter and acronym definitions.
2. Special grounds may have specific layout requirements for optimum performance.

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Terminal voltage (reference to GND unless otherwise noted)				
USB_IN	USB power input of the charger	-0.3	+25	V
WLS_IN	Wireless (DC) power input of the charger	-0.3	+25	V
MID_CHG [1]	Mid joint point of QUSB, QWLS, and charger buck input	-0.3	+25	V
CFH	Flying capacitor high side node	-0.3	+25	V
VSW_CHG	Charger buck/boost switch node	-0.3	+14	V
CFL	Flying capacitor low side node	-0.3	+14	V
	CFH to VSW_CHG, VSW_CHG to CFL, CFL to PGND	-0.3	+18	V
	VSW_CHG to VPH_PWR	-0.3	+16	V
CBAL	Balance node for flying capacitor	-0.3	+18	V
VDRV_H	Bootstrap capacitor high-side connection			
	Converter not switching	-0.3	+18	V
	Converter switching	-0.3	+27	V
VDRV_L	Bootstrap capacitor low-side connection			
	Converter not switching	-0.3	+18	V
	Converter switching	-0.3	+22	V
CC1_ID, CC2 [1]	USB Type-C CC1/CC2 pins	-0.3	+22	V
SBU1, SBU2 [1]	USB Type-C SBU1/SBU2 pins			
VPH_PWR	System power input/output node (applies to both 1S and 2S application)			
VBATT_PWR	Battery power input/output node (applies to both 1S and 2S application)			
	DC	-0.3	+6	V
	Transient	-0.3	+7	V
VBATT2	Powers VARB node			
	DC	-0.3	+12	V
	Transient	-0.3	+14	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
All other pins		-0.3	Lower of +6 V and (Vxx + 0.5 V) [2]	V
Temperature ratings				
T_s	Storage temperature [3, 4]	-55	+150	°C

1. The device needs to be powered/biased via USB_IN, WLS_IN or > 2.5 V VBATT_PWR before applying voltage on any of the other output I/Os
2. Vxx is USB_IN, WLS_IN, or VBATT_PWR
3. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
4. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage and thermal conditions (Table 3-2). The PM8350B/PM8350BH/PM8350BHS meets all performance specifications listed in Section 3.10 through Section 3.5, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Unit
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +125	°C
Power pads					
USB_IN WLS_IN MID_CHG	USB power input of the charger Wireless (DC) power input of the charger Mid joint point of QUSB, QWLS, and charger buck input				
	1S application	3.7	–	16.5	V
	2S application	3.7	–	21.5	V
VSW_CHG	Charger buck/boost switch node				
	1S application	0	–	9	V
	2S application	0	–	12.5	V
VPH_PWR	System power input/output node (applies to both 1S and 2S application)				
	Steady state	2.5	3.8	5	V
	Short duration VPH excursions beyond normal operating voltage range (< 1ms)	2.1	–	5.25	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ	Max	Unit
VBATT_PWR	Battery power input/output node (applies to both 1S and 2S application)	2.5	3.8	5	V
Infrastructure supplies					
VDD_1P8_SYS	1.8 V supply from core PMIC to power I/O	1.75	–	1.85	V
VDD_xx	All power supply pads not listed elsewhere	2.5	3.8	5	V
Signal pins					
All others	Voltage on any non-power-supply pin	0	–	Lower of +6 V and (Vxx + 0.5 V) [1]	V

1. Vxx is USB_IN, WLS_IN or VBATT_PWR

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default settings.

Table 3-3 DC power supply currents

Parameter	Symbol	Min	Typ	Max	Units
Battery supply current, active mode [1] (1S and 2S application)	IDD_{ACTIVE_BAT}	–	565	848	µA
Charger supply current, active mode (1S and 2S application) [2]	IDD_{ACTIVE_CHG}	–	3965	5948	µA
Battery supply current, sleep mode [3] (1S and 2S application)	IDD_{SLEEP}	–	179	268	µA
Battery supply current, off mode [4]	IDD_{OFF}				
1S application		–	28	42	µA
2S application		–	31	46	µA
Battery supply current, ship mode [5]	IDD_{SHIP}				
1S application		–	13	19	µA
2S application		–	15	23	µA

1. IDD_{ACTIVE_BAT} is the total supply current from a main battery with PM8350B/PM8350BH/PM8350BHS on, Qualcomm battery gauge in active state, charger in standby and OLED, haptics modules are off. XBL has been loaded.
2. IDD_{ACTIVE_CHG} is the total supply current running off the charger with PM8350B/PM8350BH/PM8350BHS on, Qualcomm battery gauge in active state, and OLED, haptics modules are off. XBL has been loaded.
3. IDD_{SLEEP} is the total supply current from a main battery with PM8350B/PM8350BH/PM8350BHS on, Qualcomm battery gauge in low power mode, charger in standby, sleep_b=1 and OLED, haptics modules are off. XBL is loaded and the MPM sleep sequence is executed.
4. IDD_{OFF} is the total supply current from a main battery with PM8350B/PM8350BH/PM8350BHS off. This only applies when the temperature is between -30°C and 60°C.
5. IDD_{SHIP} is the total supply current from a main battery with PM8350B/PM8350BH/PM8350BHS off and in ship mode. BATFET is open. This only applies when the temperature is between -30°C and 60°C.

3.4 Digital logic characteristics

The charger has unique digital signaling characteristics as listed within Section 3.5; all other PM8350B/PM8350BH/PM8350BHS digital I/O characteristics are specified in Table 3-4.

Table 3-4 Digital I/O specifications

Parameter	Symbol	Condition	LLimit	ULimit	Unit
Input voltage, logic high [1]	V_{IH}		0.65 • V_{IO}	V_{IO} + 0.3	V
Input voltage, logic low [1]	V_{IL}		-0.3	0.35 • V_{IO}	V
Output voltage, logic high [1]	V_{OH}	$I_{out} = I_{oh}$	V_{IO} - 0.45	V_{IO}	V
Output voltage, logic low	V_{OL}	$I_{out} = I_{ol}$	0.0	0.45	V
Schmitt trigger hysteresis	V_{HYST}		15	–	mV
Output current, logic high [2]	I_{OH}		3	–	mA
Output current, logic low [2]	I_{OL}		–	-3	mA
Input leakage current, digital input [3]	I_L		-200	+200	nA
Input capacitance, digital input or I/O	C_{IN-D}		–	5	pF

1. V_{IO} = VDD_1P8_SYS, unless otherwise noted.
2. The output current specification applies to all digital outputs unless otherwise specified. It is superseded by specifications on specific pins.
3. GPIOs comply with the input leakage specification when configured either as a digital input or in tri-state mode.

3.5 Charger

T_A = -30°C to +85°C, V_{USB_IN} = +5.0 V, +9.0 V, +12.0 V, +20 V, V_{FLT} = +4.4 V, V_{BATT} = +3.9 V, F_{SW} = 0.533 MHz, unless otherwise noted. All voltages are relative to GND.

3.5.1 Input power specifications

Table 3-5 Input power source control and protection

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input voltage monitoring						
V_{COARSE_DET}/ VLT_VT	USB/WLS input coarse detection threshold	V_{USB_IN}/V_{WLS_IN} rising and falling	0.6	1.0	1.3	V
	Deglitch filter time for USB/WLS_IN I_{PD}	V_{USB_IN}/V_{WLS_IN} falling, extending USB/WLS_IN I_{PD}	–	25	–	ms
	Deglitch filter time for ship mode exit	V_{USB_IN}/V_{WLS_IN} rising	–	25	–	ms
	Deglitch filter time for USB/WLS_LT_VT INT	V_{USB_IN}/V_{WLS_IN} rising and falling	–	1	–	ms

Table 3-5 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{UVLO}	USB/WLS input undervoltage lockout (UVLO) threshold	V_{IN} [1] falling; for LV options	3.5	3.6	3.7	V
		V_{IN} [1] falling; for MV options	6.6	6.9	7.2	V
		V_{IN} [1] falling; for HV options	9.3	9.6	9.9	V
	Hysteresis	V_{IN} [1] rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} and V_{WLS_IN} [1] rising and falling	–	20	–	ms
V_{OVLO}	USB/WLS input overvoltage lockout (OVLO) threshold	V_{IN} [1] rising, for LV options	6.2	6.4	6.6	V
		V_{IN} [1] rising, for MV options	16.5	17	17.5	V
		V_{IN} [1] rising, for HV option 1	13.5	14	14.5	V
		V_{IN} [1] rising, for HV option 2	16.5	17	17.5	V
		V_{IN} [1] rising, for HV option 3	19.5	20	20.5	V
		V_{IN} [1] rising, for HV option 4	21.5	22	22.5	V
	Hysteresis	V_{IN} [1] falling	–	200	–	mV
	Response time [2]	V_{IN} [1] rising at 5 V/µs, HV threshold	–	–	2	µs
		V_{IN} [1] rising at 5 V/µs, LV or MV threshold	–	10	–	ms
	Deglitch filter time	V_{IN} [1] falling	–	100	–	ms
V_{ASHDN}	USB/WLS input auto-shutdown threshold	V_{IN} [1]–V_{SYS}, V_{IN} [1] falling	50	130	190	mV
	Hysteresis	V_{IN} [1] rising	–	80	–	mV
	Deglitch filter time	V_{IN} [1] rising and falling	–	20	–	ms
V_{REVI}	USB/WLS input reverse-current threshold	V_{IN} [1]–V_{SYS}, V_{IN} [1] falling	-70	-130	-190	mV
	Hysteresis	V_{IN} [1] rising	–	80	–	mV
	Deglitch filter time	V_{IN} [1] falling	–	100	–	µs
		V_{IN} [1] rising	–	1	–	ms
Input current limit						
I_{SUSP_USB}	USB_IN suspend mode current	USB_IN path in suspend mode, V_{USB_IN} = 5 V, V_{BAT} = 4.5 V	–	0.5	1.0	mA
		USB_IN path in suspend mode, V_{USB_IN} = 5 V, V_{BAT} = 3.6 V	–	0.5	1.0	mA
I_{SUSP_WLS}	WLS suspend mode current	WLS path in suspend mode, $V_{UVLO} < V_{WLS\_IN} < V_{OVLO}$	–	0.5	1.0	mA

Table 3-5 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LIM_USB}	USB path maximum input current limit	USB 2.0 option: 100 mA mode, T = 0°C to +70°C, USB_IN = 5 V	70	85	100	mA
		USB 3.0 option: 150 mA mode, T = 0°C to +70°C, USB_IN = 5 V	115	–	150	mA
		USB 2.0 option: 500 mA mode, T = 0°C to +70°C, USB_IN = 5 V	450	475	500	mA
		USB 3.0 option: 900 mA mode, T = 0°C to +70°C, USB_IN = 5 V	810	855	900	mA
		Type-C 1.5 A mode, T = 0°C to +70°C, USB_IN = 5 V	1350	1425	1500	mA
		Type-C 3.0 A mode, T = 0°C to +70°C, USB_IN = 5 V	2700	2850	3000	mA
		USB high-current mode [3] (0 A–50 mA–5.0 A programmable), V_{USB_IN} = 5 V to 20 V, 0.5 A ≤ I_{LIM_USB} ≤ 5 A, T = 0°C to +70°C	0.9 × I_{LIM_USB}	0.95 × I_{LIM_USB}	I_{LIM_USB}	mA
I_{LIM_WLS}	WLS path maximum input current limit	[0 A:50 mA:3 A] programmable	0	–	3	A
	Accuracy	V_{WLS_IN} = 5 V to 20 V, 0.5A ≤ I_{LIM_WLS} ≤ 3 A, T=0°C to +70°C [3]	0.9 × I_{LIM_WLS}	0.95 × I_{LIM_WLS}	I_{LIM_WLS}	mA
Automatic input current limiting (AICL)						
V_{AICL}	LV AICL voltage collapse threshold	Programmable range (8 settings in 100 mV steps); V_{USB_IN} falling	4.1	–	4.8	V
	MV AICL voltage collapse threshold	Programmable range (8 settings in 200 mV steps); V_{USB_IN} falling	7.2	–	8.6	V
	HV AICL voltage collapse threshold	Programmable range (8 settings in 200 mV steps); V_{USB_IN} falling	10.2	–	11.6	V
	AICL voltage collapse threshold – continuous mode	Programmable range 4.1 V: 100 mV: 4.8 V 5.0 V: 200 mV: 12.8 V 13.2 V: 400 mV: 19.2 V V_{USB/WLS_IN} falling	4.1	–	19.2	V
	Accuracy	V_{USB/WLS_IN} falling	-3.5		3.5	%
	Hysteresis	V_{USB/WLS_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB/WLS_IN} rising and falling; Programmable in 30 μs, 1/5/30 ms	0.03	5	30	ms
	Accuracy		-8	–	25	%
t_{AICL_step}	AICL step duration in discrete method	I_{LIM_USB} or I_{LIM_WLS} rising; Programmable in 5, 10, 30, 40 ms	5	10	40	ms
	Accuracy		-1	–	15	%
t_{AICL_rerun}	AICL rerun timer	Programmable in 3, 12, 45, 360 sec	3	45	360	s
	Accuracy		-5	–	20	%
Input missing poller						
I_{IN_LOW}	I_{IN_LOW} comparator threshold		100	130	200	mA
	Deglitch filter time	I_{IN} rising or falling	–	1	–	ms
$I_{PD\_USB\_IN}$	USB_IN pull-down current source	V_{USB_IN} OV or UV	5	10	15	mA

Table 3-5 Input power source control and protection (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{PD\_WLS\_IN}$	WLS_IN pull-down current source	V_{WLS_IN} OV or UV	5	10	15	mA
$I_{PD\_MID\_CHG}$	MID_CHG pull-down current source	V_{USB_IN} or V_{WLS_IN} UV	20	30	40	mA
t_{IMP}	Input missing poller active timing	Charger buck disabled, current sink enabled	–	10	–	ms
$t_{IMP\_ATTEMPT}$	Number of IMP attempts	IMP conditions = true	–	–	3	
t_{IMP_RETRY}	After three attempts, the time before the IMP attempts to re-enable	IMP conditions = true	–	1	–	s
V_{IMP}	Input missing detection voltage threshold	Input missing poller active, charger buck disabled, 20 mA current sink enabled	–	V_{REVI}	–	V
Surge protection						
USB_IN surge protection	IEC 61000-4-5 1.2/50 µs voltage surge waveform, ext. TVS diode [4]		-350	–	350	V
Maximum QUSB/QWLS VDS during surge	IEC 61000-4-5 1.2/50 µs voltage surge waveform, ext. TVS diode [4]		–	–	25	V

1. For the PM8350B charger, V_{IN} is V_{USB_IN} for the USB path or V_{WLS_IN} for wireless input path.
2. The OVP response time is defined as from V_{IN} rises above V_{OVLO}, to switcher stops switching.
3. The USB ICL accuracy is trimmed targeting V_{USB_IN} = 5 V. For ICL accuracy at V_{USB_IN} > 5 V, software needs to adjust ICL gain trim code depending on V_{USB_IN}
4. External TVS diode: WillSemi ESD56161D24 25V reverse breakdown voltage, 30 V maximum clamping voltage at 150 A.

Table 3-6 USB Type-C and BC1.2 specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
APSD for BC1.2						
V_{DP_SRC}	D+ source voltage	Load ≤ 250 µA	0.6	0.65	0.7	V
V_{DM_SRC}	D- source voltage	Load ≤ 250 µA	0.6	0.65	0.7	V
V_{DAT_REF}	Data detect voltage		0.3	0.35	0.4	V
V_{DP_UP}	D+ pull-up voltage		3	3.3	3.6	V
I_{DM_SINK}	D- sink current		25	50	75	µA
I_{DP_SINK}	D+ sink current		25	50	75	µA
I_{DP_SRC}	Data contact detect current source		3.5	5.5	7.5	µA
R_{DM_DWN}	D- pull-down resistance		14.25	19.5	24.8	kΩ
$t_{DCD\_TIMEOUT}$	DCD timeout	Option 1	321	328	335	ms
		Option 2	642	656	670	ms
$t_{DP\_SRC\_ON}$	D+ source on time		100	–	–	ms
$t_{ENUM\_TIMEOUT}$	SDP enumeration timeout		–	–	2	min
t_{DPSRC_HICRNT}	D+ source off to high current		40	–	–	ms
t_{DPSRC_CON}	D+ source off to connect		40	–	–	ms
USB Type-C						
CC_{CAP}	Maximum CC pin capacitance		200	–	600	pF

Table 3-6 USB Type-C and BC1.2 specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{OPEN}	Sink minimum open-circuit CC impedance to ground	In Disabled or ErrorRecovery state	126	–	–	kΩ
$V_{CC\_CLAMP\_SNK}$	Sink CC clamp voltage	As Rd during shutdown	0.88	1.1	1.32	V
R_{PD_SNK}	Sink crude sensor pull-down resistor	Before source attach	150 [1]	200	250	kΩ
R_{PU_SRC}	Sink crude sensor pull-up resistor	Before sink attach	75 [2]	100	125	kΩ
Rd	Sink Rd pull-down resistor		4.59	5.1	5.61	kΩ
I_{RP_SRC}	Source Rp current source – default USB		64	80	96	µA
	Source Rp current source – 1.5 A		166	180	194	µA
	Source Rp current source – 3.0 A		304	330	356	µA
vSafe0V			0	–	0.8	V
vSafe5V			4.75	–	5.5	V
$V_{BUS\_RMV\_5V}$	Sink VBUS removal detection threshold if = 5 V (vSinkDisconnect)	V_{USB_IN} falling; for determining exit from Attached.SNK state	0.8	2.5	3.67	V
	Hysteresis	V_{USB_IN} rising	–	500	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{BUS\_RMV\_9V}$	Sink VBUS removal detection threshold if = 9 V	V_{USB_IN} falling; for determining exit from Attached.SNK state	6.6	6.9	7.2	V
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{BUS\_RMV\_12V}$	Sink VBUS removal detection threshold if = 12 V	V_{USB_IN} falling; for determining exit from Attached.SNK state	9.3	9.6	9.9	V
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$V_{SNK\_RMV\_PPS}$	Sink VBUS removal detection threshold if > 5 V through PD (vSinkDisconnectPD)	[3.7 V:0.1 V:5.2 V], 16 steps	3.7	–	5.2	V
		[5.4 V:0.2 V:11.6 V], 32 steps	5.4	–	11.6	V
		[12 V:0.4 V:18 V], 16 steps	12	–	18	V
	Accuracy	V_{USB_IN} falling	-3.5	–	3.5	%
	Hysteresis	V_{USB_IN} rising	–	200	–	mV
	Deglitch filter time	V_{USB_IN} falling	–	10	–	ms
$t_{CCDebounce}$	Time a port shall wait before it can determine it is attached	Transitioning between the AttachWait.SNK/SRC state and the Attached.SNK/SRC state; programmable range (103, 125, 150, 175)	100	150	200	ms
$t_{PDDebounce}$	Time a port shall wait before it can determine it is either detached or there has been a change in the Type-C current advertisement	Programmable in 12, 14, 16, 18 ms	10	14	20	ms
Vconn switch						
V_{CONN}	V_{CONN} voltage range	V_{CONN} enabled, 3.2 V ≤ V_{PH_PWR} ≤ 4.5 V	3.0	–	4.5	V
		V_{CONN} enabled, external 5 V boost	3.0	–	5.5	V
	V_{CONN} load	V_{CONN} enabled, V_{PH_PWR} ≥ 3.2 V	1.5	–	–	W
R_{VCONN}	V_{CONN} switch resistance	V_{CONN} enabled, V_{PH_PWR} ≥ 3.2 V T = 0°C to +70°C	–	–	400	mΩ

Table 3-6 USB Type-C and BC1.2 specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OCP_VCONN}	V_{CONN} overcurrent protection threshold	V_{CONN} enabled, $V_{PH\_PWR} \geq 3.2$ V T = 0°C to +70°C, 100 mA option	10	100	200	mA
		200 mA option	100	200	350	mA
		300 mA option	200	300	450	mA
		400 mA option	300	400	600	mA
		500 mA option	450	500	750	mA
$V_{DIP\_VCONN\_SS}$	V_{PH_PWR} dip when V_{CONN} soft-start	10 µF V_{CONN} load; enable V_{CONN}	0	–	200	mV
t_{VCONN_ON}	V_{CONN} powering on time	From the source supplies VBUS (reaches vSafe5V) to V_{CONN} reaches the min. valid voltage.	–	–	2	ms
t_{VCONN_OFF}	V_{CONN} powering off time	From the time that a Sink is detached or as commanded until V_{CONN} supply is disabled and the bulk capacitance is removed	–	–	35	ms
SBU						
I_{SBU_SRC1}	SBU current source 1	For Type-C connector water detection	2.25	2.5	2.75	µA
I_{SBU_SRC2}	SBU current source 2	For Type-C connector water detection	75	80	85	µA
VBUS-to-VPH pass-through mode						
$I_{DD\_VPH\_PT}$	Charger I_{USB} during USB-to-VPH pass-through mode (USB_SUSPEND = 1, U2PH_BYP_EN = 1) [3]	3.0 V < VBAT < 4.5 V, VBAT ≤ VBUS < VBAT + 0.8 V, VBUS < 4.8 V, T = 25°C	0.4	0.6	0.8	mA
		3.0 V < VBAT < 3.8 V, VBAT + 1 V ≤ VBUS < 4.8 V, T = 25°C	1.4	1.5	1.7	mA

1. R_{PD_SNK} (min) must be higher than min. zOPEN (126 kΩ) so the source does not treat R_{PD_SNK} as Rd.
2. R_{PU_SRC} (min) must be higher than max. Rp (56 kΩ) so the sink does not treat RPU_SRC as Rp
3. $I_{USB\_VPH\_PT}$ is the IUSB consumed by charger when the rest of the chip is in sleep condition: Qualcomm battery gauge in low power mode, OLED driver modules off, Haptics modules off, SBL/PSI loaded and the MSM sleep sequence is executed.

3.5.2 Battery charger specifications

Table 3-7 1S battery charger specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{TRKL}	Trickle charge current	$V_{BATT} < V_{TRKL}$	25	50	75	mA
V_{TRKL}	Trickle charge to precharge threshold		2.0	2.1	2.2	V
I_{PRE_CHG}	Precharge current range	Programmable (8 settings in 50 mA steps)	250	–	600	mA
	Accuracy	T= 0°C to +70°C	± 10% of setting ± 10 mA			
V_{P2F}	Pre-charge to fast-charge voltage threshold		V_{SYS_MIN}[1]			V
I_{FC}	Fast charge current (FCC) range	Programmable (200 settings in 50 mA steps)	0	–	10.0 [2]	A
	Accuracy	T = 0°C to +70°C, $I_{FC} < 3.0$ A	-10	–	10	%
		T = 0°C to +70°C, $I_{FC} \geq 3.0$ A	-5	–	5	%
		T = 25°C, $I_{FC} < 3.0$ A	-5	–	5	%
		T = 25°C, $I_{FC} \geq 3.0$ A	-2.5	–	2.5	%
	FCC soft-start slew rate	Programmable stepper: 50 mA every 25/50/100/200 µs	25	–	200	50 mA/ X µs
	FCC soft-stop slew rate	Programmable stepper: 50 mA every 25/50/100/200 µs	25	–	200	50 mA/ X µs
V_{FLT}	Float voltage range	Programmable (120 settings with 10 mV steps), T = 0°C to +70°C	3.6	–	4.79	V
	Accuracy	$V_{FLT} < 4.2$ V, T = 0°C to +70°C	-1	–	1	%
		$V_{FLT} \geq 4.2$ V, T = 0°C to +70°C	-0.5	–	0.5	%
I_{TERM}	Charge termination current range	IADC range	50	200	750	mA
	Accuracy	IADC internal current sense, V_{BATT} = 4.2 V–4.55 V, I_{TERM} = 200 mA, T = 0°C to +70°C	-25	–	25	mA
	Deglitch filter time	Charger sniffs FG making IADC requests	100	–	4000	ms
I_{TERM_ANA}	I_{TERM} analog comparator range	Programmable (8 settings in 50 mA steps)	100	300	450	mA
	Accuracy	T = 0°C to +70°C	± 10% of setting ± 50			mA
	Deglitch filter time	Charger in CV regulation AND $I_{BAT} < I_{TERM\_ANA}$	–	200	–	ms
V_{RECHG}	VBAT ADC based automatic recharge threshold	Programmable VBAT range	3.6	–	4.8	V
	Accuracy	T = 0°C to +70°C	-20	–	+20	mV
	Deglitch filter time	Charger make 1 VBAT ADC request (16 # of average) every 1 sec	8	–	4000	ms
SoC_{RECHG}	SoC-based automatic recharge threshold	Programmable SoC range	0	–	100	%
	Accuracy	T = 0°C to +70°C	-1	–	+1	%
	Deglitch filter time	FG update SoC every 1 sec	100	–	4000	ms
$V_{INHIBIT}$	VBAT ADC based charger Inhibit threshold voltage range	Programmable VBAT range	3.6	–	4.8	mV
	Accuracy	T = 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} falling, 50/100/150/200 mV	50	100	200	mV

Table 3-7 1S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LOW_BATT}	VBAT ADC based low-battery voltage/SYSOK detection (triggers PMIC power-on) threshold range		2.4	2.8	3.2	V
	Accuracy	T = 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} rising, 50/100/150/200 mV	50	100	200	mV
V_{BATT_OV}	Battery overvoltage lockout	V_{BATT} rising, above V_{FLT}	30	40	50	mV
	Hysteresis	V_{BATT} falling	10	20	30	mV
	Deglitch filter time	V_{BATT} rising or falling; Programmable in 5/10/15/20 ms	5	–	20	ms
$V_{SYS\_HV\_ALM}$	V_{SYS} high-voltage alarm	Programmable (8 settings in 100 mV steps)	4.3	4.8	5.0	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	50	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYS\_HV\_ALM}$, Programmable (10/100/1000 µs)	10	10	1000	µs
V_{SYS_OV}	System overvoltage protection threshold	Programmable (8 settings in 100 mV steps)	4.5	5.0	5.2	V
	Accuracy		-2	–	+2	%
	Hysteresis	V_{SYS} falling	–	75	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYSOV}$, Programmable (10/100/1000 µs)	10	100	1000	µs

1. On PMIC5 chargers, the QBAT linear operation is removed, and pre-charge to fast-charge transition happens when V_{BAT} reaches V_{SYS_MIN} threshold.
2. The PM8350B charger can charge up to 6 A only. The 10 A setting is in case one or multiple SMB1396/SMB1398 are used in parallel to charge the battery.

Table 3-8 2S battery charger specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{TRKL}	Trickle charge current	At 1S battery level [1]	50	100	150	mA
		At 2S battery level [2]	25	50	75	mA
V_{TRKL}	Trickle charge to precharge threshold	At 2S battery level [2]	4.0	4.2	4.4	V
I_{PRE_CHG}	Precharge current range	At 1S battery level [1]: 8 settings in 50 mA steps	250	–	600	mA
		At 2S battery level [2]: 8 settings in 25 mA steps	125	–	300	mA
	Accuracy	T= 0°C to +70°C	± 10% of setting ± 10 mA			
V_{P2F}	Pre-charge to fast-charge voltage threshold	At 2S battery level [2]	$2 \times V_{SYS\_MIN}$			V
I_{FC}	Fast charge current (FCC) range	At 2S battery level [2]: 200 settings in 50 mA steps	0	–	10.0 [3]	A
	Accuracy	T = 0°C to +70°C, $I_{FC} < 3.0$ A	-10	–	10	%
		T = 0°C to +70°C, $I_{FC} \geq 3.0$ A	-5	–	5	%
		T = 25°C, $I_{FC} < 3.0$ A	-5	–	5	%
		T = 25°C, $I_{FC} \geq 3.0$ A	-2.5	–	2.5	%

Table 3-8 2S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FLT}	Float voltage range	At 1S battery level [1]: 120 settings with 10 mV steps	3.6	–	4.79	V
		At 2S battery level [2]: 120 settings with 20 mV steps	7.2	–	9.58	V
	Accuracy	$V_{FLT} < 4.2$ V, T = 0°C to +70°C	-1	–	1	%
		$V_{FLT} \geq 4.2$ V, T = 0°C to +70°C	-0.5	–	0.5	%
I_{TERM}	Charge termination current range	IADC range	50	200	750	mA
	Accuracy	IADC internal current sense, V_{BATT} = 4.2 V–4.55 V, I_{TERM} = 200 mA, T = 0°C to +70°C	-25	–	25	mA
	Deglitch filter time	Charger sniffs FG making IADC requests	100	–	4000	ms
I_{TERM_ANA}	I_{TERM} analog comparator range	At 1S battery level: [100 mA: 50 mA: 450 mA]	100	300	450	mA
		At 2S battery level: [50 mA: 25 mA: 225 mA]	50	150	225	mA
	Accuracy	T = 0°C to +70°C	± 10% of setting ± 50			mA
	Deglitch filter time	Charger in CV regulation AND $I_{BAT} < I_{TERM\_ANA}$	–	200	–	ms
V_{RECHG}	VBAT ADC based automatic recharge threshold	At 1S battery level [1]	3.6	–	4.8	V
		At 2S battery level [2]	7.2	–	9.6	V
	Accuracy	T = 0°C to +70°C	-20	–	+20	mV
	Deglitch filter time	Charger make 1 VBAT ADC request (16 # of average) every 1 sec	8	–	4000	ms
SoC_{RECHG}	SoC-based automatic recharge threshold	Programmable SoC range	0	–	100	%
	Accuracy	T = 0°C to +70°C	-1	–	+1	%
	Deglitch filter time	FG update SoC every 1 sec	100	–	4000	ms
$V_{INHIBIT}$	VBAT ADC based charge Inhibit threshold voltage range	At 1S battery level [1]	3.6	–	4.8	V
		At 2S battery level [2]	7.2	–	9.6	V
	Accuracy	T = 0°C to +70°C	-20	–	20	mV
	Hysteresis	VBATT falling, 50/100/150/200 mV	50	100	200	mV
V_{LOW_BATT}	VBAT ADC based low-battery voltage/SYSOK detection (triggers PMIC power-on) threshold range	At 1S battery level [1]	2.4	2.8	3.2	V
		At 2S battery level [2]	4.8	–	6.4	V
	Accuracy	T = 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} rising; 50/100/150/200 mV	50	100	200	mV
V_{BATT_OV}	Battery overvoltage lockout	V_{BATT} (2S) rising, above V_{FLT}	60	80	100	mV
	Hysteresis	V_{BATT} (2S) falling	20	40	60	mV
	Deglitch filter time	V_{BATT} (2S) rising or falling; Programmable in 5/10/15/20 ms	5.0	–	20	ms

Table 3-8 2S battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{SYS\_HV\_ALM}$	V_{SYS} high-voltage alarm	Programmable (8 settings in 100 mV steps)	4.3	4.8	5.0	V
	Accuracy		-2.0	–	+2.0	%
	Hysteresis	V_{SYS} falling	–	50	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYS\_HV\_ALM}$, Programmable (10/100/1000 µs)	10	10	1000	µs
V_{SYS_OV}	System overvoltage protection threshold	Programmable (8 settings in 100 mV steps)	4.5	5.0	5.2	V
	Accuracy		-2.0	–	+2.0	%
	Hysteresis	V_{SYS} falling	–	75	–	mV
	Deglitch filter time	$V_{SYS} > V_{SYSOV}$, Programmable (10/100/1000 µs)	10	100	1000	µs

1. For 2S battery charging, PM8350BHS charger has to work with SMB1399 voltage charger. This spec is defined at PM8350BHS charger output, that is 1S battery level, for PM8350BHS simulation and testing purpose
2. This spec is defined at SMB1399 output, that is, 2S battery level, for system level application purpose.
3. The PM8350BHS charger can charge up to 6 A only (1S level), which translates to 3 A at 2S level. The 10 A at 2S level is in case one or multiple SMB1396/SMB1398 are used in parallel to charge the battery.

3.5.3 Buck regulator specifications

Table 3-9 Buck regulator specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_5V LDO						
V_{DD_5V}	VDD_5V LDO regulated output voltage	I_{OUT} = 20 mA, $V_{USB\_IN}/V_{WLS\_IN} \geq 5.0$ V, In 3LBk/D2CP mode	4.8	5	5.2	V
		I_{OUT} = 20 mA, $V_{USB\_IN}/V_{WLS\_IN} \geq 5.0$ V, In boost mode	4.6	4.8	5.0	V
$V_{DD\_5V\_UVLO}$	VDD_5V LDO undervoltage lockout	V_{USB_IN}/V_{WLS_IN} rising	2.6	2.8	3.0	V
		V_{USB_IN}/V_{WLS_IN} falling	2.0	2.2	2.4	V
I_{DD_5V}	VDD_5V LDO output current	$V_{USB\_IN}/V_{WLS\_IN} \geq 5.0$ V	20	–	–	mA
PWM buck regulator						
V_{SYS_MIN}	Minimum VPH regulated output voltage range	Group 1: [2.8 V:0.2 V:3.4 V]	2.8	3.0	3.4	V
		Group 2: [4.0 V:0.2 V:4.6 V]; to be used in factory mode	4.0	–	4.6	V
	Accuracy	500 mA load, $V_{BAT} < V_{SYS\_MIN}$	-2.0	–	+2.0	%
V_{SYS}	V_{PH_PWR} (V_{SYS}) output voltage	V_{IN} present, during trickle/precharging, $V_{BAT} < V_{SYS\_MIN} - V_{BAT\_TRACK}$		V_{SYS_MIN}		V
		V_{IN} present, during precharging, $V_{SYS\_MIN} - V_{BAT\_TRACK} < V_{BAT} < V_{SYS\_MIN}$		$V_{BAT} + V_{BAT\_TRACK}$		V
		V_{IN} present, during fast charging, $V_{BAT} > V_{SYS\_MIN}$		$V_{BAT} + (I_{CHG} \times RDSON_{BF})$		V
		V_{IN} present, charging terminated or disabled		$V_{BAT} + V_{BAT\_TRACK}$		V

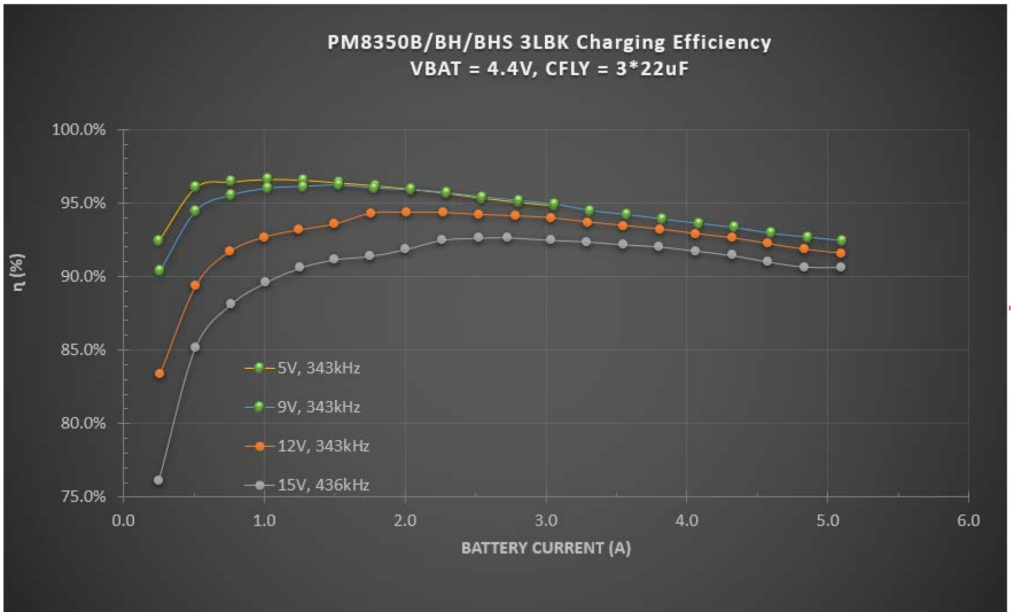
Table 3-9 Buck regulator specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_TRACK}	V_{BAT} tracking voltage during precharge	VPH = VBAT * (1 + X) X = 7%, 8%, 9%		9		%
				8		%
				7		%
	V_{BAT} tracking voltage after EoC	VPH = VBAT * (1 + X) X = 0%, 0.5%, 1%, 2%, 3%		3		%
				2		%
				1		%
				0.5		%
				0		%
	Accuracy		-20		20	mV
I_{BUCK_DC}	Buck DC max output current	8 programmable settings ([3 A:500 mA:6.5 A]) See Note 1 for Vin and Fsw [1], Vsys = 3.6 V-4.6 V	5.5	6	9	A
F_{SW_BUCK} [1]	Buck switching frequency range	8 programmable settings	0.343	–	0.800	MHz
	Accuracy	T = 0ºC to +70ºC	-6	–	6	%
DC_{BUCK}	Buck duty cycle		0	–	98	%
$\Delta V_{SYSLOAD}$ [2]	V_{SYS} output voltage load regulation	I_{SYS} = 0.1 A to 4 A, VBATT = 3.9 V, PWM mode, FSW = 1.0 MHz, charging disabled [2]	–	5	–	
V_{DIP_BUCK} [2]	Buck voltage dip due to positive load transient	V_{USB_IN}/V_{MID_CHG} = 5.0 V I_{LIM_USB} = 3 A, V_{BATT} = 0 V, V_{PH} = V_{SYS_MIN}, F_{SW} = 600 kHz, I_{SYS_LOAD} [2] 0.1 A to 2 A in 1 A/µs	-500	–	–	mV
V_{SPIKE_BUCK} [2]	Buck V_{OUT} (V_{PH}) voltage spike due to negative load transient	V_{USB_IN}/V_{MID_CHG} = 5/7/9/12 V, V_{BATT} = V_{FLT} (charging done) [2], F_{SW}, I_{SYS_LOAD} 4.0 A to 0.1 A in 1 A/µs	–	–	500	mV
	Buck V_{OUT} (V_{PH}) variation due to positive line transient	Charging disabled, V_{BAT} = 0 V/3.5 V/4.5 V, V_{PH} = V_{SYS_MIN} or V_{BAT_TRACK}, I_{SYS} = 2 A, V_{IN} = 5 V to 9 V, 9 V to 12 V, 12 V to 15 V, 15 V to 20 V in 1 V/10 µs	-100	–	100	mV
	Buck V_{OUT} (V_{PH}) variation due to negative line transient	Charging disabled, V_{BAT} = 0 V/3.5 V/4.5 V, V_{PH} = V_{SYS_MIN} or V_{BAT_TRACK}, I_{SYS} = 2 A, V_{IN} = 20 V to 15 V, 15 V to 12 V, 12 V to 9 V, 9 V to 5 V in -1 V/10 µs	-100	–	100	mV
$V_{P\text{-}P\_BUCK\_PWM}$	Buck output ripple in PWM mode	2 A load, V_{BATT} = 3.9 V, PWM mode, F_{SW} = 530 kHz [2]	–	25	50	mV
$V_{P\text{-}P\_BUCK\_PSM}$	Buck output ripple in PSM mode	No load, V_{BATT} = 3.0 V, pulse skip mode	–	50	100	mV
I_{DD_BUCK}	Buck active supply current	Switcher enabled, no load, USB_IN = 5/9/12/15/20 V, V_{SYS} = 3.5/4/4.5 V, pulse skip mode	–	2	5	mA
		Switcher enabled, no load, USB_IN = 5/9/12/15/20 V, V_{SYS} = 3.5/4/4.5 V, PWM mode	–	30	–	mA
R_{DSON_QUSB}	QUSB (16 V) $R_{DS(ON)}$	T = 0°C to +70°C	–	10	15	mΩ
R_{DSON_QWLS}	QWLS (16 V) $R_{DS(ON)}$	T = 0°C to +70°C	–	20	30	mΩ
R_{DSON_Q1}	Q1 (16 V) on-resistance	T = 0°C to +70°C	–	12	16	mΩ
R_{DSON_Q2}	Q2 (12 V) on-resistance	T = 0°C to +70°C	–	8	12	mΩ
R_{DSON_Q3}	Q3 (12 V) on-resistance	T = 0°C to +70°C	–	8	12	mΩ

Table 3-9 Buck regulator specifications (cont.)

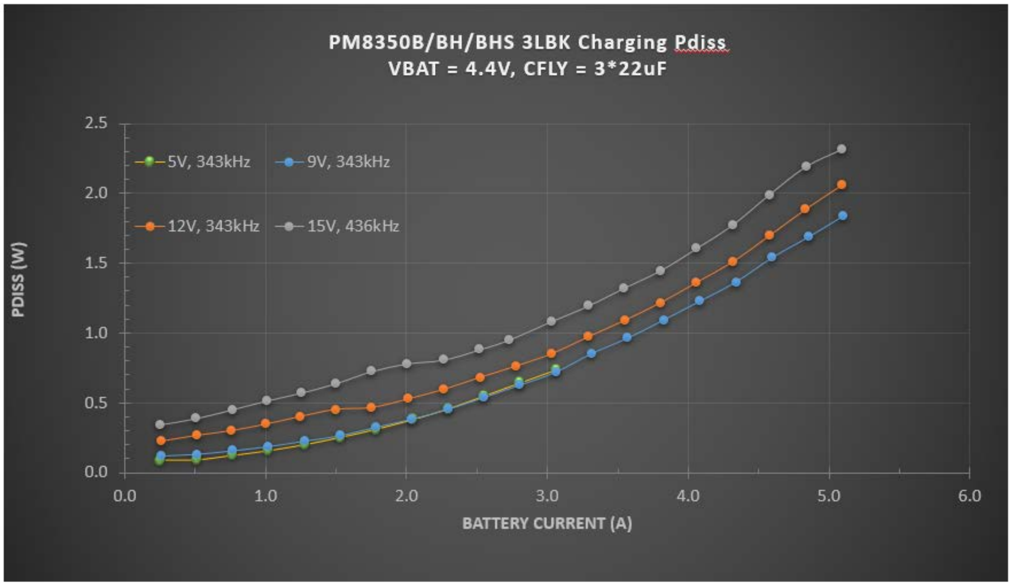
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DSON_Q4}	Q4 (12 V) on-resistance	T = 0°C to +70°C	–	8	12	mΩ
R_{DSON_QBYP}	QBYP on-resistance	T = 0°C to +70°C	–	15	20	mΩ
η	Efficiency [1]	5 V V_{USB_IN}, 4 V V_{BAT}, I_{CHG} = 3 A	–	94.8	–	%
		5 V V_{USB_IN}, 4 V V_{BAT}, I_{CHG} = 4 A	–	TBD	–	%
		5 V V_{USB_IN}, 4 V V_{BAT}, I_{CHG} = 5 A	–	TBD	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	94.9	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	93.6	–	%
		9 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	92.4	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	94	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	92.9	–	%
		12 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	91.6	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 3 A	–	92.5	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 4 A	–	91.8	–	%
		15 V V_{USB_IN}, 4.4 V V_{BAT}, I_{CHG} = 5 A	–	90.6	–	%

1. Fsw based on VIN:
   4.5 V~12 V: 343 kHz
   12 V~15 V: 436 kHz
   15 V~20 V: TBD kHz
2. C_{SYS} = 22 µF, C_{USB_IN} = 4.7 µF, C_{MID} = 4.7 µF



Measured data under the following conditions: USB_IN = 5/9/12/15 V (measured at the USB_IN input capacitor), Vbatt = 4.4 V, Fsw = 343 kHz (USB_IN = 5/9 V/12 V), 436 kHz (USB_IN=15 V) Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF, Cvph = 2 ×10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-1 PM8350B/BH/BHS 3LBk Charging Efficiency



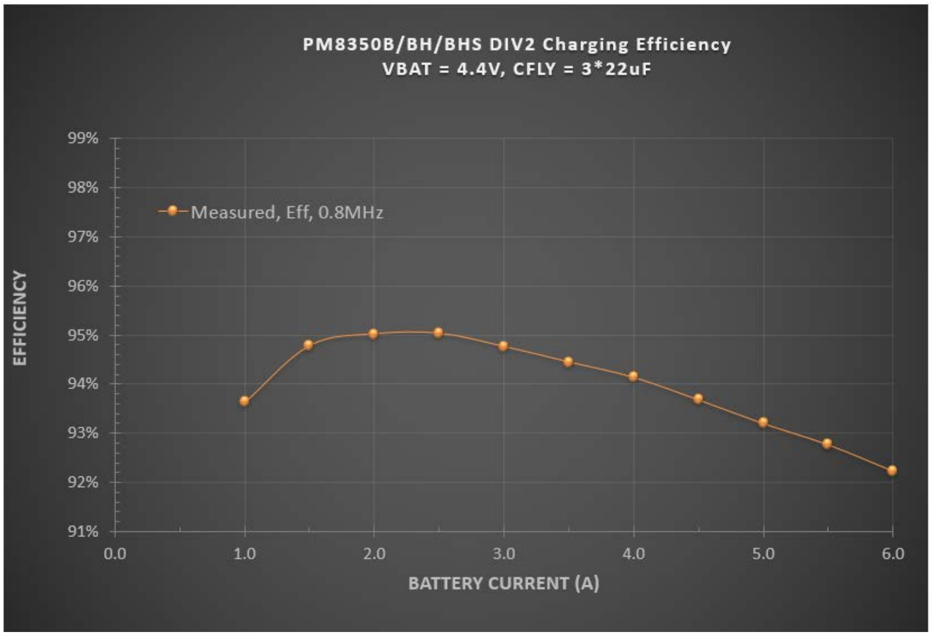
Measured data under the following conditions: USB_IN = 5/9/12/15 V (measured at the USB_IN input capacitor), Vbatt = 4.4 V, Fsw = 343 kHz (USB_IN = 5/9 V/12 V), 436 kHz (USB_IN=15 V) Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF, Cvph = 2 × 10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-2 PM8350B/BH/BHS 3LBk Charging Pdiss

3.5.4 Div2 charge pump specifications

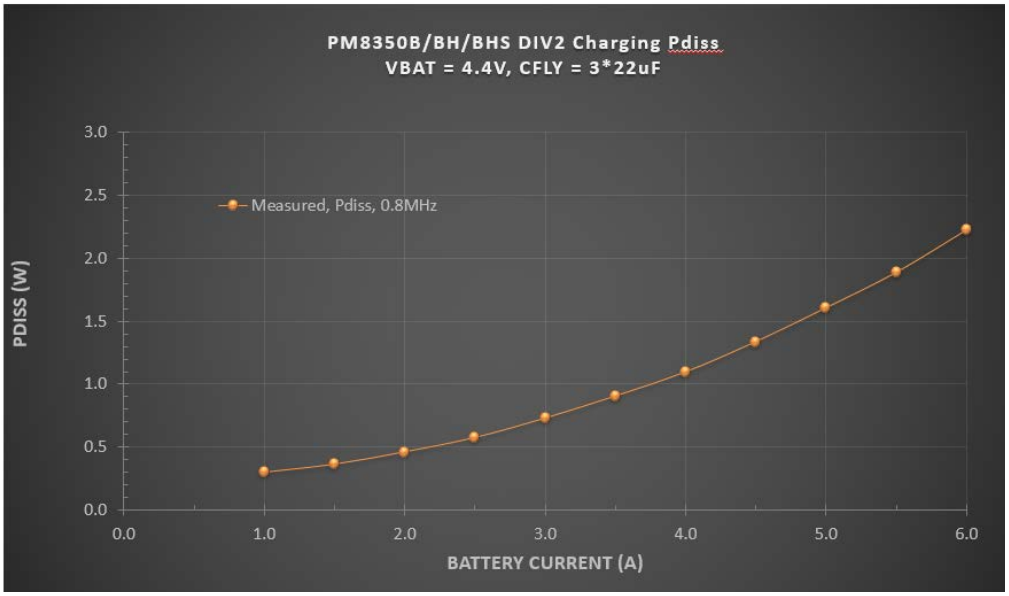
Table 3-10 Div2 charge pump specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3LBk <----> D2Cp mode transition						
$V_{CMB\_WIN\_HI}$	Combo WIN_HIGH comparator (V_{MID}/2 vs. VPH)	Programmable threshold: V_{MID}/2 - VPH = 4/5/6/7 A × 30 mΩ Req	90	120	150	mV
			120	150	180	mV
			140	180	220	mV
			170	210	250	mV
		Accuracy	-15	–	+15	mV
		Hysteresis	–	15	–	mV
		Deglitch, ($V_{MID}/2 - V_{PH}$) > $V_{CMB\_WIN\_HI}$	–	100	–	μs
			–	200	–	μs
			–	400	–	μs
			–	800	–	μs
		Deglitch, ($V_{MID}/2 - V_{PH}$) < $V_{CMB\_WIN\_HI} - V_{HYST}$	–	0.1	–	ms
			–	0.5	–	ms
			–	1	–	ms
			–	10	–	ms
$V_{CMB\_WIN\_LO}$	Combo WIN_LOW comparator (V_{MID}/2 vs. VPH)	Programmable threshold: V_{MID}/2 - VPH = 2.0/2.5/3.0/3.5 A × 30 mΩ Req	–	-100	–	mV
			–	-50	–	mV
			–	30	–	mV
			–	60	–	mV
		Accuracy	-25	–	+25	mV
		Hysteresis	–	15	–	mV
		Deglitch, ($V_{MID}/2 - V_{PH}$) < $V_{CMB\_WIN\_LO}$	–	100	–	μs
			–	200	–	μs
			–	400	–	μs
			–	800	–	μs
		Deglitch, ($V_{MID}/2 - V_{PH}$) > $V_{CMB\_WIN\_LO} + V_{HYST}$	–	0.1	–	ms
			–	0.5	–	ms
			–	1	–	ms
			–	10	–	ms
DC_{D2CP}	Div2 CP duty cycle		–	50	–	%
Div2 operation						
η	Efficiency	V_{USB_IN} = 9 V, V_{BAT} = 4.4 V, Fsw = 800 kHz, IOUT = 3 A	–	94.8	–	%
		V_{USB_IN} = 9 V, V_{BAT} = 4.4 V, Fsw = 800 kHz, IOUT = 4 A	–	94.1	–	%
		V_{USB_IN} = 9 V, V_{BAT} = 4.4 V, Fsw = 800 kHz, IOUT = 5 A	–	93.2	–	%



Measured data under the following conditions: USB_IN = 9 V (measured at the USB_IN input capacitor), Vbatt = 4.4 V, Fsw = 800 kHz
Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF,
Cvph = 2 ×10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-3 PM8350B/BH/BHS DIV2 charging efficiency



Measured data under the following conditions: USB_IN = 9 V (measured at the USB_IN input capacitor), Vbatt = 4.4 V, Fsw = 800 kHz
Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF,
Cvph = 2 × 10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-4 PM8350B/BH/BHS DIV2 Charging Pdiss

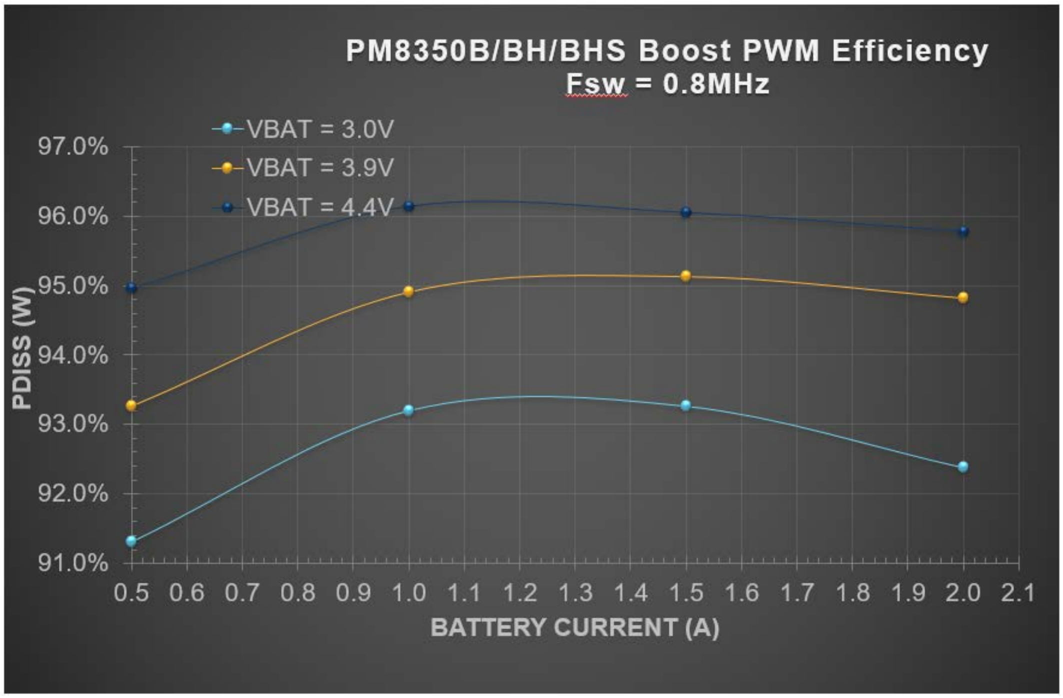
3.5.5 Reverse boost specifications

Table 3-11 Reverse boost specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWM boost regulator						
V_{BOOST}	Boost regulated output voltage range	Programmable (8 settings in 100 mV steps)	4.8	5.0	5.5	V
	Boost regulated output voltage accuracy	All settings	-2	–	2	%
I_{BOOST}	Boost output current rating	$V_{BATT} > V_{BAT\_BST\_UVLO}$	1.5	–	–	A
$V_{BAT\_BST\_UVLO}$	Battery undervoltage lockout for low power boost (1.5 A)	Programmable (4 settings in 100 mV steps)	2.4	2.7	3.2	V
	Accuracy	T = 0°C to +70°C	-20	–	20	mV
	Hysteresis	V_{BATT} rising, all settings, 50/100/150/200 mV	50	100	200	mV
V_{BOOST_OCP}	Boost overcurrent shutdown threshold	$I_{BOOST} > I_{BOOST\_LIM}$, V_{USB_IN} falling	–	V_{SYS} $+V_{ASHDN}$	–	V
t_{BOOST_OCP}	Boost short-current shutdown glitch threshold	$V_{USB\_IN} > V_{BOOST\_OCP}$, V_{USB_IN} falling	–	20	–	ms
$T_{BOOST\_OCP\_RETRY}$	Number of boost re-start attempts	$I_{BOOST} > I_{BOOST\_LIM}$	–	–	3	
V_{BOOST_SCP}	Boost short-current protection threshold	$I_{BOOST} > I_{BOOST\_LIM}$, $V_{USB\_IN} < V_{BOOST\_OCP}$, V_{USB_IN} falling	–	1	–	V
$V_{P\text{-}P\_BOOST\_PWM}$	PWM boost output ripple	500 mA load, V_{BATT} = 4.0 V, PWM mode, F_{SW} = 0.8 MHz	–	50	100	mV
$V_{P\text{-}P\_BOOST\_PFM}$	PFM boost output ripple	No load, V_{BATT} = 4.0 V, pulse skip mode	–	100	150	mV
V_{DIP_BOOST}	Boost voltage dip due to positive load transient	V_{BATT} = 4.0 V, F_{SW} = 0.8 MHz, V_{BOOST} = 5.0 V, C_{USB_IN} = 4.7 µF, C_{MID_CHG} = 10 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 0.1 A to 1.5 A in 1 A/µs	-500	–	–	mV
V_{SPIKE_BOOST}	Boost voltage spike due to negative load transient	V_{BATT} = 4.0 V, F_{SW} = 0.8 MHz, V_{BOOST} = 5.0 V, C_{USB_IN} = 4.7 µF, C_{MID_CHG} = 10 µF, I_{BOOST_LIM} = 1.5 A, I_{LOAD} 1.5 A to 0.1 A in 1 A/µs	–	–	+500	mV
	Boost V_{OUT} (V_{USB/WLS_IN}) variation due to positive line transient	V_{BAT_CELL} = 3.5 V/4.0/4.5 V, Battery ESR = 100 mΩ, V_{USB/WLS_IN} = 5.0 V, $I_{USB/WLS}$ = 1 A, I_{SYS} = 4 A to 0 A in 1 A/µs	-200	–	200	mV
	Boost V_{OUT} (V_{USB/WLS_IN}) variation due to negative line transient	V_{BAT_CELL} = 3.5 V/4.0/4.5 V, Battery ESR = 100 mΩ, V_{USB/WLS_IN} = 5.0 V, $I_{USB/WLS}$ = 1 A, I_{SYS} = 0 A to 4 A in 1 A/µs	-200	–	200	mV
F_{SW_BOOST}	Boost switching frequency range	8 programmable settings (19.2 MHz/ [24:2:10])	0.8	0.8	1.92	MHz
	Boost switching frequency accuracy	T = 0°C to +70°C	-6	–	6	%
I_{DD_BOOST}	Boost supply current	V_{BATT} = 4.0 V, V_{BOOST} = 5.0 V, PFM, OTG Mode, No load	–	–	1.5	mA
		V_{BATT} = 4.0 V, V_{BOOST} = 5.0 V, PFM, Type-C Source Mode, Rp-3A pull-up (330 uA) enabled	–	–	2.2	mA

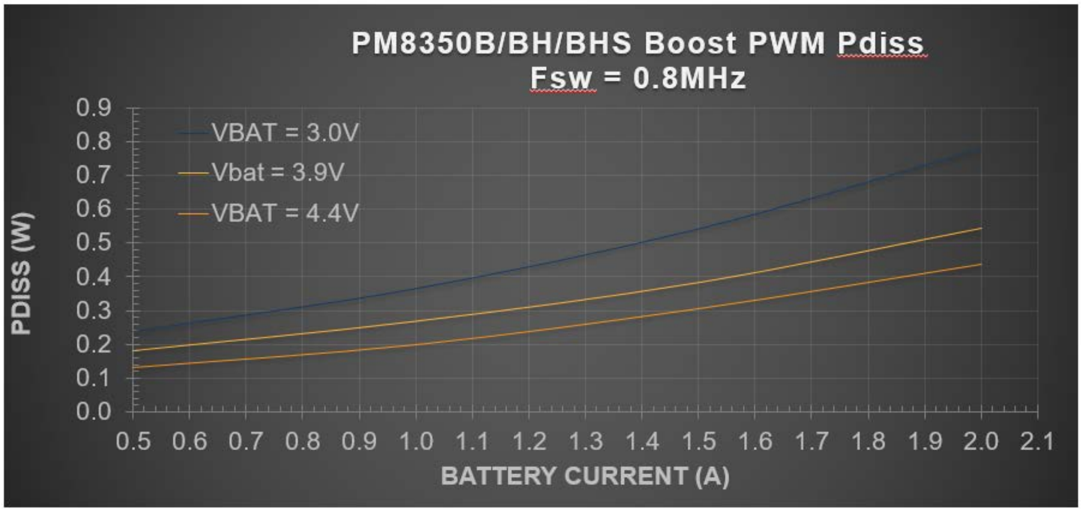
Table 3-11 Reverse boost specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Eff_{\_BOOST\_PWM}$	Boost efficiency in PWM mode	V_{BATT} = 4.0 V, PWM mode, F_{SW} = 0.8 MHz, 1.0 A Load	–	95	–	%
		V_{BATT} = 4.0 V, PWM mode, F_{SW} = 0.8 MHz, 1.5 A Load	–	95	–	%
$Eff_{\_BOOST\_PFM}$	Boost efficiency in PFM mode	V_{BATT} = 4.0 V, PFM mode, 10 mA load	–	81	–	%
DC_{BOOST}	Boost duty cycle		0	–	75	%



Measured data under the following conditions: USB_IN = 5 V (measured at the USB_IN input capacitor), Vbatt = 3/3.9/4.4 V, Fsw = 800 kHz
Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF, Cvph = 2 × 10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-5 PM8350B/BH/BHS Reverse Boost Efficiency



Measured data under the following conditions: USB_IN = 5 V (measured at the USB_IN input capacitor), Vbatt = 3/3.9/4.4 V, Fsw = 800 kHz
Cyntec HTQL25201B 0.47 µH 13.5 mΩ inductor; Cusb = 4.7 µF, Cmid = 2 × 10 µF, Cvph = 2 ×10 µF, Cvbat = 10 µF, Cfly = 3 × 22 µF

Figure 3-6 PM8350B/BH/BHS Reverse Boost Pdiss

3.5.6 Battery interface specification

Table 3-12 Battery interface specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QBAT						
R_{DSON_BF}	QBAT on-resistance	Battery FET (5 V), VPH_PWR to VBAT_PWR ball-to-ball resistance	–	5.0	6.6	mΩ
I_{BF_DC}	Maximum continuous DC QBAT current	Battery discharging	–	–	10	A
I_{BF_PEAK}	Peak QBAT current	Battery discharging, maximum 10 ms	–	–	12	A
$I_{LKG\_ VBAT\_SNS\_P}$	Leakage current into VBAT_SNS_P	PMIC Off, VBAT_SNS_P = 2.5 V, VBAT_SNS_M = 0 V	–	–	1	µA
		PMIC On, VBAT_SNS_P = 2.5 V to 4.5 V, VBAT_SNS_M = 0 V	–	–	2	µA
		PMIC On, VBAT_SNS_P = 5.0 V to 9.0 V, VBAT_SNS_M = 0 V	–	–	4	µA
QBAT soft-start						
$R_{DSON\_BF\_SS}$	Soft-start QBAT on-resistance		–	5.0		Ω
t_{BF_SS}	VPH rise time upon VBAT insertion	100 µF ~ 500 µF VPH_PWR capacitance; VPH from 10% to 90% of VBA; VBAT = 2.5 V - 4.5 V	0.25	–	10	ms
I_{BF_SS}	IBAT during QBAT soft-start	100 µF ~ 500 µF VPH_PWR capacitance; measured from VBAT insertion + 50 µs to VPH = VBAT; VBAT = 2.5 V - 4.5 V	–	–	1.5	A

Table 3-12 Battery interface specification (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QBAT fast-on						
	Charger to battery switch-over time	From V_{IN} drop below V_{UVLO} to QBAT starts to conduct, 2A I_{SYS}	–	–	10	µs
	VPH_PWR voltage dip below VBAT_PWR upon input removal	V_{USB_IN} = 5 V, I_{LIM_USB} = 3 A, VPH_PWR = 3.6 V, V_{BATT} = 3.5 V, charging disabled; 2 A I_{SYS}; C_{BAT} = 10 µF, CSYS = 22 µF	–	–	200	mV
R_{PD_VPH}	VPH pull-down load		–	100	–	Ω
Battery supplemental mode (BSM)						
V_{BSM_DET}	BSM detection comparator threshold	V_{PH_PWR} – V_{BAT_PWR} Programmable (8 settings in 10 mV steps)	-100	-50	-30	mV
		Accuracy	-25	–	+25	mV
t_{BSM_ENTRY}	BSM activation time	From V_{PH_PWR} drop below V_{BSM_DET} to QBAT starts to conduct	–	–	5	µs
$V_{PH\_DIP\_BSM}$	V_{PH_PWR} voltage dip below V_{BAT_PWR} upon BSM	V_{USB_IN} = 5 V, I_{LIM_USB} = 500 mA, V_{PH_PWR} = 3.6 V, V_{BATT} = 3.5 V, charging disabled; I_{SYS} rises from 100 mA to 3 A in 20 µs; C_{BAT} = 10 µF, C_{SYS} = 22 µF	–	–	200	mV
$I_{BSM\_TERM\_ANA}$	Analog BSM termination comparator range	Programmable (8 settings in 50 mA steps)	100	200	450	mA
	$I_{BSM\_TERM\_ANA}$ comparator accuracy	T = 0°C to +70°C	± 10% of setting ± 50			mA
$t_{BSM\_EXIT\_ANA}$	Analog BSM termination time	From IBAT across $I_{BSM\_TERM\_ANA}$ to QBAT stops conducting	–	–	5	µs
$I_{BSM\_TERM\_DIG}$	Digital BSM termination IADC samples	Programmable consecutive samples to determine IBAT (into the battery) exceeding 0mA	1	–	4	
$t_{BSM\_EXIT\_DIG}$	Digital BSM termination time	From IBAT (into the battery) exceeding 0 mA to QBAT stops conducting	–	–	50	ms

3.5.7 Miscellaneous specifications

Table 3-13 Miscellaneous specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VARB generation						
V_{ARB}	V_{ARB} voltage range	V_{USB_IN}/V_{WLS_IN} 3.5 V to 25 V	3.0	–	5.5	V
Thermal control and protection						
T_{CHG_TEMP}	Charger temp sensor accuracy	T_{CHG_TEMP} = 40°C to 80°C, V_{USB_IN}/V_{WLS_IN} ≥ 5 V	-2.0	–	+2.0	°C
		T_{CHG_TEMP} = 0°C to 150°C, V_{USB_IN}/V_{WLS_IN} ≥ 5 V	-3.0	–	+3.0	°C
T_{TEMP_RST}	Charger hot reset threshold	T_{DIE} rising, Programmable range in 10°C steps	100	120	130	°C
		Accuracy	-3.0	–	+3.0	°C
		Hysteresis, T_{DIE} falling	4.0	–	6.0	°C
T_{SHDN}	Charger over-temp shutdown threshold	T_{DIE} rising, Programmable range in 5°C steps	145	155	160	°C
		Accuracy	-3.0	–	+3.0	°C
		Hysteresis, T_{DIE} falling	15	20	25	°C
$T_{DIE\_REG\_L}$	Charger die temperature regulation window lower threshold	T_{DIE} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-3.0	–	+3.0	°C
$T_{DIE\_REG\_H}$	Charger die temperature regulation window upper threshold	T_{DIE} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-3.0	–	+3.0	°C
$T_{SKIN\_REG\_L}$	WLS/SKIN temperature regulation window lower threshold	T_{DIE} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2.0	–	+2.0	°C
$T_{SKIN\_REG\_H}$	WLS/SKIN temperature regulation window upper threshold	T_{DIE} rising, ADC-based digital comparator	-40	–	100	°C
		Accuracy	-2.0	–	+2.0	°C
$T_{CONN\_REG\_L}$	USB connector temperature regulation window lower threshold	T_{CONN} falling, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2.0	–	+2.0	°C
$T_{CONN\_REG\_H}$	USB connector temperature regulation window upper threshold	T_{CONN} rising, ADC-based digital comparator	40	–	100	°C
		Accuracy	-2.0	–	+2.0	°C
Watchdog and safety timers						
t_{CTOPC}	Pre-charge safety timer	Programmable (48 min to 191 min)	-6.0	–	6.0	%
t_{CTOFC}	Complete charge safety timer	Programmable (382 min to 1527 min)	-6.0	–	6.0	%
t_{CHG_HO}	Charger startup holdoff timer	Eight programmable settings	50	300	700	ms
		Accuracy	-1	–	15	%
t_{WD_SNARL}	Watchdog snarl timer	Programmable (1/16, 0.125, 0.25, 0.5, 1, 2, 4, 8) sec Accuracy	1/16 -6	– –	8.0 6.0	s %
t_{WD_BARK}	Watchdog bark timer	Programmable 16/32/64/128 sec Accuracy	16 -6	– –	128 6.0	s %
t_{WD_BITE}	Watchdog bite timer	Programmable 1/2/4/8 sec Accuracy	1 -6	– –	8.0 6.0	s %

3.6 Qualcomm battery gauge

The Qualcomm battery gauge hardware is basically an ADC scheduler that collects battery voltage, current, and temperature data.

Table 3-14 Qualcomm battery gauge performance specifications

Specification	Test conditions	Min	Typ	Max	Unit
Battery temperature reading error using 100 K, 1%, 4250 K beta thermistor, and 100 K pull-up	Ratiometric calibration data (0°C to 50°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-1.0	–	1.0	°C
	Ratiometric calibration data (-20°C to 70°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-1.5	–	1.5	°C
Battery temperature reading error using 10 K to 100 K, 1%, 4250 K beta thermistor, and 30 K pull-up	Ratiometric calibration data (0°C to 50°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-2.0	–	2.0	°C
	Ratiometric calibration data (-20°C to 70°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-3.0	–	3.0	°C
Battery temperature reading error using 10 K to 100 K, 1%, 4250 K beta thermistor, and 100 K pull-up	Ratiometric calibration data (0°C to 50°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-3.0	–	3.0	°C
	Ratiometric calibration data (-20°C to 70°C), VBAT = 2.5 to 5.25 V, IBAT = 0 A	-5.0	–	5.0	°C

3.7 ADC

This module contains all of the multiplexer circuitry for the PM8350B device, as well as two analog-to-digital converters (ADCs); one for voltage signals known as the VADC, and the other for current signals known as the IADC. This module is stand-alone from the other modules and takes care of all analog-to-digital needs on the PM8350B device for the charger module, battery interface module, the Qualcomm battery gauge module, GPIOs, and battery current limiting (BCL). The below tables are valid for the temperature range of -20°C to 70°C.

Table 3-15 Analog multiplexer and scaling functions

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
0	0	REF_GND	Pin: GND_MBG	1/1	Open	0 to 1.875
1	1	1P25VREF	Pin: REF_BYP	1/1	Open	0 to 1.875
2	2	VREF_VADC	Internal: VADC LDO	1/1	Open	0 to 1.875
3	3	DIE_TEMP	Internal: DIE_TEMP	1/1	Open	0 to 1.875
4	4	AMUX_THM1	Pin: BATT_THERM	1/1	Open	0 to 1.875
5	5	AMUX_THM2	Pin: BATT_ID	1/1	Open	0 to 1.875
6	6	AMUX_THM3 using SMB_TEMP input	Pin: SMB_TEMP	1/1	Open	0 to 1.875
7	7	AMUX_THM4	Pin: USB_THERM	1/1	Open	0 to 1.875
8	8	AMUX_THM5	Pin: OPTION	1/1	Open	0 to 1.875
9	9	AMUX_THM6	Pin: GPIO_06 (LV)	1/1	Open	0 to 1.875
A	10	AMUX1_GPIO	Pin: GPIO_01 (MV)	1/1	Open	0 to 1.875
B	11	AMUX2_GPIO	Pin: GPIO_02 (MV)	1/1	Open	0 to 1.875
C	12	AMUX3_GPIO	Pin: GPIO_03 (MV)	1/1	Open	0 to 1.875
D	13	AMUX4_GPIO	Pin: GPIO_04 (MV)	1/1	Open	0 to 1.875
8E	142	VPH_PWR	Pin: VPH_PWR	1/3	Open	0 to 5
8F	143	VBATT_SNS_P	Pin: VBATT_SNS_P	1/3 for 1S 1/6 for 2S	Open	1S: 0 to 5 2S: 0 to 9.6
10	16	CHG_TEMP	Pin: CHG_TEMP	1/1	Open	0 to 1.875
11	17	USB_IN_V/16	Pin: USB_IN	1/16	Open	0 to 25
12	18	VDC/16	Pin: WLS_IN	1/16	Open	0 to 25
13	19	CC1_ID	Pin: CC1_ID	1/1	Open	0 to 1.875
94	148	SBUx	Pin: SBU1/SBU2	1/3	Open	0 to 5.5
15	21	VREF_BAT_THERM	Pin: VREF_BAT_THERM	1/1	Open	0 to 1.875
96	150	VBAT_2S_MID	Pin: VBATT_2S_MID	1/3	Open	0 to 5
17	23	IIN_FB	Pin: IIN_FB	1/1	Open	0 to 1.875
24	36	AMUX_THM1	Pin: BATT_THERM	1/1	30 K	0 to 1.875
25	37	AMUX_THM2	Pin: BATT_ID	1/1	30 K	0 to 1.875

Table 3-15 Analog multiplexer and scaling functions (cont.)

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
26	38	AMUX_THM3	Pin: SMB_TEMP	1/1	30 K	0 to 1.875
27	39	AMUX_THM4	Pin: USB_THERM	1/1	30 K	0 to 1.875
28	40	AMUX_THM5	Pin: OPTION	1/1	30 K	0 to 1.875
29	41	AMUX_THM6	Pin: GPIO_06 (LV)	1/1	30 K	0 to 1.875
2A	42	AMUX1_GPIO	Pin: GPIO_01 (MV)	1/1	30 K	0 to 1.875
2B	43	AMUX2_GPIO	Pin: GPIO_02 (MV)	1/1	30 K	0 to 1.875
2C	44	AMUX3_GPIO	Pin: GPIO_03 (MV)	1/1	30 K	0 to 1.875
2D	45	AMUX4_GPIO	Pin: GPIO_04 (MV)	1/1	30 K	0 to 1.875
33	51	CC1_ID	Pin: CC1_ID	1/1	30 K	0 to 1.875
44	68	AMUX_THM1	Pin: BATT_THERM	1/1	100 K	0 to 1.875
45	69	AMUX_THM2	Pin: BATT_ID	1/1	100 K	0 to 1.875
46	70	AMUX_THM3	Pin: SMB_TEMP	1/1	100 K	0 to 1.875
47	71	AMUX_THM4	Pin: USB_THERM	1/1	100 K	0 to 1.875
48	72	AMUX_THM5	Pin: OPTION	1/1	100 K	0 to 1.875
49	73	AMUX_THM6	Pin: GPIO_06 (LV)	1/1	100 K	0 to 1.875
4A	74	AMUX1_GPIO	Pin: GPIO_01 (MV)	1/1	100 K	0 to 1.875
4B	75	AMUX2_GPIO	Pin: GPIO_02 (MV)	1/1	100 K	0 to 1.875
4C	76	AMUX3_GPIO	Pin: GPIO_03 (MV)	1/1	100 K	0 to 1.875
4D	77	AMUX4_GPIO	Pin: GPIO_04 (MV)	1/1	100 K	0 to 1.875
53	83	CC1_ID	Pin: CC1_ID	1/1	100 K	0 to 1.875
64	100	AMUX_THM1	Pin: BATT_THERM	1/1	400 K	0 to 1.875
65	101	AMUX_THM2	Pin: BATT_ID	1/1	400 K	0 to 1.875
66	102	AMUX_THM3	Pin: SMB_TEMP	1/1	400 K	0 to 1.875
67	103	AMUX_THM4	Pin: USB_THERM	1/1	400 K	0 to 1.875
68	104	AMUX_THM5	Pin: OPTION	1/1	400 K	0 to 1.875
69	105	AMUX_THM6	Pin: GPIO_06 (LV)	1/1	400 K	0 to 1.875
6A	106	AMUX1_GPIO	Pin: GPIO_01 (MV)	1/1	400 K	0 to 1.875
6B	107	AMUX2_GPIO	Pin: GPIO_02 (MV)	1/1	400 K	0 to 1.875
6C	108	AMUX3_GPIO	Pin: GPIO_03 (MV)	1/1	400 K	0 to 1.875
6D	109	AMUX4_GPIO	Pin: GPIO_04 (MV)	1/1	400 K	0 to 1.875
73	115	CC1_ID	Pin: CC1_ID (23)	1/1	400 K	0 to 1.875
8A	138	AMUX1_GPIO	Pin: GPIO_01 (MV)	1/3	Open	0 to 5
8B	139	AMUX2_GPIO	Pin: GPIO_02 (MV)	1/3	Open	0 to 5
8C	140	AMUX3_GPIO	Pin: GPIO_03 (MV)	1/3	Open	0 to 5

Table 3-15 Analog multiplexer and scaling functions (cont.)

Channel number (hex)	Channel number (dec)	Description	Source	Scaling	Internal pull-up	Input range (V)
8D	141	AMUX4_GPIO	Pin: GPIO_04 (MV)	1/3	Open	0 to 5
8F	143	VBATT_SNS_P	Pin: VBATT_SNS_P	1/3	Open	0 to 9.6
94	148	SBUx	Pin: SBU1/SBU2	1/3	Open	0 to 5.5
96	150	VBAT_2S_MID	Pin: VBATT_2S_MID	1/3	Open	0 to 5

Table 3-16 ADC electrical specifications

Parameter	Conditions	Min	Typ	Max	Unit
1/1 channel end-to-end gain error for absolute calibration	Absolute calibration data result (-20°C to 70°C), VBAT = 2.5 to 5.25 V	-0.5	–	0.5	mV
1/1 channel end-to-end offset error for absolute calibration	Absolute calibration data result (-20°C to 70°C), VBAT = 2.5 to 5.25 V	-2	±0.5	2	mV
1/1 channel end-to-end accuracy with internal pull-up and ratiometric calibration	Ratiometric calibration data result (reported ratio will be within specified tolerance of actual ratio) (-20°C to 70°C), VBAT = 2.5 to 5.25 V	-0.6	0.3	0.6	%
1/3 channel end-to-end accuracy	Calibrated data result, (-20°C to 70°C), VBAT = 2.5 to 5.25 V, input = 0.5 V to 5.25 V	-0.45	–	0.45	%
1/3 channel end-to-end accuracy on VBATT_SNS_P to PACK_SNS_M inputs	Calibrated data result, 25°C, VBAT = 2.5 to 5.25 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to SYS_GND	-0.2	–	0.2	%
1/3 channel end-to-end accuracy on VBATT_SNS_P to PACK_SNS_M inputs	Calibrated data result, (-20°C to 70°C), VBAT = 2.5 to 5.25 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to SYS_GND	-0.3	–	0.3	%
1/6 channel end-to-end accuracy on VBATT_SNS_P to PACK_SNS_M inputs	Calibrated data result, (-20°C to 70°C), VBAT = 5 V to 10.5 V, VBAT_SNS and PACK_SNS pins with ±200 mV of offset relative to SYS_GND	-0.3	–	0.3	%
ADC resolution (LSB) for absolute measurement	1/1 channel	–	64.879	–	µV
	Scaled to 1/3 channel	–	194.637	–	µV
	Scaled to 1/6 channel	–	389.274	–	µV
ADC resolution (LSB) for ratio measurement	1/1 channel, ratiometric calibration - result is a 14 bit ratio from 0 (0x0000) to 1 (0x4000)	–	0.006104	–	%
Analog bandwidth (anti-alias filter)		–	500	–	kHz
ADC LDO voltage		1.847	1.875	1.903	V
ADC sample clock		–	4.8	–	MHz
ADC conversion time	1K decimation ratio, 4.8 MHz sample clock, SINC2 conversion	–	654	700	µs
Current consumption – ADC only	VADC active – does not include other PMIC infrastructure	N/A	450	500	µA
Current consumption – ADC and required infrastructure hardware	VADC, MBG, and ADC clock source active	N/A	1000	1500	µA

Table 3-16 ADC electrical specifications (cont.)

Parameter	Conditions	Min	Typ	Max	Unit
100 k pull-up	Trimmed value	99.5	100	100.5	kΩ
400 k pull-up	Trimmed value	398	400	402	kΩ
30 k pull-up	Trimmed value	29.7	30	30.3	kΩ
Pull-up temperature coefficient		-100	–	100	ppm/°C
Pull-up aging	Value change over time and temperature cycling	-0.5	–	0.5	%
1/1 channel AMUX input resistance		10	–	–	MΩ
1/3 and 1/6 channel AMUX input resistance		1	–	–	MΩ
Leakage current - all pins using internal pull-up resistors	With Vbatt and aVdd present, apply 1.8 V to pin and monitor current, (-20°C to 70°C), VBAT = 2.5 to 5.25 V	–	–	10	nA
Balancing FET resistance (Only in ADC_BG AHM)	Rdson for both cell balancing FETs (0°C to 70°C), VBAT = 6.8 to 10 V, with mid-node at 3.4 V to 5 V	10	20	30	Ω

Table 3-17 Internal current sensing specifications

Parameter	Conditions	Min	Typ	Max	Unit
Battery current sensing range	VBAT = 3.0 V to 4.75 V T = 0 to 70°C	8.5	10	–	A
Battery current sensing offset	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 8.5 A T = 25°C	-11	–	+11	mA
Battery current sensing offset	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 8.5 A T = 0 to 70°C	-15	–	+15	mA
Battery current gain error	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 1 A T = 0 to 70°C	-2	–	+2	%
Battery current gain error	VBAT = 3.0 V to 4.75 V IBAT = 1 A to 5 A T = 25°C	-3	–	+3	%
Battery current gain error	VBAT = 3.0 V to 4.75 V IBAT = 1 A to 5 A T = 0 to 70°C	-4	–	+4	%
Battery current gain error	VBAT = 3.0 V to 4.75 V IBAT = 5 A to 8.5 A T = 25°C	-3.5	–	+3.5	%
Battery current gain error	VBAT = 3.0 V to 4.75 V IBAT = 5 A to 8.5 A T = 0 to 70°C	-5	–	+5	%
ADC LSB		–	305.185	–	µA
Current sensing noise	VBAT = 3.0 V to 4.75 V IBAT = 1 A to 8.5 A T = 0 to 70°C	–	–	20	mA

Table 3-18 External current sensing specifications

Parameter	Conditions	Min	Typ	Max	Unit
Battery current sensing range	VBAT = 3.0 V to 4.75 V T = 0 to 70°C	10	–	–	A
Battery current sensing offset	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 11 A T = 25°C Offset auto calibration enabled	-6	–	+6	mA
Battery current sensing offset	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 11 A T = 0 to 70°C Offset auto calibration enabled	-6	–	+6	mA
Battery current relative error	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 11 A T = 25°C	-0.75	–	+0.75	%
Battery current relative error	VBAT = 3.0 V to 4.75 V IBAT = 0 A to 11 A T = 0 to 70°C	-1	–	+1	%
ADC LSB		–	305.185	–	µA
Sense resistor value [1]	Programmable external sense range	1	2	5	mΩ
Sense resistor accuracy	This is recommended accuracy. Sense resistor error is not included in the error specifications above and must be added to the error specifications for end to end accuracy.	–	0.50	1	%
Current sensing noise	VBAT = 3.0 V to 4.75 V IBAT = 1 A to 10 A T = 0 to 70°C	–	–	–	
	1 mΩ sense resistor	–	20	–	mA
	2 mΩ sense resistor	–	10	–	mA
	5 mΩ sense resistor	–	5	–	mA

1. OPTION pin (103) must be pulled low with resistor as show below to configure PMIC to support external sensing:
    - 2S, 5 mΩ Rsense: 0 Ω (GND)
    - 2S, 2 mΩ Rsense: 23.2 kΩ
    - 2S, 1 mΩ Rsense: 45.2 kΩ
    - 2S, internal sensing: 78.7 kΩ
    - 1S, 5 mΩ Rsense: 127 kΩ
    - 1S, 2 mΩ Rsense: 221 kΩ
    - 1S, 1 mΩ Rsense: 432 kΩ
    - 1S, internal sensing: Open (float)

Table 3-19 BAT_THERM range and accuracy

Parameter	Minimum value	Ideal value	Maximum value
Thermistor value	10 K, B = 4250	100 K, B = 4250	100 K, B = 4250
Internal pull-up value	30 K	100 K	100 K
Maximum error	1°C	0.9°C	0.9°C

Table 3-20 BAT_ID range and accuracy

Parameter	Minimum value	Ideal value	Maximum value
BAT_ID value	1 K	100 K	450 K
Internal pull-up value	100 K	100 K	100 K
Maximum error	9%	0.7%	0.5%

3.8 Battery current limiting (BCL)

BCL is a feature that supports system-wide mitigation based on high battery current or low battery voltage conditions. BCL on the PM8350B device uses the ADC module, dedicated hardware comparators, and signals from other hardware modules to trigger mitigation levels that are then relayed to the system to ensure mitigation is done when needed. This aids in preventing brownouts, UVLO, or OCP conditions that will cause abrupt hardware shutdowns.

Table 3-21 BCL specifications

Parameter	Min	Typ	Max	Unit
Comparator accuracy	-50	–	50	mV
Comparator hysteresis Low1/2 comparators	–	1% of $V_{threshold}$	–	V
I (Vbat) (per AHM) Active Off	 – –	 4 0.01	 – –	 µA µA
I (aVdd) (per AHM) Active Off	 – –	 10 0.01	 – –	 µA µA
Current monitoring range	0.078	–	10	A
Current monitoring accuracy (ADC accuracy) VBAT = 3.0 V to 4.75 V IBAT = 5 A to 8.5 A T = 0 to 70°C	-5% (internal) -1% (external)		5% (internal) -1% (external)	% %

3.9 OLED

The PM8350B/BH/BHS generates the biases for AMOLED displays. Pertinent performance specifications are listed in Table 3-22 through Table 3-24 below.

NOTE: Unless otherwise stated, T_A= -30°C to +85°C, VPH = 3.8 V, VOUT = 4.6 V. All voltages are relative to GND.

Table 3-22 ELVDD (OLED positive rail) specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPH	Input voltage range (operational)	Module operational range where performance specifications are met	2.5	3.8	5.0	V
I_{OUT}	Output current capability		800	–	–	mA
	Minimum VPH for rated performance	V_{OUT} = 4.6 V, I_{OUT} = 500 mA V_{OUT} = 4.6 V, I_{OUT} = 800 mA	2.5 2.9	– –	– –	V V
	Output voltage programming		4.6	4.6	5.2	V
	Resolution		–	25	–	mV
	DC accuracy	VPH = 3.8 V V_{OUT} = 4.6 V I_{OUT} = no load T_A = -30°C to +85°C	-0.8	–	0.8	%
		VPH = 3.8 V V_{OUT} = 4.6 V I_{OUT} = no load T_A = 25°C	-0.5	–	0.5	%
	DC line regulation	VPH = 2.5 V to 4.8 V V_{OUT} = 4.6 V I_{OUT} = 100 mA T_A = 25°C	–	0.015	–	%/V
	DC load regulation	VPH = 3.8 V V_{OUT} = 4.6 V I_{OUT} = no load - 800 mA T_A = 25°C	–	0.05	–	%/A
F_{SW}	Switching frequency		–	2.4	–	MHz
	No load ground current	VPH = 3.8 V I_{OUT} = no load V_{OUT} = 4.6 V T_A = 25°C	–	3.5	–	mA

Table 3-22 ELVDD (OLED positive rail) specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L	Inductor	Face value	2.2	2.2	–	µH
C	Capacitor	Capacitor face value at MID_ELVDD rail	30	–	–	µF
		Capacitor face value at VREG_ELVDD output	10	–	–	µF
		Capacitor face value at display connector	10	–	–	µF
	Output discharge times	Fast discharge enabled	–	2	–	ms
	Short circuit protection	Module is enabled Threshold is V_{OUT} < VPH	–	0.6	–	V
	Short circuit debounce	Programmable: 1 µs, 2 µs, 4 µs, and 16 µs	–	1	–	µs
	Overload protection threshold	Module is enabled V_{OUT} = 4.6 V to 5.2 V Threshold is a percentage of output voltage setting	–	85	–	%
	Overload protection debounce	Settings for 1, 2, 4, 8 ms	1	4	8	ms
R_{disp}	Discharge resistor	Fast discharge	–	90	–	Ω
		Slow discharge	–	150	–	Ω
I_{SHD}	Shutdown current	VPH_PWR = 4.8 V Module is disabled	–	1	–	µA
tss_disp	Soft start time	$V_{OUT} = 0.92 \times V_{OUT}$ VPH = 3.8 V, no load, QCT nominal BOM	–	1.7	–	ms

NOTE: Unless otherwise stated, T_A= -30°C to +85°C, VPH = 3.8 V, VOUT = -2.4 V. All voltages are relative to GND.

Table 3-23 ELVSS (OLED negative rail) specifications

Symbol/Single or dual phase operation	Parameter	Conditions	Min	Typ	Max	Unit
VPH	Input voltage range (operational)	Module operational range where performance specifications are met T_A = -30°C to 85°C	2.5	–	5.0	V
Single phase	Minimum VPH for rated performance Single phase	V_{OUT} = -6.6 V, I_{OUT} = 500 mA T_A = 25°C	2.9	–	–	V
Dual phase	Minimum VPH for rated performance Dual phase	V_{OUT} = -6.6 V, I_{OUT} = 800 mA T_A = 25°C	2.9	–	–	V
V_{OUT}	Output voltage Programming		-0.8	–	-6.6	V
Single or dual	DC accuracy	VPH = 3.8 V V_{OUT} = -2.4 V I_{OUT} = 100 mA T_A = 25°C	-25	–	25	mV
		VPH = 3.8 V V_{OUT} = -6.6 V I_{OUT} = 100 mA T_A = -30°C to 85°C	-60	–	60	mV
Single phase	DC load regulation	VPH = 3.8 V V_{OUT} = -2.4 V I_{OUT} = no load - 500 mA T_A = 25°C	–	0.1	–	%/A
Dual phase	DC load regulation	VPH = 3.8 V V_{OUT} = -2.4 V I_{OUT} = no load - 800 mA T_A = 25°C	–	0.1	–	%/A
Single phase	DC line regulation	VPH = 2.9 V to 5 V V_{OUT} = -2.4 V I_{OUT} = 100 mA T_A = 25°C	–	0.02	–	%/V

Table 3-23 ELVSS (OLED negative rail) specifications (cont.)

Symbol/Single or dual phase operation	Parameter	Conditions	Min	Typ	Max	Unit
Dual phase	DC line regulation	VPH = 2.9 V to 5 V V_{OUT} = -2.4 V I_{OUT} = 100 mA T_A = 25°C	–	0.02	–	%/V
F_{SW}	Switching frequency		–	1.48	–	MHz
Single phase	No load ground current	VPH = 3.8 V V_{OUT} = -4.0 V I_{OUT} = no load T_A = 25°C	–	1.1	–	mA
Dual phase	No load ground current	VPH = 3.8 V V_{OUT} = -4.0 V I_{OUT} = no load T_A = 25°C	–	1.5	–	mA
C_{OUT}	Output capacitor - single phase	Labeled value, VREG_ELVSS output	20	–	–	µF
	Output capacitor - dual phase	Labeled value, VREG_ELVSS output	40	–	–	µF
	Capacitor at display connector	Labeled value	10	–	–	µF
T_ss	Soft start time		–	1	–	ms
R_discharge	Discharge resistor	Output pulldown on module disable VPH = 3.8 V V_{OUT} = -4.0 V T_A = 25°C Fast discharge Slow discharge	– –	30 230	– –	Ω Ω
Overload	Overload protection threshold	V_{OUT} = -2.4 V VPH = 3.8 V Threshold is a percentage of target voltage	–	85	–	%
	ELVDD and ELVSS startup SCP	Positive voltage threshold at end of power up delay timer	–	200	–	mV
	Overload debounce time	Programmable settings	–	1	–	ms
Slew rate		Programmable settings	1	12	15	ms

NOTE: Unless otherwise stated, T_A= -30°C to +85°C, VPH = 3.8 V, VOUT = 7.6 V. All voltages are relative to GND.

Table 3-24 OLEDB bias performance specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPH	Input voltage range (operational)	Module operational range where performance specifications are met	2.5	–	5.0	V
	Minimum VPH for rated performance	V_{OUT} = 7.6 V, I_{OUT} = 150 mA T_A = 25°C	2.9	–	–	V
V_{OUT}	Output voltage programming	Programmable settings	5	–	8	V
	Fine programming resolution		–	25	–	mV
	DC accuracy	VPH = 3.8 V V_{OUT} = 5 V to 8 V, I_{OUT} = 30 mA T_A = 25°C	-0.5	–	0.5	%
I_{OUT}	Output current capacity		150	–	–	mA
	DC load regulation	VPH = 2.5 V V_{OUT} = 5 V to 8 V I_{OUT} = no load - 100 mA T_A = -30°C to +85°C	–	7	–	mV
	DC line regulation	VPH = 2.5 V to 4.8 V V_{OUT} = 7.6 V I_{OUT} = 30 mA T_A = 25°C	–	0.02	–	%/V
F_{SW}	Switching frequency		–	1.48	–	MHz
C_{OUT}	Output capacitor	Face value at output pin VREG_OLEDB	–	40	–	µF
		Labeled value, at display connector	–	10	–	µF
L_{OLEDB}	Boost inductor	Face value	–	6.8	–	µH
T_{PRECHG}	Startup precharge time	Starting V_{OUT} = 0 V Final V_{OUT} = VPH - 0.35 V VPH = 3.8 V I_{OUT} = 10 mA, T_A = 25°C	–	1	–	ms
T_ss	Soft start time	After precharge done Final VOUT = 90% of target voltage 5.0 V to 8.0 V VPH = 3.8 V I_{OUT} = 10 mA, T_A = 25°C	–	0.7	–	ms

Table 3-24 OLEDB bias performance specification (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{DISCHARGE}$	Discharge resistor	Output pulldown on module disable VPH = 3.8 V, T_A = 25°C	–	75	–	Ω
SCP	Short circuit protection threshold	VPH-V_{OUT}, module is enabled	–	1	–	V
	Debounce time		–	3	–	µs
Overload	Overload protection threshold	V_{OUT} = 5.0 V to 8.0 V percentage threshold based on output voltage settings	–	85	–	%
	Overload debounce time	Programmable settings = 1, 2, 4 ms	1	1	8	ms

Table 3-25 DDIC LDO regulator specifications

Parameter	Comments		Min	Typ	Max	Units	Note
Input voltage range			0.32	–	1.4	V	
Output voltage range			0.32	–	1.304	V	
V_{OUT} step size			–	8	–	mV	
Normal power mode							
Rated load current	Maximum load current at which all specifications are met at 100 mV headroom. Higher load current is possible at increased headroom.		300	–	–	mA	1
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error)	Measured at C_{OUT}. $I_{RATIO} = I_{LOAD}/I_{RATED}$ Headroom = 100 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	$V_{OUT} \geq 0.8$ V	- 1.3% - (12 mV + 30 mV) × I_{RATIO}	–	+1.3%	$\%V_{OUT}$	2
Overall DC error at nondefault voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error)	Measured at C_{OUT}. $I_{RATIO} = I_{LOAD}/I_{RATED}$ Headroom = 100 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	$V_{OUT} \geq 0.5$ V	- 2% - (12 mV + 30 mV) × I_{RATIO}	–	+2%	$\%V_{OUT}$	2
		$V_{OUT} < 0.5$ V, up to $I_{RATED}/4$)	- (10 + 3 + 8)	–	+10	mV	
Load transient undershoot, overshoot	Max load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 × I_{RATED} or higher. Compared to final settled value. Headroom = 100 mV		–40	–	+70	mV	
Startup settling time	To within 1% of final value. UL is with maximum C_{OUT} and max V_{SET}. LL is with minimum C_{OUT} and min V_{SET}		8	–	300	µs	3
Startup in-rush current	During start-up. Variation due to bulk capacitor size.		–	40	400	mA	
Dropout voltage	From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}	For Vph ≥ 3 V	–	–	54	mV	4
		For Vph < 3 V	–	–	65	mV	
Over current protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.		600	–	900	mA	

Table 3-25 DDIC LDO regulator specifications (cont.)

Parameter	Comments		Min	Typ	Max	Units	Note
Output noise density	Measured at C_{OUT}. LDO contribution only, assumes clean V_{IN}.	Headroom = 100 mV				$\mu V/\sqrt{Hz}$	
		100 Hz ≤ f ≤ 1 kHz	–	3	–		
		1 kHz ≤ f ≤ 10 kHz	–	1.5	–		
		10 kHz ≤ f ≤ 100 kHz	–	1.2	–		
		100 kHz ≤ f ≤ 1 MHz	–	0.5	–		
Power supply ripple rejection ratio (PSRR)	$I_{LOAD} = I_{RATED}$. From V_{IN} to V_{OUT}. Measured at C_{OUT}.	Headroom = 100 mV					
		50 Hz to 1 kHz	45	55	–	dB	
		1 kHz to 10 kHz	30	40	–	dB	
		10 kHz to 100 kHz	25	30	–	dB	
		100 kHz to 1 MHz	10	20	–	dB	
Ground current, no load (AHC disabled)	Measured at the battery. I_Q may be much higher if LDO is operated in drop-out condition.		–	95	130	µA	
Low-power mode							
Rated load current	Maximum load current at which all specifications are met. Higher load current is possible at increased headroom.		30	–	–	mA	1
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error)	Measured at C_{OUT}. Headroom = 100 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	$V_{OUT} \geq 0.8$ V	- (2.5% + 1.2 mV + 3mV)	–	+2.5%	$\%V_{OUT}$	2
Overall DC error at nondefault voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error)	Measured at C_{OUT}. Headroom = 100 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	$V_{OUT} \geq 0.5$ V)	- (3% + 1.2 mV + 3 mV)	–	+3%	$\%V_{OUT}$	2
		$V_{OUT} < 0.5$ V, up to $I_{RATED}/4$)	-20	–	+20	mV	

Table 3-25 DDIC LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units	Note
Load transient undershoot, overshoot	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 × I_{RATED} or higher. Compared to final settled value. Headroom = 100 mV	–40	–	+70	mV	
Dropout voltage	From package V_{IN} pin to V_{OUT} pin. Load at LPM I_{RATED}	–	–	85	mV	
Overcurrent protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.	60	–	90	mA	
Ground current, no load	Measured at the battery. I_Q may much be higher if LDO is operated in dropout condition. PMOS UL excludes the FF/125 corner (~20 µA).	–	20	26	µA	5
Normal and low-power mode						
Ground current, with load	% of the load current	–	–	0.5	% I_{LOAD}	
LDO discharge time to below 100 mV	Strong pulldown enabled. Typical at nominal C_{OUT}, UL is with maximum C_{OUT}.	–	0.1	2	ms	
VREG_OK threshold – during enable or step up		85%	90%	95%	V_{OUT}	
Forced bypass mode						
Ground current		–	2	5	µA	6
Retention mode						
Rated load current	Maximum load current at which all specifications are met.	30	–	–	mA	
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation and trim error)	Measured at Cout	-2.5%	–	2.5% + 25 mV		
Overall DC error at non default voltage (includes load and line regulation, temperature, VBAT, MBG variation and trim error)	Measured at Cout	-3%	–	3% + 25 mV		
Output ripple		–	25	50	mVpp	

Table 3-25 DDIC LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units	Note
Load transient undershoot, overshoot	Load step of $I_{BASELINE}$ to 10 × $I_{BASELINE}$ in 10 ms, with baseline current of 0.01 × I_{RATED} to 0.5 × I_{RATED}. Headroom = 100 mV. Compared to final settled value.	-40	–	70	mV	
Ground current, no load	Measured at the battery. IQ may much be higher if LDO is operated in drop-out condition.	–	1.5	2.5	μA	

1. The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom, (this is, the difference between V_{IN} and V_{OUT}). For low-power mode, the LDO should be switched to normal power mode if the load current is expected to be above the rated current.
2. At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull down may need to be enabled to meet the specifications.
3. The settling time is for startup, and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.
4. Dropout voltage is defined as follows:
   a. Apply the specified load current.
   b. Set $V_{IN} = V_{OUT} + 0.5$ V.
   c. Measure the output voltage.
   d. Reduce V_{IN} until V_{OUT} is reduced by 100 mV.
   e. Calculate dropout voltage as $V_{IN} - V_{OUT}$ in this condition.
5. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in the low headroom configuration. Disabling the current limiting feature or giving enough headroom per the dropout requirement can prevent mistriggering and reduce the ground current.
6. In bypass mode, there is an active gate to source clamp to protect the LV NMOS.

3.10 Haptics

Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics are used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as confirmation of touchscreen contact, or dynamic feedback to enhance gaming experiences. Electrical specifications are listed in Table 3-27.

Unless otherwise specified, test conditions assume that VHPWR = 3.8 V, T_A = -30°C to +85°C.

Table 3-26 Haptics driver electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{HPWR_DC}	H-bridge driver input supply average DC voltage applied at HPWR		5.0	–	10.6	V
V_{HPWR_TRAN}	H-bridge driver input supply voltage applied at HVDD	Applied for < 1 ms	2	–	13	V
V_{HOUT_AVG}	Differential output drive voltage averaged over one PWM cycle.	V_{HPWR} = 10.6 V, No load	0	–	10.2	V
I_{LIM}	Cycle-by-cycle output current limit	Programmable: 1, 1.5, 2 A	–	1.5	–	A
I_{HVDD}	Module operating current	Switching, I_{HOUT} = 0, HPWR = 10.5 V	–	4	5	mA
		Switching, I_{HOUT} = 0, HPWR = 5 V	–	2.5	3	mA
IQ_SHD	Module shutdown current	T_A ≤ 60°C, HPWR = VPH ≤ 4.8 V (boost disabled)	–	1	–	µA
		T_A ≤ 60°C, HPWR > VPH (boost enabled - retention mode)	–	2	–	µA
R_{DSON}	ON resistance of high side switch	V_{HPWR} > 5 V	–	350	–	mΩ
	ON resistance of low side switch		–	150	–	mΩ
F_{PWM}	Internal PWM frequency	Programmable	150	–	1200	kHz
ΔF_{PWM}	Internal PWM frequency inaccuracy		-6	–	6	%
T_{LRA}	Open loop LRA drive programmable frequency	Programmable	75	–	1000	Hz

Table 3-27 PM8350B 5 V Haptics boost electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_dc	DC input voltage range at VPH_PWR	Full parametric compliance	2.5	–	5.0	V
VIN_trans	Transient input voltage range at VPH_PWR	Bounded by UVLO and max battery voltage. Transient < 1 ms	2	–	5.25	V
Vout			–	5	–	V
Iout [1]	Output current (continuous) 2.2 µH inductor 3 A current limit	Vout = 5 V, VPH > 4.2 V Vout = 5 V, 3.8 V < VPH < 4.2 V Vout = 5 V, 3.4 V < VPH < 3.8 V Vout = 5 V, 3.0 V < VPH < 3.4 V Vout = 5 V, 2.5 V < VPH < 3.0 V	– – – – –	– – – – –	1650 1450 1250 1100 850	mA mA mA mA mA
	Extend operational output current range	Vout = 5 V, 2.15 V < Vin < 2.5 V, T = 25°C	–	750	–	mA
Ipk_limit	Peak inductor current limit		–	3	–	A
Fsw	Switching frequency		–	0.8	–	MHz

Table 3-27 PM8350B 5 V Haptics boost electrical specifications (cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
L	Inductor value	Derated at DC bias current at Isat	1.54	–	–	µH
Cout_min	Output capacitance (derated)	Derated for temp, voltage, aging. Typical BOM = 4 × 4.7 µF 0402	5	–	–	µF
Vout_acc	VOUT DC accuracy	Across temp and voltage	-2	–	2	%
R_dson,p	High side PFET Rds, on		–	110	–	mΩ
R_dson,n	Low side NFET Rds, on		–	60	–	mΩ
IQ_SHD	Module shutdown current	VPH = 2.5 V to 4.8 V	–	0.4	–	µA
IQ_stby	No load ground current	VPH = 3.8 V, no load, low power retention mode	–	–	7.5	µA
		VPH = 3.8 V, no load, fast recovery retention	–	–	30	µA
IQ_BST	Module operating current	VPH = 3.8 V, switching, no load, active pulse skip enabled, VOUT = 5 V	–	–	1.8	mA
Vout ripple	Steady state ripple	Not in PSM. Load is within Iout_max limits	–	–	150	mV_pk pk
	Steady state ripple in PSM operation	PSM operation. VIN = 5 V, Vout = 5 V	–	–	400	mV_pk pk

1. The Iout limits use the reference BOM of 2.2 µH inductor

Table 3-28 PM8350BH/BHS 10 V Haptics boost electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_dc	DC input voltage range at VPH_PWR	Full parametric compliance	2.5	–	5.0	V
VIN_trans	Transient input voltage range at VPH_PWR	Bounded by UVLO and max battery voltage. Transient < 1 ms	2	–	5.25	V
Vout_prgm	Programmable output voltage range	Programmable with 50 mV steps	5	–	10	V
Iout (Vout = 10 V)	Output current (continuous) 1 µH inductor 4.4 A current limit	Vout = 10 V, VPH > 4.2 V	–	–	1050	mA
		Vout = 10 V, 3.8 V < VPH < 4.2 V	–	–	950	mA
		Vout = 10 V, 3.4 V < VPH < 3.8 V	–	–	800	mA
		Vout = 10 V, 3.0 V < VPH < 3.4 V	–	–	650	mA
		Vout = 10 V, 2.5 V < VPH < 3.0 V	–	–	450	mA
	Extend operational output current range	Vout = 10 V, 2.15 V < VPH < 2.5 V T = 25°C	–	300	–	mA
Iout (Vout = 5 V, OTG mode settings)	Output current (continuous) 1 µH inductor 4.4 A current limit	Vout = 5 V, VPH > 4.2 V	–	–	2200	mA
		Vout = 5 V, 3.8 V < VPH < 4.2 V	–	–	1800	mA
		Vout = 5 V, 3.4 V < VPH < 3.8 V	–	–	1600	mA
		Vout = 5 V, 3.0 V < VPH < 3.4 V	–	–	1500	mA
		Vout = 5 V, 2.5 V < VPH < 3.0 V	–	–	1150	
	Extend operational output current range	Vout = 5 V, 2.15 V < VPH < 2.5 V T = 25°C	–	1000	–	mA
Ipk_limit	Peak inductor current limit		–	4.4	–	A
	Ipk_limit_acc		-10	–	10	%
Fsw	Switching frequency		–	3.2	–	MHz
L	Inductor value	Derated at DC bias current at Isat	0.7	–	–	µH

Table 3-28 PM8350BH/BHS 10 V Haptics boost electrical specifications (cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Cout_min	Output capacitance (derated)	Derated for temp, voltage, aging. Vout = 10 V Typical BOM = 4 × 4.7 µF 0402	2	–	–	µF
Vout_acc	VOUT DC accuracy	Across temp and voltage	-2	–	2	%
R_dson,p	High side PFET Rds, on		–	100	–	mΩ
R_dson,n	Low side NFET Rds, on		–	50	–	mΩ
IQ_SHD	Module shutdown current	VPH = 3.8 V, T = 25°C	–	0.4	–	µA
IQ_stby	No load ground current	VPH = 3.8 V, no load, low power retention mode, RM_VSET=7.5 V	–	–	10	µA
		VPH = 3.8 V, no load, fast recovery retention, RM_VSET=7.5 V	–	–	40	µA
IQ_BST	Module operating current	VPH = 3.8 V, switching, no load, active pulse skip enabled, VOUT = 10 V	–	–	3	mA
T_startup	Start up time	Fast recovery retention mode voltage = 7.5 V transition to 10 V Active Mode vreg_ready	–	–	220	µs
		LPRM retention mode voltage = 7.5 V transition to 10 V Active Mode vreg_ready	–	–	250	µs
		Soft start. VPH = 3.8 V to VREG_BST = 10 V	–	–	250	µs
Vout ripple	Steady state ripple	Load is within Iout_max limits. Vout = 10 V	–	–	120	mV_pk pk
	Steady state ripple in PSM operation	VIN = 5 V, Vout = 10 V	–	–	200	mV_pk pk

4 Mechanical information

4.1 Device physical dimensions

The PM8350B/PM8350BH/PM8350BHS is available in the 165 FOWNSP package that includes ground pins for improved grounding, mechanical strength, and thermal continuity. The 165 FOWPSP package has a 6.24 mm × 4.42 mm body with a maximum height of 0.57 mm. Pad 1 is located by an indicator mark on the top of the package. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download *Package Outline Drawing, FOWNSP165, 6.24 × 4.42 × 0.57 mm, M330* (NT90-PP422-1) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PP422-1

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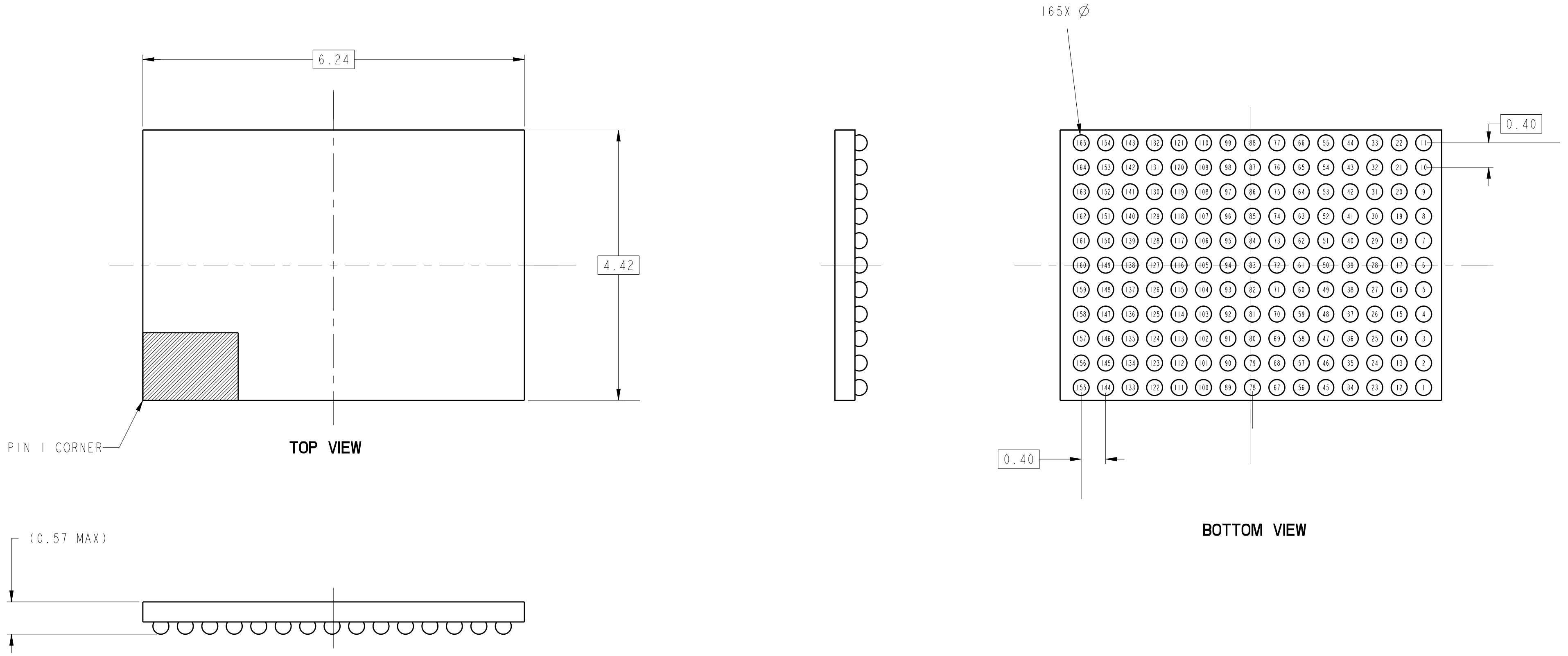

Figure 4-1 165 FOWNSP package outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

4.2.1 PM8350B/PM8350BH/PM8350BHS part marking

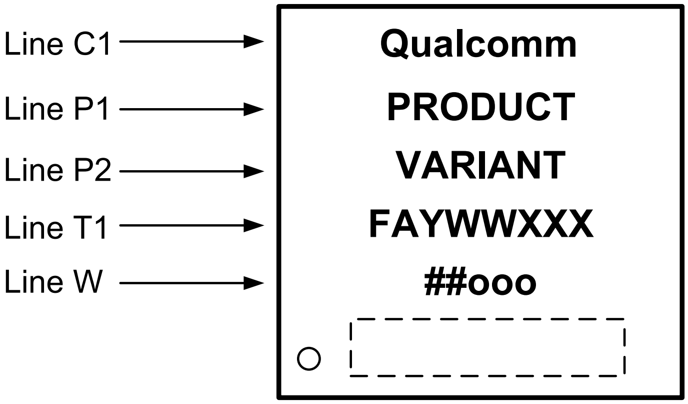

Figure 4-2 Device marking (top view, not to scale)

Table 4-1 PM8350B/PM8350BH/PM8350BHS device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ PM8350B ■ PM8350BH ■ PM8350BHS
P2	VARIANT (PRR-BB)	Device variant information ■ See Table 4-3 for the assigned values.
T1	FAYWWXXX	F = wafer fab source of supply code ■ F = F for TSMC A = assembly (ball drop) code ■ A = E for ASE, Taiwan ■ A = T for NEPES, Philippines Y = single/last digit of year WW = two-digit work week of year specified by Y
W	##ooo	## = wafer number ooo = optional engineering information
	○ Blank or random	Pin 1 or pin A1 indicator Additional content, as necessary

4.3 Device ordering information

4.3.1 Specification-compliant devices

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-2 and Table 4-3.

Table 4-2 Device identification code for PM8350B/PM8350BH/PM8350BHS

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example 1	PM-8350B	-0	-FOWNSP	165			-MT	-00	-0	
Example 2	PM-8350BH	-0	-FOWNSP	165			-MT	-00	-0	
Example 3	PM-8350BHS	-0	-FOWNSP	165			-MT	-00	-0	

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: PM-8350B-0-FOWNSP165-MT-00-0
- Example 2: PM-8350BH-0-FOWNSP165-MT-00-0
- Example 3: PM-8350BHS-0-FOWNSP165-MT-00-0

Table 4-2 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification details

Device	Sample type [1]	Product configuration code (P)	Product revision code (RR)	Feature code (BB) [2]	Hardware version	Source configuration code (S) [3]
PM8350B	ES1	0	00	–	v1.0	0
PM8350BH	ES1	0	00	–	v1.0	0
PM8350BHS	ES1	0	00	–	v1.0	0
PM8350B	ES2/CS [4]	0	01	–	v2.0	0
PM8350BH	ES2/CS [4]	0	01	–	v2.0	0
PM8350BHS	ES2/CS [4]	0	01	–	v2.0	0
PM8350B	CS [5]	0	01	00	v2.0	0
PM8350BH	CS [5]	0	01	00	v2.0	0
PM8350BHS	CS [5]	0	01	00	v2.0	0

1. ES2 PMIC devices must be paired with other ES2 PMIC devices only. ES1 and ES2 PMIC devices cannot be mixed and matched on the same design. There is no concern with ES1 or ES2 devices mixed/matched with any version of the SM8350 device.
2. BB is the feature code that identifies an IC’s specific feature set, which distinguishes it from other versions or variants.
3. S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-4.
4. PM8350B/BH/BHS ES2 and CS parts have the same PRR code. All devices with date code YWW ≥ 029 or from the following lots are of CS quality:
   000FE027YXH.0E004
   000FE022ZSS.0E006
   E00FT0246K8.0D014
   000FE027YXH.0E002
   000FE027YXH.0E052
   E00FT0246K8.0D006
   000FE027YXH.0E003
   000FE027YXH.0E055
   000FE027YXH.0E003
   000FE027YXH.0E055
   000FE027YXH.0E005
   E00FT0246K8.0D007
   E00FT0246K8.0D005
   E00FT0296WM.0D007
   000FE027YXH.0E007
5. CS parts with PRR = 001 and BB = 00 have *Charger Issue 4-15* fixed as documented in *PM8350B/PM8350BH/PM8350BHS Device Revision Guide* (80-PT205-4). It is recommended to use these parts for SM8350/SM8450/SM8475 designs.

Table 4-4 Source configuration code

S value	Die	F value = F
0	Digital	TSMC

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package’s moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-5.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hrs.	≤ 30°C/60% RH; PM8350B/PM8350BH/PM8350BHS rating
4	72 hrs.	≤ 30°C/60% RH
5	48 hrs.	≤ 30°C/60% RH
5a	24 hrs.	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM8350B/PM8350BH/PM8350BHS devices are classified as MSL3; the qualification temperature was 260°C +0°/-5°C***. This qualification temperature (260°C +0°/-5°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE: Click the following link to download the *PM8350B/BH/BHS 165FOWNSP Package Thermal Model Icepak* (HS11-PT205-5HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PT205-5HW

Click the following link to download the *PM8350B/BH/BHS 165FOWNSP Package Thermal Model Flowtherm* (HS11-PT205-6HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PT205-6HW

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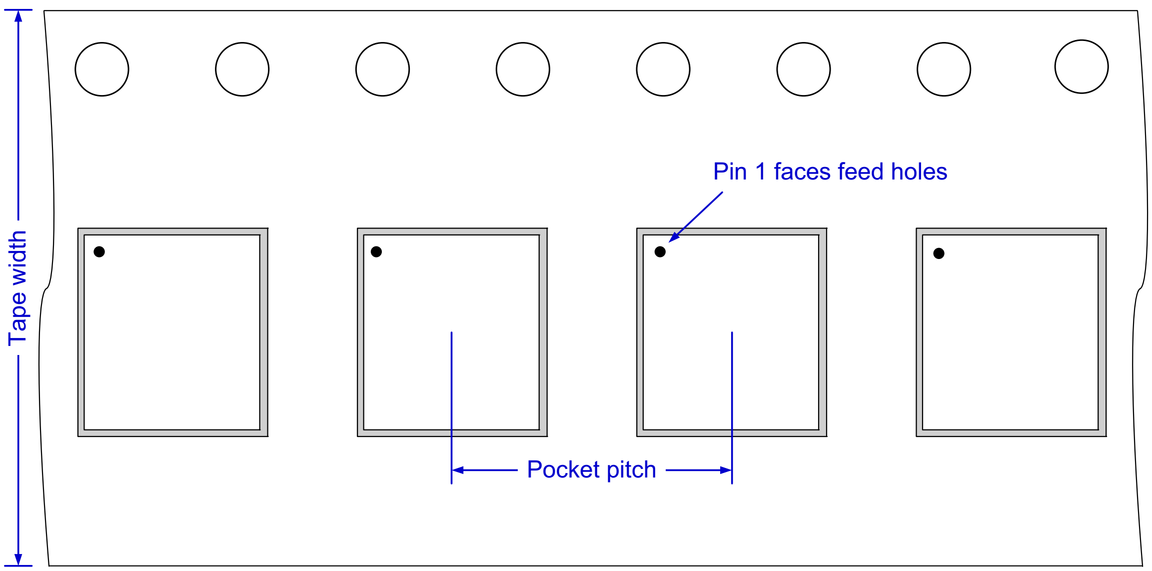
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM8350B/PM8350BH/PM8350BHS tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	16 mm
Units per reel:	4000	Hub diameter:	178 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

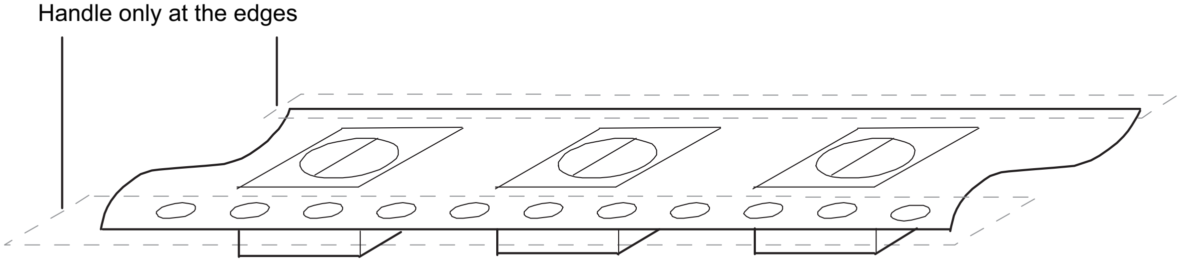


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8350B/PM8350BH/PM8350BHS devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the FOWNSP165 should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

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7 Part reliability

7.1 Reliability qualifications summary: TSMC

Table 7-1 Silicon reliability results: TSMC

Device qualification Tests, standards, and conditions	Sample size number of lots TSMC	Result
Early life failure rate (ELFR) in DPPM HTOL: JESD22-A108-A Total samples from three different wafer lots	240 (3 lots × 80 pcs)	Pass DPPM < 1000
Average failure rate (AFR) in FIT (λ) failures per billion device hours; functional HTOL JESD22-A108-A (Total samples from three different wafer lots)	240 (3 lots × 80 pcs)	Pass FIT < 50
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	240 (3 lots × 80 pcs)	Pass MTTF > 20
ESD – human body model (HBM) rating JESD22-A114-F	42 (2 lots × 21 pcs)	Pass 2000 V
ESD – charged device model (CDM) rating JESD22-C101-E	48 (2 lots × 24 pcs)	Pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C	18 (3 lots × 6)	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vddmax per device specification; temperature: 85°C	18 (3 lots × 6)	Pass

Table 7-2 Package reliability results for TSMC

Package qualification Tests, standards, and conditions	Sample source (ASE)	Sample source (NEPES)	Results
Moisture resistance test (MRT): MSL3; J-STD-020-D 3 × reflow cycles at 255°C +5/-0°C	462 (3 lots × 154 pcs)	462 (3 lots × 154 pcs)	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Minimum soak time at minimum/maximum temperature: 5 minutes Cycle rate: 2 cycles per hour (CPH) MSL3 preconditioning: JESD22-A113-F Reflow temperature: 255°C +5/-0°C	231 (3 lots × 77 pcs)	231 (3 lots × 77 pcs)	Pass
Unbiased highly accelerated stress test (UHAST): JESD22-A118 MSL3 preconditioning: JESD22-A113-F Reflow temperature: 255°C +5/-0°C	231 (3 lots × 77 pcs)	231 (3 lots × 77 pcs)	Pass
High-temperature storage life: JESD22-A103-D Temperature 150°C, 1000 hours	231 (3 lots × 77 pcs)	231 (3 lots × 77 pcs)	Pass
Biased highly accelerated stress test (BHAST): JESD22-A110 MSL3 preconditioning: JESD22-A113 Reflow temperature: 260°C +0/-5°C	77 (1 lot)	77 (1 lot)	Pass
Physical dimensions: JESD22-B100-A	15 (1 lot)	15 (1 lot)	Pass
Solder ball shear: JESD22-B117-B Total samples from three assembly lots at each SAT	45 (3 lots × 15 pcs)	45 (3 lots × 15 pcs)	Pass

7.2 Qualification sample description

Table 7-3 Device characteristics

Category	Definition
Device name	PM8350B/PM8350BH/PM8350BHS
Package type	FOWNSP165
Package body size	6.24 mm × 4.42 mm × 0.57 mm
Solder ball composition	SAC405
Process	150 nm
Fab sites	■ TSMC
Assembly sites	■ ASE, Taiwan ■ NEPES, Philippines
Solder ball pitch	0.40 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	November 2019	Initial release
B	March 2020	■ Global: Removed ERM support ■ Cover page: Updated the key features and high-level block diagram ■ Figure 1-1 PM8350B/PM8350BH/PM8350BHS high-level functional block diagram: Updated the block diagram ■ Table 1-1 PM8350B/PM8350BH/PM8350BHS features: Updated OLED and Haptocs feature ■ Section 1.3 PM8350B SKUs: Updated the table and added a note for PM8350BHS ■ Chapter 3 Electrical specifications: Added this chapter ■ Section 4.2 Part marking: Added this section ■ Section 4.3 Device ordering information: Added this section ■ Section 4.4 Device moisture-sensitivity level: Added this section ■ Section 4.5 Thermal characteristics: Added this section ■ Chapter 5 Carrier, storage, and handling information: Added this chapter ■ Chapter 6 PCB mounting guidelines: Added this chapter
C	September 2020	■ Table 1-1 PM8350B/PM8350BH/PM8350BHS features: Updated the haptics feature ■ Section 1.3 PM8350B SKUs: Updated the Haptics boost support for PM8350B ■ Table 3-21 ELVDD (OLED positive rail) specifications: Updated the output current value ■ Table 3-22 ELVSS (OLED negative rail) specifications: Updated the table ■ Table 3-24 Haptics driver electrical specifications: Updated the minimum value of H-bridge driver input supply voltage and updated the IHVDD specification ■ Table 3-25 PM8350B 5 V Haptics boost electrical specifications: Updated this table ■ Table 3-26 PM8350BH/BHS 10 V Haptics boost electrical specifications: Updated this table ■ Table 4-3 Device identification details: Updated the device identification details for ES2 samples

Revision	Date	Description
D	October 2020	■ Cover page: Added LDO supply feature ■ Table 1-1 PM8350B/PM8350BH/PM8350BHS features: Added LDO supply feature ■ Section 1.3 PM8350B SKUs: Added a note for haptics boost ■ Table 2-7 Pad descriptions – GPIO and other pins: Updated the functional description of option 3 and option 4 pins ■ Table 3-1 Absolute maximum ratings: Updated the maximum voltage value of all other pins parameter ■ Table 3-3 DC power supply currents: Added the units column ■ Table 3-5 Input power source control and protection: Updated the VOVLO conditions and voltage values ■ Table 3-6 USB Type-C and BC1.2 specifications: Updated the VCONN overcurrent protection threshold values and SBU current source values. Also added the VBUS-to-VPH Pass-Through Mode parameter ■ Table 3-8 2S battery charger specifications: Updated this table ■ Table 3-9 Buck regulator specifications: Updated this table ■ Figure 3-1 PM8350B/BH/BHS 3LBk Charging Efficiency: Added the efficiency plot ■ Figure 3-2 PM8350B/BH/BHS 3LBk Charging Pdiss: Added the efficiency plot ■ Figure 3-3 PM8350B/BH/BHS DIV2 charging efficiency: Added the efficiency plot ■ Figure 3-4 PM8350B/BH/BHS DIV2 Charging Pdiss: Added the efficiency plot ■ Figure 3-5 PM8350B/BH/BHS Reverse Boost Efficiency: Added the efficiency plot ■ Figure 3-6 PM8350B/BH/BHS Reverse Boost Pdiss: Added the efficiency plot ■ Table 3-10 Div2 charge pump specifications: Updated this table ■ Table 3-11 Reverse boost specifications: Updated this table ■ Table 3-12 Battery interface specification: Updated this table ■ Table 3-13 Miscellaneous specifications: Updated this table ■ Table 3-16 ADC electrical specifications: Updated the balancing FET resistance values ■ Table 3-18 External current sensing specifications: Added this table ■ Table 3-21 BCL specifications: Updated the accuracy specifications ■ Table 3-22 ELVDD (OLED positive rail) specifications: Added a note and updated the specification values ■ Table 3-23 ELVSS (OLED negative rail) specifications: Added a note and updated the specification values ■ Table 3-24 OLEDB bias performance specification: Added a note and updated the specification values ■ Table 3-25 DDIC LDO regulator specifications: Added this table ■ Table 3-26 Haptics driver electrical specifications: Updated the LRA drive programmable frequency ■ Table 4-3 Device identification details: Updated the device identification details for CS samples and added a note ■ Chapter 7 Part reliability: Added this chapter

Revision	Date	Description
E	January 2021	■ Table 2-2 Pad descriptions – charger: Updated the functional description for pin 40 and pin 57 ■ Table 3-8 2S battery charger specifications: Updated this table ■ Table 3-15 Analog multiplexer and scaling functions: Updated this table ■ Table 3-16 ADC electrical specifications: Updated this table ■ Table 4-1 PM8350B/PM8350BH/PM8350BHS device marking line definitions: Updated the assembly site ■ Table 4-3 Device identification details: Updated the YWW code and added additional lot details ■ Table 7-2 Package reliability results for TSMC: Updated the package reliability results for assembly source ■ Table 7-3 Device characteristics: Updated the assembly site
F	June 2021	■ Table 3-24 OLEDB bias performance specification: Updated the typical value of output capacitor ■ Table 4-3 Device identification details: Updated this table ■ Table 7-1 Silicon reliability results: TSMC: Updated the sample size ■ Table 7-2 Package reliability results for TSMC: Updated this sample size
G	September 10, 2021	■ Table 2-7 Pad descriptions – GPIO and other pins: Updated the configurable function for GPIO_06 ■ Table 4-3 Device identification details: Updated note 5
H	September 30, 2021	■ Table 3-5 *Input power source control and protection*: Updated the minimum value of USB/WLS input auto-shutdown threshold