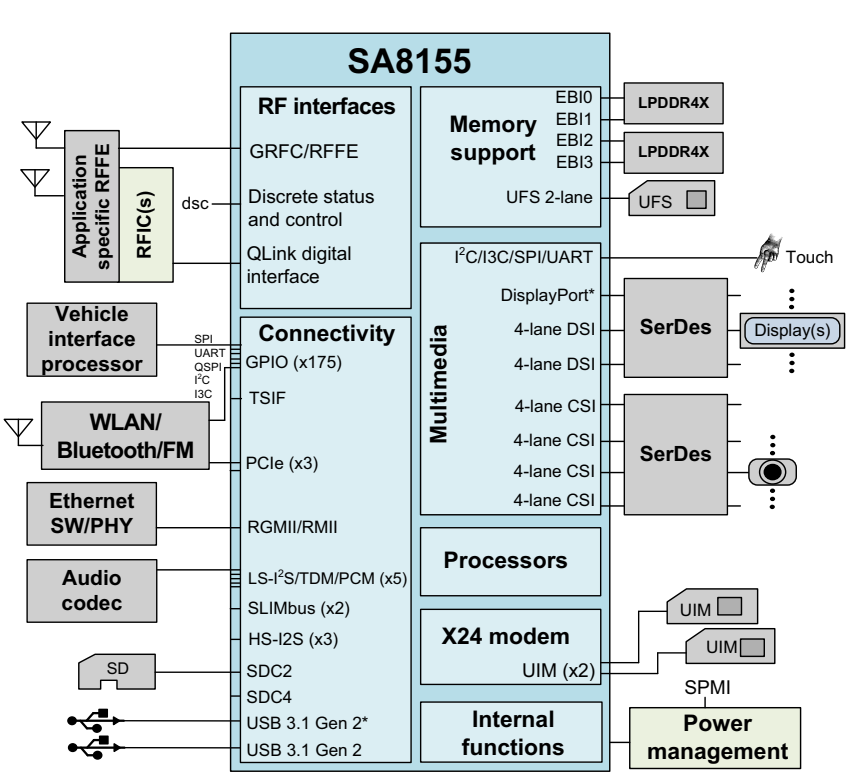
Qualcomm Technologies, Inc.

Device description

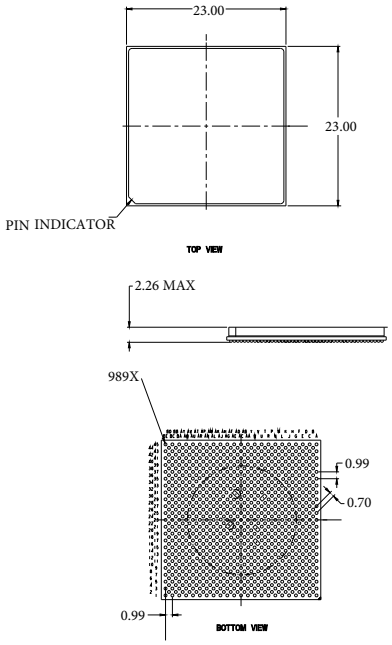
SA8155 is the new generation Qualcomm® Snapdragon™ automotive infotainment SoC with an integrated LTE modem. It is designed with the 7 nm process, for superior performance and power efficiency. SA8155 includes the following key components:

- Qualcomm® Kryo™ 485 CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 640 GPU for the highest in graphics performance and power efficiency
- Qualcomm® Hexagon™ 696 DSP with quad Hexagon Vector eXtensions (HVX) processor
- Qualcomm® Spectra™ 380 image processing engine
- Adreno 554 VPU for high-quality, ultra HD video encode and decode
- Adreno 895 DPU for ultra HD multidisplay support
- Qualcomm® NPU130 neural processing unit for high-performance machine learning use cases
- Qualcomm® Location Suite with support for GPS, GLONASS, BeiDou, Galileo, and QZSS systems
- Four 16-bit high-speed LPDDR4X SDRAM with optional low-power features
- Integrated Snapdragon X24 LTE modem with Cat20 download speeds up to 2.0 Gbps

SA8155 high-level block diagram and FCBGA989+HS drawing



* One USB 3.1 interface supports concurrent DisplayPort.



Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

NOTE: Unless otherwise specified, SA8155 refers to the SA8155/SA8150 and SA8155P/SA8150P chipsets throughout this document. Wherever appropriate, exceptions are specified

1.1 Functional block diagram

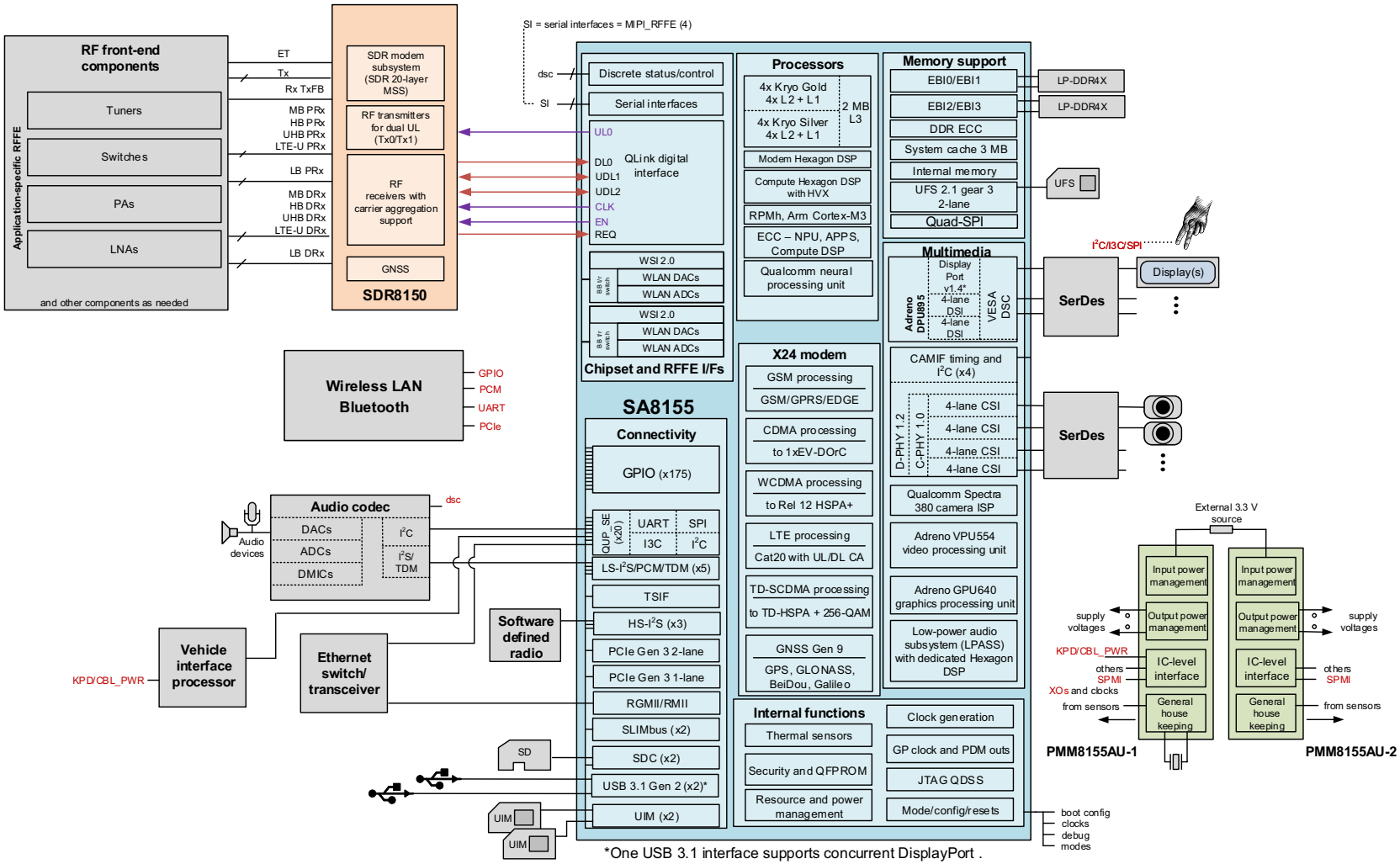


Figure 1-1 SA8155 functional block diagram and example application

1.2 SA8155 features

NOTE: Some of the hardware features integrated within the SA8155 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled SA8155 features.

Table 1-1 SA8155 variant feature set comparison

Feature	SA8150/SA8150P	SA8155/SA8155P
Kryo Gold	1920 MHz	2131.2 MHz
Kryo Gold Prime	2227.2 MHz	2419.2 MHz
Kryo Silver	1785.6 MHz	1785.6 MHz
LPDDR4X	2092.8 MHz	2092.8 MHz
GPU	500 MHz	700 MHz
Video decode/encode	4K60/4K30	4K120/4K60

Table 1-2 SA8155 features

Feature	SA8155 capability
Processors	
Applications	Kryo 485 – 64-bit applications processor with a 2 MB L3 cache ■ Quad high-performance Kryo Gold cores □ Three Kyro Gold cores with a 256 KB L2 cache per core, targeting up to 2.1312 GHz □ One Kyro Gold prime core with a 512 KB L2 cache, targeting 2.4192 GHz ■ Quad low-power Kryo Silver cores with a 128 KB L2 cache per core, targeting up to 1.7856 GHz
Digital signal processing	Compute Hexagon 696 DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Coprocessor (HCP) 1.1 ■ Used for video playback enhancements, virtual reality, computer vision, video capture enhancement, deep learning, and so on ■ Targeting up to 1.5 GHz and with a 1.0 MB L2 cache ■ The HCP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions. Audio Hexagon DSP dedicated to audio subsystem, targeting up to 1.5 GHz and with a 512 kB L2 cache Modem Hexagon DSP to support extended audio processing or 7x DLCA, 2x ULCA, and 20-layer MIMO (SA8155 only) General-purpose Hexagon DSP for advanced audio processing and other use cases All Hexagon DSPs are cache-based processors with full access to DDR memory.
Always-on system	Always-on subsystem with always-on processor Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication

Table 1-2 SA8155 features (cont.)

Feature	SA8155 capability
Artificial intelligence	Qualcomm NPU130 dedicated neural processing unit for performance and always-on neural network (NN) use cases. It incorporates an NN matrix engine to ensure efficient execution of various neural networks and their parameters. The NPU may be used for advanced computer vision, including lane-departure warning, pedestrian detection, and natural-language processing, in conjunction with the compute Hexagon DSP subsystem.
Memory support	
System memory via EBI	Four-channel high-speed memory – LPDDR4X SDRAM with optional low-power features (4x 16-bit) up to 2092.8 MHz clock and 16 GB 3 MB system cache
External memory Via UFS Via SDC Via QSPI	 UFS 2.1 gear 3 – two lanes for on-board memory (UFS 3.1 gear 4 supported, see Section 3.9.5 *UFS interface*) SD v3.0 4-bit for SD card NOR flash
RF support	
RF operating bands (not applicable to SA8155P/SA8150P)	Defined by the RF transceiver device
Air interfaces (not applicable to SA8155P/SA8150P) GSM CDMA WCDMA TD-SCDMA LTE Advanced techniques	See Table 1-3. Yes Yes Yes Yes Yes (Cat20 with 2.0 Gbps DL capability) Up to seven DLCA across five bands, up to three ULCA across two bands, and up to 20 DL layers
GNSS – Qualcomm Location Suite engine	Gen 9; GPS L1 and L2/L5, GLONASS, BeiDou, and Galileo

Table 1-2 SA8155 features (cont.)

Feature	SA8155 capability
Multimedia	
Adreno display processing unit (DPU) Display interface/performance	Adreno DPU 895 Two 4-lane MIPI DSI with VESA DSC v1.1 ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 20 Gbps total ■ C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 34 Gbps total DisplayPort v1.4 at 8.1 Gbps/lane, 32.4 Gbps/port, over USB 3.1 with support for MST and VESA DSC v1.1 and forward error correction (FEC). Concurrent DisplayPort USB3 and USB2 are supported.
Display processing	Up to a maximum of 24 MP; example configurations: 3x 4K **or** 4x 2880 × 1080 **or** 2x 4K + 1x 2880 × 1080
Pixel processing	Qualcomm® TruPalette™ display – HDR10+ and HDR10 tone mapping, color gamut mapping, six-zone, memory color, and picture adjust Qualcomm® Low-Power Picture Enhancement display – compression (UBWC3.0, DSC v1.1), CABL, FOSS, Assertive Display v4, Q-sync, and destination scaler with DE
Camera support Performance	Qualcomm Spectra 380 ISP ■ Pixel processing: 2 × IFE + 2 × IFE_L ■ Data formats: Bayer RGB, YUV, zzHDR, iHDR, RCCB, 10/8 bit YUV output ■ Statistics: Exposure, white balance, focus (HDR BHist, Tintless BG, AWB BG, BHist, Row/Col SUM) ■ 14 bit depth max, multiple pixel raw dump channels per CSID/IFE ■ Processing features: Bayer processing, offset correction, lens roll off correction, bad pixel corrections, directional scalers, color LUTs, color space transform, noise reduction, and local tone mapping.
Camera interface	Four 4-lane MIPI CSI configurable in 4 + 4 + 4 + 4 or split 2s configuration ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 40 Gbps total ■ C-PHY v1.0: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 68 Gbps total
Adreno video processing unit (VPU)	■ Adreno VPU 554 – fifth-generation UHD video processing unit ■ Video decode up to 4K120 ■ Video encode up to 4K60 ■ Concurrent 4K60 decode and 4K30 encode ■ Native decode support for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs ■ Native encode support for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs ■ New computer vision processor (CVP) for object detection and tracking
Adreno graphic processing unit (GPU)	■ Adreno 640 GPU ■ OpenGL ES 3.2, Vulkan and Vulkan Compute, DX12.x ■ OpenCL 2.0 full profile, DirectCompute

Table 1-2 SA8155 features (cont.)

Feature	SA8155 capability
Audio	
Low-power audio subsystem (LPASS)	
Processing	■ Qualcomm® Noise and Echo Cancellation ■ Dedicated audio LPASS Hexagon DSP with a 512 kB L2 cache ■ Qualcomm® Voice Suite processing engine to offload voice user interface and voice call processing ■ Qualcomm Voice Suite in-car communication, low-power voice activation, voice recognition, high-fidelity playback, and surround sound ■ Qualcomm Voice Suite source tracking, sound focus, multi-channel echo cancellation, feedback cancellation, and support for up to four car microphones ■ Qualcomm® Voice Activation
Codecs	■ Voice codecs: enhanced voice services, EVRC, EVRC-B, EVRC-WB; GSM-FR, GSM-EFR, and GSM-HR; AMR-NB and AMR-WB ■ Audio codecs: AAC, AAC-LC, HE-AAC v1, HE-AAC v2, and FLAC
Audio interfaces	
SLIMbus	■ Two; highly multiplexed, high-speed interfaces
LS-I^{2}S (muxed with PCM/TDM pins)	■ Up to five interfaces (pin multiplexed with PCM/TDM interfaces): four interfaces with two data lanes each; one interface with four data lanes for a total of 12 data lanes ■ Four MCLKs up to 512 × 48 kHz (24.576 MHz); clock master or slave independent of the source of frame sync/word select ■ Up to 512 bits/frame, 32 bits/channel, and 32 channels/interface.
PCM/TDM (muxed with LS-I^{2}S pins)	■ Multi-lane TDM (master and slave capable) ■ Up to five interfaces (pin multiplexed with I^{2}S): four interfaces with two data lanes each; one interface with four data lanes ■ Up to 512 bits/frame, 32 bits/channel, and 32 channels/interface ■ Short, long, and one-slot sync mode ■ Maximum clock frequency of 24.576 MHz
HS-I^{2}S	■ Three high-speed (up to 73.728 MHz) receive interfaces for software defined radio (SDR) ■ Two receive-only data lanes per interface; clock and word select in slave mode
Connectivity	
Qualcomm universal peripheral (QUP) serial engines	20 GPIO-based QUP SEs: 7 bits each for four QUP SEs and 4 bits each for the other 16 QUP SEs; multiplexed serial interface functions Six secondary serial cluster (SSC)-based QUP SEs: Up to 6 bits; multiplexed serial interface functions
UART (4 MHz)	UART (64 B FIFO) interface available on all QUP SEs, with the exception of GPIO QUP6/QUP7/QUP11–QUP16 and SSC QUP3/QUP4/QUP5, which have HS-UART (128 B FIFO)
I^{2}C master (1 MHz)	I^{2}C interface available on all QUP SEs (except for SSC QUP4); dedicated controller for each port

Table 1-2 SA8155 features (cont.)

Feature	SA8155 capability
I3C master (12.5 MHz)	I3C interface available on GPIO QUP3/QUP4/QUP8/QUP9 and SSC QUP0/QUP1
SPI master (48 MHz)	SPI master interfaces available on all GPIO QUP SEs and SSC QUP1/QUP2/QUP3/QUP5; dedicated controller for each port. GPIO QUP17 and QUP19 have limited maximum frequency.
SPI slave (48 MHz)	SPI slave interface available on GPIO QUP0/QUP1/QUP2/QUP9/QUP10/ QUP15 for vehicle-interface-processor (VIP) and/or CAN transceiver
CCI I^2C master (1 MHz)	Four dedicated I^2C interfaces for devices using CSI ports
UIM	Two – UIM1 dual voltages (1.8 V/2.95 V); UIM2 single voltage (1.8 V)
Quad-SPI (75 MHz)	QSPI NOR flash with UFS support for fast, reliable, and secure automotive boot
USB	■ One USB 3.1 Gen 2 - USB1 (HS+SS) - with DisplayPort concurrency ■ One USB 3.1 Gen 2 - USB2 (HS+SS)
PCIe	Two – one 2-lane PCIe Gen 3 (RC/EP) and one 1-lane PCIe Gen 3 (RC)
RGMII	One RGMII interface with MDIO for Ethernet with AVB (1.8 V only for RGMII and MDIO).
RMII	One RMII interface with MDIO for Ethernet with AVB (1.8 V only for RMII and MDIO). RMII MAC master-mode only.
Secure digital interfaces	■ Two 4-bit ports (SDC2 and SDC4); SD 3.0 ■ SDC2 is dual-voltage ■ SD card
TSIF	Transport stream interface
Wireless connectivity	QCA6696 (dual MAC 11ax)
Configurable GPIOs	
Number of GPIO ports	175 – GPIO_0 to GPIO_174
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current up to 16 mA
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General hardware security features	Secure boot 3.0, secure debug, TrustZone, Qualcomm® Trusted Execution Environment v5, hardware supported KeyStore, combined image signing
Crypto engines	Crypto engine v5 (CE5), FIPS certifiable, Inline crypto engine (ICE) based disk encryption, PRNG with TRNG seed
TrustZone services	Secure file system, eFuse read/write, RPMB, Crypto lib
DRM support in hardware	PlayReady SL3000 on selected software programs and with a pre-agreement, Widevine level 1
QFPROM	640 bits of QFPROM available for general purpose and OEM-specific usage beyond predefined QFPROM regions configured by the OEM
Access control	Programmable security domain protection and sand-boxing

Table 1-2 SA8155 features (cont.)

Feature	SA8155 capability
Safety	SA8155 device has been developed as an SEooC (safety element out of context) targeting assumed system level ASIL B use cases. Contact QTI for access to functional safety details of this device
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, design for software debug (DFSD) and ETM
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset and RF front end (RFFE) interface features (Not applicable to SA8155P/SA8150P)	
SDR RF transceiver QLink digital interface	■ One dedicated downlink lane, one dedicated uplink lane, and two bidirectional uplink/downlink lanes ■ Improved layout, routing, package, and signal integrity
Power management	2-line SPMI; plus other lines, as needed, via GPIOs
Fabrication technology and package	
Process technology	7 nm process
Package type and dimensions	FCBGA989+HS: 23.0 × 23.0 × 2.26 mm maximum (including metallic heat spreader)

1.2.1 Air interface features

Table 1-3 Key modem features (not applicable to SA8155P/SA8150P)

Standard	Feature descriptions
LTE	
Category	20
Carrier aggregation	FDD and TDD; downlink up to 140 MHz, uplink up to 40 MHz
CA direction	Uplink and downlink
Other LTE support	■ FeICIC-IC ■ ePDCCH ■ TM9 (FDD up to four Tx, TDD up to eight Tx) ■ 4-way Rx diversity ■ 8 × 4 MIMO
eMBMS	
Multiplexing	FDD and TDD
Voice options	
CSFB	GSM, CDMA, and WCDMA
Simultaneous voice and data	■ 1xSLTE and 1xSRLTE ■ hVoLTE and hSRLTE

Table 1-3 Key modem features (not applicable to SA8155P/SA8150P) (cont.)

Standard	Feature descriptions
Multi-SIM	
3G	3G + GSM DSDS
4G	4G + GSM DSDS
Connectivity management	
ePDG	LTE with Wi-Fi IP mobility
QCF	Qualcomm connectivity framework
NSRM	Power optimization for applications
CNE	LTE/3G – Wi-Fi selection
3G	
Multicarrier HSUPA	2C

Note: Features listed in Table 1-3 are not applicable to SA8155P.

Table 1-4 Position location and navigation summary

Standard	Feature descriptions
Qualcomm Location Suite engine with global navigation satellite system (GNSS) support	
Gen 9	Multifrequency GPS L1 and L2/L5, GLONASS, BeiDou, and Galileo

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O parameter definitions

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
PX_0	Pad group 0 (control signals); 1.8 V
PX_1	Pad group 1 (EBI pads); 1.1 V
PX_2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_5	Pad group 5 (UIM1 or GPIO); 1.8 V or 2.95 V for SA8155 UIM1, or 1.8 V for SA8155P GPIO
PX_6	Pad group 6 (UIM2 or GPIO); 1.8 V for SA8155 UIM2, or 1.8 V for SA8155P GPIO

Table 2-1 I/O parameter definitions (cont.)

Symbol	Description
PX_10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.8 V
PX_13	Pad group 13 (internal circuits); 1.85 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin map

The SA8155 is available in the FCBGA989+HS. It includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details.

A high-level view of the bottom pin assignments is shown in Figure 2-1.

The text within Figure 2-1 is difficult to read when viewing an 8½ inch × 11 inch hard copy. Other viewing options are available:

- Print that one page on an 11 inches × 17 inches sheet.
- View the graphic soft copy and zoom in; the resolution is sufficient for comfortable reading.
- Download the *SA8155 Pin Assignment and GPIO Configuration Spreadsheet* (80-PE986-1A) – this Microsoft Excel spreadsheet lists all SA8155 pin numbers and pin names.

NOTE: Click the following link to download the pin assignment spreadsheet (80-PE986-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-PE986-1A

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

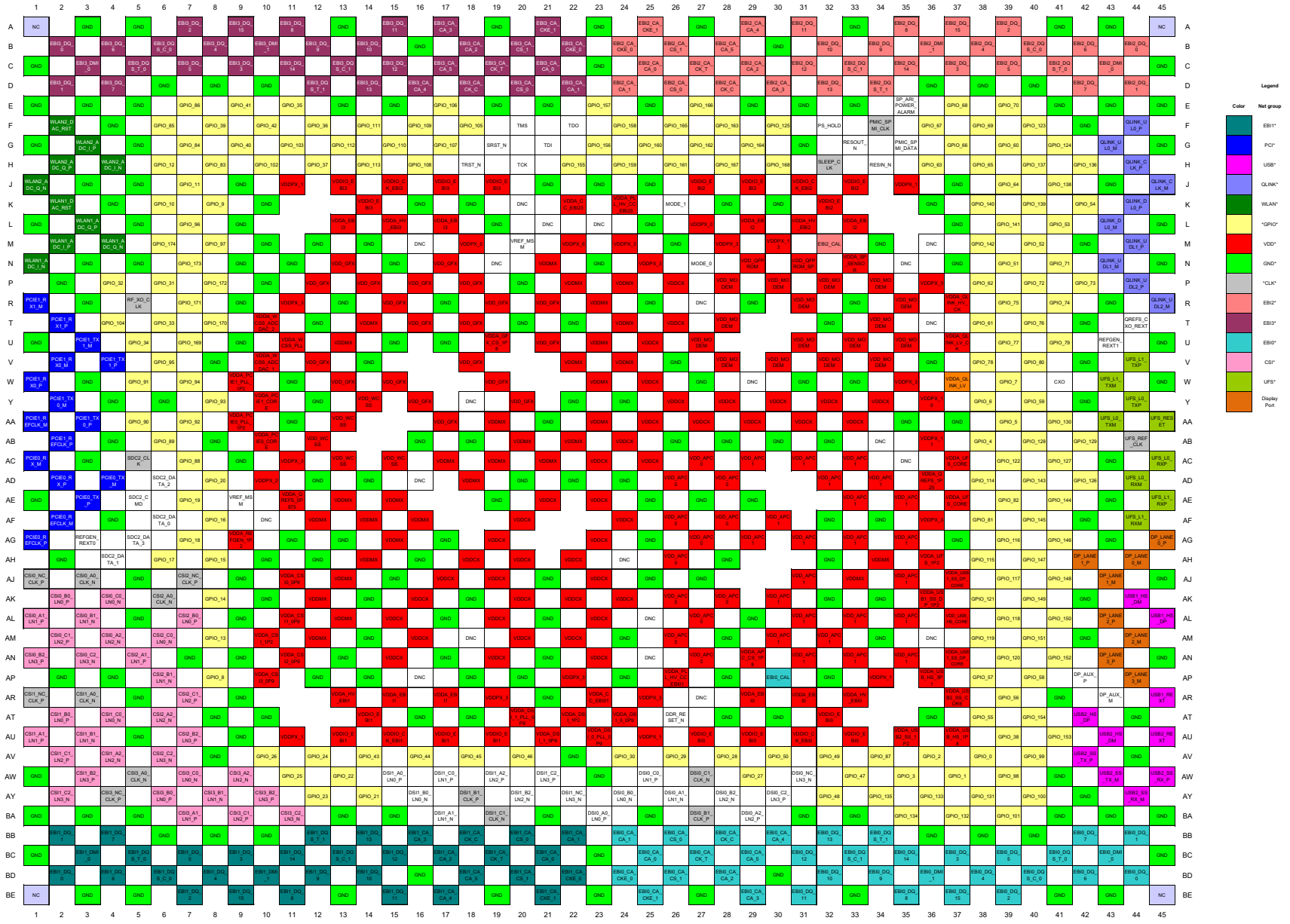


Figure 2-1 SA8155 pin assignments (Top view)

2.3 Pin descriptions

Table 2-2 Pin descriptions – primary pins

Pin #	Pin name	Pad voltage	Pad type	Functional description
AJ3	CSI0_A0_CLK_N	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
AL1	CSI0_A1_LN1_P	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
AM4	CSI0_A2_LN2_N	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
AK2	CSI0_B0_LN0_P	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY), trio lane 0 – B
AL3	CSI0_B1_LN1_N	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
AN1	CSI0_B2_LN3_P	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
AK4	CSI0_C0_LN0_N	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
AM2	CSI0_C1_LN2_P	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
AN3	CSI0_C2_LN3_N	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
AJ1	CSI0_NC_CLK_P	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – positive MIPI CSI 0 (C-PHY), no connect
AR3	CSI1_A0_CLK_N	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A
AU1	CSI1_A1_LN1_P	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A
AV4	CSI1_A2_LN2_N	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A
AT2	CSI1_B0_LN0_P	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – positive MIPI CSI 1 (C-PHY), trio lane 0 – B
AU3	CSI1_B1_LN1_N	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B
AW3	CSI1_B2_LN3_P	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B
AT4	CSI1_C0_LN0_N	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C
AV2	CSI1_C1_LN2_P	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C
AY2	CSI1_C2_LN3_N	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AR1	CSI1_NC_CLK_P	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
AK6	CSI2_A0_CLK_N	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – negative MIPI CSI 2 (C-PHY), trio lane 0 – A
AN5	CSI2_A1_LN1_P	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – positive MIPI CSI 2 (C-PHY), trio lane 1 – A
AT6	CSI2_A2_LN2_N	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – negative MIPI CSI 2 (C-PHY), trio lane 2 – A
AL7	CSI2_B0_LN0_P	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
AP6	CSI2_B1_LN1_N	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – negative MIPI CSI 2 (C-PHY), trio lane 1 – B
AU7	CSI2_B2_LN3_P	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – positive MIPI CSI 2 (C-PHY), trio lane 2 – B
AM6	CSI2_C0_LN0_N	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – negative MIPI CSI 2 (C-PHY), trio lane 0 – C
AR7	CSI2_C1_LN2_P	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – positive MIPI CSI 2 (C-PHY), trio lane 1 – C
AV6	CSI2_C2_LN3_N	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – negative MIPI CSI 2 (C-PHY), trio lane 2 – C
AJ7	CSI2_NC_CLK_P	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – positive MIPI CSI 2 (C-PHY), no connect
AW5	CSI3_A0_CLK_N	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A
BA7	CSI3_A1_LN1_P	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A
AW9	CSI3_A2_LN2_N	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A
AY6	CSI3_B0_LN0_P	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B
AY8	CSI3_B1_LN1_N	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B
AY10	CSI3_B2_LN3_P	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B
AW7	CSI3_C0_LN0_N	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C
BA9	CSI3_C1_LN2_P	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C
BA11	CSI3_C2_LN3_N	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AY4	CSI3_NC_CLK_P	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect
W41	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
AR43	DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – minus
AP42	DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – plus
AH44	DP_LANE0_M	–	AO	DisplayPort lane 0– minus
			AI	USB super-speed 1 receive 1– minus
AG45	DP_LANE0_P	–	AO	DisplayPort lane 0– plus
			AI	USB super-speed 1 receive 1– plus
AJ43	DP_LANE1_M	–	AO	DisplayPort lane 1– minus
			AO	USB super-speed 1 transmit 1– minus
AH42	DP_LANE1_P	–	AO	DisplayPort lane 1– plus
			AO	USB super-speed 1 transmit 1– plus
AM44	DP_LANE2_M	–	AO	DisplayPort lane 2– minus
			AO	USB super-speed 1 transmit 0 – minus
AL43	DP_LANE2_P	–	AO	DisplayPort lane 2– plus
			AO	USB super-speed 1 transmit 0– plus
AP44	DP_LANE3_M	–	AO	DisplayPort lane 3 – minus
			AI	USB super-speed 1 receive 0 – minus
AN43	DP_LANE3_P	–	AO	DisplayPort lane 3 – plus
			AI	USB super-speed 1 receive 0 – plus
BA23	DSI0_A0_LN0_P	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – positive MIPI DSI 0 (C-PHY), trio lane 0 – A
AY26	DSI0_A1_LN1_N	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – negative MIPI DSI 0 (C-PHY), trio lane 1 – A
BA29	DSI0_A2_LN2_P	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – positive MIPI DSI 0 (C-PHY), trio lane 2 – A
AY24	DSI0_B0_LN0_N	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – negative MIPI DSI 0 (C-PHY), trio lane 0 – B
BA27	DSI0_B1_CLK_P	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – positive MIPI DSI 0 (C-PHY), trio lane 1 – B
AY28	DSI0_B2_LN2_N	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – negative MIPI DSI 0 (C-PHY), trio lane 2 – B
AW25	DSI0_C0_LN1_P	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – positive MIPI DSI 0 (C-PHY), trio lane 0 – C
AW27	DSI0_C1_CLK_N	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – negative MIPI DSI 0 (C-PHY), trio lane 1 – C

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AY30	DSI0_C2_LN3_P	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3 – positive MIPI DSI 0 (C-PHY), trio lane 2 – C
AW31	DSI0_NC_LN3_N	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3 – negative MIPI DSI 0 (C-PHY), no connect
AW15	DSI1_A0_LN0_P	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 0 – positive MIPI DSI 1 (C-PHY), trio lane 0 – A
BA17	DSI1_A1_LN1_N	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 1 – negative MIPI DSI 1 (C-PHY), trio lane 1 – A
AW19	DSI1_A2_LN2_P	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 2 – positive MIPI DSI 1 (C-PHY), trio lane 2 – A
AY16	DSI1_B0_LN0_N	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 0 – negative MIPI DSI 1 (C-PHY), trio lane 0 – B
AY18	DSI1_B1_CLK_P	DSI	AO	MIPI DSI 1 (D-PHY), differential clock – positive MIPI DSI 1 (C-PHY), trio lane 1 – B
AY20	DSI1_B2_LN2_N	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 2 – negative MIPI DSI 1 (C-PHY), trio lane 2 – B
AW17	DSI1_C0_LN1_P	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 1 – positive MIPI DSI 1 (C-PHY), trio lane 0 – C
BA19	DSI1_C1_CLK_N	DSI	AO	MIPI DSI 1 (D-PHY), differential clock – negative MIPI DSI 1 (C-PHY), trio lane 1 – C
AW21	DSI1_C2_LN3_P	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 3 – positive MIPI DSI 1 (C-PHY), trio lane 2 – C
AY22	DSI1_NC_LN3_N	DSI	AO	MIPI DSI 1 (D-PHY), differential lane 3 – negative MIPI DSI 1 (C-PHY), no connect
AT26	DDR_RESET_N	PX_1	DO	LPDDR4X reset (shared by EBIs)
BC25	EBI0_CA_CA_0	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 0
BB24	EBI0_CA_CA_1	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 1
BD28	EBI0_CA_CA_2	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 2
BE29	EBI0_CA_CA_3	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 3
BB30	EBI0_CA_CA_4	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 4
BC29	EBI0_CA_CA_5	PX_1	DO	EBI0 LPDDR4X command/address 0 bit 5
BB28	EBI0_CA_CK_C	PX_1	DO	EBI0 LPDDR4X differential clock (C)
BC27	EBI0_CA_CK_T	PX_1	DO	EBI0 LPDDR4X differential clock (T)
BD24	EBI0_CA_CKE_0	PX_1	DO	EBI0 LPDDR4X clock enable 0
BE25	EBI0_CA_CKE_1	PX_1	DO	EBI0 LPDDR4X clock enable 1
BB26	EBI0_CA_CS_0	PX_1	DO	EBI0 LPDDR4X chip select 0
BD26	EBI0_CA_CS_1	PX_1	DO	EBI0 LPDDR4X chip select 1
AP30	EBI0_CAL	–	AI	EBI0/1 LPDDR4X calibration resistor

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
BC43	EBI0_DMI_0	PX_1	DO	EBI0 LPDDR4X data mask for byte 0
BD36	EBI0_DMI_1	PX_1	DO	EBI0 LPDDR4X data mask for byte 1
BD44	EBI0_DQ_0	PX_1	B	EBI0 LPDDR4X data bit 0
BB44	EBI0_DQ_1	PX_1	B	EBI0 LPDDR4X data bit 1
BD32	EBI0_DQ_10	PX_1	B	EBI0 LPDDR4X data bit 10
BE31	EBI0_DQ_11	PX_1	B	EBI0 LPDDR4X data bit 11
BC31	EBI0_DQ_12	PX_1	B	EBI0 LPDDR4X data bit 12
BB32	EBI0_DQ_13	PX_1	B	EBI0 LPDDR4X data bit 13
BC35	EBI0_DQ_14	PX_1	B	EBI0 LPDDR4X data bit 14
BE37	EBI0_DQ_15	PX_1	B	EBI0 LPDDR4X data bit 15
BE39	EBI0_DQ_2	PX_1	B	EBI0 LPDDR4X data bit 2
BC37	EBI0_DQ_3	PX_1	B	EBI0 LPDDR4X data bit 3
BD38	EBI0_DQ_4	PX_1	B	EBI0 LPDDR4X data bit 4
BC39	EBI0_DQ_5	PX_1	B	EBI0 LPDDR4X data bit 5
BD42	EBI0_DQ_6	PX_1	B	EBI0 LPDDR4X data bit 6
BB42	EBI0_DQ_7	PX_1	B	EBI0 LPDDR4X data bit 7
BE35	EBI0_DQ_8	PX_1	B	EBI0 LPDDR4X data bit 8
BD34	EBI0_DQ_9	PX_1	B	EBI0 LPDDR4X data bit 9
BD40	EBI0_DQS_C_0	PX_1	B	EBI0 LPDDR4X differential data strobe for byte 0 (C)
BC33	EBI0_DQS_C_1	PX_1	B	EBI0 LPDDR4X differential data strobe for byte 1 (C)
BC41	EBI0_DQS_T_0	PX_1	B	EBI0 LPDDR4X differential data strobe for byte 0 (T)
BB34	EBI0_DQS_T_1	PX_1	B	EBI0 LPDDR4X differential data strobe for byte 1 (T)
BC21	EBI1_CA_CA_0	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 0
BB22	EBI1_CA_CA_1	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 1
BC17	EBI1_CA_CA_2	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 2
BB16	EBI1_CA_CA_3	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 3
BE17	EBI1_CA_CA_4	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 4
BD18	EBI1_CA_CA_5	PX_1	DO	EBI1 LPDDR4X command/address 0 bit 5
BB18	EBI1_CA_CK_C	PX_1	DO	EBI1 LPDDR4X differential clock (C)
BC19	EBI1_CA_CK_T	PX_1	DO	EBI1 LPDDR4X differential clock (T)
BD22	EBI1_CA_CKE_0	PX_1	DO	EBI1 LPDDR4X clock enable 0
BE21	EBI1_CA_CKE_1	PX_1	DO	EBI1 LPDDR4X clock enable 1
BB20	EBI1_CA_CS_0	PX_1	DO	EBI1 LPDDR4X chip select 0
BD20	EBI1_CA_CS_1	PX_1	DO	EBI1 LPDDR4X chip select 1
BC3	EBI1_DMI_0	PX_1	DO	EBI1 LPDDR4X data mask for byte 0
BD10	EBI1_DMI_1	PX_1	DO	EBI1 LPDDR4X data mask for byte 1

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
BD2	EBI1_DQ_0	PX_1	B	EBI1 LPDDR4X data bit 0
BB2	EBI1_DQ_1	PX_1	B	EBI1 LPDDR4X data bit 1
BD14	EBI1_DQ_10	PX_1	B	EBI1 LPDDR4X data bit 10
BE15	EBI1_DQ_11	PX_1	B	EBI1 LPDDR4X data bit 11
BC15	EBI1_DQ_12	PX_1	B	EBI1 LPDDR4X data bit 12
BB14	EBI1_DQ_13	PX_1	B	EBI1 LPDDR4X data bit 13
BC11	EBI1_DQ_14	PX_1	B	EBI1 LPDDR4X data bit 14
BE9	EBI1_DQ_15	PX_1	B	EBI1 LPDDR4X data bit 15
BE7	EBI1_DQ_2	PX_1	B	EBI1 LPDDR4X data bit 2
BC9	EBI1_DQ_3	PX_1	B	EBI1 LPDDR4X data bit 3
BD8	EBI1_DQ_4	PX_1	B	EBI1 LPDDR4X data bit 4
BC7	EBI1_DQ_5	PX_1	B	EBI1 LPDDR4X data bit 5
BD4	EBI1_DQ_6	PX_1	B	EBI1 LPDDR4X data bit 6
BB4	EBI1_DQ_7	PX_1	B	EBI1 LPDDR4X data bit 7
BE11	EBI1_DQ_8	PX_1	B	EBI1 LPDDR4X data bit 8
BD12	EBI1_DQ_9	PX_1	B	EBI1 LPDDR4X data bit 9
BD6	EBI1_DQS_C_0	PX_1	B	EBI1 LPDDR4X differential data strobe for byte 0 (C)
BC13	EBI1_DQS_C_1	PX_1	B	EBI1 LPDDR4X differential data strobe for byte 1 (C)
BC5	EBI1_DQS_T_0	PX_1	B	EBI1 LPDDR4X differential data strobe for byte 0 (T)
BB12	EBI1_DQS_T_1	PX_1	B	EBI1 LPDDR4X differential data strobe for byte 1 (T)
C25	EBI2_CA_CA_0	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 0
D24	EBI2_CA_CA_1	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 1
C29	EBI2_CA_CA_2	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 2
D30	EBI2_CA_CA_3	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 3
A29	EBI2_CA_CA_4	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 4
B28	EBI2_CA_CA_5	PX_1	DO	EBI2 LPDDR4X command/address 0 bit 5
D28	EBI2_CA_CK_C	PX_1	DO	EBI2 LPDDR4X differential clock (C)
C27	EBI2_CA_CK_T	PX_1	DO	EBI2 LPDDR4X differential clock (T)
B24	EBI2_CA_CKE_0	PX_1	DO	EBI2 LPDDR4X clock enable 0
A25	EBI2_CA_CKE_1	PX_1	DO	EBI2 LPDDR4X clock enable 1
D26	EBI2_CA_CS_0	PX_1	DO	EBI2 LPDDR4X chip select 0
B26	EBI2_CA_CS_1	PX_1	DO	EBI2 LPDDR4X chip select 1
M32	EBI2_CAL	–	AI	EBI2/3 LPDDR4X calibration resistor
C43	EBI2_DMI_0	PX_1	DO	EBI2 LPDDR4X data mask for byte 0
B36	EBI2_DMI_1	PX_1	DO	EBI2 LPDDR4X data mask for byte 1
B44	EBI2_DQ_0	PX_1	B	EBI2 LPDDR4X data bit 0

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
D44	EBI2_DQ_1	PX_1	B	EBI2 LPDDR4X data bit 1
B32	EBI2_DQ_10	PX_1	B	EBI2 LPDDR4X data bit 10
A31	EBI2_DQ_11	PX_1	B	EBI2 LPDDR4X data bit 11
C31	EBI2_DQ_12	PX_1	B	EBI2 LPDDR4X data bit 12
D32	EBI2_DQ_13	PX_1	B	EBI2 LPDDR4X data bit 13
C35	EBI2_DQ_14	PX_1	B	EBI2 LPDDR4X data bit 14
A37	EBI2_DQ_15	PX_1	B	EBI2 LPDDR4X data bit 15
A39	EBI2_DQ_2	PX_1	B	EBI2 LPDDR4X data bit 2
C37	EBI2_DQ_3	PX_1	B	EBI2 LPDDR4X data bit 3
B38	EBI2_DQ_4	PX_1	B	EBI2 LPDDR4X data bit 4
C39	EBI2_DQ_5	PX_1	B	EBI2 LPDDR4X data bit 5
B42	EBI2_DQ_6	PX_1	B	EBI2 LPDDR4X data bit 6
D42	EBI2_DQ_7	PX_1	B	EBI2 LPDDR4X data bit 7
A35	EBI2_DQ_8	PX_1	B	EBI2 LPDDR4X data bit 8
B34	EBI2_DQ_9	PX_1	B	EBI2 LPDDR4X data bit 9
B40	EBI2_DQS_C_0	PX_1	B	EBI2 LPDDR4X differential data strobe for byte 0 (C)
C33	EBI2_DQS_C_1	PX_1	B	EBI2 LPDDR4X differential data strobe for byte 1 (C)
C41	EBI2_DQS_T_0	PX_1	B	EBI2 LPDDR4X differential data strobe for byte 0 (T)
D34	EBI2_DQS_T_1	PX_1	B	EBI2 LPDDR4X differential data strobe for byte 1 (T)
C21	EBI3_CA_CA_0	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 0
D22	EBI3_CA_CA_1	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 1
B18	EBI3_CA_CA_2	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 2
A17	EBI3_CA_CA_3	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 3
D16	EBI3_CA_CA_4	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 4
C17	EBI3_CA_CA_5	PX_1	DO	EBI3 LPDDR4X command/address 0 bit 5
D18	EBI3_CA_CK_C	PX_1	DO	EBI3 LPDDR4X differential clock (C)
C19	EBI3_CA_CK_T	PX_1	DO	EBI3 LPDDR4X differential clock (T)
B22	EBI3_CA_CKE_0	PX_1	DO	EBI3 LPDDR4X clock enable 0
A21	EBI3_CA_CKE_1	PX_1	DO	EBI3 LPDDR4X clock enable 1
D20	EBI3_CA_CS_0	PX_1	DO	EBI3 LPDDR4X chip select 0
B20	EBI3_CA_CS_1	PX_1	DO	EBI3 LPDDR4X chip select 1
C3	EBI3_DMI_0	PX_1	DO	EBI3 LPDDR4X data mask for byte 0
B10	EBI3_DMI_1	PX_1	DO	EBI3 LPDDR4X data mask for byte 1
B2	EBI3_DQ_0	PX_1	B	EBI3 LPDDR4X data bit 0
D2	EBI3_DQ_1	PX_1	B	EBI3 LPDDR4X data bit 1
B14	EBI3_DQ_10	PX_1	B	EBI3 LPDDR4X data bit 10

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
A15	EBI3_DQ_11	PX_1	B	EBI3 LPDDR4X data bit 11
C15	EBI3_DQ_12	PX_1	B	EBI3 LPDDR4X data bit 12
D14	EBI3_DQ_13	PX_1	B	EBI3 LPDDR4X data bit 13
C11	EBI3_DQ_14	PX_1	B	EBI3 LPDDR4X data bit 14
A9	EBI3_DQ_15	PX_1	B	EBI3 LPDDR4X data bit 15
A7	EBI3_DQ_2	PX_1	B	EBI3 LPDDR4X data bit 2
C9	EBI3_DQ_3	PX_1	B	EBI3 LPDDR4X data bit 3
B8	EBI3_DQ_4	PX_1	B	EBI3 LPDDR4X data bit 4
C7	EBI3_DQ_5	PX_1	B	EBI3 LPDDR4X data bit 5
B4	EBI3_DQ_6	PX_1	B	EBI3 LPDDR4X data bit 6
D4	EBI3_DQ_7	PX_1	B	EBI3 LPDDR4X data bit 7
A11	EBI3_DQ_8	PX_1	B	EBI3 LPDDR4X data bit 8
B12	EBI3_DQ_9	PX_1	B	EBI3 LPDDR4X data bit 9
B6	EBI3_DQS_C_0	PX_1	B	EBI3 LPDDR4X differential data strobe for byte 0 (C)
C13	EBI3_DQS_C_1	PX_1	B	EBI3 LPDDR4X differential data strobe for byte 1 (C)
C5	EBI3_DQS_T_0	PX_1	B	EBI3 LPDDR4X differential data strobe for byte 0 (T)
D12	EBI3_DQS_T_1	PX_1	B	EBI3 LPDDR4X differential data strobe for byte 1 (T)
N27	MODE_0	PX_0	DI-S PD	Mode control bits. 00 for mission mode. 11 for boundary scan mode.
K26	MODE_1	PX_0	DI-S PD	
AF2	PCIE0_REFCLK_M	–	AO	PCIe 0 Gen 3 reference clock – minus
AG1	PCIE0_REFCLK_P	–	AO	PCIe 0 Gen 3 reference clock – plus
AC1	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – minus
AD2	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – plus
AD4	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – minus
AE3	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – plus
AA1	PCIE1_REFCLK_M	–	AI, AO	PCIe 1 Gen 3 reference clock – minus
AB2	PCIE1_REFCLK_P	–	AI, AO	PCIe 1 Gen 3 reference clock – plus
V2	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive 0 – minus
W1	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive 0 – plus
R1	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive 1 – minus
T2	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive 1 – plus
Y2	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit 0 – minus
AA3	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit 0 – plus
U3	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit 1 – minus
V4	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit 1 – plus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
F34	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
G35	PMIC_SPMI_DATA	PX_0	B	Slave and PBUS interface for PMICs – data
F32	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
J45	QLINK_CLK_M	–	AO	QLink clock – minus
H44	QLINK_CLK_P	–	AO	QLink clock – plus
L43	QLINK_DL0_M	–	AI	QLink downlink lane 0 – minus
K44	QLINK_DL0_P	–	AI	QLink downlink lane 0 – plus
N43	QLINK_UDL1_M	–	AI	QLink uplink/downlink lane 1 – minus
M44	QLINK_UDL1_P	–	AI	QLink uplink/downlink lane 1 – plus
R45	QLINK_UDL2_M	–	AI	QLink uplink/downlink lane 2 – minus
P44	QLINK_UDL2_P	–	AI	QLink uplink/downlink lane 2 – plus
G43	QLINK_UL0_M	–	AO	QLink uplink lane 0 – minus
F44	QLINK_UL0_P	–	AO	QLink uplink lane 0 – plus
T44	QREFS_CXO_REXT	PX_11	AI	External resistor for on-die clocking
AG3	REFGEN_REXT0	PX_3	AI	East-side high-speed interface – external resistor
U43	REFGEN_REXT1	PX_3	AI	West-side high-speed interface – external resistor
H34	RESIN_N	PX_0	DI	Reset input
G33	RESOUT_N	PX_3	DO	Reset output
R5	RF_XO_CLK	PX_3	DI	WLAN reference clock
AC5	SDC2_CLK	PX_2	DO	Secure digital controller 2 clock
AE5	SDC2_CMD	PX_2	B	Secure digital controller 2 command
AF6	SDC2_DATA_0	PX_2	B	Secure digital controller 2 data bit 0
AH4	SDC2_DATA_1	PX_2	B	Secure digital controller 2 data bit 1
AD6	SDC2_DATA_2	PX_2	B	Secure digital controller 2 data bit 2
AG5	SDC2_DATA_3	PX_2	B	Secure digital controller 2 data bit 3
H32	SLEEP_CLK	PX_3	DI	Sleep clock
E35	SP_ARI_POWER_ ALARM	PX_13	DI	Reserved
G19	SRST_N	PX_3	DI-PU	JTAG reset for debug
H20	TCK	PX_3	DI-PU	JTAG clock input
G21	TDI	PX_3	DI-PU:nppdkp	JTAG data input
F22	TDO	PX_3	DO-Z	JTAG data output
F20	TMS	PX_3	DI-PU:nppdkp	JTAG mode select input
H18	TRST_N	PX_3	DI-PD:nppukp	JTAG reset
AA45	UFS_RESET	PX_10	DO-Z PD:nppukp	UFS reset

Table 2-2 Pin descriptions – primary pins (cont.)

Pin #	Pin name	Pad voltage	Pad type	Functional description
AD44	UFS_L0_RXM	–	AI	UFS receive lane 0 – minus
AC45	UFS_L0_RXP	–	AI	UFS receive lane 0 – plus
AA43	UFS_L0_TXM	–	AO	UFS transmit lane 0 – minus
Y44	UFS_L0_TXP	–	AO	UFS transmit lane 0 – plus
AF44	UFS_L1_RXM	–	AI	UFS receive lane 1 – minus
AE45	UFS_L1_RXP	–	AI	UFS receive lane 1 – plus
W43	UFS_L1_TXM	–	AO	UFS transmit lane 1 – minus
V44	UFS_L1_TXP	–	AO	UFS transmit lane 1 – plus
AB44	UFS_REF_CLK	PX_10	DO-Z PD:nppukp	UFS reference clock
AK44	USB1_HS_DM	–	AI, AO	USB high-speed 1 data – minus
AL45	USB1_HS_DP	–	AI, AO	USB high-speed 1 data – plus
AR45	USB1_REXT	–	AI	External resistor for USB high-speed 1
AU43	USB2_HS_DM	–	AI, AO	USB high-speed 2 data – minus
AT42	USB2_HS_DP	–	AI, AO	USB high-speed 2 data – plus
AU45	USB2_REXT	–	AI	External resistor for USB high-speed 2
AY44	USB2_SS_RX_M	–	AI	USB super-speed 2 receive – minus
AW45	USB2_SS_RX_P	–	AI	USB super-speed 2 receive – plus
AW43	USB2_SS_TX_M	–	AO	USB super-speed 2 transmit – minus
AV42	USB2_SS_TX_P	–	AO	USB super-speed 2 transmit – plus
N1	WLAN1_ADC_I_N	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase minus
M2	WLAN1_ADC_I_P	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, in-phase plus
M4	WLAN1_ADC_Q_N	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature minus
L3	WLAN1_ADC_Q_P	PX_3	AI, AO	WLAN chain 1 analog-to-digital converter, quadrature plus
K2	WLAN1_DAC_RST	PX_3	AI, AO	WLAN chain 1 digital-to-analog converter external resistor
H4	WLAN2_ADC_I_N	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase minus
G3	WLAN2_ADC_I_P	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, in-phase plus
J1	WLAN2_ADC_Q_N	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature minus
H2	WLAN2_ADC_Q_P	PX_3	AI, AO	WLAN chain 2 analog-to-digital converter, quadrature plus
F2	WLAN2_DAC_RST	PX_3	AI, AO	WLAN chain 2 digital-to-analog converter external resistor

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE: Board designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all SA8155 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

Table 2-3 Pin descriptions – GPIO pins

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AV38	GPIO_0		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L0[0]			QUP 0, lane 0: SPI_MISO/UART_CTS/I2C_ SDA/SPI-S_MOSI	
AW37	GPIO_1		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[0]			QUP 0, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL/SPI-S_MISO	
AV36	GPIO_2		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[0]			QUP 0, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
AW35	GPIO_3		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[0]			QUP 0, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
AB38	GPIO_4		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[6]			QUP 6, lane 2: SPI_CLK/UART_TX	
		RGMII_TXD1/RMII_TXD1			RGMII/RMII transmit data 1	
AA39	GPIO_5		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[6]			QUP 6, lane 3: SPI_CS0/UART_RX	
		RGMII_TXD2			RGMII transmit data 2	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
Y38	GPIO_6		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L0[6]			QUP 6, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
		RGMII_TXD3			RGMII transmit data 3	
		QUP_L6_0_CS			QUP 0, lane 6: SPI_CS3	
W39	GPIO_7		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[6]			QUP 6, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
		RGMII_MDC			RGMII management interface clock	
		QUP_L5_0_CS			QUP 0, lane 5: SPI_CS2	
AP8	GPIO_8		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA			MDP vertical sync – primary A	
K8	GPIO_9		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA			MDP vertical sync – secondary A	
		QUP_L0[10]			QUP 10, lane 0: SPI_MISO/UART_CTS/I2C_ SDA/SPI-S_MOSI	
K6	GPIO_10		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_E			MDP vertical sync – external	
		DP_HOT_PLUG_DETECT			DisplayPort hot plug detect	
		QUP_L1[10]			QUP 10, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL/SPI-S_MISO	
J7	GPIO_11		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[10]			QUP 10, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
H6	GPIO_12		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[10]			QUP 10, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
AM8	GPIO_13		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK0			Camera master clock 0	
		QDSS_GPIO_TRACEDATA_ LOCB[0]			QDSS trace data 0 B	
AK8	GPIO_14		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK1			Camera master clock 1	
		QDSS_GPIO_TRACEDATA_ LOCB[1]			QDSS trace data 1 B	
AH8	GPIO_15		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK2			Camera master clock 2	
		QDSS_GPIO_TRACEDATA_ LOCB[2]			QDSS trace data 2 B	
AF8	GPIO_16		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK3			Camera master clock 3	
		QDSS_GPIO_TRACEDATA_ LOCB[3]			QDSS trace data 3 B	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AH6	GPIO_17		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Dedicated camera control interface I2C 0 serial data	
		QDSS_GPIO_TRACEDATA_ LOCB[4]			QDSS trace data 4 B	
AG7	GPIO_18		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Dedicated camera control interface I2C 0 clock	
		QDSS_GPIO_TRACEDATA_ LOCB[5]			QDSS trace data 5 B	
AE7	GPIO_19		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1			Dedicated camera control interface I2C 1 serial data	
		QDSS_GPIO_TRACEDATA_ LOCB[6]			QDSS trace data 6 B	
AD8	GPIO_20		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL1			Dedicated camera control interface I2C 1 clock	
		QDSS_GPIO_TRACEDATA_ LOCB[7]			QDSS trace data 7 B	
AY14	GPIO_21		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera control interface timer 0	
		GCC_GP2_CLK_MIRB			Global general-purpose clock 2 B	
		QDSS_GPIO_TRACEDATA_ LOCB[8]			QDSS trace data 8 B	
AW13	GPIO_22		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera control interface timer 1	
		GCC_GP3_CLK_MIRB			Global general-purpose clock 3 B	
		QDSS_GPIO_TRACECLK_ LOCB			QDSS trace clock B	
AY12	GPIO_23		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER2			Camera control interface timer 2	
		QUP_L0[18]			QUP 18, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QDSS_GPIO_TRACEDATA_ LOCB[9]			QDSS trace data 9 B	
AV12	GPIO_24		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3			Camera control interface timer 3	
		CCI_ASYNC_IN1			Camera control interface async 1	
		QUP_L1[18]			QUP 18, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
		QDSS_GPIO_TRACEDATA_ LOCB[10]			QDSS trace data 10 B	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AW11	GPIO_25		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER4			Camera control interface timer 4	
		CCI_ASYNC_IN2			Camera control interface async 2	
		QUP_L2[18]			QUP 18, lane 2: SPI_CLK/UART_TX	
		QDSS_GPIO_TRACEDATA_ LOCB[11]			QDSS trace data 11 B	
AV10	GPIO_26		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_ASYNC_IN0			Camera control interface async 0	
		QUP_L3[18]			QUP 18, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_ LOCB[12]			QDSS trace data 12 B	
AW29	GPIO_27		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[15]			QUP 15, lane 0: SPI_MISO/UART_CTS/I2C_ SDA/SPI-S_MOSI	
		GP_MN			General-purpose M/N:D counter output	
		QDSS_GPIO_TRACEDATA_ LOCB[15]			QDSS trace data 15 B	
AV28	GPIO_28		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L1[15]			QUP 15, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL/SPI-S_MISO	
		QDSS_GPIO_TRACECTL_ LOCB			QDSS trace control B	
AV26	GPIO_29		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[15]			QUP 15, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
		QDSS_GPIO_TRACEDATA_ LOCB[13]			QDSS trace data 13 B	
AV24	GPIO_30		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[15]			QUP 15, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
		QDSS_GPIO_TRACEDATA_ LOCB[14]			QDSS trace data 14 B	
P6	GPIO_31		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Dedicated camera control interface I2C 2 serial data	
		QDSS_GPIO_TRACEDATA_ LOCA[13]			QDSS trace data 13 A	
P4	GPIO_32		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Dedicated camera control interface I2C 2 clock	
		QDSS_GPIO_TRACEDATA_ LOCA[0]			QDSS trace data 0 A	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
T6	GPIO_33		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA3			Dedicated camera control interface I2C 3 serial data	
		QUP_L5_9_CS			QUP 9, lane 5: SPI_CS2	
		QDSS_GPIO_TRACEDATA_LOCA[1]			QDSS trace data 1 A	
U5	GPIO_34		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL3			Dedicated camera control interface I2C 3 clock	
		QUP_L6_9_CS			QUP 9, lane 6: SPI_CS3	
E11	GPIO_35		PX_3	PD:nppukp	Configurable I/O	N
		PCIE0_RST_N (optional)			Bit-banged PCIe 0 reset RC output [1]	
F12	GPIO_36		PX_3	PU:nppdkp	Configurable I/O	Y
		PCIE0_CLKREQ_N			PCIe 0 clock request RC input	
H12	GPIO_37		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L4_9_CS			QUP 9, lane 4: SPI_CS1	
AU39	GPIO_38		PX_3	PD:nppukp	Configurable I/O	Y
		USB_PHY_PS			USB PHY port select	
F8	GPIO_39		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[9]			QUP 9, lane 0: SPI_MISO/UART_CTS/I2C_SDA/SPI-S_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA[6]			QDSS trace data 6 A	
G9	GPIO_40		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[9]			QUP 9, lane 1: SPI_MOSI/UART_RFR/I2C_SCL/SPI-S_MISO	
		QDSS_GPIO_TRACEDATA_LOCA[7]			QDSS trace data 7 A	
E9	GPIO_41		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L2[9]			QUP 9, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
		QDSS_GPIO_TRACEDATA_LOCA[14]			QDSS trace data 14 A	
F10	GPIO_42		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[9]			QUP 9, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
		QDSS_GPIO_TRACEDATA_LOCA[15]			QDSS trace data 15 A	
AV14	GPIO_43		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L0[13]			QUP 13, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
AV16	GPIO_44		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[13]			QUP 13, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AV18	GPIO_45		PX_3	PU:nppdkp	Configurable I/O	N
		QUP_L2[13]			QUP 13, lane 2: SPI_CLK/UART_TX	
		QDSS_CTI_TRIG0_OUT_MIRB			QDSS trigger output 0 B	
AV20	GPIO_46		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[13]			QUP 13, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG0_IN_MIRB			QDSS trigger input 0 B	
AW33	GPIO_47		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[14]			QUP 14, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QDSS_GPIO_TRACEDATA_ LOCA[12]			QDSS trace data 12 A	
AY32	GPIO_48		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L1[14]			QUP 14, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
		QDSS_GPIO_TRACEDATA_ LOCA[10]			QDSS trace data 10 A	
AV32	GPIO_49		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L2[14]			QUP 14, lane 2: SPI_CLK/UART_TX	
		QDSS_CTI_TRIG1_OUT_MIRA			QDSS trigger output 0 A	
AV30	GPIO_50		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[14]			QUP 14, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG1_IN_MIRA			QDSS trigger input 0 A	
N39	GPIO_51		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[4]			QUP 4, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
M40	GPIO_52		PX_3	PD:nppukp	Configurable I/O	
		QUP_L1[4]			QUP 4, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
L41	GPIO_53		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L2[4]			QUP 4, lane 2: SPI_CLK/UART_TX	
K42	GPIO_54		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[4]			QUP 4, lane 3: SPI_CS0/UART_RX	
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	
AT38	GPIO_55		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[17]			QUP 17, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QUP_L2[19]			QUP 19, lane 2: SPI_CLK/UART_TX	
AR39	GPIO_56		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L1[17]			QUP 17, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
		QUP_L3[19]			QUP 19, lane 3: SPI_CS0/UART_RX	
		QDSS_CTI_TRIG1_IN_MIRB			QDSS trigger input 1 B	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AP38	GPIO_57		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[17]			QUP 17, lane 2: SPI_CLK/UART_TX	
		QUP_L0[19]			QUP 19, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QDSS_CTI_TRIG0_OUT_MIRA			QDSS trigger output 0 A	
AP40	GPIO_58		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[17]			QUP 17, lane 3: SPI_CS0/UART_RX	
		QUP_L1[19]			QUP 19, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
		QDSS_CTI_TRIG1_OUT_MIRB			QDSS trigger output 1 B	
		QDSS_CTI_TRIG0_IN_MIRA			QDSS trigger input 0 A	
Y40	GPIO_59		PX_3	PD:nppukp	Configurable I/O	N
		RGMII_MDIO			RGMII management interface I/O	
		QUP_L4_0_CS			QUP 0, lane 4: SPI_CS1	
G39	GPIO_60		PX_3	PD:nppukp	Configurable I/O	Y
		GPS_TX_AGGRESSOR_MIRA			Tx level may degrade GNSS receiver (A)	
		BOOT_CONFIG[7]			Boot configuration bit 7	
T38	GPIO_61		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK_REQUEST			QLink request	
P38	GPIO_62		PX_3	PD:nppukp	Configurable I/O	N
		QLINK_ENABLE			QLink enable	
H36	GPIO_63		PX_3	PD:nppukp	Configurable I/O	N
		WMSS_RESET_N			Worldwide modem subsystem reset output	
J39	GPIO_64		PX_3	PD:nppukp	Configurable I/O	N
		GRFC8			Generic RF controller bit 8	
		BOOT_CONFIG[2]			Boot configuration bit 2	
H38	GPIO_65		PX_3	PD:nppukp	Configurable I/O	N
		GRFC9			Generic RF controller bit 9	
		BOOT_CONFIG[0]			Boot configuration bit 0	
G37	GPIO_66		PX_3	PD:nppukp	Configurable I/O	N
		GRFC10			Generic RF controller bit 10	
F36	GPIO_67		PX_3	PD:nppukp	Configurable I/O	N
		GRFC11			Generic RF controller bit 11	
		BOOT_CONFIG[4]			Boot configuration bit 4	
E37	GPIO_68		PX_3	PD:nppukp	Configurable I/O	Y
		GRFC12			Generic RF controller bit 12	
		PA_INDICATOR_1_OR_2			PA transmit indicator	
		BOOT_CONFIG[1]			Boot configuration bit 1	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
F38	GPIO_69		PX_3	PD:nppukp	Configurable I/O	N
		MSS_LTE_COXM_TXD			UART Tx for LTE coexistence	
		BOOT_CONFIG[3]			Boot configuration bit 3	
E39	GPIO_70		PX_3	PD:nppukp	Configurable I/O	Y
		MSS_LTE_COXM_RXD			UART Rx for LTE coexistence	
		BOOT_CONFIG[6]			Boot configuration bit 6	
N41	GPIO_71		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA			RF front-end 0 interface data	
		GRFC0			Generic RF controller bit 0	
		BOOT_CONFIG[10]			Boot configuration bit 10	
P40	GPIO_72		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_CLK			RF front-end 0 interface clock	
		GRFC1			Generic RF controller bit 1	
P42	GPIO_73		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_DATA			RF front-end 1 interface data	
		GRFC2			Generic RF controller bit 2	
		BOOT_CONFIG[11]			Boot configuration bit 11	
R41	GPIO_74		PX_3	PD:nppukp	Configurable I/O	N
		RFFE1_CLK			RF front-end 1 interface clock	
		GRFC3			Generic RF controller bit 3	
R39	GPIO_75		PX_3	PD:nppukp	Configurable I/O	N
		RFFE2_DATA			RF front-end 2 interface data	
		GRFC4			Generic RF controller bit 4	
T40	GPIO_76		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE2_CLK			RF front-end 2 interface clock	
		GRFC5			Generic RF controller bit 5	
		GPS_TX_AGGRESSOR_MIRD			Tx level may degrade GNSS receiver (D)	
U39	GPIO_77		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE3_DATA			RF front-end 3 interface data	
		GRFC6			Generic RF controller bit 6	
		GPS_TX_AGGRESSOR_MIRE			Tx level may degrade GNSS receiver (E)	
		BOOT_CONFIG[9]			Boot configuration bit 9	
V38	GPIO_78		PX_3	PD:nppukp	Configurable I/O	N
		RFFE3_CLK			RF front-end 3 interface clock	
		GRFC7			Generic RF controller bit 7	
U41	GPIO_79		PX_3	PD:nppukp	Configurable I/O	N
		GRFC13			Generic RF controller bit 13	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
V40	GPIO_80		PX_3	PD:nppukp	Configurable I/O	N
		GRFC14			Generic RF controller bit 14	
AF38	GPIO_81		PX_3	PD:nppukp	Configurable I/O	Y
		GRFC15			Generic RF controller bit 15	
		GPS_TX_AGGRESSOR_MIRB			Tx level may degrade GNSS receiver (B)	
		QUP_L4_1_CS			QUP 1, lane 4: SPI_CS1	
		MDP_VSYNC_P_MIRB			MDP vertical sync – primary B	
AE39	GPIO_82		PX_3	PD:nppukp	Configurable I/O	N
		GRFC16			Generic RF controller bit 16	
		GPS_TX_AGGRESSOR_MIRC			Tx level may degrade GNSS receiver (C)	
		QUP_L5_1_CS			QUP 1, lane 5: SPI_CS2	
		MDP_VSYNC_S_MIRB			MDP vertical sync – secondary B	
H8	GPIO_83		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[12]			QUP 12, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QUP_L3[16]			QUP 16, lane 3: SPI_CS0/UART_RX	
		QDSS_GPIO_TRACEDATA_ LOCA[2]			QDSS trace data 2 A	
G7	GPIO_84		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[12]			QUP 12, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
		QUP_L2[16]			QUP 16, lane 2: SPI_CLK/UART_TX	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
F6	GPIO_85		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[12]			QUP 12, lane 2: SPI_CLK/UART_TX	
		QUP_L1[16]			QUP 16, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL	
E7	GPIO_86		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[12]			QUP 12, lane 3: SPI_CS0/UART_RX	
		QUP_L0[16]			QUP 16, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
AV34	GPIO_87		PX_3	PD:nppukp	Configurable I/O	Y
AC7	GPIO_88		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF1_CLK			Transport stream interface 1 clock	
		QUP_L0[8]			QUP 8, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
		QSPI_CS_N_0			Quad-SPI chip select 0	
AB6	GPIO_89		PX_3	PD:nppukp	Configurable I/O	N
		TSIF1_EN			Transport stream interface 1 enable	
		QUP_L1[8]			QUP 8, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
		QSPI_DATA[0]			Quad-SPI data bit 0	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AA5	GPIO_90		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF1_DATA			Transport stream interface 1 data	
		QUP_L2[8]			QUP 8, lane 2: SPI_CLK/UART_TX	
		QSPI_DATA[1]			Quad-SPI data bit 1	
		SDC4_CMD			Secure digital controller 4 command	
W5	GPIO_91		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF1_SYNC			Transport stream interface 1 sync	
		QUP_L3[8]			QUP 8, lane 3: SPI_CS0/UART_RX	
		QSPI_DATA[2]			Quad-SPI data bit 2	
		SDC4_DATA[3]			Secure digital controller 4 data bit 3	
AA7	GPIO_92		PX_3	PD:nppukp	Configurable I/O	N
		TSIF2_CLK			Transport stream interface 2 clock	
		QUP_L2[11]			QUP 11, lane 2: SPI_CLK/UART_TX	
		QSPI_CLK			Quad-SPI clock	
		SDC4_CLK			Secure digital controller 4 clock	
Y8	GPIO_93		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF2_EN			Transport stream interface 2 enable	
		QUP_L3[11]			QUP 11, lane 3: SPI_CS0/UART_RX	
		QSPI_DATA[3]			Quad-SPI data bit 3	
		SDC4_DATA[2]			Secure digital controller 4 clock data bit 2	
W7	GPIO_94		PX_3	PD:nppukp	Configurable I/O	N
		TSIF2_DATA			Transport stream interface 2 data	
		QUP_L0[11]			QUP 11, lane 0: SPI_MISO/UART_CTS/I2C_ SDA	
		QSPI_CS_N_1			Quad-SPI chip select 1	
		SDC4_DATA[1]			Secure digital controller 4 clock data bit 1	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
V6	GPIO_95		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF2_SYNC			Transport stream interface 2 sync	
		QUP_L1[11]			QUP 11, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
		SDC4_DATA[0]			Secure digital controller 4 data bit 0	
		QUP_L4_8_CS			QUP 8, lane 4: SPI_CS1	
L7	GPIO_96		PX_3	PD:nppukp	Configurable I/O	Y
		TSIF2_ERROR			Transport stream interface 2 error	
		QUP_L5_8_CS			QUP 8, lane 5: SPI_CS2	
M8	GPIO_97		PX_3	PD:nppukp	Configurable I/O	Y
		SD_WRITE_PROTECT			Secure digital card write protection	
		TSIF1_ERROR			Transport stream interface 1 error	
		QUP_L6_8_CS			QUP 8, lane 6: SPI_CS3	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AW39	GPIO_98		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L0[7]			QUP 7, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
AV40	GPIO_99		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[7]			QUP 7, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
AY40	GPIO_100		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[7]			QUP 7, lane 2: SPI_CLK/UART_TX	
BA39	GPIO_101		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[7]			QUP 7, lane 3: SPI_CS0/UART_RX	
H10	GPIO_102		PX_3	PD:nppukp	Configurable I/O	N
		PCIE1_RST_N (optional)			Bit-banged PCIe 1 reset RC output [1]	
G11	GPIO_103		PX_3	PU:nppdkp	Configurable I/O	Y
		PCIE1_CLKREQ_N			PCIe 1 clock request RC input	
T4	GPIO_104		PX_3	PD:nppukp	Configurable I/O	Y
F18	GPIO_105		PX_6	PD:nppukp	Configurable I/O	N
		UIM2_DATA			UIM2 data (1.8 V only)	
E17	GPIO_106		PX_6	PD:nppukp	Configurable I/O	N
		UIM2_CLK			UIM2 clock (1.8 V only)	
G17	GPIO_107		PX_6	PD:nppukp	Configurable I/O	N
		UIM2_RESET			UIM2 reset (1.8 V only)	
H16	GPIO_108		PX_3	PD:nppukp	Configurable I/O	Y
		UIM2_PRESENT			UIM2 presence detection	
F16	GPIO_109		PX_5	PD:nppukp	Configurable I/O	N
		UIM1_DATA			UIM1 data (dual voltage)	
G15	GPIO_110		PX_5	PD:nppukp	Configurable I/O	N
		UIM1_CLK			UIM1 clock (dual voltage)	
F14	GPIO_111		PX_5	PD:nppukp	Configurable I/O	N
		UIM1_RESET			UIM1 reset (dual voltage)	
G13	GPIO_112		PX_3	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT			UIM1 presence detection	
H14	GPIO_113		PX_3	PD:nppukp	Configurable I/O	Y
		UIM_BATT_ALARM			UIM battery alarm	
		USB2PHY_AC_EN1			USB1 AC coupling control	
AD38	GPIO_114		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[1]			QUP 1, lane 0: SPI_MISO/UART_CTS/I2C_ SDA/SPI-S_MOSI	
		RGMII_TXC/RMII_REF_CLK			RGMII transmit clock signal/RMII reference clock	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AH38	GPIO_115		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L1[1]			QUP 1, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL/SPI-S_MISO	
		RGMII_RXC			RGMII receive clock signal	
AG39	GPIO_116		PX_3	PD:nppukp	Configurable I/O	N
		QUP_L2[1]			QUP 1, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
		RGMII_RX_CTL/RMII_CRS_DV			RGMII receive control/RMII carrier sense and RX data valid	
AJ39	GPIO_117		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[1]			QUP 1, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
		RGMII_RXD0/RMII_RXD0			RGMII/RMII receive data 0	
		QDSS_GPIO_TRACEDATA_ LOCA[3]			QDSS trace data 3 A	
AL39	GPIO_118		PX_3	PD:nppukp	Configurable I/O	Y
		RGMII_RXD1/RMII_RXD1			RGMII/RMII receive data 1	
		QDSS_GPIO_TRACEDATA_ LOCA[4]			QDSS trace data 4 A	
AM38	GPIO_119		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L2[5]			QUP 5, lane 2: SPI_CLK/UART_TX	
		RGMII_RXD2			RGMII receive data 2	
		QDSS_GPIO_TRACEDATA_ LOCA[5]			QDSS trace data 5 A	
AN39	GPIO_120		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L3[5]			QUP 5, lane 3: SPI_CS0/UART_RX	
		RGMII_RXD3			RGMII receive data 3	
		QDSS_GPIO_TRACECTL_ LOCA			QDSS trace control A	
AK38	GPIO_121		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L0[5]			QUP 5, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
		RGMII_TX_CTL/RMII_TX_EN			RGMII transmit control/RMII clock data on TX enable	
		QDSS_GPIO_TRACECLK_ LOCA			QDSS trace clock A	
AC39	GPIO_122		PX_3	PD:nppukp	Configurable I/O	Y
		QUP_L1[5]			QUP 5, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
		RGMII_TXD0/RMII_TXD0			RGMII/RMII transmit data 0	
F40	GPIO_123		PX_3	PD:nppukp	Configurable I/O	Y
		USB2PHY_AC_EN2			USB2 AC coupling control	
		QUP_L6_1_CS			QUP 1, lane 6: SPI_CS3	
G41	GPIO_124		PX_3	PD:nppukp	Configurable I/O	Y
		EMAC_PHY_INTR			Ethernet Interrupt	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
F30	GPIO_125		PX_3	PD:nppukp	Configurable I/O	Y
		HS3_MI2S_MCLK			High-speed 3 MI2S master clock	
AD42	GPIO_126		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_SCK/PCM2_ CLK/TDM2_CLK			Secondary MI2S//PCM/TDM clock	
		QUP_L0[2]			QUP 2, lane 0: SPI_MISO/UART_CTS/I2C_ SDA/SPI-S_MOSI	
AC41	GPIO_127		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_WS/PCM2_ SYNC/TDM2_SYNC			Secondary MI2S/PCM/TDM serial data word select and synchronization	
		QUP_L1[2]			QUP 2, lane 1: SPI_MOSI/UART_RFR/I2C_ SCL/SPI-S_MISO	
AB40	GPIO_128		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_DATA0/PCM2_ DIN/TDM2_DATA0			Secondary MI2S/PCM/TDM serial data channel 0	
		QUP_L2[2]			QUP 2, lane 2: SPI_CLK/UART_TX/SPI-S_CLK	
AB42	GPIO_129		PX_3	PD:nppukp	Configurable I/O	Y
		SEC_MI2S_DATA1/PCM2_ DOUT/TDM2_DATA1			Secondary MI2S/PCM/TDM serial data channel 1	
		QUP_L3[2]			QUP 2, lane 3: SPI_CS0/UART_RX/SPI-S_CS0	
AA41	GPIO_130		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_MCLK			Secondary MI2S master clock	
AY38	GPIO_131		PX_3	PD:nppukp	Configurable I/O	N
		TER_MI2S_DATA1/PCM3_ DOUT/TDM3_DATA1			Tertiary MI2S/PCM/TDM serial data channel 1	
		GCC_GP1_CLK_MIRB			Global general-purpose clock 1 B	
BA37	GPIO_132		PX_3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_MCLK			Tertiary MI2S master clock	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
		QDSS_GPIO_TRACEDATA_ LOCA[11]			QDSS trace data 11 A	
AY36	GPIO_133		PX_3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_SCK/PCM3_ CLK/TDM3_CLK			Tertiary MI2S/PCM/TDM clock	
		QDSS_GPIO_TRACEDATA_ LOCA[8]			QDSS trace data 8 A	
BA35	GPIO_134		PX_3	PD:nppukp	Configurable I/O	Y
		TER_MI2S_WS/PCM3_ SYNC/TDM3_SYNC			Tertiary MI2S/PCM/TDM serial data word select and synchronization	
		QDSS_GPIO_TRACEDATA_ LOCA[9]			QDSS trace data 9 A	
AY34	GPIO_135		PX_3	PD:nppukp	Configurable I/O	N
		TER_MI2S_DATA0/PCM3_ DIN/TDM3_DATA0			Tertiary MI2S/PCM/TDM serial data channel 0	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
H42	GPIO_136		PX_3	PD:nppukp	Configurable I/O	Y
		QUA_MI2S_MCLK			Quaternary MI2S master clock	
		GCC_GP1_CLK_MIRA			Global general-purpose clock 1 A	
		FORCED_USB_BOOT			Forced USB boot	
H40	GPIO_137		PX_3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_SCK/PCM4_ CLK/TDM4_CLK			Quaternary MI2S/PCM/TDM clock	
		GCC_GP2_CLK_MIRA			Global general-purpose clock 2 A	
J41	GPIO_138		PX_3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_WS/PCM4_ SYNC/TDM4_SYNC			Quaternary MI2S/PCM/TDM serial data word select and synchronization	
		GCC_GP3_CLK_MIRA			Global general-purpose clock 3 A	
K40	GPIO_139		PX_3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA0/PCM4_ DIN/TDM4_DATA0			Quaternary MI2S/PCM/TDM serial data channel 0	
K38	GPIO_140		PX_3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA1/PCM4_ DOUT/TDM4_DATA1			Quaternary MI2S/PCM/TDM serial data channel 1	
L39	GPIO_141		PX_3	PD:nppukp	Configurable I/O	N
		QUA_MI2S_DATA2/TDM4_ DATA2			Quaternary MI2S/PCM/TDM serial data channel 2	
M38	GPIO_142		PX_3	PD:nppukp	Configurable I/O	Y
		QUA_MI2S_DATA3/TDM4_ DATA3			Quaternary MI2S/PCM/TDM serial data channel 3	
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
AD40	GPIO_143		PX_3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_MCLK			Primary MI2S master clock	
AE41	GPIO_144		PX_3	PD:nppukp	Configurable I/O	Y
		PRI_MI2S_SCK/PCM1_ CLK/TDM1_CLK			Primary MI2S/PCM/TDM clock	
		QUP_L0[3]			QUP 3, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
AF40	GPIO_145		PX_3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_WS/PCM1_ SYNC/TDM1_SYNC			Primary MI2S/PCM/TDM word select and synchronization	
		QUP_L1[3]			QUP 3, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
AG41	GPIO_146		PX_3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_DATA0/PCM1_ DIN/TDM1_DATA0			Primary MI2S/PCM/TDM serial data channel 0	
		QUP_L2[3]			QUP 3, lane 2: SPI_CLK/UART_TX	
AH40	GPIO_147		PX_3	PD:nppukp	Configurable I/O	Y
		PRI_MI2S_DATA1/PCM1_ DOUT/TDM1_DATA1			Primary MI2S/PCM/TDM serial data channel 1	
		QUP_L3[3]			QUP 3, lane 3: SPI_CS0/UART_RX	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
AJ41	GPIO_148		PX_3	PD:nppukp	Configurable I/O	N
		QUIN_MI2S_MCLK			Quinary MI2S master clock	
AK40	GPIO_149		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_CLK			Low-power audio SLIMbus clock	
		QUIN_MI2S_SCK/PCM5_ CLK/TDM5_CLK			Quinary MI2S/PCM/TDM clock	
AL41	GPIO_150		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA0			Low-power audio SLIMbus data 0	
		QUIN_MI2S_DATA0/PCM5_ DIN/TDM5_DATA0			Quinary MI2S/PCM/TDM serial data channel 0	
AM40	GPIO_151		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_DATA1			Low-power audio SLIMbus data 1	
		QUIN_MI2S_WS/PCM5_ SYNC/TDM5_SYNC			Quinary MI2S/PCM/TDM word select and synchronization	
AN41	GPIO_152		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA2			Low-power audio SLIMbus data 2	
		QUIN_MI2S_DATA1/PCM5_ DOUT/TDM5_DATA1			Quinary MI2S/PCM/TDM serial data channel 1	
AU41	GPIO_153		PX_3	PD:nppukp	Configurable I/O	Y
		BTFM_SLIMBUS_DATA			Bluetooth/FM SLIMbus data	
AT40	GPIO_154		PX_3	PD:nppukp	Configurable I/O	N
		BTFM_SLIMBUS_CLK			Bluetooth/FM SLIMbus clock	
H22	GPIO_155		PX_3	PD:nppukp	Configurable I/O	N
		HS1_MI2S_MCLK			High-speed 1 MI2S master clock	
		SSC_0			Secondary serial cluster I/O 0 (power-on default)	
G23	GPIO_156		PX_3	PD:nppukp	Configurable I/O	N
		HS1_MI2S_SCK			High-speed 1 MI2S clock	
		SSC_1			Secondary serial cluster I/O 1 (power-on default)	
E23	GPIO_157		PX_3	PD:nppukp	Configurable I/O	N
		HS1_MI2S_WS			High-speed 1 MI2S serial data word select	
		SSC_2			Secondary serial cluster I/O 2 (power-on default)	
F24	GPIO_158		PX_3	PD:nppukp	Configurable I/O	N
		HS1_MI2S_DATA0			High-speed 1 MI2S serial data channel 0	
		SSC_3			Secondary serial cluster I/O 3 (power-on default)	
H24	GPIO_159		PX_3	PD:nppukp	Configurable I/O	N
		HS1_MI2S_DATA1			High-speed 1 MI2S serial data channel 1	
		SSC_4			Secondary serial cluster I/O 4 (power-on default)	
G25	GPIO_160		PX_3	PD:nppukp	Configurable I/O	N
		HS2_MI2S_MCLK			High-speed 2 MI2S master clock	
		SSC_5			Secondary serial cluster I/O 5 (power-on default)	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
H26	GPIO_161		PX_3	PD:nppukp	Configurable I/O	N
		HS2_MI2S_SCK			High-speed 2 MI2S clock	
		SSC_6			Secondary serial cluster I/O 6 (power-on default)	
G27	GPIO_162		PX_3	PD:nppukp	Configurable I/O	N
		HS2_MI2S_WS			High-speed 2 MI2S serial data word select	
		SSC_7			Secondary serial cluster I/O 7 (power-on default)	
F28	GPIO_163		PX_3	PD:nppukp	Configurable I/O	N
		HS2_MI2S_DATA0			High-speed 2 MI2S serial data channel 0	
		SSC_8			Secondary serial cluster I/O 8 (power-on default)	
G29	GPIO_164		PX_3	PD:nppukp	Configurable I/O	N
		HS2_MI2S_DATA1			High-speed 2 MI2S serial data channel 1	
		SSC_9			Secondary serial cluster I/O 9 (power-on default)	
F26	GPIO_165		PX_3	PD:nppukp	Configurable I/O	N
		HS3_MI2S_SCK			High-speed 3 MI2S clock	
		SSC_10			Secondary serial cluster I/O 10 (power-on default)	
E27	GPIO_166		PX_3	PD:nppukp	Configurable I/O	N
		HS3_MI2S_WS			High-speed 3 MI2S serial data word select	
		SSC_11			Secondary serial cluster I/O 11 (power-on default)	
H28	GPIO_167		PX_3	PD:nppukp	Configurable I/O	N
		HS3_MI2S_DATA0			High-speed 3 MI2S serial data channel 0	
		SSC_12			Secondary serial cluster I/O 12 (power-on default)	
H30	GPIO_168		PX_3	PD:nppukp	Configurable I/O	N
		HS3_MI2S_DATA1			High-speed 3 MI2S serial data channel 1	
		SSC_13			Secondary serial cluster I/O 13 (power-on default)	
U7	GPIO_169		PX_3	PD:nppukp	Configurable I/O	N
		WCSS1_BBD_RFA_CMD_CLK			WLAN chain 1 baseband command clock (WSI 2.0) – power-on default	
T8	GPIO_170		PX_3	PD:nppukp	Configurable I/O	N
		WCSS1_BBD_RFA_CMD_ DATA			WLAN chain 1 baseband command data (WSI 2.0) – power-on default	
R7	GPIO_171		PX_3	PD:nppukp	Configurable I/O	N
		WCSS2_BBD_RFA_CMD_CLK			WLAN chain 2 baseband command clock (WSI 2.0) – power-on default	
P8	GPIO_172		PX_3	PD:nppukp	Configurable I/O	N
		WCSS2_BBD_RFA_CMD_ DATA			WLAN chain 2 baseband command data (WSI 2.0) – power-on default	
N7	GPIO_173		PX_3	PD:nppukp	Configurable I/O	N
		WCSS_CXM_RFA_CMD_CLK			WLAN coexistence module command clock (WSI 1.0) – power-on default	

Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin #	Pin name	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup
M6	GPIO_174		PX_3	PD:nppukp	Configurable I/O	N
		WCSS_CXM_RFA_CMD_DATA			WLAN coexistence module command data (WSI 1.0) – power-on default	

1. PCIE0_RST_N/PCIE1_RST_N is a software implementation as bit bang on the same GPIOs

Table 2-4 Bottom pin descriptions – power-supply pins

Pin #	Pin name	Functional description
AC27, AD26, AD28, AF26, AF28, AG27, AH26, AK26, AK28, AL27, AM26, AN27	VDD_APC0	Power for Kryo Silver application processor
AC29, AC31, AC33, AD32, AD34, AE33, AE35, AF30, AG29, AG31, AG33, AG35, AJ31, AJ35, AK30, AL31, AL33, AL35, AM30, AM32, AN31, AN33, AN35	VDD_APC1	Power for Kryo Gold application processor
AA17, N13, N17, P12, P14, P16, P18, R15, R19, R21, T16, T18, U21, V12, V18, W13, W15, W19, Y16, Y20	VDD_GFX	Power for graphics
P28, P30, P32, P34, R31, R35, T28, T34, U27, U31, U33, U35, V28, V30, V32, V34	VDD_MODEM	Power for modem circuits
N31	VDD_QFPROM_SP	Power for programming the QFPROM; internal circuits
N29	VDD_QFPROM	Power for programming the QFPROM
AL37	VDD_USB_HS_CORE	Power for USB high-speed (HS) core circuits
AA13, AB12, AC13, AC15, Y14	VDD_WCSS	Power for WCSS circuits
AN29	VDDA_APC_CS_1P8	Power for application processor current-sensor 1.8 V circuits
AR23	VDDA_CC_EBI01	Power for EBI0/EBI1 clock circuits
K22	VDDA_CC_EBI23	Power for EBI2/EBI3 clock circuits
AM10	VDDA_CSI_1P2	Power for MIPI CSI0/1/2/3 1.2 V circuits
AJ11	VDDA_CSI0_0P9	Power for MIPI CSI0 0.9 V circuits
AL11	VDDA_CSI1_0P9	Power for MIPI CSI1 0.9 V circuits
AN11	VDDA_CSI2_0P9	Power for MIPI CSI2 0.9 V circuits
AP10	VDDA_CSI3_0P9	Power for MIPI CSI3 0.9 V circuits
AT24	VDDA_DSI_0_0P9	Power for MIPI DSI0 0.9 V circuits
AU23	VDDA_DSI_0_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V circuits
AU21	VDDA_DSI_1_0P9	Power for MIPI DSI1 0.9 V circuits
AT20	VDDA_DSI_1_PLL_0P9	Power for MIPI DSI1 PLL 0.9 V circuits
AT22	VDDA_DSI_1P2	Power for MIPI DSI0/1 1.2 V circuits

Table 2-4 Bottom pin descriptions – power-supply pins (cont.)

Pin #	Pin name	Functional description
AR29, AR31	VDDA_EBI0	Power for EBI0 PHY circuits
AR15, AR17	VDDA_EBI1	Power for EBI1 PHY circuits
L29, L33	VDDA_EBI2	Power for EBI2 PHY circuits
L13, L17	VDDA_EBI3	Power for EBI3 PHY circuits
U19	VDDA_GFX_CS_1P8	Power for graphics current sensor 1.8 V circuits
AR33	VDDA_HV_EBI0	Power for EBI0 PHY high-voltage circuits
AR13	VDDA_HV_EBI1	Power for EBI1 PHY high-voltage circuits
L31	VDDA_HV_EBI2	Power for EBI2 PHY high-voltage circuits
L15	VDDA_HV_EBI3	Power for EBI3 PHY high-voltage circuits
Y10	VDDA_PCIE1_CORE	Power for PCIE1 (2-lane) core circuits
W9	VDDA_PCIE1_PLL_1P2	Power for PCIE1 (2-lane) PLL 1.2 V circuits
AB10	VDDA_PCIE0_CORE	Power for PCIE0 (1-lane) core circuits
AA9	VDDA_PCIE0_PLL_1P2	Power for PCIE0 (1-lane) PLL 1.2 V circuits
AP26	VDDA_PLL_HV_CC_EBI01	Power for EBI0/EBI1 PLL high-voltage circuits
K24	VDDA_PLL_HV_CC_EBI23	Power for EBI2/EBI3 PLL high-voltage circuits
R37	VDDA_QLINK_HV_CK	Power for QLink high-voltage clock circuits
W37	VDDA_QLINK_LV	Power for QLink low-voltage circuits
U37	VDDA_QLINK_LV_CK	Power for QLink low-voltage clock circuits
AD36	VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits
N33	VDDA_SP_SENSOR	Power for internal circuits
AE11	VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits
AH36	VDDA_UFS_1P2	Power for UFS 1.2 V circuits
AC37, AE37	VDDA_UFS_CORE	Power for UFS core circuits
AG9	VDDA_REFGEN_1P2	Power for REFGEN circuits
AU37	VDDA_USB_HS_1P8	Power for USB1/2 high-speed (HS) 1.8 V circuits
AP36	VDDA_USB_HS_3P1	Power for USB1/2 HS 3.1 V circuits
AU35	VDDA_USB2_SS_1P2	Power for USB2 SuperSpeed (SS) 1.2 V circuits
AR37	VDDA_USB2_SS_CORE	Power for USB2 SS core circuits
AK36	VDDA_USB1_SS_DP_1P2	Power for USB1 SS and DP 1.2 V circuits
AJ37, AN37	VDDA_USB1_SS_DP_ CORE	Power for USB1 SS and DP core circuits
V10	VDDA_WCSS_ADCDAC_1	Power for WCSS ADC and DAC – chain 1
T10	VDDA_WCSS_ADCDAC_2	Power for WCSS ADC and DAC – chain 2
U11	VDDA_WCSS_PLL	Power for WCSS PLL circuits

Table 2-4 Bottom pin descriptions – power-supply pins (cont.)

Pin #	Pin name	Functional description
AA25, AA27, AA29, AA31, AA33, AB24, AC23, AC25, AE21, AE23, AF20, AF24, AG19, AG23, AH18, AH20, AH22, AJ17, AJ19, AJ23, AK16, AK20, AK22, AK24, AL15, AL19, AL23, AM16, AM20, AM22, AN15, AN19, AN23, P26, T26, U25, W25, Y26, Y28, Y30, Y32, Y34	VDDCX	Power for digital core circuits, secondary serial cluster circuits, and multimedia subsystem circuits
AU31	VDDIO_CK_EBI0	Power for EBI0 I/O clock circuits
AU15	VDDIO_CK_EBI1	Power for EBI1 I/O clock circuits
J31	VDDIO_CK_EBI2	Power for EBI2 I/O clock circuits
J15	VDDIO_CK_EBI3	Power for EBI3 I/O clock circuits
AT32, AU27, AU29, AU33	VDDIO_EBI0	Power for EBI0 I/O memory circuits
AT14, AU13, AU17, AU19	VDDIO_EBI1	Power for EBI1 I/O memory circuits
J27, J29, J33, K32	VDDIO_EBI2	Power for EBI2 I/O memory circuits
J13, J17, J19, K14	VDDIO_EBI3	Power for EBI3 I/O memory circuits
AA19, AA23, AB20, AB22, AC17, AC19, AC21, AD18, AE13, AE15, AF12, AF14, AF16, AG15, AH14, AH34, AJ13, AJ33, AK12, AL13, AM12, N21, P22, P24, R23, T14, T24, U13, U23, V22, V24, W23	VDDMX	Power for on-chip memory and secondary serial cluster memory
L27	VDDPX_0	Power for pad group 0 – control signals
AP34, AU11, AU25, J11, J35	VDDPX_1	Power for pad group 1 – EBI and DDR IO pads
Y36	VDDPX_10	Power for pad group 10 – UFS (REFCLK and RESET only)
AB36	VDDPX_11	Power for pad group 11 – CXO pad
M30	VDDPX_13	Power for pad group 13 – internal circuits
AD10	VDDPX_2	Power for pad group 2 - SDC2 pads
AC11, AF36, AP22, AR19, AR25, M24, M28, N25, P36, R11, W35	VDDPX_3	Power for pad group 3 – most I/O pads
M18	VDDPX_5	Power for pad group 5 – UIM1/GPIO pads
M22	VDDPX_6	Power for pad group 6 – UIM2/GPIO pads
AE9	VDDPX_VBIAS_SDC	Reference voltage for SDC
M20	VDDPX_VBIAS_UIM	Reference voltage for UIM

Table 2-5 Bottom pin descriptions – ground pins

Pin #	Pin name	Functional description
A3, A5, A13, A19, A23, A27, A33, A41, A43, AA11, AA21, AA35, AA37, AB4, AB8, AB16, AB18, AB26, AB28, AB30, AB32, AC3, AC9, AC43, AD12, AD14, AD20, AD22, AD24, AE1, AE19, AE25, AE27, AE29, AE43, AF4, AF32, AF34, AF42, AG11, AG13, AG17, AG25, AG37, AG43, AH2, AH10, AH12, AH16, AH28, AH32, AJ5, AJ9, AJ15, AJ21, AJ25, AJ27, AJ45, AK10, AK14, AK18, AK32, AK34, AK42, AL5, AL9, AL17, AL21, AL29, AM14, AM24, AM28, AM34, AM42, AN7, AN9, AN13, AN17, AN21, AN45, AP2, AP4, AP12, AP14, AP18, AP20, AP24, AP28, AP32, AR5, AR9, AR21, AR41, AT8, AT10, AT16, AT18, AT28, AT30, AT36, AT44, AU5, AU9, AV8, AV22, AV44, AW1, AW23, AW41, AY42, B16, B30, BA1, BA3, BA5, BA13, BA15, BA21, BA25, BA31, BA33, BA41, BA43, BA45, BB6, BB8, BB10, BB36, BB38, BB40, BC1, BC23, BC45, BD16, BD30, BE3, BE5, BE13, BE19, BE23, BE27, BE33, BE41, BE43, C1, C23, C45, D6, D8, D10, D36, D38, D40, E1, E3, E5, E13, E15, E19, E21, E25, E29, E31, E33, E41, E43, E45, F4, F42, G1, G5, G31, G45, J3, J5, J9, J21, J23, J25, J37, J43, K4, K10, K16, K18, K28, K30, K36, L1, L5, L9, L19, L25, L37, L45, M10, M12, M14, M26, M34, M42, N3, N5, N9, N11, N15, N23, N37, N45, P2, P10, P20, R3, R9, R13, R17, R25, R29, R33, R43, T12, T20, T22, T32, T42, U1, U9, U15, U17, U45, V8, V14, V26, V36, V42, W3, W11, W27, W31, W33, W45, Y4, Y6, Y12, Y22, Y24, Y42	GND	Ground

Table 2-6 Bottom pin descriptions – DNC and NC pins

Pin #	Pin name	Functional description
AL25, AN25, AB34, AC35, N35, M36, W29, AH24, R27, AM18, N19, Y18, L23, L21, AP16, M16, K20, T36, AD16, AF10, AM36, AR27	DNC	Do not connect; connected internally, do not connect externally.
A1, A45, BE1, BE45	NC	No connect; not connected internally.

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	-0.3	1.13	V
VDD_APC1	Kryo Gold application processor	-0.3	1.13	V
VDD_GFX	Graphics	-0.3	1.13	V
VDDCX	Digital core circuits	-0.3	1.13	V
VDDMX	On-chip memory	-0.3	1.13	V
VDD_MODEM	Modem circuits	-0.3	1.13	V
VDDA_CSI0_0P9	MIPI CSI0 0.9 V circuits	-0.3	1.01	V
VDDA_CSI1_0P9	MIPI CSI1 0.9 V circuits			
VDDA_CSI2_0P9	MIPI CSI2 0.9 V circuits			
VDDA_CSI3_0P9	MIPI CSI3 0.9 V circuits			
VDDA_DSI0_0P9	MIPI DSI0 0.9 V circuits			
VDDA_DSI0_PLL_0P9	MIPI DSI0 PLL 0.9 V circuits			
VDDA_DSI1_0P9	MIPI DSI1 0.9 V circuits			
VDDA_DSI1_PLL_0P9	MIPI DSI1 PLL 0.9 V circuits			
VDDA_PCIE0_CORE	PCIe 0 core circuits			
VDDA_PCIE1_CORE	PCIe 1 core circuits			

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDDA_PLL_HV_CC_EBI	EBI high-voltage circuits	-0.3	1.01	V
VDDA_QLINK_LV	QLink low-voltage circuits			
VDDA_QLINK_LV_CK	QLink low-voltage clock circuits			
VDDA_UFS1_CORE	UFS core circuits			
VDDA_USB_HS_CORE	USB digital core circuits			
VDDA_USB2_SS_CORE	USB2 SS core circuits			
VDDA_USB1_SS_DP_CORE	USB1 SS and DisplayPort core circuits			
VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits			
VDDA_SP_SENSOR	Power for internal circuits			
VDDPX_0	Digital pad circuits – control signals	-0.3	2.09	V
VDDPX_1	Digital pad circuits - EBI and DDR I/O	-0.3	1.34	V
VDDPX_2	Digital pad circuits – SDC2	-0.3	2.09 3.33	V
VDDPX_3	Digital pad circuits – most I/Os	-0.3	2.09	V
VDDPX_5	Digital pad circuits – UIM1 dual-voltage	-0.3	2.09 3.33	V
VDDPX_6	Digital pad circuits – UIM2 dual-voltage	-0.3	2.09 3.33	V
VDDPX_10	Digital pad circuits – UFS RFCLK and RESET	-0.3	1.41	V
VDDPX_13	Digital pad circuits – internal circuits	-0.3	2.09	V
VDDPX_11	Digital pad circuits – CXO	-0.3	2.09	V
VDD_QFPROM	Programming the QFPROM			
VDD_QFPROM_SP	Programming the QFPROM, internal circuits			
VDDA_APC_CS_1P8	Application processor current sensor 1.8 V circuits			
VDDA_GFX_CS_1P8	Graphics current sensor 1.8 V circuits			
VDDA_USB_HS_1P8	USB HS1/2 1.8 V circuits			
VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits	-0.3	1.485	V
VDDPX_VBIAS_SDC	Reference voltage for SDC			
VDDPX_VBIAS_UIM	Reference voltage for UIM			

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDDIO_EBI0	EBI0 I/O memory circuits	-0.3	0.75	V
VDDIO_EBI1	EBI1 I/O memory circuits			
VDDIO_EBI2	EBI2 I/O memory circuits			
VDDIO_EBI3	EBI3 I/O memory circuits			
VDDIO_CK_EBI0	EBI0 I/O clock circuits			
VDDIO_CK_EBI1	EBI1 I/O clock circuits			
VDDIO_CK_EBI2	EBI2 I/O clock circuits			
VDDIO_CK_EBI3	EBI3 I/O clock circuits			
VDDA_EBI0	EBI0 PHY circuits	-0.3	1.13	V
VDDA_EBI1	EBI1 PHY circuits			
VDDA_EBI2	EBI2 PHY circuits			
VDDA_EBI3	EBI3 PHY circuits			
VDDA_CC_EBI01	EBI0/EBI1 clock circuits			
VDDA_CC_EBI23	EBI2/EBI3 clock circuits			
VDDA_HV_EBI0	EBI0 PHY high-voltage circuits	-0.3	1.375	V
VDDA_HV_EBI1	EBI1 PHY high-voltage circuits			
VDDA_HV_EBI2	EBI2 PHY high-voltage circuits			
VDDA_HV_EBI3	EBI3 PHY high-voltage circuits			
VDDA_CSI_1P2	MIPI CSI 1.2 V circuits			
VDDA_DSI_1P2	MIPI DSI 1.2 V circuits			
VDDA_REFGEN_1P2	REFGEN circuits			
VDDA_PCIE0_PLL_1P2	PCIe0 PLL 1.2 V circuits			
VDDA_PCIE1_PLL_1P2	PCIe1 PLL 1.2 V circuits			
VDDA_QLINK_HV_CK	QLink high-voltage clock circuits			
VDDA_UFS1_1P2	UFS 1.2 V circuits			
VDDA_USB2_SS_1P2	USB2 SS 1.2 V circuits			
VDDA_USB1_SS_DP_1P2	USB1 SS and DisplayPort 1.2 V circuits			
VDDA_USB_HS_3P1	USB HS1/2 3.1 V circuits	-0.3	3.52	V
VDDA_WCSS_ADCDAC_1	WCSS ADC and DAC – chain 1	-0.3	1.49	V
VDDA_WCSS_ADCDAC_2	WCSS ADC and DAC – chain 2			
VDD_WCSS	WCSS circuits	-0.3	0.935	V
VDDA_WCSS_PLL	WCSS PLL circuits			
Thermal conditions				
T_s [1] [2]	Storage temperature	-55	150	°C

1. The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.
2. For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-4). The SA8155 device meets all performance specifications listed in Section 3.5 through Section 3.11, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded)..

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [1]		Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor			
	Turbo	0.660	1.030	V
	Nominal-L1	0.640	0.998	V
	Nominal	0.605	0.938	V
	SVS L1	0.560	0.910	V
VDD_APC1	Kryo Gold application processor			
	Turbo-L1	0.764	1.030	V
	Turbo	0.764	0.974	
	Nominal-L1	0.660	0.934	V
	Nominal	0.624	0.862	V
	SVS L1	0.576	0.846	V
VDD_GFX	Graphics			
	Turbo-L1	0.700	1.030	V
	Turbo	0.660	1.014	V
	Nominal-L1	0.640	0.994	V
	Nominal SVS L2	0.605	0.942	V
	SVS L1	0.560	0.866	V
VDDCX	Digital core circuits			
	Turbo-L1	0.700	1.030	V
	Turbo	0.660	0.962	V
	Nominal	0.605	0.894	V
	SVS L1	0.560	0.874	V
	Retention [2]	0.352	0.480	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [1]		Min	Max	Unit
VDDMX	On-chip memory			
	Turbo-L1	0.740	1.030	V
	Turbo	0.740	0.998	V
	Nominal-L1	0.695	0.998	V
	Nominal	0.695	0.962	V
	SVS-L1	0.695	0.942	V
	Retention [2]	0.516	0.668	V
VDD_MODEM	Modem circuits			
	Turbo-L1	0.700	1.030	V
	Turbo	0.660	0.962	V
	Nominal-L1	0.640	0.930	V
	Nominal	0.605	0.894	V
	SVS L1	0.560	0.874	V
VDDA_EBI0	EBI PHY and clock circuits			
VDDA_EBI1	Turbo	0.660	1.030	V
VDDA_EBI2	Nominal	0.640	0.998	V
VDDA_EBI3	SVS-L1	0.605	0.962	V
	Retention [2]	0.352	0.480	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for this mode in this power domain is a static setting. There is no scaling.

Table 3-3 Operating conditions

Parameter [1]		Min	Typ [2]	Max	Unit
Power supply voltages					
VDDA_CSI0_0P9	MIPI CSI0 0.9 V circuits	0.83	0.88	0.92	V
VDDA_CSI1_0P9	MIPI CSI1 0.9 V circuits				
VDDA_CSI2_0P9	MIPI CSI2 0.9 V circuits				
VDDA_CSI3_0P9	MIPI CSI3 0.9 V circuits				
VDDA_DSI0_0P9	MIPI DSI0 0.9 V circuits				
VDDA_DSI0_PLL_0P9	MIPI DSI0 PLL 0.9 V circuits				
VDDA_DSI1_0P9	MIPI DSI1 0.9 V circuits				
VDDA_DSI1_PLL_0P9	MIPI DSI1 PLL 0.9 V circuits				
VDDA_PCIE0_CORE	PCIe 0 core circuits				
VDDA_PCIE1_CORE	PCIe 1 core circuits				

Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
VDDA_PLL_HV_CC_EBI	EBI high-voltage circuits	0.83	0.88	0.92	V
VDDA_QLINK_LV	QLink low-voltage circuits				
VDDA_QLINK_LV_CK	QLink low-voltage clock circuits				
VDDA_UFS1_CORE	UFS core circuits				
VDDA_USB_HS_CORE	USB digital core circuits				
VDDA_USB2_SS_CORE	USB2 SS core circuits				
VDDA_USB1_SS_DP_ CORE	USB1 SS and DisplayPort core circuits				
VDDA_QREFS_0P875	Reference voltage for QREFS 0.875 V circuits				
VDDA_SP_SENSOR	Internal circuits				
VDDPX_0	Digital pad circuits – control signals	1.70	1.80	1.90	V
VDDPX_1	Digital pad circuits - EBI and DDR I/O	1.06	1.128	1.17	V
VDDPX_2	Digital pad circuits – SDC2	1.70	1.808	1.90	V
		2.72	2.96	3.03	V
VDDPX_3	Digital pad circuits – most I/Os	1.70	1.80	1.90	V
VDDPX_5	Digital pad circuits – UIM1 dual-voltage	1.70	1.808	1.90	V
		2.72	2.928	3.03	V
VDDPX_6	Digital pad circuits – UIM2 dual-voltage	1.70	1.808	1.90	V
		2.72	2.928	3.03	V
VDDPX_10	Digital pad circuits – UFS clock	1.12	1.20	1.28	V
VDDPX_13	Digital pad circuits – internal circuits	1.70	1.856	1.90	V
VDDPX_11	Digital pad circuits – CXO	1.70	1.80	1.90	V
VDD_QFPROM	Programming the QFPROM				
VDD_QFPROM_SP	Programming the QFPROM, internal circuits				
VDDA_APC_CS_1P8	Application processor current sensor 1.8 V circuits				
VDDA_GFX_CS_1P8	Graphics current sensor 1.8 V circuits				
VDDA_USB_HS_1P8	USB HS1/2 1.8 V circuits				
VDDA_QREFS_1P25	Reference voltage for QREFS 1.25 V circuits	1.125	1.25	1.35	V
VDDPX_VBIAS_SDC	Reference voltage for SDC				
VDDPX_VBIAS_UIM	Reference voltage for UIM				

Table 3-3 Operating conditions (cont.)

Parameter [1]		Min	Typ [2]	Max	Unit
VDDIO_EBI0	EBI0 I/O memory circuits	0.57	0.6	0.65	V
VDDIO_EBI1	EBI1 I/O memory circuits				
VDDIO_EBI2	EBI2 I/O memory circuits				
VDDIO_EBI3	EBI3 I/O memory circuits				
VDDIO_CK_EBI0	EBI0 I/O clock circuits				
VDDIO_CK_EBI1	EBI1 I/O clock circuits				
VDDIO_CK_EBI2	EBI2 I/O clock circuits				
VDDIO_CK_EBI3	EBI3 I/O clock circuits				
VDDA_HV_EBI0	EBI0 PHY high-voltage circuits	1.15	1.20	1.25	V
VDDA_HV_EBI1	EBI1 PHY high-voltage circuits				
VDDA_HV_EBI2	EBI2 PHY high-voltage circuits				
VDDA_HV_EBI3	EBI3 PHY high-voltage circuits				
VDDA_CSI_1P2	MIPI CSI 1.2 V circuits				
VDDA_DSI_1P2	MIPI DSI 1.2 V circuits				
VDDA_REFGEN_1P2	REFGEN circuits				
VDDA_PCIE0_PLL_1P2	PCIe0 PLL 1.2 V circuits				
VDDA_PCIE1_PLL_1P2	PCIe1 PLL 1.2 V circuits				
VDDA_QLINK_HV_CK	QLink high-voltage clock circuits				
VDDA_UFS1_1P2	UFS 1.2 V circuits				
VDDA_USB2_SS_1P2	USB2 SS 1.2 V circuits				
VDDA_USB1_SS_DP_1P2	USB1 SS and DisplayPort 1.2 V circuits				
VDDA_USB_HS_3P1	USB HS1/2 3.1 V circuits	2.97	3.072	3.20	V
VDDA_WCSS_ADCDAC_1	WCSS ADC and DAC – chain 1	1.25	1.304	1.36	V
VDDA_WCSS_ADCDAC_2	WCSS ADC and DAC – chain 2				
VDD_WCSS	WCSS circuits	0.675	0.752	0.85	V
VDDA_WCSS_PLL	WCSS PLL circuits				
Thermal conditions [3]					
T_a	Ambient operating temperature	-40	–	+85 ???	°C
T_j	Junction operating temperature	–	–	+105	°C

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. Typical voltages represent the recommended output settings of the companion PMIC device.
3. To maximize the device performance and useful life, follow the thermal guidelines for the system in *Thermal Design Guidance for Qualcomm Snapdragon Infotainment Chipsets* (80-PE986-14).

The TJ max specification must be met.

3.3 Power distribution network

The impedances of the distribution networks that deliver power to the SA8155 device are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the minimum/maximum values listed in Table 3-1 to be violated.

The following tables list the PDN maximum impedance specifications.

Table 3-4 PDN specifications

Power rail	Power domain	DC resistance (mΩ)		Maximum impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
		PMIC VSW BGA to SoC BGA	SMPS SENSE node to SoC BGA	(1-200 MHz)				
				R_{mid_freq} (mΩ)	L (pH)			
VREG_S1A_S2A_ S9A_S10A	VDD_APC1 (Gold)	4.7	1.6	16	127	1	AN31, AM32, AM30, AL31, AN35, AN33, AL35, AL33, AK30, AJ31, AG31, AG29, AF30, AJ35, AG35, AG33, AD32, AC31, AC29, AE35, AE33, AD34, AC33	AM28, AP32, AL29, AM34, AH28, AK32, AJ27, AH32, AF32, AK34, AG37, AF34, AE27, AE29, AB28, AB30, AB32, AA35, AA37
VREG_S3A	VDD_APC0 (Silver)	8	2.5	40	250	1	AK26, AK28, AL27, AM26, AN27, AC27, AD26, AD28, AF26, AF28, AG27, AH26	AJ25, AJ27, AL29, AM24, AM28, AP28, AB26, AB28, AB30, AD24, AE25, AE27, AE29, AG25, AH28
VREG_S1C_S2C_ S3C	VDD_GFX	3.7	1.5	21	130	1	V12, W13, W15, Y16, AA17, V18, W19, Y20, R15, T16, R19, R21, T18, U21, N13, P12, P14, P16, N17, P18	AA11, AB16, V14, Y12, AA21, Y22, R13, T12, U15, R17, T20, T22, U17, M12, M14, N11, N15, L19, P20, W11
VREG_L1A	VDD_WCSS	–	45	132	900	1	AA13, AB12, AC13, AC15, Y14	AA11, AB16, AD12, AD14, Y12
VREG_S8A	VDD_MODEM [2]	12	2.75	50	240	1	U27, V28, U31, V30, V32, U33, U35, V34, P28, T28, P30, P32, R31, P34, R35, T34	V26, W27, W31, V36, W33, M26, R29, T32, M34, R33

Table 3-4 PDN specifications (cont.)

Power rail	Power domain	DC resistance (mΩ)		Maximum impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
		PMIC VSW BGA to SoC BGA	SMPS SENSE node to SoC BGA	(1-200 MHz)				
				R_{mid_freq} (mΩ)	L (pH)			
VREG_S10C	VDD_MX	17	7.5	95	850	1	AH34, AJ33	AH32, AK32, AK34, AM34
		17	7.5	95	610	2	T14, U13	R13, T12, U15, V14
		7	2.5	32	250	3	AH14, AJ13, AK12, AL13, AM12, AE13, AE15, AF12, AF14, AG15, AD18, AF16, AA19, AB20, AC17, AC19, AA23, AB22, AC21, W23, N21, P22, P24, R23, T24, U23, V22, V24	AH12, AJ15, AK14, AM14, AD12, AD14, AG11, AG13, AD20, AE19, AG17, AB16, AA21, AB26, Y22, N23, R25, T22, V26, P20, T20
VREG_S7C_S8C_ S9C	VDD_CX	8.7	3.5	24	150	1	AA25, AA27, AB24, AC23, AC25, W25, Y26, Y28, AA29, AA31, AA33, Y30, Y32, Y34, P26, T26, U25	AB26, AB28, V26, W27, Y22, Y24, AA35, AB30, AB32, W31, W33, M26, N23, R25, T22
		7.7	3	20	120	2	AK16, AL15, AM16, AN15, AK20, AL19, AM20, AN19, AK22, AK24, AL23, AM22, AN23, AJ17, AE21, AF20, AG19, AH18, AH20, AJ19, AE23, AF24, AG23, AH22, AJ23	AK14, AL17, AM14, AN13, AN17, AP14, AK18, AL21, AN21, AP18, AP20, AM24, AP24, AG17, AH16, AJ15, AD20, AE19, AJ21, AD22, AD24, AE25, AE27, AG25, AJ25, AJ27

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

2. VDD_MODEM PDN specification is provided for audio use case (re-purposed modem processor for audio), not LTE modem use case.

Table 3-5 PDN specifications–DDR rails

Power rail	Power domain	DC resistance (mΩ)	Maximum effective impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
			(1-200 MHz)				
			R_{mid_freq} (mΩ)	L (pH)			
VREG_L11C	VDDA_EBI	52	120	1820	1	AR29, AR31	AP28, AP32, AT28, AT30
		52	120	1820	2	AR15, AR17	AP14, AP18, AT16, AT18
		52	120	1820	3	L29, L33	K28, K30, M34
		52	120	1820	4	L13, L17	K16, K18, M14, M12
VREG_S7A	VDDIO_EBI	33	20	1115	1	AT32, AU27, AU29, AU33	AT28, AT30, AP32
		33	20	1115	2	AT14, AU13, AU17, AU19	AT16, AT18, AP14, AP12
		33	20	1115	3	J27, J29, J33, K32	K28, K30, G31, J25
		33	20	1115	4	J13, J17, J19, K14	J21, L19, K18, K16

1. The PDN AC effective impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

Table 3-6 PDN specifications–SerDes rails

Power rail	Power domain	DC resistance (mΩ)		Maximum impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
		Lump	Dist.	(1-200 MHz)				
				R_{mid_freq} (mΩ)	L (pH)			
VREG_L5A	VDDA_USB_SS_DP_CORE	64	258	98	625	1	AJ37, AN37	AK34
	VDDA_QLINK_LV_CK (not applicable to SA8155P/SA8150P)		4000	138	880	2	U37	V36, W33, AA35
	VDDA_USB_SS_CORE		649	138	880	3	AR37	AT36
	VDDA_UFS_2LN_CORE		341	116	740	4	AC37, AE37	AG37, AA35
	VDDA_QLINK_LV (not applicable to SA8155P/SA8150P)		683	157	1000	5	W37	AA37
	VDDA_USB_HS_CORE		50	235	1500	6	AL37	AK34
	VDDA_PLL_HV_CC_EBI01		1200	236	1500	7	AP26	AP28
	VDDA_PLL_HV_CC_EBI23		1200	236	1500	8	K24	J25

Table 3-6 PDN specifications–SerDes rails (cont.)

Power rail	Power domain	DC resistance (mΩ)		Maximum impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
		Lump	Dist.	(1-200 MHz)				
				R_{mid_freq} (mΩ)	L (pH)			
VREG_L8C	VDDA_DSI_1P2	94	944	170	1080	1	AT22	AR21
	VDDA_USB_SS_DP_1P2		786	188	1200	2	AK36	AK34
	VDDA_CSI_1P2		661	157	1000	3	AM10	AL9
	VDDA_PCIE_1LN_PLL_1P2		1633	236	1500	4	AA9	AB8
	VDDA_PCIE_2LN_PLL_1P2		589	236	1500	5	W9	V8
	VDDA_QLINK_HV_CK (not applicable to SA8155P/SA8150P)		4000	220	1400	6	R37	N37
	VDDA_UFS_2LN_1P2		1200	212	1350	7	AH36	AG37
	VDDA_USB_SS_1P2		1500	173	1100	8	AU35	AT36
	VDDA_HV_EBI0		350	250	1592	9	AR33	AP32, AM34
	VDDA_HV_EBI1		350	250	1592	10	AR13	AP14
	VDDA_HV_EBI2		350	250	1592	11	L31	K30
	VDDA_HV_EBI3		350	250	1592	12	L15	M14
VREG_L18C	VDDA_PCIE1_CORE	60	142	114	725	1	Y10	W11
	VDDA_PCIE0_CORE		333	118	750	2	AB10	AC9
	VDDA_DSI_0_0P9		600	170	1080	3	AT24	AP24
	VDDA_DSI_1_0P9		600	196	1250	4	AU21	AV22
	VDDA_DSI_0_PLL_0P9		3500	204	1300	5	AU23	AW23
	VDDA_DSI_1_PLL_0P9		3500	196	1250	6	AT20	AR21
	VDDA_MIPI_CSI0_0P9		347	157	1000	7	AJ11	AH12
	VDDA_MIPI_CSI1_0P9		347	157	1000	8	AL11	AK10
	VDDA_MIPI_CSI2_0P9		347	157	1000	9	AN11	AP12
	VDDA_MIPI_CSI3_0P9		347	157	1000	10	AP10	AR9

Table 3-6 PDN specifications–SerDes rails (cont.)

Power rail	Power domain	DC resistance (mΩ)		Maximum impedance $Z_{specification}$ [1]		Port number	Pin number of positive ports	Pin number of negative ports
		Lump	Dist.	(1-200 MHz)				
				R_{mid_freq} (mΩ)	L (pH)			
VREG_L12A	VDDA_USB_HS_1P8	NA	75	315	2000	1	AU37	AT36
VREG_L2A	VDDA_USB_HS_3P1	NA	125	315	2000	1	AP36	AT36

1. The PDN AC impedance specification (mask) is obtained by plotting $Z_{specification}$ using R_{mid_freq} and AC Inductance (L) values. $Z_{specification}$ is the maximum impedance allowed from 1 MHz. to 200 MHz.

$$Z_{specification} = \sqrt{R_{mid\_freq}^2 + (2\pi f L)^2}$$

3.4 Average operating current

Detailed current consumption information and details about the operating modes tested are available in *SA8155 Linux Android Current Consumption Data* (80-PE986-7).

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the SA8155 device, and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-7 DC specification of 1.8 V I/Os, CXO input, and SLEEP_CLK input [1]

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDPX_x [2]	VDDPX_x + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDPX_x	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDPX_x	VDDPX_x + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDPX_x	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [3]	–	1.0	µA
I_{IL}	Input low leakage current [3]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [3]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [3]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)

Table 3-7 DC specification of 1.8 V I/Os, CXO input, and SLEEP_CLK input [1]

Parameter	Description	Min	Max	Units
I_{OZHKP}	High-level, tri-state leakage current with keeper [4]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [5]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage	VDDPX_x - 0.45	VDDPX_x	V
V_{OL}	Low-level output voltage	0.0	0.45	V

1. Only input related DC specification is applicable to CXO and SLEEP_CLK pads; HIHYS_EN = high for CXO and SLEEP_CLK pads
2. VDDPX_x can be VDDPX_0, VDDPX_3 or VDDPX_11 depending on the pad group.
3. I_{IH}, I_{IL}, I_{OZH} and I_{OZL} values are based on nominal PVT (TT/25°C).
4. Pin voltage = VDDPX_x maximum. For keeper pins, pin voltage = VDDPX_x maximum - 0.45 V.
5. Pin voltage = GND and supply = VDDPX_x maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX_x maximum.

Table 3-8 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX_2	–	VDDPX_2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDPX_2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDDPX_2	–	VDDPX_2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDPX_2	V

Table 3-9 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA

Table 3-9 SDC 1.8 V mode DC specifications (cont.)

Parameter	Description	Min	Typ	Max	Units
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-10 UICC 3 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 ×VDDPX_x (RST, CLK) and 0.4 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-11 UICC 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_x	–	VDDPX_x + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_x	V
V_{HYS}	Schmitt hysteresis voltage [2]	100	–	–	mV

Table 3-11 UICC 1.8 V mode DC specifications (VDDPX_5 and VDDPX_6) (cont.)

Parameter	Description	Min	Typ	Max	Units
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [3]	0.8 × VDDPX_x	–	VDDPX_x	V
V_{OL}	Low-level output voltage [4]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. V_{HYS} is not a required specification for UICC.
3. UICC specifies V_{OH} = 0.8 × VDDPX_x (RST) and 0.7 × VDDPX_x (CLK, I/O). The worst-case V_{OH} is used in this table.
4. UICC specifies V_{OL} = 0.2 × VDDPX_x (RST, CLK) and 0.3 V (I/O). The worst-case V_{OL} is used in this table.

Table 3-12 Digital I/O characteristics for VDDPX_10 nominal (UFS_RESET and REFCLK)

Parameter	Description	Min	Max	Units
V_{OL}	Output low-level voltage	0	0.25 × VDDPX_10	V
V_{OH}	Output high-level voltage	0.75 × VDDPX_10	VDDPX_10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ
I_{OZH}	High-level, tri-state leakage current	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All SA8155 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.6.2.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-1.

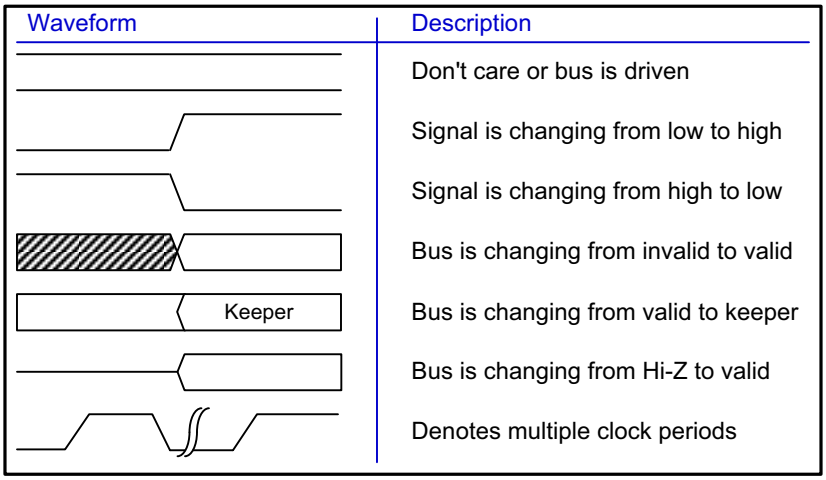


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize SA8155 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-2.

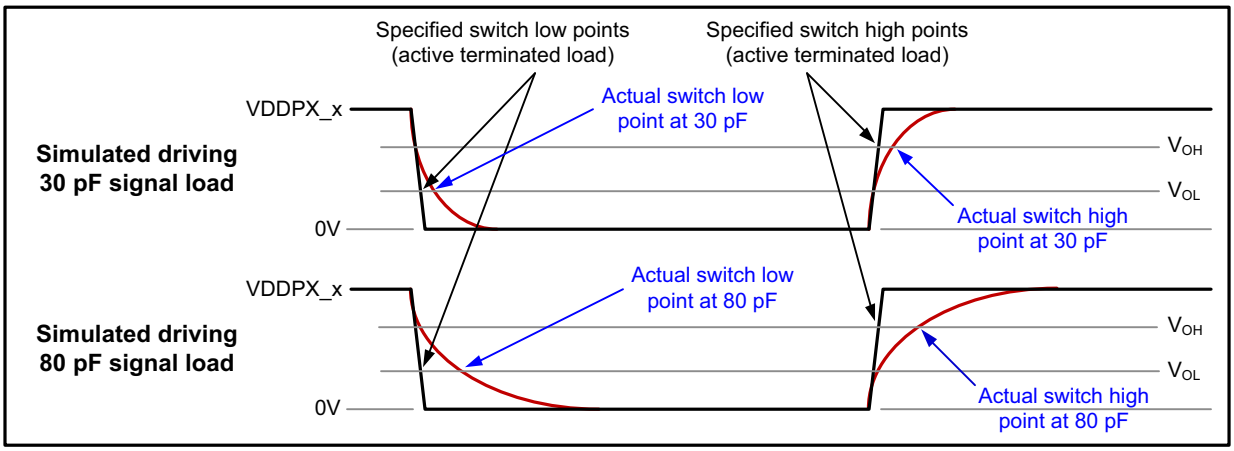


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the SA8155 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.6.3 Pad design methodology

The SA8155 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DDPX_x} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DDPX\_x}/2$ (or 50% of V_{DDPX_x}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_x} for V_{IL} and 65% of V_{DDPX_x} for V_{IH}.

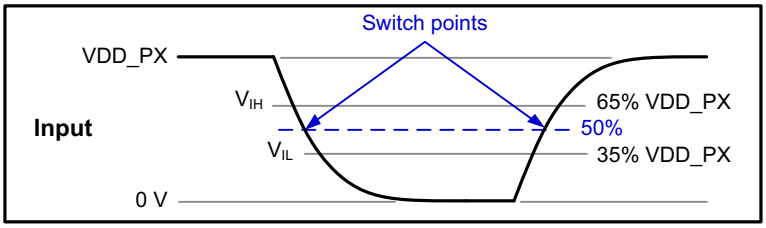


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- $V_{OH} \sim V_{DDPX\_x}$ - 50 mV or more
- $V_{OL} \sim$ 50 mV or less

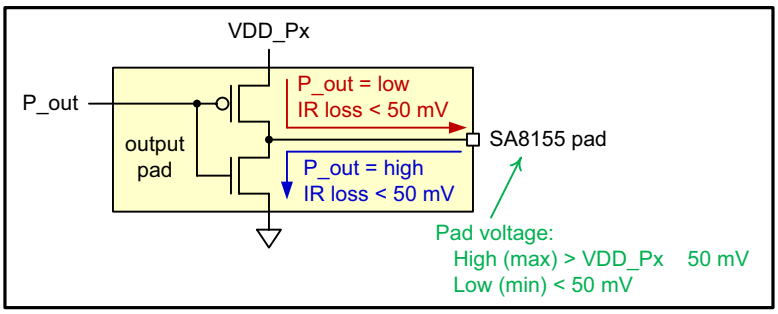


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DDPX_x} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DDPX_x} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Because the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.7 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse and hold time numbers may get better.

3.7.1 EBI memory support

The EBI0, EBI1, EBI2, and EBI3 ports are dedicated to the off-chip LPDDR SDRAM memory. It supports LPDDR4X SDRAM memory parts which are compliant to JEDEC standard for Low Power Double Data Rate 4X (LPDDR4X) SDRAM (JESD209-4B).

3.8 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.8.1 Camera interfaces

The SA8155 device supports up to four D-PHY or C-PHY camera interfaces.

Table 3-13 Supported MIPI-CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 is not supported; DPCM predictor 2 is not supported.
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.0	The maximum supported data rate is 1.5 Gsps.

3.8.2 Audio support

The Audio-related interfaces supported with SA8155 include:

- SLIMbus: Section 3.9.9
- I^2S: Section 3.9.10
- PCM/TDM: Section 3.9.11

3.8.3 Display support

The SA8155 device supports up to two D-PHY or C-PHY displays.

Table 3-14 Supported MIPI-DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	Virtual channel
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

3.9 Connectivity

The connectivity functions supported by the SA8155 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- DisplayPort interface
- Peripheral Component Interconnect Express (PCIe) interfaces
- Universal Flash Storage (UFS)

- Reduced Gigabit Media Independent Interface (RGMII)
- Reduced Media Independent Interface (RMII)
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Transport stream interface (TSIF) interfaces
- Touchscreen connections
- Through proper configuration of the 20 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - Dedicated I^2C interfaces for camera (CCI I^2C)
  - Improved Inter Integrated Circuit (I3C) interface

Pertinent specifications for these functions are detailed in the following subsections.

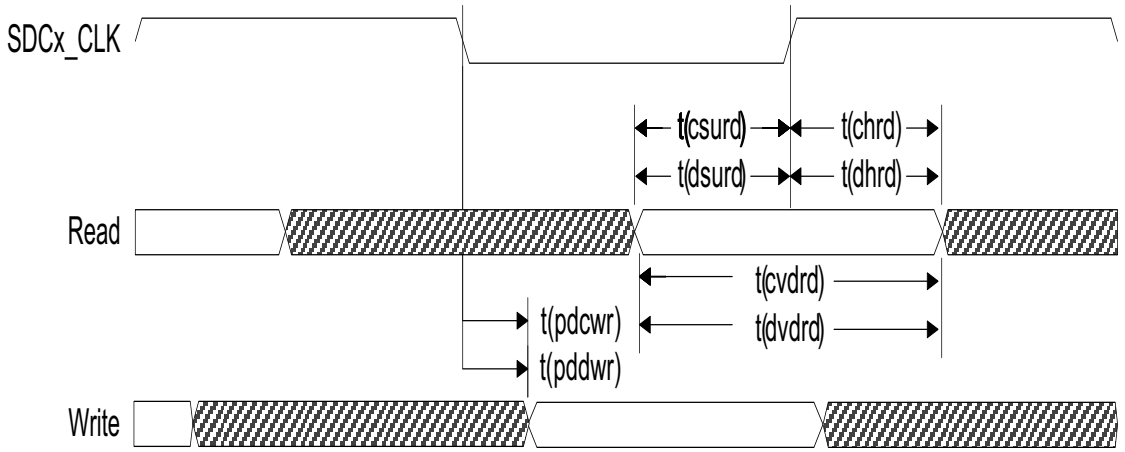
NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 SD interfaces

Table 3-15 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Single data rate SDR mode



Double data rate DDR mode

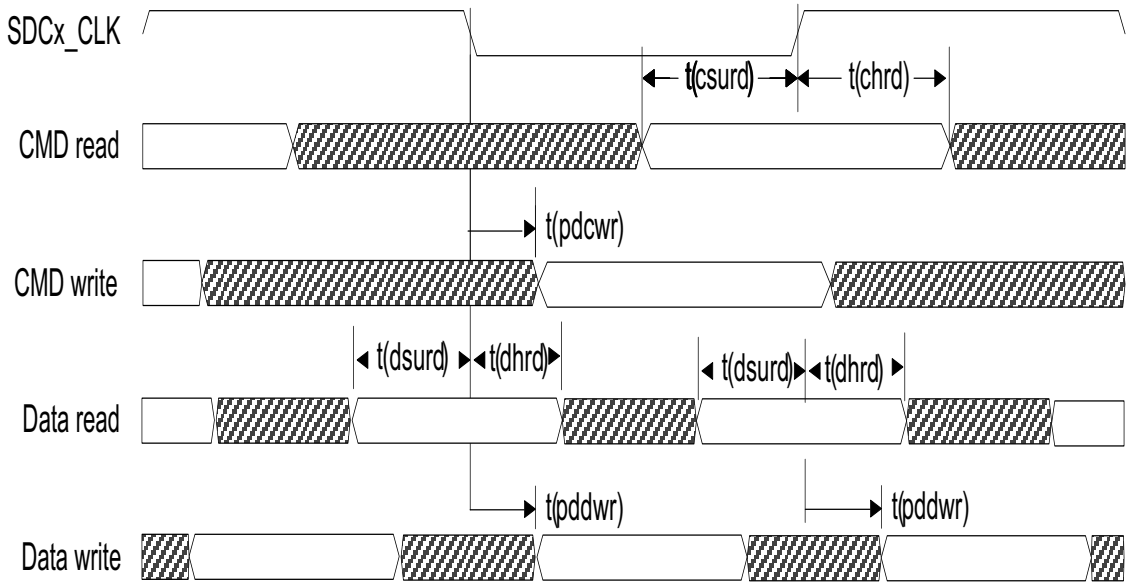


Figure 3-5 SD interface timing

3.9.2 USB interfaces

Table 3-16 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	None
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.9.3 DisplayPort

Table 3-17 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

NOTE: DisplayPort++ is not supported.

3.9.4 PCIe interface

Table 3-18 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI_Express_Base_Specification_Revision_3.0	Link configure capability

NOTE:

- SA8155 supports root complex (RC) mode only on PCIe0 port and both (RC) mode, and endpoint (EP) mode on PCIe1 port.

3.9.5 UFS interface

Table 3-19 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	Rate B, WriteBooster, Host Performance Booster (HPB), DeepSleep Power Mode, Performance Throttling

3.9.6 RGMII interface

Table 3-20 Supported RGMII standards and exceptions

Applicable standard	Feature exceptions
Reduced Gigabit Media Independent Interface (RGMII) v1.3 and v2.0	None

NOTE: RGMII interface supports 1.8 V mode only and is compliant with JESD8-7.

3.9.7 RMII interface

Table 3-21 Supported RMII standards and exceptions

Applicable standard	Feature exceptions
Reduced Media Independent Interface (RMII) v1.2	None

NOTE: RMII interface supports 1.8 V mode only and is compliant with JESD8-7.

3.9.8 UICC interface

Table 3-22 Supported UICC standards and exceptions

Applicable standard	Feature exceptions
ISO/IEC 7816-3	Class A

3.9.9 SLIMbus interface

Table 3-23 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.9.10 I^2S interfaces

Table 3-24 Supported I^2S standards and exceptions

Applicable standards	Feature exceptions
Philips I^2S Bus Specifications revised June 5, 1996	None

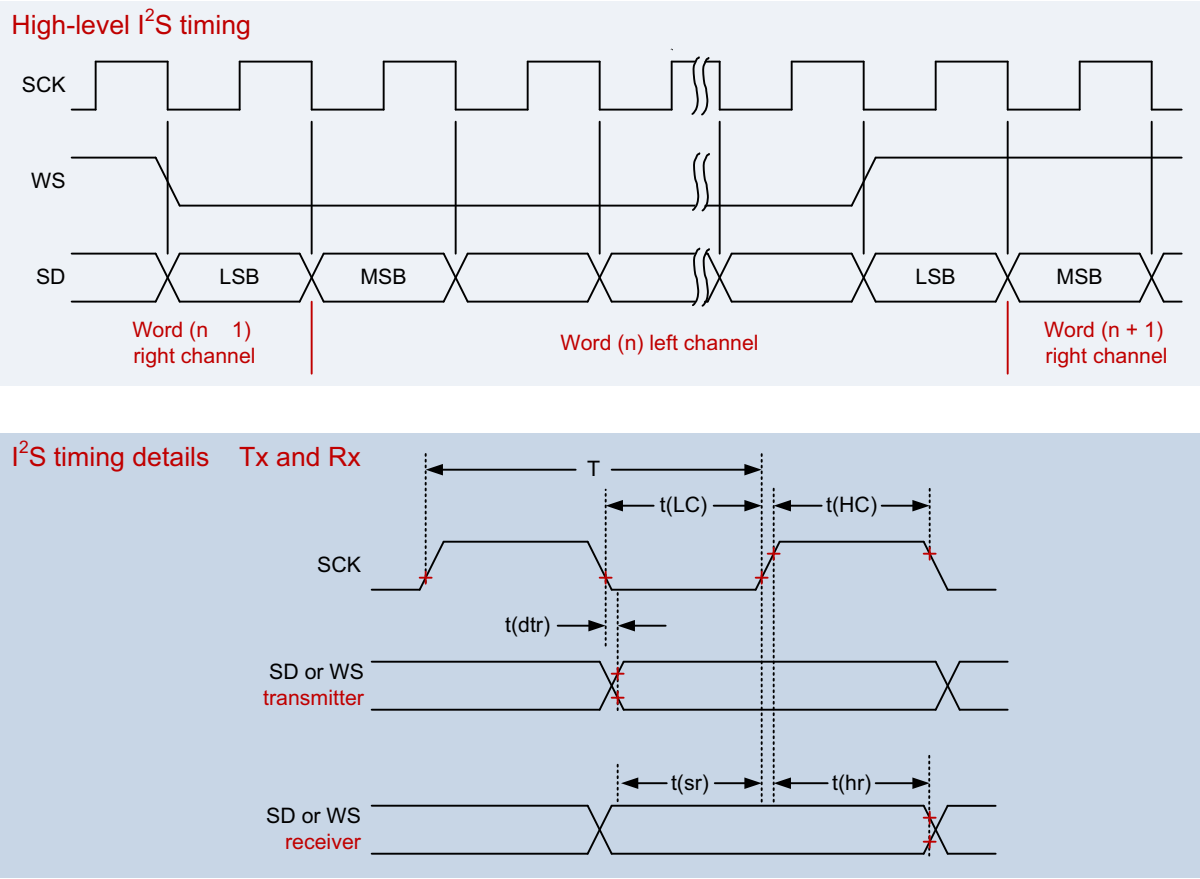


Figure 3-6 I²S timing diagram

Table 3-25 I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.40 × T	–	0.60× T	ns
t(LC)	Clock low		0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns

Table 3-25 I²S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	6.10	ns

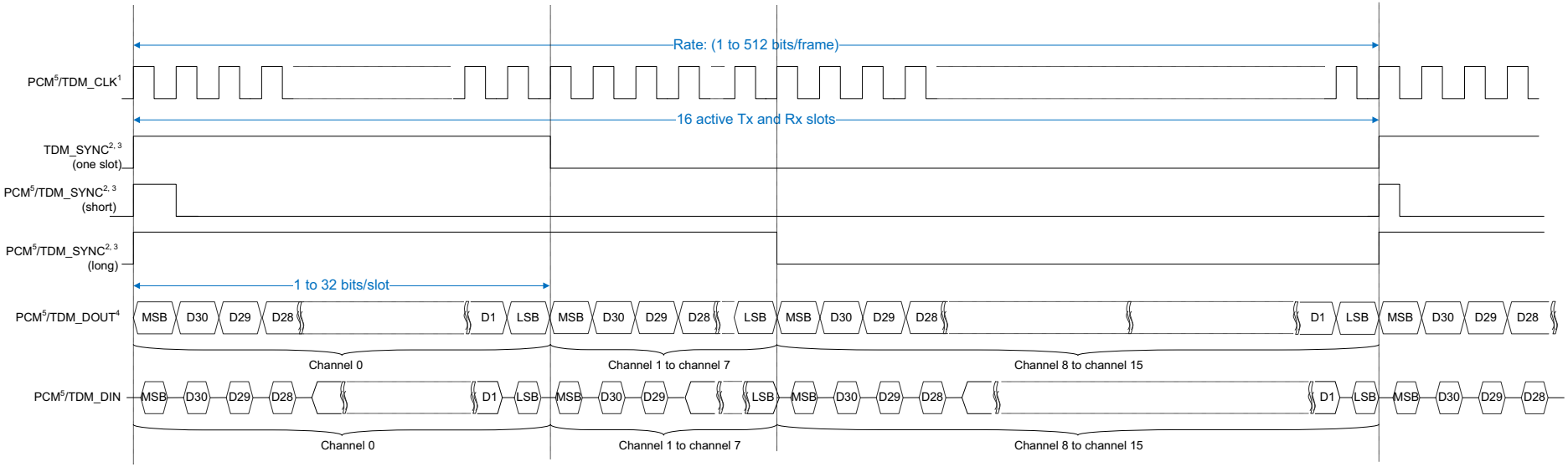
1. Load capacitance is between 10 pF and 40 pF.

Table 3-26 HS-I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using External SCK						
	Frequency	–		–	73.728	MHz
T	Clock period	–	13.56	–	–	ns
t(HC)	Clock high	–	0.40 × T	–	0.60 × T	ns
t(LC)	Clock low	–	0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time	–	2.71	–	–	ns
t(hr)	SD and WS input hold time	–	1.5	–	–	ns

1. Load capacitance is between 10 pF and 40 pF.

3.9.11 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:

1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-7 PCM/TDM audio format with different sync modes

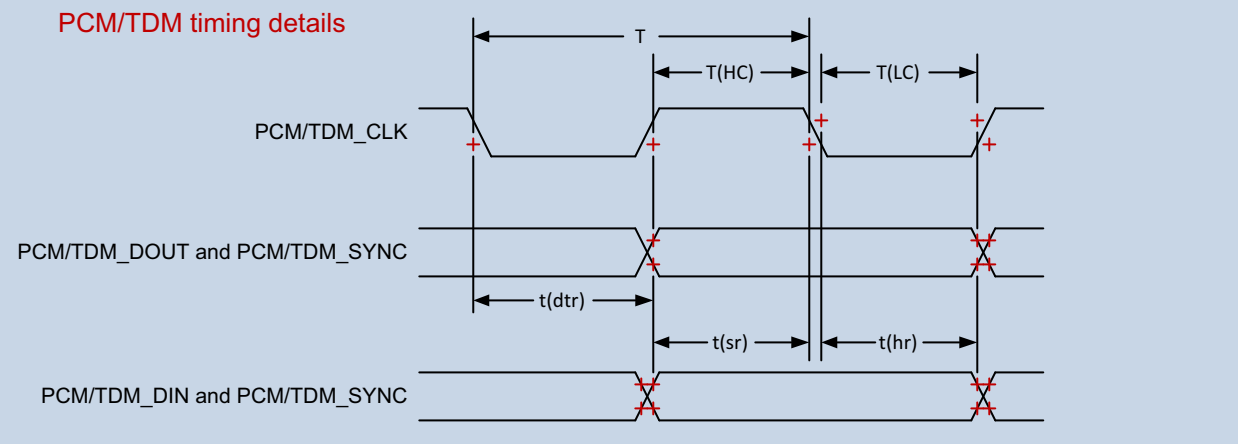


Figure 3-8 PCM/TDM timing diagram

Table 3-27 PCM/TDM interface timing parameters

Parameter [1]		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576 [2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45 × T	0.55 × T	ns
t(LC)	Clock low		0.45 × T	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns
Slave mode					
Frequency			–	24.576[2]	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.40 × T	0.60 × T	ns
t(LC)	Clock low		0.40 × T	0.60× T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	6.10	ns

1. Load capacitance is between 10 pF to 40 pF.
2. End-to-end testing for the TDM clock is completed up to 12.288 MHz.

3.9.12 TSIF

Table 3-28 Supported TSIF standards and exceptions

Applicable standard	Feature exceptions
ITU-T H.222.0 Transport Stream (HTS); also known as *ISO/IEC 13818-1*	None

3.9.13 Touchscreen connections

Touchscreen panels are supported using I^{2}C buses (Section 3.9.14) and GPIOs configured as discrete digital inputs (Section 3.5). Additional specifications are not required.

3.9.14 I^{2}C interface

Table 3-29 Supported I^{2}C standards and exceptions

Applicable standard	Feature exceptions
I^{2}C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

3.9.15 Serial peripheral interface

The SA8155 device supports SPI as master on all the 20 QUP ports and the additional Quad-SPI interface. SPI slave mode is supported on the six QUP ports as listed in Table 1-2.

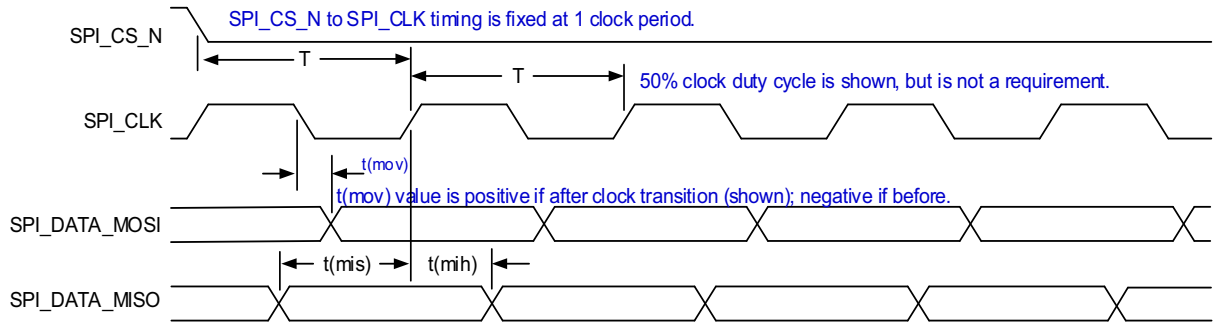


Figure 3-9 SPI master mode 0 timing diagram

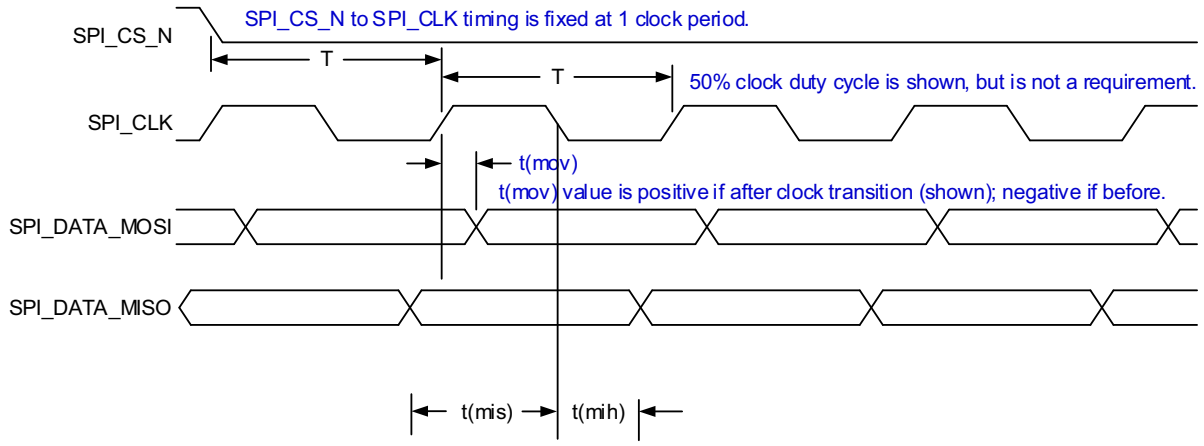


Figure 3-10 SPI master mode 1 timing diagram

NOTE: Depending on the mode configuration (Clock PHA and POL settings), Tx and Rx sampling edge could differ. The timing diagram above shows mode 0 and mode 1 as example.

Table 3-30 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	48 MHz maximum	20	–	–	ns
t(ch)	Clock high	9	–	–	ns
t(cl)	Clock low	9	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

Table 3-31 SPI master timing characteristics for QUP_17 and QUP_19

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	26 MHz maximum	38	–	–	ns
t(ch)	Clock high	17	–	–	ns
t(cl)	Clock low	17	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	3	–	–	ns
t(mih)	Master input hold	3	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

Table 3-32 SPI slave timing characteristics for QUP_0/QUP_1/QUP_2/QUP_9/QUP_10/ QUP_15

Parameter	Comments	Min	Max	Units
T (SPI slave clock period) [1]	48 MHz maximum	20.0	–	ns
t(ch)	Clock HIGH	9	–	ns
t(cl)	Clock LOW	9	–	ns
t(sov) [2]	Slave output valid	2	13	ns
t(sis)	Slave input setup	3	–	ns
t(sih)	Slave input hold	3	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.
2. The total capacitive load must not exceed 30 pF for a single slave system. For each additional slave, 10 pF should be added to the clock and data lines (not needed for chip select since it is one-to-one). For example, 40 pF for two slaves, although most systems have only a single slave. Care must be taken to verify that every slave can drive the data line fast enough to meet the timing requirement or the system must use a reduced frequency.

NOTE: Only SPI slave mode 1 (PHA = 1 and POL = 0) is supported.

3.9.15.1 Quad serial peripheral interface (QSPI)

QSPI core implements the serial peripheral interface protocol to be used for different purposes in the chip-level. The QSPI purpose is to read/write from/to a flash device through an SPI slave by transmitting the physical layer of the SPI protocol according to configurations loaded by software. QSPI core supports single, dual, and quad data bit serial transfers

QSPI core supports the following clocking modes and frequencies:

1. SDR, mode 0 (CPOL = 0, CPHA = 0), SPI clock = 60 MHz
2. DDR, mode 0 (CPOL = 0, CPHA = 0), SPI clock = 60 MHz

Table 3-33 QSPI external interface to NOR-flash device

Signal	In/out	Description
QSPI_CLK	Out	QSPI clock going to the NOR-flash device
QSPI_CS_N	Out	Chip select
QSPI_MOSI	Out	Serial data output from the QSPI core to the NOR-flash device
QSPI_MOSI_OE	Out	Data output enable
QSPI_MISO	In	Serial data input from the QSPI core to the NOR-flash device
QSPI_FB_CLK	In	Delayed version of QSPI_CLK, routed back from the I/O pad.

3.9.15.2 QSPI timing specifications

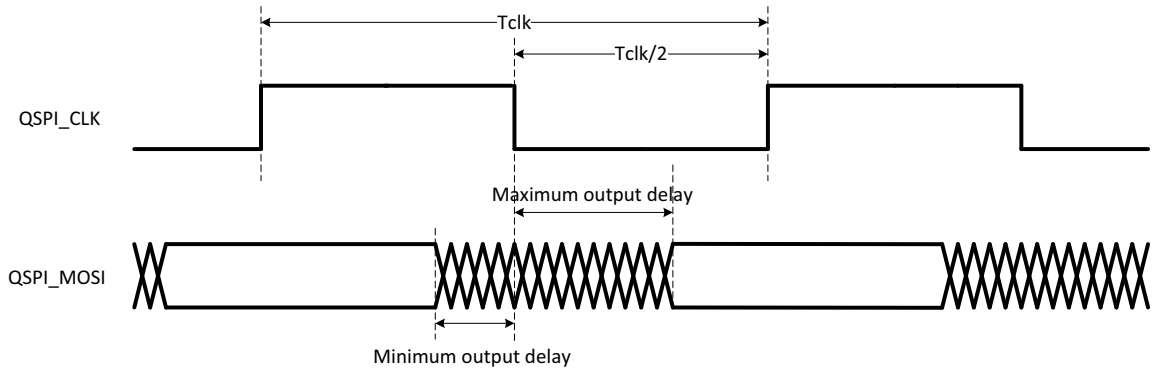


Figure 3-11 SDR output timing diagram

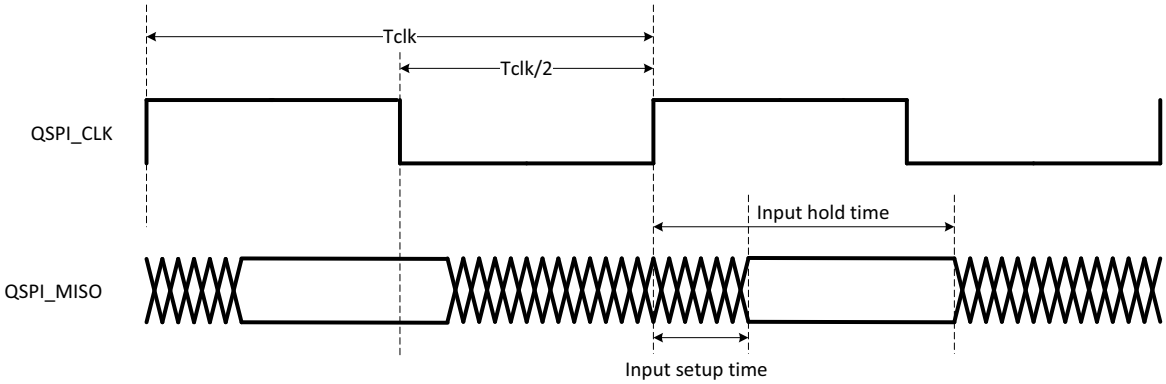


Figure 3-12 SDR input timing diagram

Table 3-34 SDR AC parameters

Parameter	Comments	Min	Max	Unit
1/T	QSPI clock frequency	–	60	MHz
t(mov)	Master output valid	-4.515	5.515	ns
t(mis)	Master input setup	2	–	ns
t(mih)	Master input hold	1	–	ns

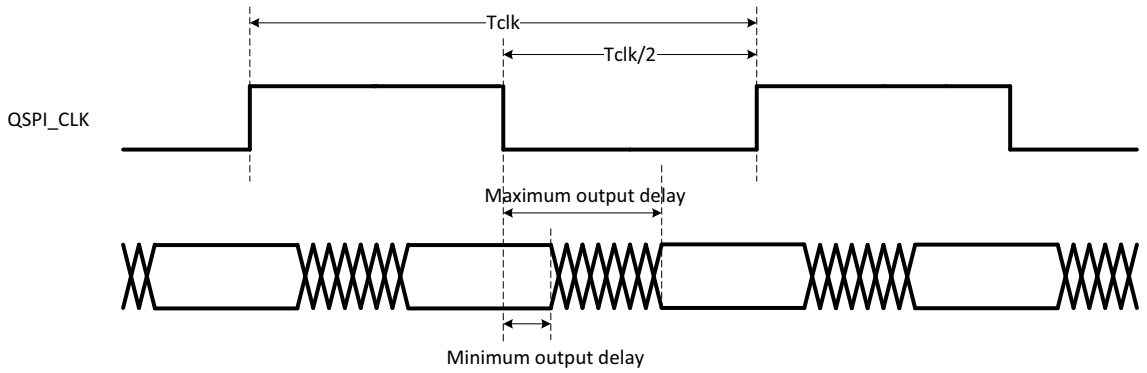


Figure 3-13 DDR output timing diagram

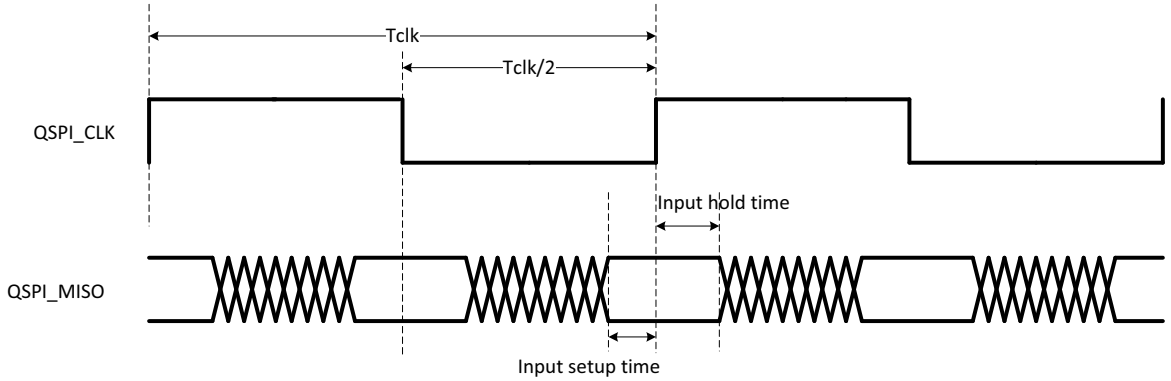


Figure 3-14 DDR input timing diagram

Table 3-35 DDR AC parameters

Parameter	Comments	Min	Max	Unit
1/T	QSPI clock frequency	–	60	MHz
t(mov)	Master output valid	1.5	6.015	ns
t(mis)	Master input setup	1.515	–	ns
t(mih)	Master input hold	1.5	–	ns

3.9.16 I3C interface

Table 3-36 I3C interface

Applicable standard	Feature exceptions
I3C Specification, version 1.0	None

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.10.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.10.1.1 19.2 MHz CXO input

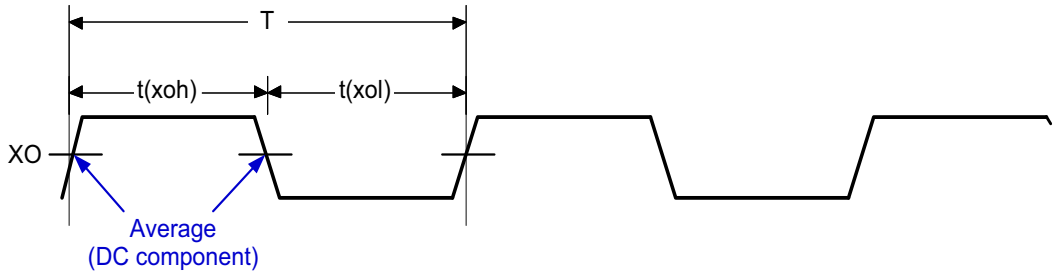


Figure 3-15 XO timing parameters

Table 3-37 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. See the *38.4 MHz Modem Crystal for Industrial Temperature and Automotive (AEC-Q200) Qualification Requirements and Approved Suppliers* (80-NJ458-29 to be released) for more information.

3.10.1.2 Sleep clock

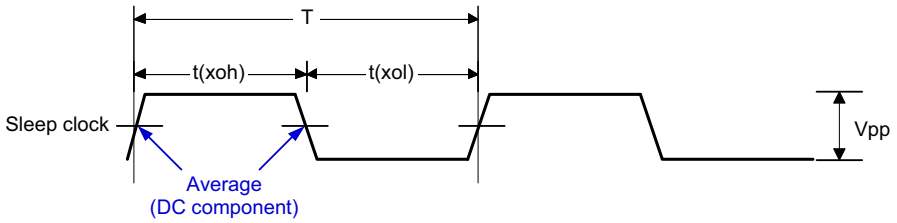


Figure 3-16 Sleep clock timing parameters

Table 3-38 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.521	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.10.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.5.

3.10.3 JTAG

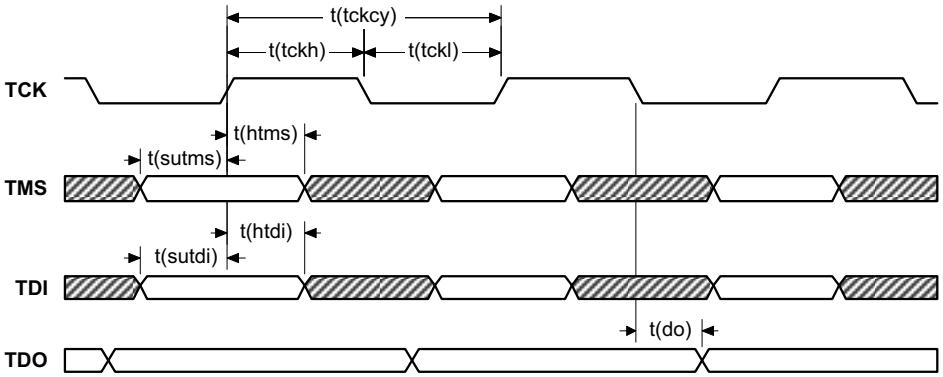


Figure 3-17 JTAG interface timing diagram

Table 3-39 JTAG interface timing characteristics

Parameter		Min	Type	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.10.4 SWD

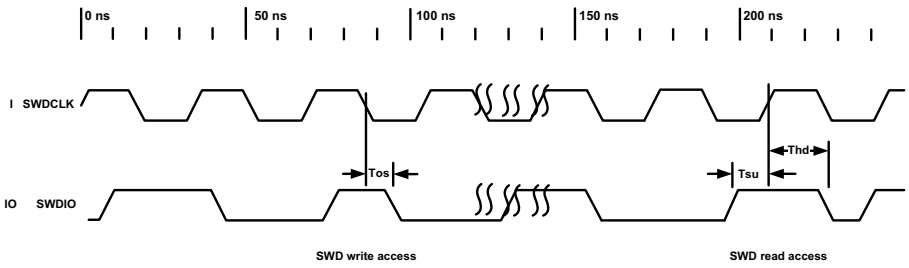


Figure 3-18 SWD write and read AC timing diagram

Table 3-40 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and rising edge of SWDCLK	6.5	–	ns
T_{hd}	Input hold time between SWDIO and rising edge of SWDCLK	6.5	–	ns

3.11 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-3. The digital I/Os must meet the logic-level requirements specified in Section 3.5. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.11.1 Qualcomm RF Front End (RFFE)

Table 3-41 Supported Qualcomm RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 2.0	None

3.11.2 System power management interface (SPMI)

Table 3-42 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

4.1 Device physical dimensions

The SA8155 device is available in the FCBGA989+HS that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The FCBGA989+HS has a 23.0 mm by 23.0 mm body, with a maximum height of 2.26 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download *PACKAGE OUTLINE DRAWING, FCBGA989+HS, 23.0 x 23.0 x 2.26 mm, S490, L1240, PL2, HEAT SPREADER* (NT90-PF731-2) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-PF731-2.

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the correct ball location. To download this text file, manually search for the NT90 in CreatePoint, and click the appropriate link in the **Related Files** line that is located directly underneath the PDF link.

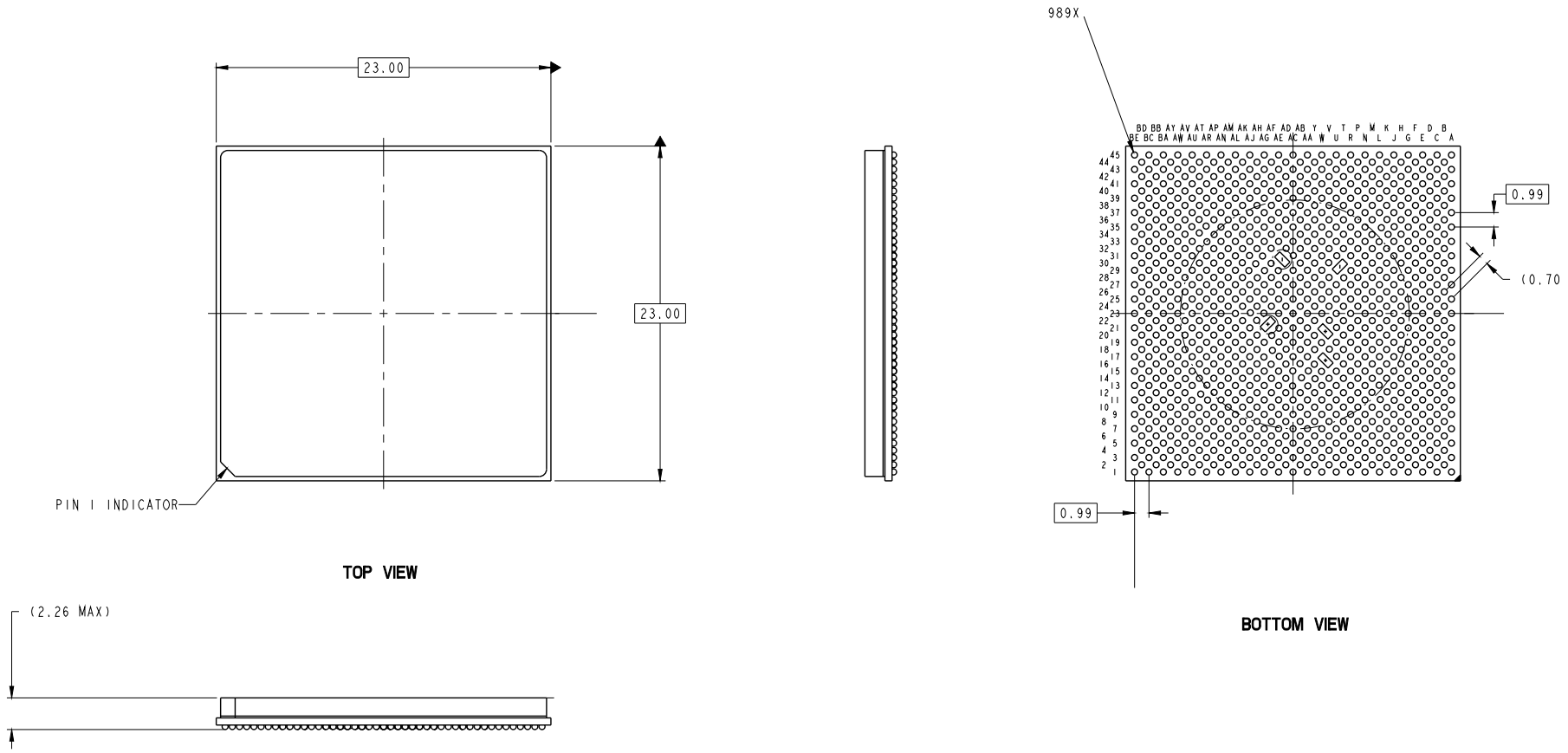


Figure 4-1 Simplified FCBGA989+HS outline drawing

NOTE: This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

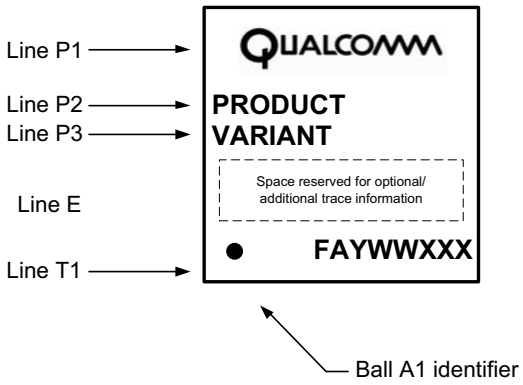


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 SA8155 marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm name or logo
P2	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ See Table 4-4 for assigned values
P3	VARIANT	P = Product variant information ■ See Table 4-4 for assigned values.
E	Blank or random	Optional or Additional trace information
T1	•	Pin 1 or pin A1 indicator
	FAYWWXXX	F = wafer fab source of supply code ■ F = F (TSMC) A = assembly site code ■ A = C (Amkor, Korea) Y = single-digit year WW = work week (based on calendar year) XXX = traceability number

NOTE: For complete marking definitions of all SA8155 variants and revisions, see the *SA8155 Device Revision Guide* (80-PE986-4).

Table 4-2 QFPROM_CORR_PTE_ROW0_LSB register (Address: 0x0784130)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants (see Table 4-3).
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number (see Table 4-3).

4.3 Device ordering information

4.3.1 Specification-compliant devices

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part. This device can be ordered using the identification code shown in Table 4-3.

Table 4-3 Device identification code

Device ID code	AAA-AAAA	-P	TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [1]
Symbol definition	Product name	Configuration code	Package type	Number of pins	Package variable	Additional package information	Shipping package	Product revision	Source code	Feature code
Example	SA-8155P	-0	-FCBGA	989		+HS	-TR	-04	-0	-AC

1. The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example:

- Example 1: SA-8155P-0-FCBGA989+HS-TR-04-0-AC

Table 4-3 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-4.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable)[1]	Hardware revision number	FEATURE_ID[2]	Hardware version	S value [3]	Comments
SA8150P	Pre-ES	200-AA	0x0 00E9 0E1	0x0	v1.0	0	SA8150P, FCBGA989+HS; No modem; Kryo Gold 1920 MHz, Kryo Gold Prime 2227.2 MHz, GPU 500 MHz
SA8155P	ES1	001-AC	0x1 00E9 0E1	0x0	v2.0	0	SA8155P, FCBGA989+HS; No modem; Kryo Gold 2131.2 MHz, Kryo Gold Prime 2419.2 MHz, GPU 700 MHz
SA8155P	ES2	003-AC	0x2 00E9 0E1	0x0	v2.1.1	0	SA8155P, FCBGA989+HS; No modem; Kryo Gold 2131.2 MHz, Kryo Gold Prime 2419.2 MHz, GPU 700 MHz
SA8155P	ES3	004-AC	0x3 00E9 0E1	0x0	v2.2	0	SA8155P, FCBGA989+HS; No modem; Kryo Gold 2131.2 MHz, Kryo Gold Prime 2419.2 MHz, GPU 700 MHz
SA8150P	ES3	004-AB	0x3 00E9 0E1	0x1	v2.2	0	SA8150P, FCBGA989+HS; No modem; Kryo Gold 1920 MHz, Kryo Gold Prime 2227.2 MHz, GPU 500 MHz
SA8155P	CS [4]	004-AC	0x3 00E9 0E1	0x0	v2.2	0	SA8155P, FCBGA989+HS; No modem; Kryo Gold 2131.2 MHz, Kryo Gold Prime 2419.2 MHz, GPU 700 MHz
SA8150P	CS [4]	004-AB	0x3 00E9 0E1	0x1	v2.2	0	SA8150P, FCBGA989+HS; No modem; Kryo Gold 1920 MHz, Kryo Gold Prime 2227.2 MHz, GPU 500 MHz
SA8155P	CS2	005-AC	0x3 00E9 0E1	0x0	v2.2	0	SA8155P, FCBGA989+HS; No modem; Kryo Gold 2131.2 MHz, Kryo Gold Prime 2419.2 MHz, GPU 700 MHz
SA8150P	CS2	005-AB	0x3 00E9 0E1	0x1	v2.2	0	SA8150P, FCBGA989+HS; No modem; Kryo Gold 1920 MHz, Kryo Gold Prime 2227.2 MHz, GPU 500 MHz

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.

3. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-5.
4. Devices with PRR code = 004 and date code of YWW ≥ 013 are CS parts.

Table 4-5 Source configuration codes

S value	Die	F value = F
0	Digital	TSMC
Other columns and rows will be added in future revisions of this document, if needed.		

4.4 Daisy chain devices

The SA8155 daisy chain ordering part number is TP-FCBGA989+HS.

4.5 Device moisture sensitivity level

Non-hermetically sealed packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; SA8155 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The SA8155 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.6 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following links to download the *SA8155 PACKAGE THERMAL MODEL ICEPAK* (HS11-PE986-5HW) and the S*A8155 PACKAGE THERMAL MODEL FloTHERM* (HS11-PE986-6HW) from the CreatePoint website. from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PE986-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-PE986-6HW

After successfully logging on, the document is downloaded.

4.7 Package loading during heat sink attachment

The maximum static load should not exceed 52 N.

The specification above has been determined through limited compressive testing with uniform loading applied perpendicular to the integrated heat spreader lid surface of the packages at 125°C up to 2000 hours. It was determined that the above load recommendation is within safe working limits to ensure negligible solder ball collapse and BGA shorting risk. The end user is encouraged to validate the acceptable loading range based on intended application, motherboard. and heat sink attach configurations.

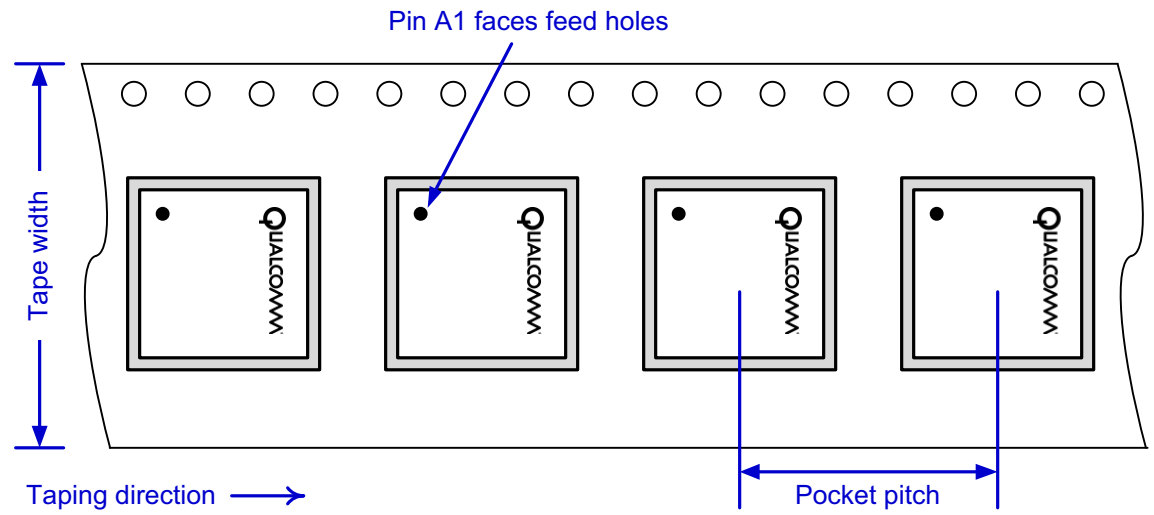
5 Carrier, handling, and storage information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the SA8155 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Dual	Reel diameter:	330 mm	Tape width:	44 mm
Units per reel:	500	Hub diameter:	178 mm	Pocket pitch:	32 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

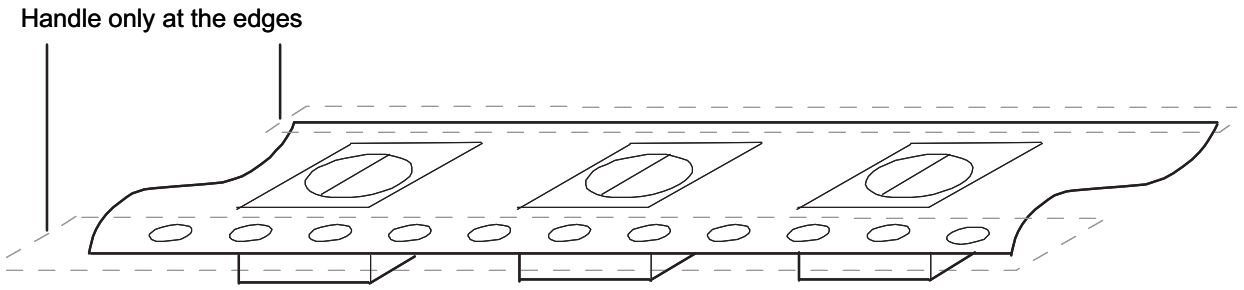


Figure 5-2 Tape handling

5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

Each tray of the SA8155 contains up to 60 devices. Production orders of the SA8155 that are shipped in matrix tray carriers will be in 10 + 1 tray stacks of 600 units. The stacking configuration and quantity for sample orders will vary.

Table 5-1 Matrix tray approved sources of supply

Key dimensions (mm)	
Array	5 × 12 (60)
M	16.95
M1	17.25
M2	25.50
M3	25.50

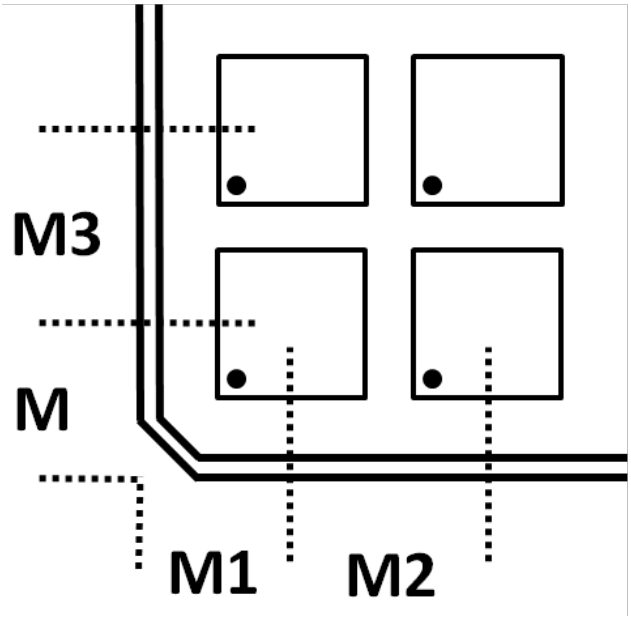


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

SA8155 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.5.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the SA8155 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the SA8155 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C for 12 hours. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD counter measures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the SA8155 ESD ratings.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its Sn/Ag/Cu solder balls use SAC405/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

Board level under-fill may be required for this device to pass board reliability testing. A keep-out region should be added to facilitate possible application of under-fill, if needed. See the *SMT Assembly Guidelines* (SM80-P0982-1) for guidance on material selection and processing.

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy-chain components.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the following link to download *DAISY CHAIN INTERCONNECT, FCBGA989+HS, 23.0 x 23.0 x 2.26 mm,* (DS90-PF731-3) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-PF731-3

After successfully logging on, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

7 Part reliability

7.1 Reliability qualifications summary

The SA8155 device has been qualified to AEC-Q100 Grade 3 specification. The qualification plan is summarized in Table 7-1.

.

Table 7-1 AEC-Q100 qualification plan

Stress test	ABV	Test#	Test method	Test condition/Pre and Post ATE (Identify temp, RH, and Bias)	Requirement		Results Fail/Total S.S	Comments
					S.S per lot	# lots		
Test group A – accelerated environment stress tests								
Preconditioning	PC	A1	JEDEC-J-STD-020, JESD22-A113	MSL 3, 3X reflow (pre and post ATE @ R)	77	6	0F/462	
Preconditioning + Bias HAST	BHAST	A2	JEDEC-JESD22-A110	130°C/85% RH for 96 hours (pre and post ATE @ R and H)	77	3	0F/231	
Preconditioning + unbiased HAST/temperature humidity	UHAST	A3	JEDEC-JESD22-A118	85°C/85% RH for 1000 hours (pre and post ATE @ R)	77	3	0F/231	
Preconditioning + temperature cycle	TC	A4	JEDEC-JESD22-A104	Ta = -55°C to +125°C for 500 cycles (pre and post ATE @ R and H)	77	6	0F/462	
High temperature storage life	HTSL	A6	JEDEC-JESD22-A103	Ta = +150°C for 500 hours (pre and post ATE @ R and H)	77	6	0F/462	
Test group B – accelerated lifetime simulation tests								
High temperature operating life	HTOL	B1	JEDEC-JESD22-A108	Tj = 125°C for 1000 hours (pre and post ATE @ R, C, and H)	77	3	0F/231	Drift Analysis performed from T0 to T1000 hours. All shifts within acceptable limits
Early life failure rate	ELFR	B2	AEC Q100-008	Tj = 125°C for 48 hours (pre and post ATE @ R and H)	800	3	0F/2400	
NVM endurance, data retention, and operational life	EDR	B3	–	–	–	–	–	No NVM memory on device
Test group C – package assembly integrity tests								
Wire bond shear	WBS	C1	–	–	–	–	–	Not Applicable, not a wirebonded package
Wire bond pull strength	WBPS	C2	–	–	–	–	–	Not Applicable, not a wirebonded package

Table 7-1 AEC-Q100 qualification plan

Stress test	ABV	Test#	Test method	Test condition/Pre and Post ATE (Identify temp, RH, and Bias)	Requirement		Results Fail/Total S.S	Comments
					S.S per lot	# lots		
Solderability	S	C3	–	–	–	–	–	Not a leadframe package
Physical dimensions	PD	C4	–	Package outline drawing	10	3	0F/30	CPK ≥ 1.67
Solder ball shear	SBS	C5	JESD22-B117	5 balls each from a minimum of 10 devices, ≥ 500 g/ball for pad opening 470 µm	10	3	0F/50	CPK ≥ 1.67
Lead integrity	LI	C6	–	–	–	–	–	Not a leadframe package
Test group D – die fabrication reliability tests								
Electromigration	EM	D1	JP001A	–	–	–	–	Pass
Time dependent dielectric breakdown	TDDB	D2	JP001A	–	–	–	–	Pass
Hot carrier injection	HCI	D3	JP001A	–	–	–	–	Pass
Negative bias temperature instability	NBTI	D4	JP001A	–	–	–	–	Pass
Stress migration	SM	D5	JP001A	–	–	–	–	Pass
Test group E – electrical verification tests								
Pre- and post-stress electrical test	TEST	E1	–	–	–	–	–	–
ESD - human body model	HBM	E2	AEC-Q100-002	Pass target +/- 1 kV with margin (pre and post ATE @ R and H)	3	1	0F/3	Passing ESD HBM Level +1 kV
ESD - charged device model	CDM	E3	AEC-Q100-011	Pass +/- 250 V (pre and post ATE @ R and H)	3	2	0F/6	Passing ESD CDM Level +/-150 V
Latch up	LU	E4	AEC-Q100-004	Ta = 85°C, Current injection +/- 100 mA, over voltage test @ 1.5x VDD (pre and post ATE @ R and H)	6	1	0F/6	–
Electrical distribution	ED	E5	–	–	–	–	–	Available for review
Fault grading	FG	E6	–	–	–	–	–	Available for review
Characterization	CHAR	E7	–	–	–	–	–	Available for review
Electromagnetic compatibility	EMC	E9	–	–	–	–	–	Not performed. System level test

Table 7-1 AEC-Q100 qualification plan

Stress test	ABV	Test#	Test method	Test condition/Pre and Post ATE (Identify temp, RH, and Bias)	Requirement		Results Fail/Total S.S	Comments
					S.S per lot	# lots		
Short circuit characterization	SC	E10	–	–	–	–	–	Not applicable. Not >12 V or a power device
Soft error rate	SER	E11	–	–	–	–	–	Available for review
Test group F – defect screening tests								
Process average test	PAT	F1	–	–	–	–	–	Available for review
Statistical bin/yield analysis	SBA	F2	–	–	–	–	–	Available for review

7.2 Device characteristics

Table 7-2 Device characteristics

Device name	SA8155
Package type	FCBGA989+HS
Package body size	23.0 mm × 23.0 mm × 2.26 mm
Ball count	989
Ball composition	SAC405/Ni
Fab process	7 nm
Fab sites	TSMC
Assembly sites	Amkor
Solder ball pitch	0.7 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	February 2018	Initial release
B	May 2018	■ Global: Updated product name from SDM855A to SA8155 and SDA855A to SA8155P throughout document. ■ Section 1 Introduction: Updated several product features. Read in entirety. ■ Figure 2-1 SA8155 pin assignments (Top view): Updated the pin diagram ■ Table 2-1 I/O parameter definitions: Replaced and with or in the description for PX_6 and add a new row for PX_11 ■ Table 2-2 Pin descriptions – primary pins: Renamed the following pins: □ USB1_SS_RX0_M to DP_LANE3_M □ USB1_SS_RX0_P to DP_LANE3_P □ USB1_SS_RX1_M to DP_LANE0_M □ USB1_SS_RX1_P to DP_LANE0_P □ USB1_SS_TX0_M to DP_LANE2_M □ USB1_SS_TX0_P to DP_LANE2_P □ USB1_SS_TX1_M to DP_LANE1_M □ USB1_SS_TX1_P to DP_LANE1_P and added functional description ■ Section 2.2 Pin map: Added the document CreatePoint link ■ Table 2-3 Pin descriptions – GPIO pins: Added TDM, PCM functionality behind I2S and corrected SPI-Slave MISO and MOSI pin functionality. ■ Table 2-4 Bottom pin descriptions – power-supply pins: Renamed VDDPX_11 to CXO pad group.

Revision	Date	Description
C	September 2018	■ SA8155 high-level block diagram and FCBGA989+HS drawing: Updated the package outline drawing ■ Table 1-1 SA8155 features: □ Updated ULCA from 3x ULCA to 2x ULCA under Digital signal processing □ Added RMII feature □ Added a note for HS-I^2S □ Figure 2-1 SA8155 pin assignments (Top view): Updated the pin diagram as per the legend ■ Table 2-3 Pin descriptions – GPIO pins: □ Corrected typos for GPIO[35] and GPIO[36] □ Added Wakeup function column and updated this column for GPIOs as applicable □ Added alternate function RMII for GPIO[4], GPIO[114], GPIO[116], GPIO[117], GPIO[118], and GPIO[121] □ Corrected the function name for GPIOs with I^2S port muxing □ Removed RFFE4 and RFFE5 functions □ Added USB AC coupling control function on GPIO_113 and GPIO_123 ■ Table 2-4 Bottom pin descriptions – power-supply pins: Corrected the pin-name for pins N29 and N31 ■ Chapter 3 Electrical specifications: Added this chapter ■ Chapter 4 Mechanical information: Added all other sections in this chapter ■ Section 4.1 Device physical dimensions: Changed the maximum height of the package from 2.25 mm to 2.26 mm. ■ Figure 4-1 Simplified FCBGA989+HS outline drawing: Updated the package outline drawing ■ Figure 5-1 Carrier tape drawing with part orientation: Updated this image ■ Section 5.1.2 Matrix tray information: Added this section ■ Chapter 7.2 Device characteristics: □ Changed the maximum height of the package from 2.25 mm to 2.26 mm. □ Changed the solder ball pitch from 0.35 mm to 0.7 mm
D	November 2018	■ Table 1-1 SA8155 variant feature set comparison: Added this table ■ Table 1-2 SA8155 features: Updated this table ■ Table 2-2 Pin descriptions – primary pins: Updated the functional description column for pins N27 and K26 ■ Table 3-2 Operating conditions: Added thermal conditions ■ Table 3-3 PDN specifications: Updated this table and added footnote ■ Table 3-30 SPI master timing characteristics for QUP_17 and QUP_19: Updated this table for min value ■ Table 3-35 I3C interface: Updated this table ■ *Section 6.2 SMT assembly guidelines:* Updated this section

Revision	Date	Description
E	January 2019	■ Chapter 1 *Introduction:* Added a note to specify the usage of SA8155 chipset ■ Table 1-1 *SA8155 variant feature set comparison*: Updated the Kryo Gold and GPU frequency ■ Table 1-2 *SA8155 features*: Updated SA8155 features and capability ■ Table 1-3 *Key modem features (not applicable to SA8155P/SA8150P)*: Updated the title to indicate the applicability of SA8155 ■ Table 2-3 *Pin descriptions – GPIO pins*: Updated various GPIO functional description ■ Table 3-3 *PDN specifications*: Updated the PDN specification values ■ Table 3-4 *PDN specifications–DDR rails*: Updated the PDN specification value ■ Table 3-5 *PDN specifications–SerDes rails*: Updated the PDN specification values ■ Table 3-36 *XO timing parameters*: Updated the reference document in the footnote ■ Table 4-3 *Device identification details*: Updated the device identification details for ES2 and ES3 samples ■ Table 7-1 *Device characteristics*: Updated the ball count and ball composition

Revision	Date	Description
F	March 2019	■ *SA8155 high-level block diagram and FCBGA989+HS drawing: Updated the high-level block diagram* ■ *Figure 1-1 SA8155 functional block diagram and example application: Updated the functional block diagram* ■ *Table 1-1 SA8155 variant feature set comparison: Added information on Video decode/encode* ■ *Table 1-2 SA8155 features: Updated the following features:* □ *Removed security feature* □ *Updated System memory via EBI* □ *Updated Display interface/performance* □ *Updated Audio interfaces* □ *Updated Connectivity features* □ *Updated USB feature* ■ *Table 2-2 Pin descriptions – primary pins: Updated the following pins:* □ *Updated the Pad type for all CSI pins* □ *Updated the Pad type for QREFS_CXO_REXT, REFGEN_ REXT0, REFGEN_REXT1, USB1_REXT, and USB2_REXT* □ *Realigned DisplayPort pins before DSI pins and updated the pad type for DP pins* ■ *Table 2-3 Pin descriptions – GPIO pins: Updated the following pins:* □ *Added PX prefix to all the Pad voltage values* □ *Changed the pin # for GPIO_126 pin from AD22 to AD42* ■ *Table 3-1 Absolute maximum ratings: Updated the thermal conditions with storage temperature* ■ *Table 3-2 Operating conditions: Updated the minimum and typical voltage values for the following parameters: VDDA_CSI0_0P9, VDDA_PLL_HV_CC_EBI, and VDDA_HV_EBI0* ■ *Table 3-3 PDN specifications: Updated the PDN specification* ■ *Table 3-4 PDN specifications–DDR rails: Updated the maximum effective impedance values for VREG_S7A* ■ *Table 3-5 PDN specifications–SerDes rails: Updated the Power domain names of VDDA_PCIE_2LN_CORE to VDDA_PCIE1_ CORE and VDDA_PCIE_1LN_CORE to VDDA_PCIE0_CORE* ■ *Table 3-17 Supported PCIe standards and exceptions: Updated the feature exception* ■ *Table 4-3 Device identification code: Updated the device identification code* ■ *Table 4-4 Device identification details: Added the device identification details for SM8150P ES3 sample* ■ *Table 7-1 AEC-Q100 qualification plan:* Added new table

Revision	Date	Description
G	May 2019	■ *Table 1-2 SA8155 features: Updated the SPI frequency* ■ *Table 2-2 Pin descriptions – primary pins: Updated the pad type* ■ *Table 2-3 Pin descriptions – GPIO pins: Updated the pin number for GPIO_149* ■ *Table 3-3 PDN specifications: Updated the DC resistance values* ■ *Table 3-5 PDN specifications–SerDes rails: Updated the DC resistance values* ■ *Table 3-31 SPI slave timing characteristics for QUP_0/QUP_ 1/QUP_2/QUP_9/QUP_10/ QUP_15: Added a note about SPI slave mode 1 support* ■ *Table 4-4 Device identification details: Updated the feature ID for 004-AB variant* ■ *Section 4.7 Package loading during heat sink attachment*: Updated the details
H	November 2019	■ *Table 1-1 SA8155 variant feature set comparison:* Updated the LPDDR4X frequency ■ *Table 1-2 SA8155 features:* □ Updated the Kryo Gold frequency □ Updated the LPDDR4X frequency □ Updated the UFS 3.0 support ■ *Table 2-2 Pin descriptions – primary pins:* □ Updated the pad type for CSI pins □ Updated the functional description of AJ43, AH42, and AL43 pins ■ *Table 2-3 Pin descriptions – GPIO pins:* Updated the PCIe details and added alternate functions for GPIO_24, GPIO_25, and GPIO_26 ■ Table 3-3 *Operating conditions*: Added a note for T_J max ■ Table 3-4 *PDN specifications*: Updated the DC resistance titles ■ Table 3-6 *PDN specifications–SerDes rails*: Updated this table ■ Table 3-7 *DC specification of 1.8 V GPIOs, CXO input, and SLEEP_CLK input1*: Updated the table caption and specifications ■ Table 3-14 *Supported MIPI_DSI standards and exceptions*: Updated the feature exception of *MIPI Alliance Specification for Display Serial Interface* standard ■ Section 3.9.3 *DisplayPort*: Added a note for DP++ support ■ Table 3-38 *Sleep-clock timing parameters*: Updated the typical values of sleep clock period and sleep clock frequency ■ Section 6.1 *RoHS compliance*: Updated the solder ball composition ■ Section 6.3 *Daisy-chain components*: Updated the daisy chain document number and download link
Revision I was omitted in accordance with QTI document conventions.		

Revision	Date	Description
J	March 2020	■ Updated the document title ■ Removed obsolete document references throughout ■ Table 3-1 *Absolute maximum ratings*: Updated the table ■ Table 3-2 *Operating conditions for voltage rails with AVS Type-1:* Added the table ■ Table 3-3 *Operating conditions*: Updated the table ■ Table 3-19 *Supported UFS standards and exceptions:* Updated the table ■ Table 3-26 *HS-I^2S interface timing:* Updated the table ■ Table 3-30 *SPI master timing characteristics:* Updated the comments column for T (SPI clock period) ■ Table 3-32 *SPI slave timing characteristics for QUP_0/QUP_1/QUP_2/QUP_9/QUP_10/ QUP_15*: Updated the table ■ Table 3-34 *SDR AC parameters:* Updated the table ■ Table 3-35 *DDR AC parameters:* Updated the table ■ Table 4-4 *Device identification details*: Added CS samples ■ Section 4.5 *Device moisture sensitivity level*: Updated this section ■ Section 4.7 *Package loading during heat sink attachment*: Deleted the note
K	June 2020	■ Table 1-3 *Key modem features (not applicable to SA8155P/SA8150P)*: Updated the Audio Interfaces ■ Table 2-2 *Pin descriptions – primary pins*: Updated the Functional description for the pin AN1 ■ Section 3.1 *Absolute maximum ratings*: Updated the section ■ Table 3-1 *Absolute maximum ratings*: Updated the maximum value for VDDPX_0 ■ Table 3-7 *DC specification of 1.8 V IOs, CXO input, and SLEEP_CLK input1*: Updated the table title and a foot note ■ Section 4.3.1 *Specification-compliant devices*: Updated the section ■ Table 4-4 *Device identification details*: Updated the date code for CS samples ■ Section 4.5 *Device moisture sensitivity level:* Updated the section with a minor update ■ Section 5.1.2 *Matrix tray information*: Updated the section ■ Table 5-1 *Matrix tray approved sources of supply*: Added the array details ■ Section 5.3.1*Baking*: Updated the Caution ■ Table 7-1 *AEC-Q100 qualification plan*: Updated the table

Revision	Date	Description
L	October 2020	■ Table 1-1 *SA8155 variant feature set comparison*: Updated the table for Video decode/encode ■ Table 1-2 *SA8155 features:* Added Safety feature ■ Table 2-2 *Pin descriptions – primary pins*: Updated the pad voltage of the pins W41, and T44 ■ Table 3-25 *I^2S interface timing:* Updated the table ■ Table 3-27 PCM/TDM interface timing parameters: Updated the table ■ Section 3.9.15 *Serial peripheral interface*: Added a note ■ Section 4.3.1 *Specification-compliant devices*: Updated the example ■ Table 4-4 *Device identification details*: Updated the foot note for CS date code ■ Section 7.1 *Reliability qualifications summary*: Updated the description
M	November 2020	■ Table 1-2 *SA8155 features:* Updated the description for the safety feature ■ Table 3-1 *Absolute maximum ratings*: Updated storage temperature minimum value ■ Table 3-25 *I^2S interface timing*: Reverted the incorrect changes made in the previous revision of the document ■ Table 3-27 *PCM/TDM interface timing parameters*: Reverted the incorrect changes made in the previous revision of the document
N	May 2021	■ Table 2-3 *Pin descriptions – GPIO pins*: Removed the alternate function Audio reference clock for the pin AJ41 ■ Table 3-4 *PDN specifications*: Removed the pin AH34 from power rail VREG_S10C ■ Table 3-2 *Operating conditions for voltage rails with AVS Type-1*: Updated the table ■ Section 3.9.6 *RGMII interface*: Added a note ■ Section 3.9.7 *RMII interface*: Added a note
Revision O was omitted in accordance with QTI document conventions.		
P	August 2021	■ Table 1-2 *SA8155 features:* Updated the version for UFS ■ Table 2-3 *Pin descriptions – GPIO pins*: Corrected the typo in alternate function for GPIO_117 ■ Table 3-19 *Supported UFS standards and exceptions*: Updated the UFS version and feature exceptions ■ Figure 3-9 *SPI master mode 0 timing diagram*: Updated the figure title ■ Figure 3-10 SPI master mode 1 timing diagram: Added this diagram ■ Section 7.1 *Reliability qualifications summary*: Updated the AEC-Q100 to AEC-Q100 grade 3 specification
Revision Q was omitted in accordance with QTI document conventions.		
R	September 2021	■ *Figure 3-9 SPI master mode 0 timing diagram*: Updated the diagram ■ *Figure 3-10 SPI master mode 1 timing diagram*: Updated the diagram

Revision	Date	Description
Revision S was omitted in accordance with QTI document conventions		
T	December 2021	■ Global: Changed all instances of secure processing unit to internal circuits throughout the document ■ Table 1-2 *SA8155 features*: Updated the security features ■ Table 2-1 *I/O parameter definitions*: Updated the description for PX_13 ■ Table 2-2 *Pin descriptions – primary pins*: Updated the functional description for pin number E35 ■ Table 4-2 *QFPROM_CORR_PTE_ROW0_LSB register (Address: 0x0784130)*: Updated the table title with actual register name and address
U	June 3, 2022	■ Table 3-1 *Absolute maximum ratings*: Updated the maximum value for power supply voltages VDDPX_1, VDDIO_EBI0/1/2/3, and VDDIO_CK_EBI0/1/2/3
V	June 27, 2022	■ Table 3-1 *Absolute maximum ratings*: Updated the maximum value for parameter power supply voltage VDDPX_1
W	July 2022	■ Table 4-4 *Device identification details*: □ Added CS2 sample type □ Updated the comments column and footnote 4
Revision X was omitted in accordance with QTI document conventions		
Y	October 2022	■ Section 4.6 *Thermal characteristics*: Updated the link of the reference documents

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